OKI Semiconductor

This version: Mar. 2001
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MSM82C59A-2RS/GS/JS

PROGRAMMABLE INTERRUPT CONTROLLER

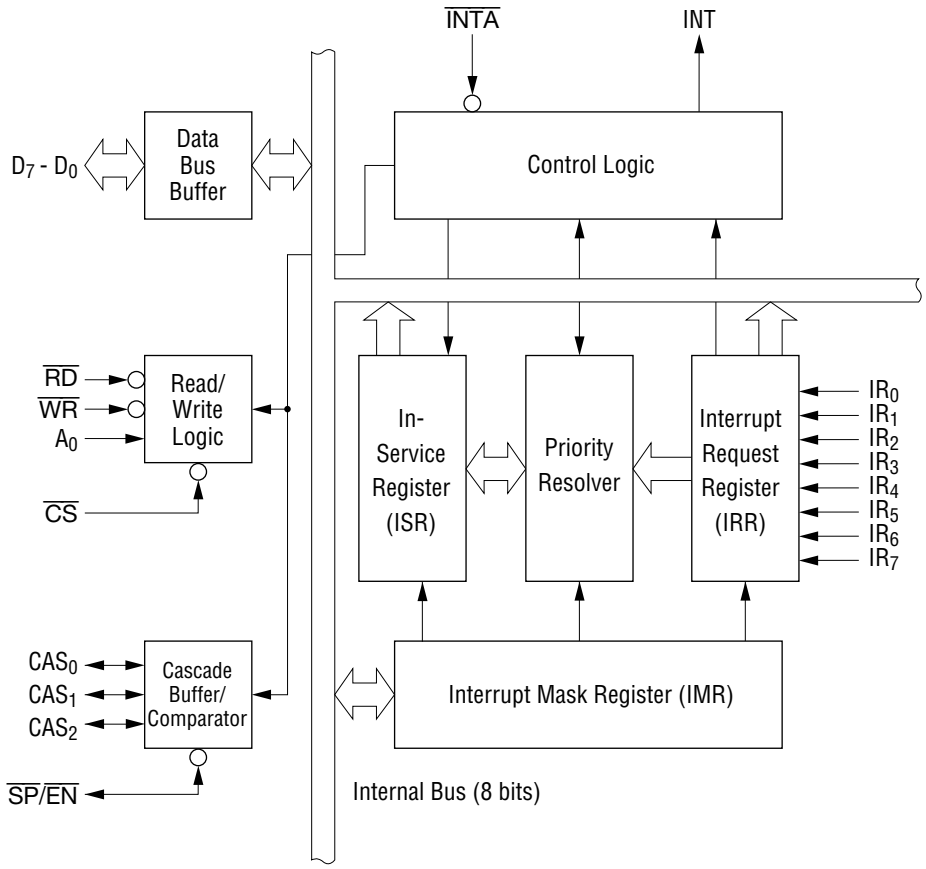
GENERAL DESCRIPTION

The MSM82C59A-2 is a programmable interrupt for use in MSM80C85AH and MSM80C86A-10/88A-10 microcomputer systems.
Based on CMOS silicon gate technology, this device features an extremely low standby current of 100 µA (max.) in chip non-selective status. During interrupt control status, the power consumption is very low with only 5 mA (max.) being required.
Internally, the MSM82C59A-2 can control priority interrupts up to 8 levels, and can be expanded up to 64 levels by cascade connection of a number of devices.

FEATURES

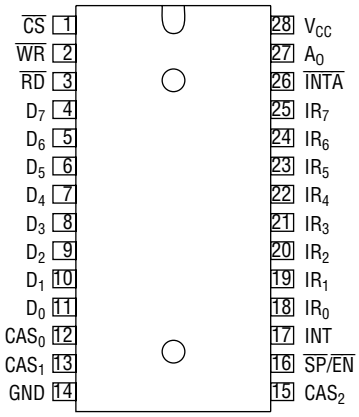
- Silicon gate CMOS technology for high speed and low power consumption
- 3 V to 6 V single power supply
- MSM80C85AH system compatibility (MAX. 5 MHz)
- MSM80C86A-10/88A-10 system compatibility (MAX. 8 MHz)
- 8-level priority interrupt control
- Interrupt levels expandable up to 64 levels
- Programmable interrupt mode
- Maskable interrupt
- Automatically generated CALL code (85 mode)
- TTL compatible
- 28-pin Plastic DIP (DIP28-P-600-2.54): (Product name: MSM82C59A-2RS)
- 28-pin Plastic QFJ (QFJ28-P-S450-1.27): (Product name: MSM82C59A-2JS)
- 32-pin Plastic SSOP (SSOP32-P-430-1.00-K): (Product name: MSM82C59A-2GS-K)

BLOCK DIAGRAM

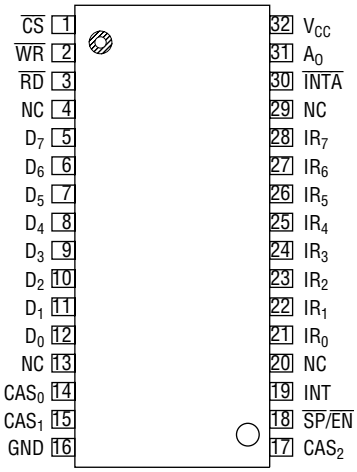


MSM82C59A-2 Internal Block Diagram

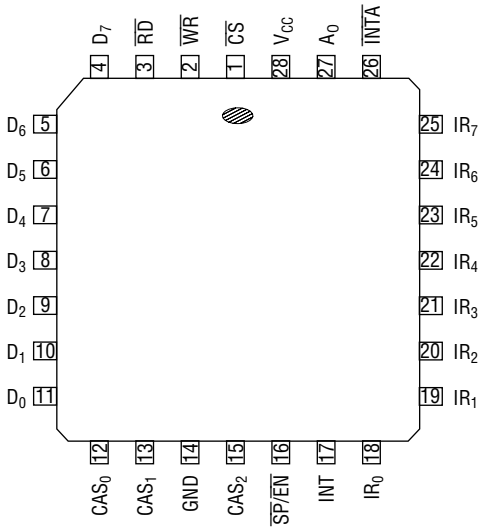
PIN CONFIGURATION (TOP VIEW)



28-pin Plastic DIP



32-pin Plastic SSOP



28-pin Plastic QFJ

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating			Unit
			MSM82C59A-2RS	MSM82C59A-2GS	MSM82C59A-2JS	
Power Supply Voltage	V_{CC}	Respect to GND	–0.5 to +7			V
Input Voltage	V_{IN}		–0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		–0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{STG}	—	–55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	0.9	0.7	0.9	W

OPERATING RANGES

Parameter	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	–40 to +85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	–40	+25	+85	°C
"L" Level Input Voltage	V_{IL}	–0.5	—	+0.8	V
"H" Level Input Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V

DC CHARACTERISTICS

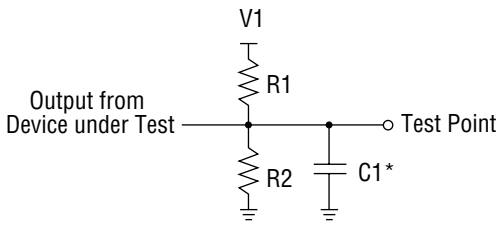
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Level Output Voltage	V_{OL}	I_{OL} = 2.5 mA	V_{CC} = 4.5 V to 5.5 V Ta = –40°C to +85°C	—	—	0.4	V
"H" Level Output Voltage	V_{OH}	I_{OH} = –2.5 mA		3.0	—	—	V
		I_{OH} = –100 µA		V_{CC} – 0.4	—	—	
Input Leak Current	I_{LI}	0 ≤ V_{IN} ≤ V_{CC}		–1	—	+1	µA
IR Input Leak Current	I_{LIR}			–300	—	+10	µA
Output Leak Current	I_{LO}	0 ≤ V_{OUT} ≤ V_{CC}		–10	—	+10	µA
Standby Power Supply Current	I_{CCS}	$\overline{CS}$ = V_{CC}, IR = V_{CC} V_{IL} = 0 V, V_{IH} = V_{CC}		—	0.1	100	µA
Average Operation Power Supply Current	I_{CC}	V_{IN} = 0 V/V_{CC} C_L = 0 pF		—	—	5	mA

AC CHARACTERISTICS

Ta = –40°C to +85°C, V_{CC} = 5 V ±10%

Parameter	Symbol	Min.	Max.	Unit	TEST Conditions	
Address Setup Time (to $\overline{RD}$)	t_{AHRL}	10	—	ns	—	Read $\overline{INTA}$ timing
Address Hold Time (after $\overline{RD}$)	t_{RHAX}	5	—	ns		
$\overline{RD}$/$\overline{INTA}$ Pulse Width	t_{RLRH}	160	—	ns		
Address Setup Time (to $\overline{WR}$)	t_{AHWL}	0	—	ns	—	Write timing
Address Hold Time (after $\overline{WR}$)	t_{WHAX}	0	—	—		
$\overline{WR}$ Pulse Width	t_{WLWH}	190	—	ns		
Data Setup Time (to $\overline{WR}$)	t_{DVWH}	160	—	ns		
Data Hold Time (after $\overline{WR}$)	t_{WHDX}	0	—	ns		
IR Input Width(Low)	t_{JLJH}	100	—	ns	—	$\overline{INTA}$ sequence
CAS Input Setup Time (to $\overline{INTA}$) (Slave)	t_{CVIAL}	40	—	ns		
End of $\overline{RD}$ to Next $\overline{RD}$ End of $\overline{INTA}$ to Next $\overline{INTA}$	t_{RHRL}	160	—	ns	—	Other timing
End of $\overline{WR}$ to Next $\overline{WR}$	t_{WHWL}	190	—	ns		
End of Command to Next Command	t_{CHCL}	400	—	ns		
Data Valid Following $\overline{RD}$/ $\overline{INTA}$	t_{RLDV}	—	120	ns	1	Delay times
Data Floating Following $\overline{RD}$/ $\overline{INTA}$	t_{RHDZ}	10	85	ns	2	
INT Output Delay Time	t_{JHIH}	—	300	ns	1	
CAS Valid Following 1 st. $\overline{INTA}$ (master)	t_{IALCV}	—	360	ns	1	
$\overline{EN}$ Active Following $\overline{RD}$/$\overline{INTA}$	t_{RLEL}	—	100	ns	1	
$\overline{EN}$ Inactive Following $\overline{RD}$/ $\overline{INTA}$	t_{RHEH}	—	150	ns	1	
Data Valid after Address	t_{AHDV}	—	200	ns	1	
Data Valid after CAS	t_{CVDV}	—	200	ns	1	

AC Test Circuits

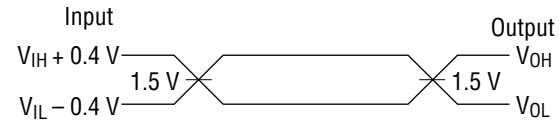


* Includes Stray and Jig Capacitance

Test Condition Definition Table

Test Condition	V1	R1	R2	C1
1	1.7 V	523 Ω	Open	100 pF
2	4.5 V	1.8k Ω	1.8k Ω	30 pF

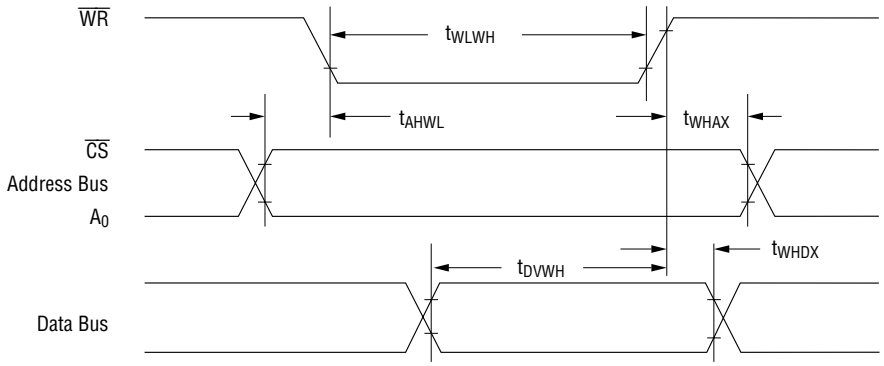
A.C. Testing Input, Output Waveform



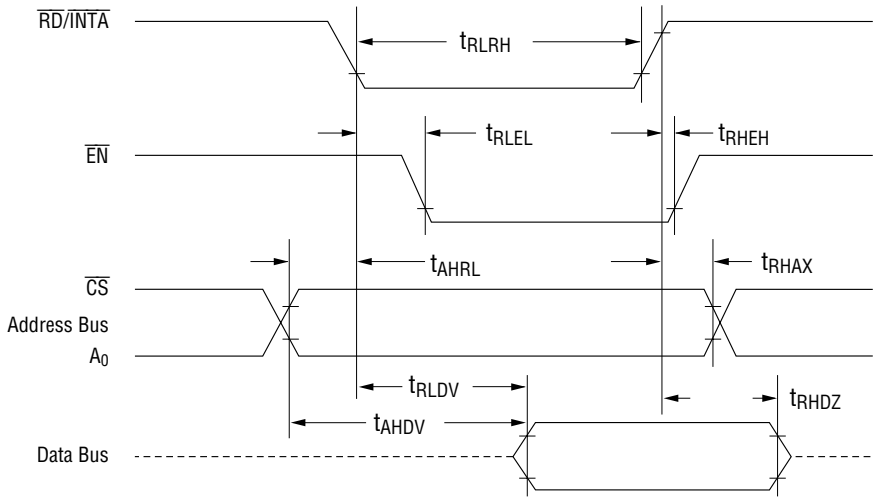
A. C. Testing: All input signals must switch between V_{IL} – 0.4 V and V_{IH} + 0.4 V.
T_R and T_F must be less than of equal to 15 ns.

TIMING CHART

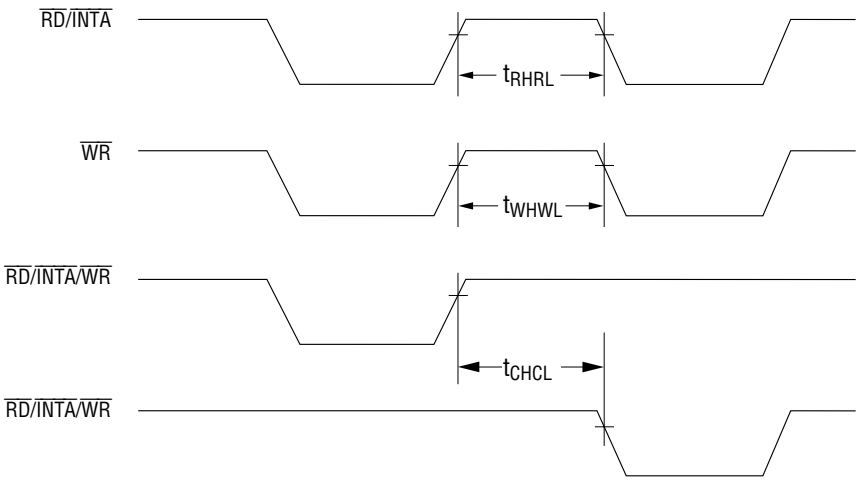
Write Timing



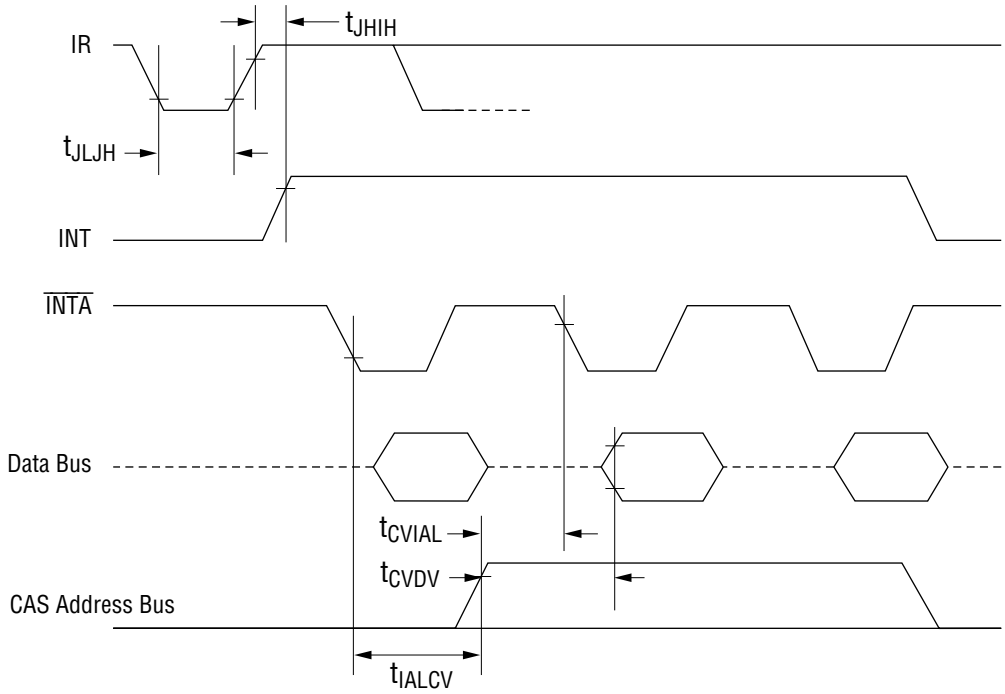
Read/INTA Timing



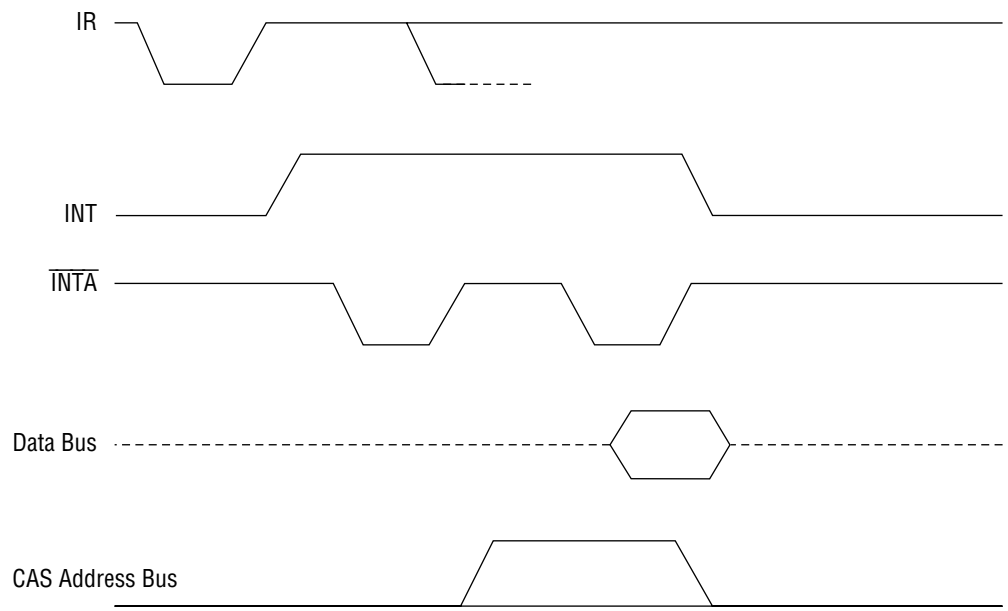
Other Timing



$\overline{\text{INTA}}$ Sequence (85 mode)



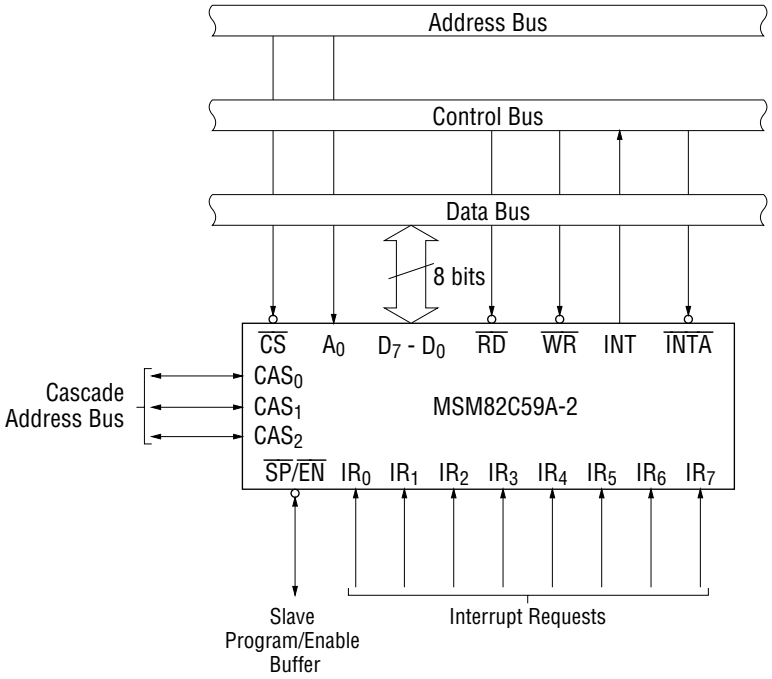
$\overline{\text{INTA}}$ Sequence (86 mode)



PIN FUNCTION DESCRIPTION

Pin Symbol	Name	Input/Output	Function
D_7 - D_0	Bidirectional Data Bus	Input/Output	This 3-state 8-bit bidirectional data bus is used in reading status registers and writing command words through the $\overline{RD}$/$\overline{WR}$ signal from the CPU, and also in reading the CALL instruction code by the $\overline{INTA}$ signal from the CPU.
$\overline{CS}$	Chip Select Input	Input	Data transfer with the CPU is enabled by $\overline{RD}$/$\overline{WR}$ when this pin is at low level. The data bus (D_0 thru D_7) is switched to high impedance when the pin is at high level. Note that $\overline{CS}$ does not effect $\overline{INTA}$.
$\overline{RD}$	Read Input	Input	Data is transferred from the MSM82C59A-2 to the CPU when this pin is at low level. IRR (Interrupt Request Register), ISR (In-Service Register), IMR (Interrupt Mask Register), or a Poll word is selected by OCW3 and A_0.
$\overline{WR}$	Write Input	Input	Commands are transferred from the CPU to the MSM82C59A-2 when this pin is at low level.
A_0	Address Input	Input	This pin is used together with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ signals to write commands in the command registers, and to select and read status registers. This is normally connected to the least significant bit of the address bus. (A_0 for MSM80C85AH, A_1 for MSM80C86A-10/88A-10).
CAS_0 - $_2$	Cascade Address	Input/Output	These pins are outputs when the MSM82C59A-2 is used as the master, and inputs when used as a slave (in cascade mode). These pins are outputs when in single mode.
$\overline{SP}$/$\overline{EN}$	Slave Program Input/Enable Buffer Output	Input/Output	This dual function pin is used as an output to enable the data bus buffer in Buffered mode, and as an input for deciding whether the MSM82C59A-2 is to be master ($\overline{SP}$/$\overline{EN}$ = 1) or slave ($\overline{SP}$/$\overline{EN}$ = 0) during Non-buffered mode.
INT	Interrupt Output	Output	When an interrupt request is made to the MSM82C59A-2, the INT output is switched to high level, and INT interrupt is sent to the CPU.
$\overline{INTA}$	Interrupt Acknowledge Input	Input	When this pin is at low level, the CALL instruction code or the interrupt vector data is enabled onto the data bus. When the CPU acknowledges the INT interrupt, $\overline{INTA}$ is sent to the MSM82C59A-2. (Interrupt acknowledge sequence).
IR_0 - $_7$	Request Input	Input	These interrupt request input pins for the MSM82C59A-2 can be set to edge trigger mode or level trigger mode (by ICW1). In edge trigger mode, interrupt request is executed by the rising edge of the IR input and holds it until that input is acknowledged by the CPU. In level trigger mode, interrupt requests are executed by high level IR inputs and holds them until that input is acknowledged by the CPU. These pins have a pull up resistor.

SYSTEM INTERFACE



BASIC OPERATION DESCRIPTION

Data transfers between the 82C59A-2 internal registers and the data bus are listed below.

A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Function	Opearation
0	×	×	0	1	0	IRR, ISR, or Poll Word → Data Bus	Read
1	×	×	0	1	0	IMR → Data bus	Read
0	0	0	1	0	0	Data Bus → OCW2	Write
0	0	1	1	0	0	Data Bus → OCW3	Write
0	1	×	1	0	0	Data Bus → 1CW1	Write
1	×	×	1	0	0	Data Bus → OCW1, ICW2, ICW3, ICW4	Write
×	×	×	1	1	0	Data Bus Set to High Impedance (when $\overline{INTA}$ = 1)	—
×	×	×	×	×	1		
×	×	×	0	0	×	Combinations Prohibited	—

OPERATION DESCRIPTION

The MSM82C59A-2 has been designed for real time interrupt driven microcomputer systems. The MSM82C59A-2 is capable of handling up to 8 levels of interrupt requests, and can be expanded to cover a maximum of 64 levels when connected to other MSM82C59A-2 devices. Programming involves the use of system software in the same way as other microcomputer peripheral I/O devices. Selection of priority mode involves program execution, and enables the method of requesting interrupts to be processed by the MSM82C59A-2 to be suitably configured for system requirements. That is, the priority mode can be dynamically updated or reconfigured during the main program at any time. A complete interrupt structure can be defined as required, based on the entire system environment.

(1) Functional Description of Each Block

Block Name	Description of Function
IRR, ISR	IR input line interrupts are processed by a cascaded interrupt request register (IRR) and the in-service register (ISR). The IRR stores all request levels where interrupt service is requested, and the ISR stores all interrupt levels being serviced.
Priority Resolver	This logic block determines the priority level of the bits set in the IRR. The highest priority level is selected, and the corresponding ISR bit is set during $\overline{INTA}$ pulses.
Read/Write Logic	This block is capable of receiving commands from the CPU. These command words (ICW) and the operation command words (OCW) store the various control formats for MSM82C59A-2 operations. This block is also used to transfer the status of the MSM82C59A-2 to the Data Bus.
Cascade Buffer Comparator	This functional block is involved in the output and comparison of all MSM82C59A-2 IDs used in the system. These three I/O pins (CAS_0 thru CAS_2) are outputs when the MSM82C59A-2 operates as a master, and inputs when it operates as a slave. When operating as a master, the MSM82C59A-2 sends a slave ID output to the slave where an interrupt has been applied. Furthermore, the selected slave sends the preprogrammed subroutine address onto the data bus during next one or two $\overline{INTA}$ pulses from the CPU.

(2) Interrupt Sequence

The major features of the MSM82C59A-2 used in microcomputer systems are the programmability and the addressing capability of interrupt routines. This latter feature enables direct or indirect jumping to specific interrupt routines without polling the interrupt devices. The operational sequence during an interrupt varies for different CPUs. The procedure for the 85 system (MSM80C85AH) is outlined below.

(i) One or more interrupt requests (IR_0 thru IR_7) becomes high, and the corresponding IRR bit is set.
(ii) The MSM82C59A-2 evaluates these requests, and sends an INT signal to the CPU if the request is judged to be suitable.
(iii) The CPU issues an $\overline{INTA}$ output pulse upon reception of the INT signal.
(iv) Upon reception of the $\overline{INTA}$ signal from the CPU, the MSM82C59A-2 releases the CALL instruction code (11001101) to the 8-bit data bus.

(v) A further two $\overline{\text{INTA}}$ pulses are then sent to the MSM82C59A-2 from the CPU by this CALL instruction.
(vi) These two $\overline{\text{INTA}}$ pulses result in a preprogrammed subroutine address being sent from the MSM82C59A-2 to the data bus. The lower 8-bit address is released by the first $\overline{\text{INTA}}$ pulse, and the higher 8-bit address is released by the second pulse.
The Falling Edge of the second $\overline{\text{INTA}}$ signal sets the ISR bit with the highest priority, and the Rising Edge of it resets the IRR bit.
(vii) 3-byte CALL instructions are thus released by the MSM82C59A-2. In Automatic End Of Interrupt (AEOI) mode, the IRS bit is reset at the end of the third $\overline{\text{INTA}}$ pulse. In other cases, the ISR bit remains set until reception of a suitable EOI command at the end of the interrupt routine.

The procedure for the 86 system (MSM80C86A-10/88A-10) is identical to the first three steps of the 85 system. The subsequent steps are described below.
(iv) Upon reception of the $\overline{\text{INTA}}$ signal from the CPU, the ISR bit with the highest priority is set, and the corresponding IRR bit is reset. In this cycle, the MSM82C59A-2 sets the data bus to high impedance without driving the Data Bus.
(v) The CPU generates a second $\overline{\text{INTA}}$ output pulse, resulting in an 8-bit pointer to the data bus by the MSM82C59A-2.
The Falling Edge of the $\overline{\text{INTA}}$ signal sets the ISR bit with the highest priority, and the Rising Edge of it resets the IRR bit.
(vi) This completes the interrupt cycle. In AEOI mode, the ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse. In other cases, the ISR bit remains set until reception of 3 suitable EOI command at the end of the interrupt routine.

If the interrupt request is canceled prior to step (iv), that is, before the first $\overline{\text{INTA}}$ pulse has been received, the MSM82C59A-2 operates as if a level 7 interrupt has been received, and the vector byte and CAS line operate as if a level 7 interrupt has been requested.

(3) Interrupt Sequence Output

85 Mode (MSM80C85AH)

The sequence in this case consists of three $\overline{\text{INTA}}$ pulses. A CALL operation code is released to the data bus by the first $\overline{\text{INTA}}$ pulse.

Contents of the First Interrupt Vector Byte

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CALL Code	1	1	0	0	1	1	0	1

The lower address of the interrupt service routine is released to the data bus by the second $\overline{\text{INTA}}$ pulse. If A_5-A_7 are programmed with an address interval of 4, A_0-A_4 are automatically inserted. And if A_6 and A_7 are programmed at an address interval of 8, A_0-A_5 are automatically inserted.
Contents of the second interrupt vector byte

Contents of the Second Interrupt vector byte

IR	Interval = 4							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	A_7	A_6	A_5	1	1	1	0	0
6	A_7	A_6	A_5	1	1	0	0	0
5	A_7	A_6	A_5	1	0	1	0	0
4	A_7	A_6	A_5	1	0	0	0	0
3	A_7	A_6	A_5	0	1	1	0	0
2	A_7	A_6	A_5	0	1	0	0	0
1	A_7	A_6	A_5	0	0	1	0	0
0	A_7	A_6	A_5	0	0	0	0	0
IR	**Interval = 8**							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	A_7	A_6	1	1	1	0	0	0
6	A_7	A_6	1	1	0	0	0	0
5	A_7	A_6	1	0	1	0	0	0
4	A_7	A_6	1	0	0	0	0	0
3	A_7	A_6	0	1	1	0	0	0
2	A_7	A_6	0	1	0	0	0	0
1	A_7	A_6	0	0	1	0	0	0
0	A_7	A_6	0	0	0	0	0	0

The higher address of the interrupt service routine programmed by the second bytes (A_8 - A_{15}) of the initialization sequence is released to the data bus.

Contents of the Third Interrupt Vector Byte

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

86 Mode (MSM80C86A-10/88A-10)

Apart from the two interrupt acknowledge cycles and the absence of a CALL operation code, the 86 mode is the same as the 85 mode. The first $\overline{\text{INTA}}$ cycle freezes interrupt status to resolve the priority internally in the same way as in 85 mode. When the device is used as a master, an interrupt code is issued to the cascade line at the end of the $\overline{\text{INTA}}$ pulse. During this first cycle, the data bus buffer is kept at high impedance without any data to the CPU. During the second $\overline{\text{INTA}}$ cycle, the MSM82C59A-2 sends a byte of interrupt code to the CPU. Note that in 86 mode, the Address Interval (ADI) control status is ignored and A_5-A_{10} is not used.

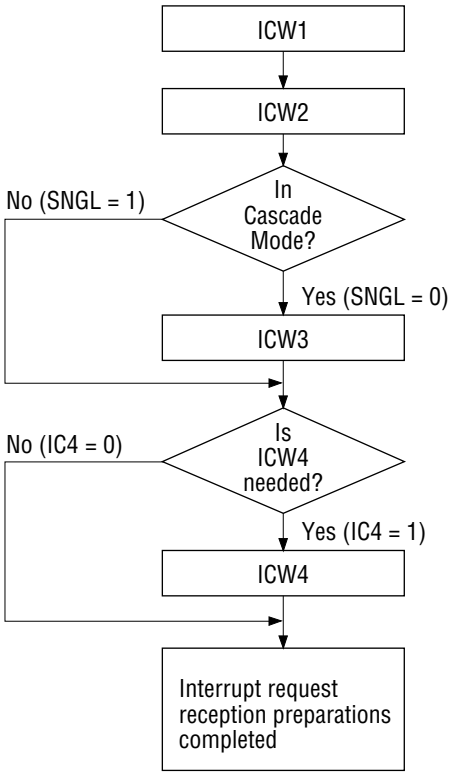
Contents of Interrupt Vector Byte in 86 System Mode

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_7	T_7	T_6	T_5	T_4	T_3	1	1	1
IR_6	T_7	T_6	T_5	T_4	T_3	1	1	0
IR_5	T_7	T_6	T_5	T_4	T_3	1	0	1
IR_4	T_7	T_6	T_5	T_4	T_3	1	0	0
IR_3	T_7	T_6	T_5	T_4	T_3	0	1	1
IR_2	T_7	T_6	T_5	T_4	T_3	0	1	0
IR_1	T_7	T_6	T_5	T_4	T_3	0	0	1
IR_0	T_7	T_6	T_5	T_4	T_3	0	0	0

(4) Programming the MSM82C59A-2

The MSM82C59A-2 receives two types of command words generated by the CPU.

(i) Initialization Command Words (ICW1 thru ICW4)
Before commencing normal operations, each MSM82C59A-2 in the system must be initialized by two to four $\overline{WR}$ pulse sequence.



Initialization Sequence

(ii) Operation Command Words (OCW1 thru OCW3)
These commands are used in operating the MSM82C59A-2 in the following modes.
a. Fully Nested Mode
b. Rotating Priority Mode
c. Special Mask Mode
d. Polled Mode
The OCW can be written into the MSM82C59A-2 any time after initialization has been completed.

(5) Initialization Command Words (ICW1 thru ICW4)

When a command is issued with $D_4 = 1$ and $A_0 = 0$, it is always regarded as an Initialization Command Word 1 (ICW1). Starting of the initialization sequence by ICW1 results in automatic execution of the following steps.

a. The edge sense circuit is reset, and a low to high transition is necessary to generate an interrupt.
b. The interrupt mask register is cleared.
c. The IR_7 input is assigned priority 7 (lowest priority)
d. Slave mode address is set to 7.
e. The Special Mask Mode is cleared, and the Status Read is set to IRR.
f. All ICW4 functions are cleared if IC4 = 0, resulting in a change to Non-Buffered mode, no-Auto EOI, and 85 mode.

Note: Master/slave in ICW4 can only be used in buffered mode.

(i) Initialization Command Words 1 and 2 (ICW1 and ICW2)

A_4 thru A_{15}: (Starting address of interrupt service routines)
In 85 mode, 8 request levels CALL 8 locations at equivalent intervals in the memory. The memory location interval can be set at this stage to 4 or 8 by program. (→ADI)Hence, either 32 or 64 bytes/page respectively are used in the 8 routines.
The address format is 2 bytes long (A_0 thru A_{15}). When the routine interval is 4, A_0 thru A_4 are inserted automatically by the MSM82C59A-2, and A_5 thru A_{15} are programmed externally. When the interval is 8, on the other hand, A_0 thru A_5 are inserted automatically by the MSM82C59A-2, and A_6 thru A_{15} are programmed externally. In 86 mode, T_3 thru T_7 are inserted in the 5 most significant bits of the vector type. And the MSM82C59A-2 sets the 3 least significant bits according to the interrupt level. A_0 thru A_{10} are ignored, and the ADI (address interval) has no effect.

LTIM: The MSM82C59A-2 is operated in level triggered mode when LTIM = 1, and the interrupt input edge circuit becomes disabled.

ADI: Designation of the CALL address interval. Interval = 4 when ADI = 1, and interval = 8 when ADI = 0.

SNGL: SNGL = 1 indicates the existence of only one MSM82C59A-2 in the system. ICW3 is not required when SNGL = 1.

IC4: ICW4 is required when this bit is set, but not required when IC4 = 0.

(ii) Initialization Command Word 3 (ICW3)

This command word is written when there is more than one MSM82C59A-2 used in cascade connections in the system, and is loaded into an 8-bit slave register. The functions of this slave register are listed below.

a. In a master mode system (BUF = 1 and M/ S = 1 in ICW4 or $\overline{SP}/\overline{EN}$ = 1). "1" is set in each bit where a slave has been connected.
   In 85 mode, the master MSM82C59A-2 releases byte 1 of the CALL sequence to enable the corresponding slave to release byte 2 or 3 (only byte 2 in 86 mode) through the cascade line.
b. In slave mode (BUF = 1 and M/S = 0 in ICW4 or $\overline{SP}/\overline{EN}$ = 0). Bits 0 thru 2 identify the slave. The slave compares these bits with the cascade input, and releases bytes 2 and 3 of the CALL sequence (only byte 2 in 86 mode) if a matching result is obtained.

(iii) Initialization Command Word 4 (ICW4)

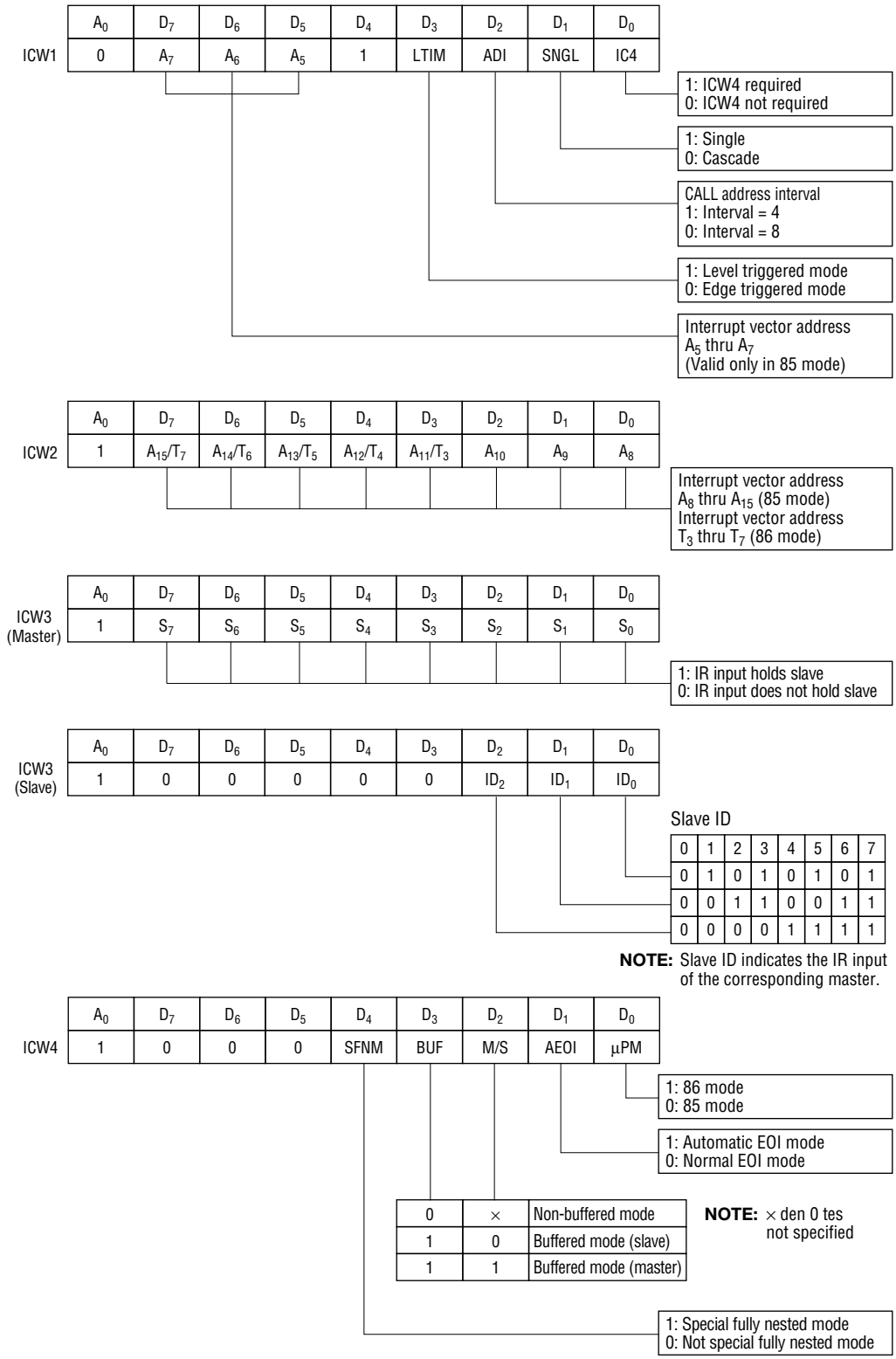
SFNM: Special Fully Nested Mode is programmed when SFNM = 1.

BUF: Buffered mode is programmed when BUF = 1. In Buffered mode, $\overline{SP}/\overline{EN}$ is an output, and Master/slave is selected by the M/S bit.

M/S: If buffered mode is selected, the MSM82C59A-2 is programmed as the master when M/S = 1, and as a slave when M/S = 0. M/S is ignored, however, when BUF = 0.

AEOI: Automatic End Of Interrupt mode is programmed by AEOI = 1.

µPM: (Microprocessor mode)
The MSM82C59A-2 is set to 85 system operation when µPM = 0, and to 86 system operation when µPM = 1.



Initialization Command Words (ICW1 thru ICW4)

(6) Operation Command Words (OCW1 thru OCW3)

When Initialization Command Words (ICWs) are programmed in the MSM82C59A-2, the interrupt input line is ready to receive interrupt requests. The Operation Command Words (OCWs) enable the MSM82C59A-2 to be operated in various modes while the device is in operation.

(i) Operation Command Word 1 (OCW1)
OCW1 sets and resets the mask bits of the Interrupt Mask Register (IMR). M0 thru M7 represent 8 mask bits. The channel is masked when M = 1, but is enabled when M = 0.

(ii) Operation Command Word 2 (OCW2)
R, SL, EOI: The Priority Rotation and End of Interrupt mode plus combinations of the two are controlled by combinations of these 3 bits. These combinations are listed in the operation command word format table.
L2, L1, L0: These bits indicate the specified interrupt level when SL = 1.

(iii) Operation Command Word 3 (OCW3)
ESMM: This enables the Special Mask Mode. The special mask mode can be set and reset by the SMM bit when ESMM = 1. The SMM bit is ignored when ESMM = 0.
SMM: (Special Mask Mode)
The MSM82C59A-2 is set to Special Mask Mode when ESMM = 1 and SMM = 1, and is returned to normal mask mode when ESMM = 1 and SMM = 0. SMM is ignored when ESMM = 0.

	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0

Interrupt Mask
1: Mask set
0: Mask reset

	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OCW2	0	R	SL	EOI	0	0	L2	L1	L0

Active IR Level

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

0	0	1	Non-specific EOI command	End of interrupt
0	1	1	Specific EOI command (NOTE)	
1	0	1	Rotate on non-specific EOI command	Automatic rotation
1	0	0	Rotate in automatic EOI mode (SET)	
0	0	0	Rotate in automatic EOI mode (Clear)	
1	1	1	Rotate on specific EOI command (NOTE)	Specific rotation
1	1	0	Set priority comand (NOTE)	
0	1	0	No operation	

NOTE: L0 thru L2 used

	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OCW3	0	0	ESMM	SMM	0	1	P	RR	RIS

Read Register Command

0	1	0	1
0	0	1	1
No operation		Read IRR by next $\overline{RD}$	Read ISR by next $\overline{RD}$

Polling
1: Poll command
0: No-poll command

Special Mask Mode

0	1	0	1
0	0	1	1
No operation		Reset special mask mode	Set special mask mode

Operation Command Words (OCW1 thru OCW3)

(7) Fully Nested Mode

As long as the MSM82C59A-2 has not been programmed to another mode, this Fully Nested mode is set automatically after initialization. The interrupt requests are ordered in priority sequentially from 0 to 7 (where 0 represents highest priority). If an interrupt is then requested and is acknowledged highest priority, a corresponding vector address is released, and the corresponding bit in the in-service register (ISR) is set. The IS bit remains set until an End of Interrupt (EOI) command is issued from the microprocessor before returning from the interrupt service routine, or until the rising edge of the last $\overline{\text{INTA}}$ pulse arrives when the AEOI bit has been set.
When the IS bit is set, interrupts of the same or lower priority are inhibited - only interrupts of higher priority can be generated. In this case, interrupts can be acknowledged only when the internal interrupt enable F/F in the microprocessor has been enabled again through software. Following the initialization sequence, IR0 has the highest priority, and IR7 has the lowest. This priority can be changed by rotating priority mode in OCW2.

(8) End of Interrupt (EOI)

When the AEOI bit in ICW4 is set, the in-service (IS) bit is automatically reset by the rising edge of the last $\overline{\text{INTA}}$ pulse, or else is reset only when an EOI command is issued to the MSM82C59A-2 prior to returning from the interrupt service routine.
And in cascade mode, the EOI command must be issued twice - once for the master, and once for the corresponding slave.
EOI commands are classified into specific EOI commands and Non-Specific EOI commands. When the MSM82C59A-2 is operated in Fully Nested mode, the IS bit to be reset can be determined on EOI. If the Non-Specific EOI command is issued, the highest IS bit of those that are set is reset automatically, because the highest IS level is always the last servicing level in the Fully Nested mode, the MSM82C59A-2 will no longer be able to determine the last acknowledged level. In this case, it will be necessary to issue a Specific EOI which includes the IS level to be reset as part of the command. When the MSM82C59A-2 is in Special Mask mode, care must be taken to ensure that IS bits masked by the IMR bit can not reset by the Non-Specific EOI.

(9) Automatic End of Interrupt (AEOI) Mode

When AEOI = 1 in ICW4, the MSM82C59A-2 continues to operate in AEOI mode until programmed again by ICW4. In this mode, the MSM82C59A-2 automatically performs Non-Specific EOI operation at the rising edge of the last $\overline{\text{INTA}}$ pulse (the third pulse in 85 systems, and the second pulse in 86 systems). In terms of systems, this mode is best used in nested multiple level interrupt configurations. It is not necessary when there is only one MSM82C59A-2. AEOI mode is only used in a master MSM82C59A-2 device, not in a slave.

(10) Automatic Rotation (Devices with Equal Priority)

In some applications, there is often a number of devices with equal priority. In this mode, the device where an interrupt service has just been completed is set to the lowest priority. At worst, therefore, a particular interrupt request device may have to wait for seven other devices to be serviced at least once each. There are two methods for Automatic Rotation using OCW2 - Rotation on Non-Specific EOI command, and Rotation in Automatic EOI mode.

Before Rotation
(IR4 the highest priority requesting service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
IS Status	0	1	0	1	0	0	0	0
Priority Status	7	6	5	4	3	2	1	0

Lowest Highest

After Rotation
(IR4 was serviced, all other priorities rotated correspondingly)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
IS Status	0	1	0	0	0	0	0	0
Priority Status	2	1	0	7	6	5	4	3

Highest Lowest

(11) Specific Rotation (Specific Priority)

All priority levels can be changed by programming the lowest priority level (Set Priority Command in OCW2). For example, if IR5 is programmed as the device of lowest priority, IR6 will have the highest priority. In this mode, the internal status can be updated during OCW2 by software control. This is unrelated, however, to the EOI command in the same OCW2.
Priority level can also be changed by using the OCW2 Rotate On Specific EOI command.

(12) Interrupt Mask

Interrupt inputs can be masked individually by Interrupt Mask Registers (IMR) programmed through the OCW1. Each interrupt channel is masked (disabled) when the respective IMR bit is set to "1". IR0 is masked by bit 0, and IR1 is masked by bit 1. Masking of any particular channel has no effect on other channels.

(13) Special Mask Mode

In some applications, there is a need for dynamic updating of the system's priority level structure by software control during execution of an interrupt service routine. For example, it may be necessary to inhibit the lower priority requests for part of the execution of a certain routine while enabling for another part. In this case, it is difficult to enable all lower priority requests if the IS bit has not yet been reset by the EOI command after an interrupt request has been acknowledge (during execution of a service routine). All of these requests would normally be disabled.
Hence the use of the Special Mask mode. When a mask bit is set by OCW1 in this mode, the corresponding interrupt level requests are disabled. And all other unmasked level requests (at both higher and lower priority levels) are enabled. Interrupts can thus be enabled selectively by loading the mask register.
In this mode, the specific EOI Command should be used.
This Special Mask mode is set by OCW3 ESMM = 1 and SMM = 1, and reset by ESMM = 1 and SMM = 0.

(14) POLL Command

In this mode, the INT output is not used, the internal interrupt enable F/F of the microprocessor is reset, and interrupt inputs are disabled. Servicing the I/O device is executed by software using the Poll command.
The Poll command is issued by setting P in OCW3 to "1". The MSM82C59A-2 regards the next $\overline{RD}$ pulse as reception of an interrupt, and if there is a request, the corresponding IS bit is set and the priority level is read out. Interrupts are frozen between $\overline{WR}$ and $\overline{RD}$.

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Poll Word	1	0	0	0	0	W2	W1	W0

W0 thru W2: Binary coded highest priority level of service being requested.
1: Set to "1" when there is an interrupt.

This mode is useful when there is a command routine for a number of levels, and the $\overline{INTA}$ sequence is not required. ROM space can thus be saved.

(15) Reading MSM82C59A-2 Status

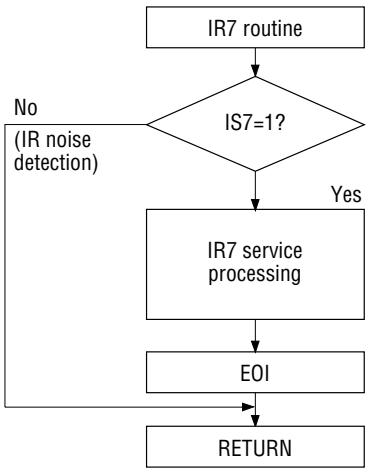
The status of a number of internal registers can be read out for updating user information on the system. The following registers can be read by means of OCW3 (IRR and ISR) and OCW1 (IMR).

a. IRR: (Interrupt Request Register) 8-bit register for storing interrupt requesting levels.
b. ISR: (In-Service Register) 8-bit register for storing priority levels being serviced.
c. IMR: (Interrupt Mask Register) 8-bit register for storing interrupt request lines to be masked.

The IRR can be read when a Read Register Command is issued with OCW3 (RR = 1 and RIS = 0) prior to the $\overline{RD}$ pulse, and the ISR can be read when a Read Register command is issued with OCW3 (RR = 1 and RIS = 1) prior to the $\overline{RD}$ pulse. And as long as the read status does not change, OCW3 is not required each time before the status is read. This is because the MSM82C59A-2 remembers whether IRR or ISR was selected by the previous OCW3. But this is not true when poll is used.
The MSM82C59A-2 is set to IRR after initialization. OCW3 is not required to read IMR. IMR is issued to the data bus if $\overline{RD}$ = 0 and A_0 = 1 (OCW1).
Reading status is disabled by polling when P = 1 and RR = 1 in OCW3.

(16) Edge and Level Trigger Mode

This mode is programmed by using bit 3 (LTIM) in ICW1. When LTIM = 0, the interrupt request is recognized by the IR input transition from Low to High. As long as the IR input is kept at High, no other interrupt is generated. Since interrupt requests are recognized by the IR input "H" level when LTIM = 1, edge detection is not required.
The interrupt request must be cancelled before output of the EOI command, and before the interrupt is enabled in order to prevent the generation of a second interrupt by the CPU. The IR input must be held at High level until the falling edge of the first $\overline{INTA}$ pulse, irrespective of whether edge sense or level sense is employed. If the IR input is switched to Low level before the first $\overline{INTA}$ pulse, the default IR7 is generated when the interrupt is acknowledged by the CPU. This can be an effective safeguard to be adopted to detect interrupts generated by the noise glitches on the IR inputs. To take advantage of this feature, the IR7 routine is used as a "clean up" routine where the routine is simply executing a return instruction and the interrupt is subsequently ignored. When the IR7 is required for other purposes, the default IR7 can be detected by reading the ISR. Although correct IR7 interrupts involve setting of the corresponding ISR bit, the default IR7 is not set.



(17) Special Fully Nested Mode

This mode is used in large systems where the cascade mode is used and the respective Interrupt Requests within each slave have to be given priority levels. In this case, the Special Fully Nested mode is programmed to the master by using ICW4. This mode is practically identical to the normal Fully Nested mode, but differs in the following two respects.

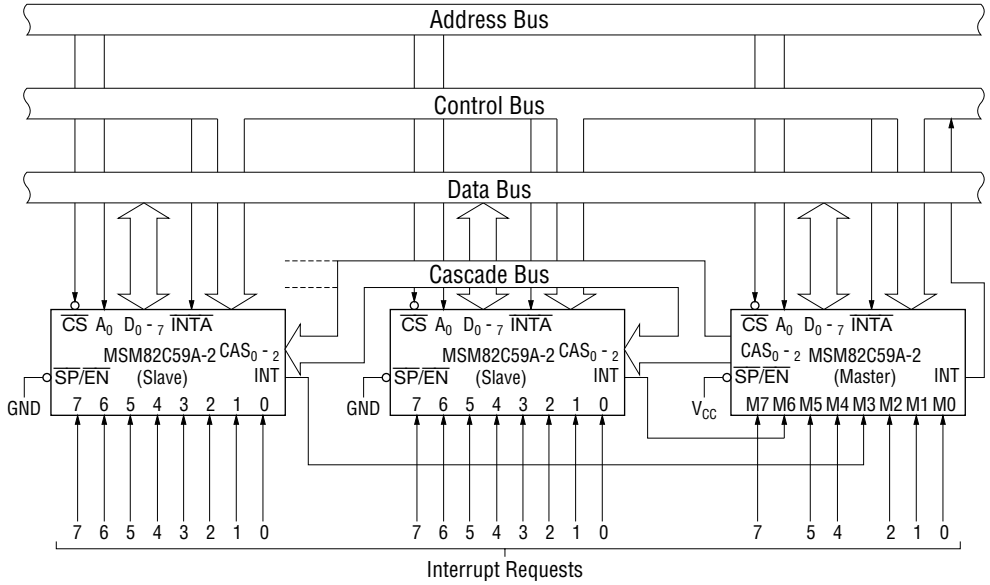
a. When an interrupt request is received from a particular slave during servicing, a new interrupt request from an IR with a higher priority level than the interrupt level of the slave being serviced is recognized by the master and the interrupt is applied to the processor without the master priority logic being inhibited by the slave. In normal Fully Nested mode, if the request is in service, a slave is masked and no other requests can be recognized from the same slave.
b. When exiting from an interrupt service routine, it is first necessary to check whether or not the interrupt which has just been serviced by soft ware was the only interrupt from that slave. This is done by sending a Non-Specific EOI command to that slave, followed by reading of the In-Service Register (ISR) to see whether that register has become all '0'. A Non-Specific EOI is sent to the master too if the ISR is empty, and if not no EOI should be sent.

(18) Buffered Mode

Control for buffer enabling is required when the MSM82C59A-2 is used in a large system where a data bus drive buffer is needed and cascade mode is used. When buffered mode is selected, the MSM82C59A-2 sends an enable signal on the $\overline{SP}/\overline{EN}$ pin to enable the buffer. In this mode, the $\overline{SP}/\overline{EN}$ output always becomes active while the MSM82C59A-2's data bus output is enabled. Therefore, the MSM82C59A-2 requires programming to enable it to distinguish master from slave. Buffered mode is programmed by bit 3 in ICW4, and the ability to distinguish master from slave is programmed by bit 2 in ICW4.

(19) Cascade Mode

To enable the MSM82C59A-2 to handle up to 64 priority levels, a maximum of 8 slaves can be easily connected to one master device.
The master controls the slaves through three cascade lines, the cascade bus executes like a slave chip select during the $\overline{INTA}$ sequence.
In cascade configuration, slave interrupt outputs (INT) are connected to master interrupt request inputs (IR). When a slave IR becomes active and is acknowledged, the master enables the corresponding slave to release the routine address for that device during bytes 2 and 3 (only byte 2 in 86 mode) of the $\overline{INTA}$ sequence.
The cascade bus line is normally kept at low level, and holds the slave address during the period from the rising edge of the first $\overline{INTA}$ pulse up to the rising edge of the third $\overline{INTA}$ pulse (or the second $\overline{INTA}$ pulse in 86 mode).
Each MSM82C59A-2 device in the system can operate in different modes in accordance with their initialization sequences. EOI commands must be issued twice, once for the master once for the corresponding slave. Each MSM82C59A-2 requires an address decoder to activate the respective chip select (CS) inputs.
Since the cascade line is normally kept at low level, note that slaves must be connected to the master IR_0 only after all slaves have been connected to the other IRs.



MSM82C59A-2 Cascade Connections

Precautions for operation

Contents: In the case of a cascade edge trigger, the low level width (TILIH) of a slave INT signal may be less than the low level width (TJLJH:100 ns min.) of a master IR input signal. This occurs when an interruption request with high order priority is provided to the slave unit before the INTA cycle ends. Fig.1 shows a system configuration, Fig.2 a bug operation timing chart, and Fig.3 a normal operation timing chart. TILIH is not specified.

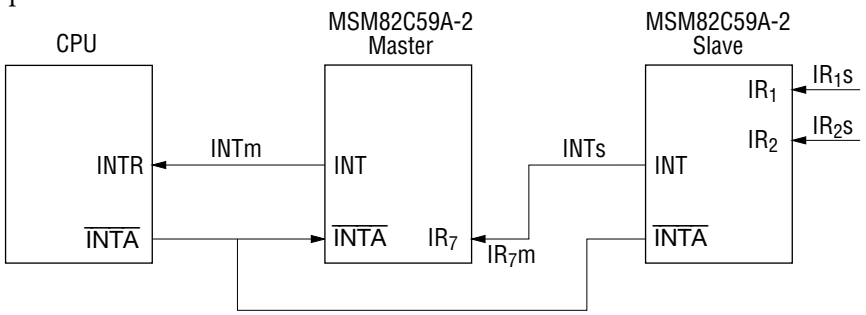


Fig. 1 System Configuration

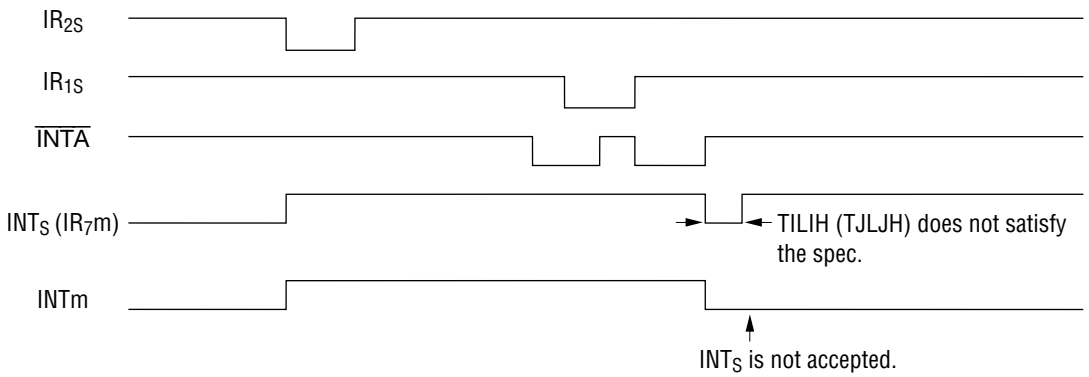


Fig. 2 Bug Operation Timing Chart

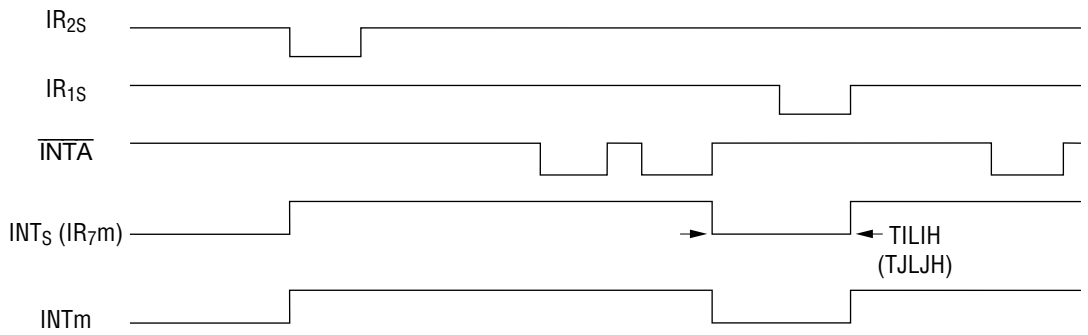
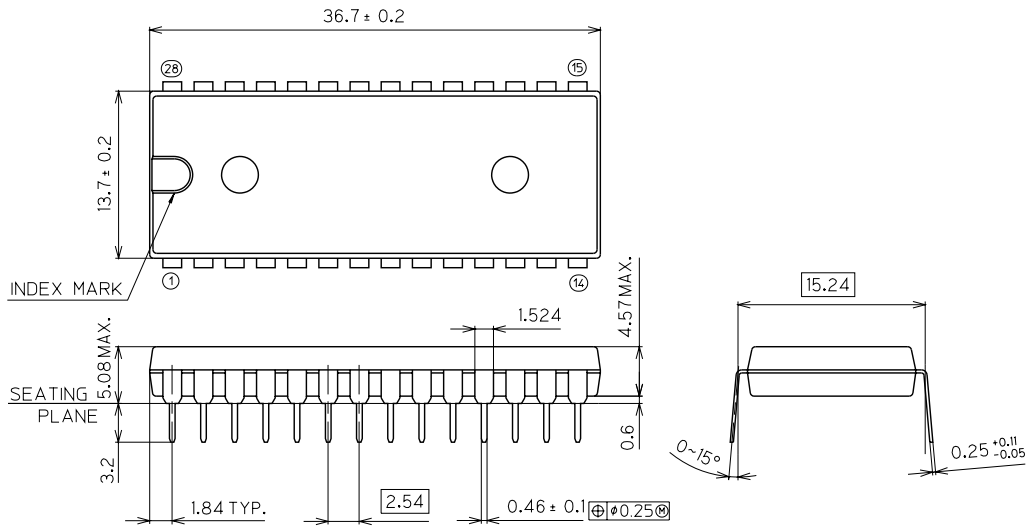


Fig. 3 Normal Operation Timing Chart

PACKAGE DIMENSIONS

(Unit : mm)

DIP28-P-600-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	4.30 TYP.
Rev. No./Last Revised	2/Dec. 11, 1996

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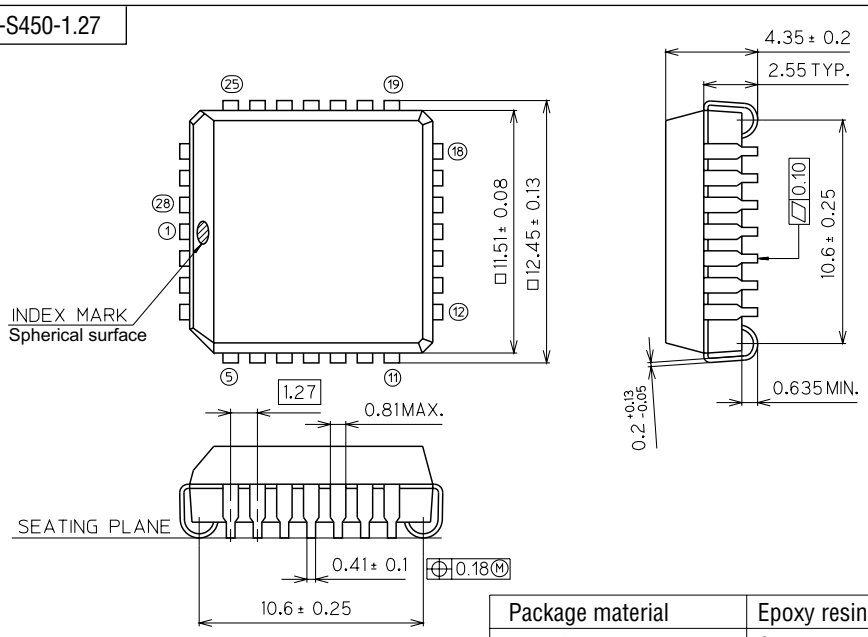
(Unit : mm)

QFJ28-P-S450-1.27



Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	1.00 TYP.
Rev. No./Last Revised	3/Nov. 11, 1996

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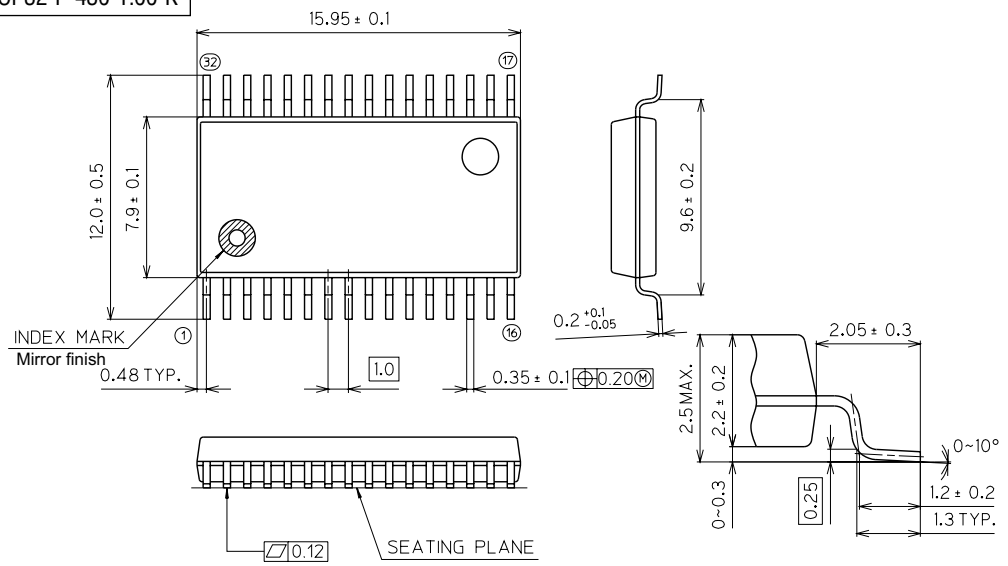
(Unit : mm)

SSOP32-P-430-1.00-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	0.60 TYP.
Rev. No./Last Revised	3/Dec. 5, 1996

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