



PECL OUTPUT VCXO IN 9x14 mm FR4/PCB SMD PACKAGE - VCFRPE Series

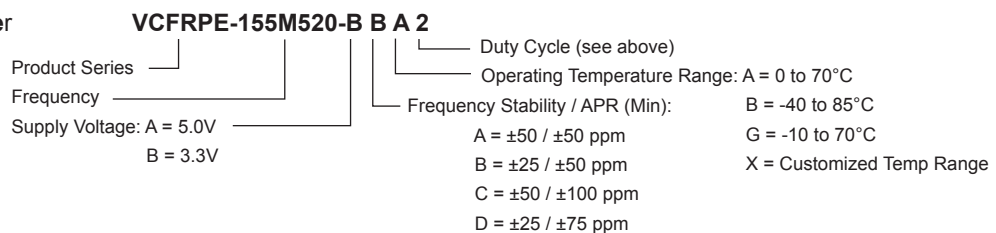
FEATURES

- RoHS Compliant (Pb-Free), Low Phase Jitter, EMI Shielded, Complementary Output Standard
- Commercial or Industrial Temperature Range, Wide Pull Range Available
- Low Profile SMD Package with Industry Standard Footprint, Compatible with J-Leaded Package

SPECIFICATIONS

Frequency Range	10 MHz to 200 MHz (PECL, Vcc=5V); to 622.08 MHz (LV-PECL, Vcc=3.3V)
Input Voltage (Vcc)	A = +5 VDC \pm 5%; B = +3.3 VDC \pm 5%
Input Current	40 mA Max @ 10.0 MHz - 40 MHz; 60 mA Max @ 40.001 MHz - 100 MHz; 100 mA Max @ 100.001 MHz - 622.08 MHz
Control Voltage (Vc)	+2.5V \pm 2.0V for 5.0V part; +1.65V \pm 1.35V for 3.3V part
Storage Temperature	-55°C to 125°C
Frequency Stability / APR (Min)	B = \pm 25 / \pm 50 ppm; C = \pm 50 / \pm 100 ppm; D = \pm 25 / \pm 75 ppm; E = \pm 20 / \pm 50 ppm
Temperature Range	A = 0°C to 70°C; B = -40°C to 85°C; G = -10°C to 70°C
Standard Stability / Pullability	BA = \pm 25 ppm / 0°C to 70°C, Absolute pull range (APR): \pm 50 ppm Minimum
Duty Cycle	0/1 = Non-tristate/Tristate 60/40% symmetry; 2/3 = Non-tristate/Tristate 55/45% symmetry
Output Load	50 Ohms to Vcc-2V or Thevenin Equiv. Bias Required
Logic "1" / Logic "0" Level	Vcc-0.96 Min, Vcc-0.81 Max / Vcc-1.85 Min, Vcc-1.65 Max
Rise/Fall Time (Tr/Tf)	1 ns Maximum at 20% to 80% Vp-p
Start-up time	10 ms Maximum
Phase Jitter (RMS, 1 Sigma)	0.4 ps Typical for fj = 12KHz to 20MHz, Multiplier IC for frequency > 155.520MHz
Modulation Bandwidth	10 kHz Minimum at -3 dB
Linearity / Slope	\pm 20% Maximum of best straight line fit / Positive
Setability at Fnom, 25°C	+2.5V \pm 0.5V for 5.0V part; +1.65V \pm 0.4V for 3.3V part
Aging	\pm 5 ppm Maximum / Year
Tristate Function	Input (Pin 2) High (> 2.5V): Output disabled Input (Pin 2) Low (< 0.5V) or floating: Output active
Enable/Disable Time	100 ns Maximum

Creating a Part Number



OUTLINE DRAWING

