

## ISD15100 SERIES

**nuvoTon**



# ISD15100 Series

**Multi-Message Record/Playback Devices**

**with Digital Audio Interface**

*Publication Release Date: May 6, 2011*

- 1 -

*Revision 1.3*

# ISD15100 SERIES



## TABLE OF CONTENTS

|       |  |    |
|-------|--|----|
| 1     | GENERAL DESCRIPTION .....                    | 3  |
| 2     | FEATURES .....                               | 3  |
| 3     | BLOCK DIAGRAM .....                          | 5  |
| 4     | PINOUT CONFIGURATION .....                   | 7  |
| 5     | PIN DESCRIPTION.....                         | 8  |
| 6     | ELECTRICAL CHARACTERISTICS .....             | 11 |
| 6.1   | ABSOLUTE MAXIMUM RATINGS .....               | 11 |
| 6.2   | OPERATING CONDITIONS .....                   | 11 |
| 6.3   | DC PARAMETERS .....                          | 11 |
| 6.4   | AC PARAMETERS .....                          | 13 |
| 6.4.1 | Internal Oscillator .....                    | 13 |
| 6.4.2 | Inputs .....                                 | 13 |
| 6.4.3 | Outputs.....                                 | 14 |
| 6.4.4 | SPI Timing .....                             | 15 |
| 6.4.5 | I <sup>2</sup> S Timing .....                | 17 |
| 7     | APPLICATION DIAGRAM.....                     | 18 |
| 8     | PACKAGE SPECIFICATION .....                  | 19 |
| 8.1   | 48 LEAD LQFP(7x7x1.4MM FOOTPRINT 2.0MM)..... | 19 |
| 9     | ORDERING INFORMATION.....                    | 20 |
| 10    | REVISION HISTORY.....                        | 21 |

# ISD15100 SERIES



---

## 1 GENERAL DESCRIPTION

The ISD15100 series is a multi-message ChipCorder<sup>®</sup> featuring digital compression, comprehensive memory management, flash storage, and integrated analog/digital audio signal paths. The message management feature is designed to make message recording simple and address-free as well as make code development easier for playback-only applications. This family utilizes flash memory to provide non-volatile audio record/playback with durations up to 16 minutes for a single-chip solution. Unlike other ChipCorder series, the ISD15100 series provides an I<sup>2</sup>S digital audio interface, faster digital recording, higher sampling frequency, and a signal path with SNR equivalent to 12bit resolution.

The ISD15100 series can take digital audio data via I<sup>2</sup>S or SPI interface. When I<sup>2</sup>S input is selected, it will replace the analog audio inputs and will support sample rates of 32, 44.1 or 48 kHz depending upon clock configuration. When SPI interface is chosen, the sample rate of the audio data sent must be one of the ISD15100 supported sample rates.

The ISD15100 series has built-in analog audio inputs, analog audio line driver, and speaker driver output. The two analog audio inputs to the device are: (1) AUXIN has a fixed gain configured by SPI command, and (2) ANAIN/ANAOOUT has a fixed gain amplifier with the gain set by two external resistors. ANAIN/ANAOOUT can also be used as a microphone differential input (ANAIN/ANAOOUT becomes MIC+/MIC-) in conjunction with an automatic gain control (AGC) circuit configured by SPI command. Analog outputs are available in three forms: (1) AUXOUT is a single-ended voltage output; (2) AUDOUT can be configured as either a single-ended voltage output or a single-ended current output; (3) BTL (bridge-tied-load) is a differential voltage output.

## 2 FEATURES

- Fast Digital Programming
  - Programming rate can go up to 1Mbits/second mainly limited by the flash memory write rate.
- Duration
  - 2 to 16 minutes based on 8kHz/4bit ADPCM
- Message Management
  - Perform address-free recording: The ISD15100 allocates memory for new recording requests and upon completion, returns a start address to the host via SPI interface
  - Store pre-recorded audio (Voice Prompts) using high quality digital compression
  - Use a simple index based command for playback
  - Execute pre-programmed macro scripts (Voice Macros) designed to control the configuration of the device and play back Voice Prompts sequences and message recordings.
- Sample Rate
  - Seven record and playback sampling frequencies are available for a given master sample rate. For example, the record and playback sampling frequencies of 4, 5.3, 6.4, 8, 12.8, 16 and 32kHz\* are available when the device is clocked at a 32kHz master sample rate.
  - For I<sup>2</sup>S operation, 32, 44.1 and 48kHz master sample rates are available with record and playback sampling frequencies scaling accordingly.
- Compression Algorithms
  - For recording
    - ADPCM: 2, 3, 4 or 5 bits per sample
    - $\mu$ -Law: 6, 7 or 8 bits per sample
    - Differential  $\mu$ -Law: 6, 7 or 8 bits per sample
    - PCM: 8, 10 or 12 bits per sample. Each sampled value is stored as a code, offering no compression but preserving maximum resolution
  - For Pre-Recorded Voice Prompts

*Publication Release Date: May 6, 2011*

## ISD15100 SERIES

**nuvoTon**

- $\mu$ -Law: 6, 7 or 8 bits per sample
- Differential  $\mu$ -Law: 6, 7 or 8 bits per sample
- PCM: 8, 10 or 12 bits per sample
- Enhanced ADPCM: 2, 3, 4 or 5 bits per sample
- Variable-bit-rate optimized compression. This allows best possible compression given a metric of SNR and background noise levels.
- Oscillator
  - Internal oscillator with internal reference: 2.048 MHz with  $\pm 10\%$  deviation
  - Internal oscillator with external resistor: 2.048 MHz with  $\pm 5\%$  deviation when  $R_{osc}$  is 80k-ohm
  - External crystal or clock input
  - I<sup>2</sup>S bit clock input
  - Crystals and resonators support standard audio sampling rates of 2.048, 4.096, 8.192, 12.288 and 11.2896MHz
- Inputs
  - AUXIN: Analog input with 2-bit gain control configured by SPI command
  - ANAIN/ANAOULT:
    - Analog input with the gain set by two external resistors from ANAOULT to ANAIN, or
    - Microphone differential input (ANAIN/ANAOULT becomes MIC+/MIC-)
  - Digital AGC:
    - Automatic gain control of digitized data from the analog input
- Outputs
  - PWM: Class D speaker driver to direct drive an 8 $\Omega$  speaker or buzzer
  - AUDOUT: configurable as a current or voltage single-ended line driver
  - AUXOUT: a single-ended voltage output
  - BTL: a differential voltage output
- I/Os
  - SPI interface: MISO, MOSI, SCLK, SSB for commands and digital audio data
  - I<sup>2</sup>S interface: I<sup>2</sup>S\_CLK, I<sup>2</sup>S\_WS, I<sup>2</sup>S\_SDI, I<sup>2</sup>S\_SDO for digital audio data
  - 8 GPIO pins (4 of the 8 GPIO pins share with I<sup>2</sup>S).
- Three 8-bit Volume Control set by SPI command for flexible mixing
  - VOLA: volume control for the digital audio data from I<sup>2</sup>S or analog inputs
  - VOLB: volume control for the digital audio data from decompression block or SPI
  - VOLC: master volume control for PWM, AUDOUT, AUXOUT and I<sup>2</sup>S outputs
- Operating Voltage: 2.7-3.6V
- Standby Current: 1uA typical
- Package: Green 48L-LQFP
- Temperature Options:
  - Industrial: -40°C to 85°C

*Publication Release Date: May 6, 2011*



**3 BLOCK DIAGRAM**

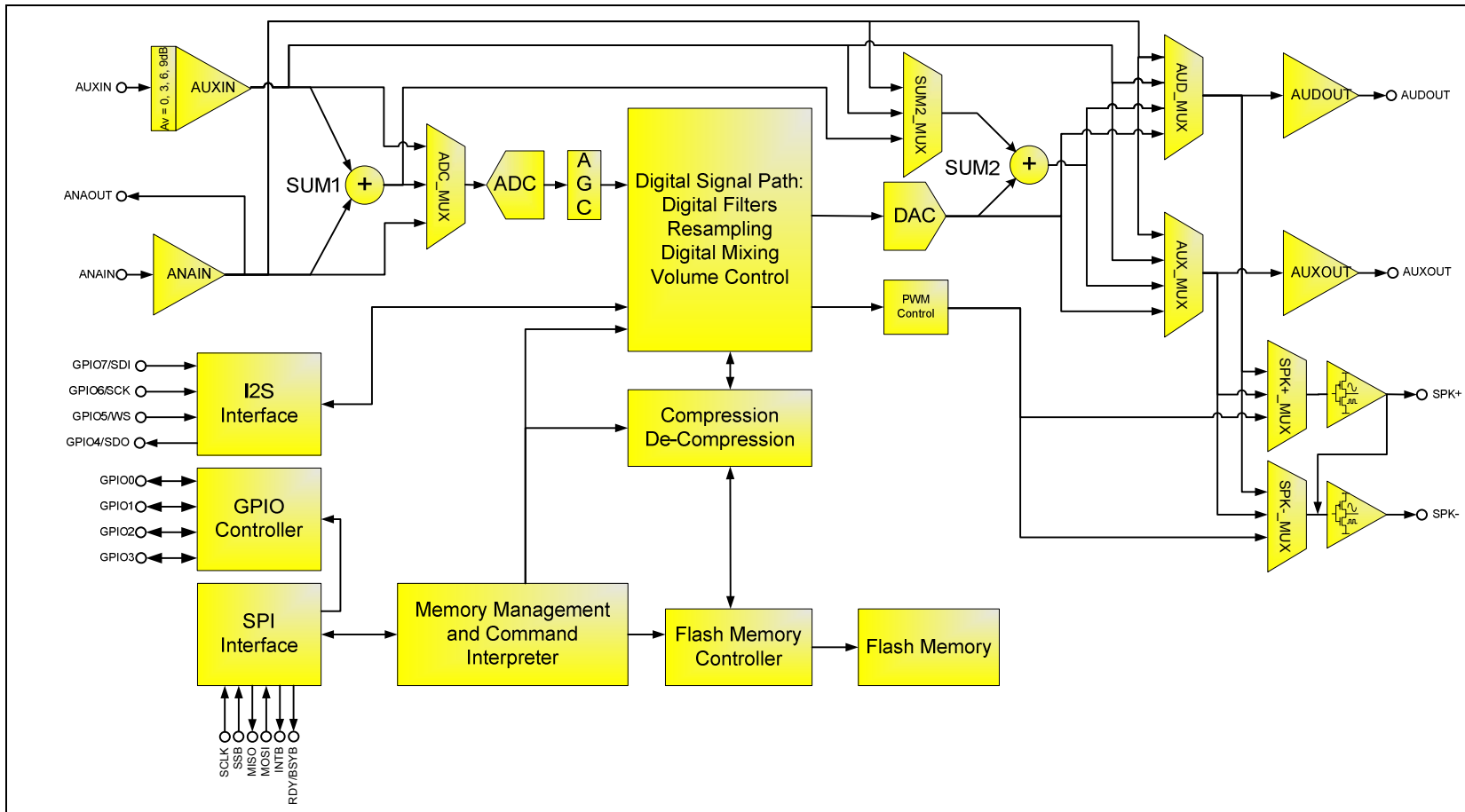


Figure 3-1 ISD15100 Block Diagram, ANAIN Selected

# ISD15100 SERIES

nuvoTon

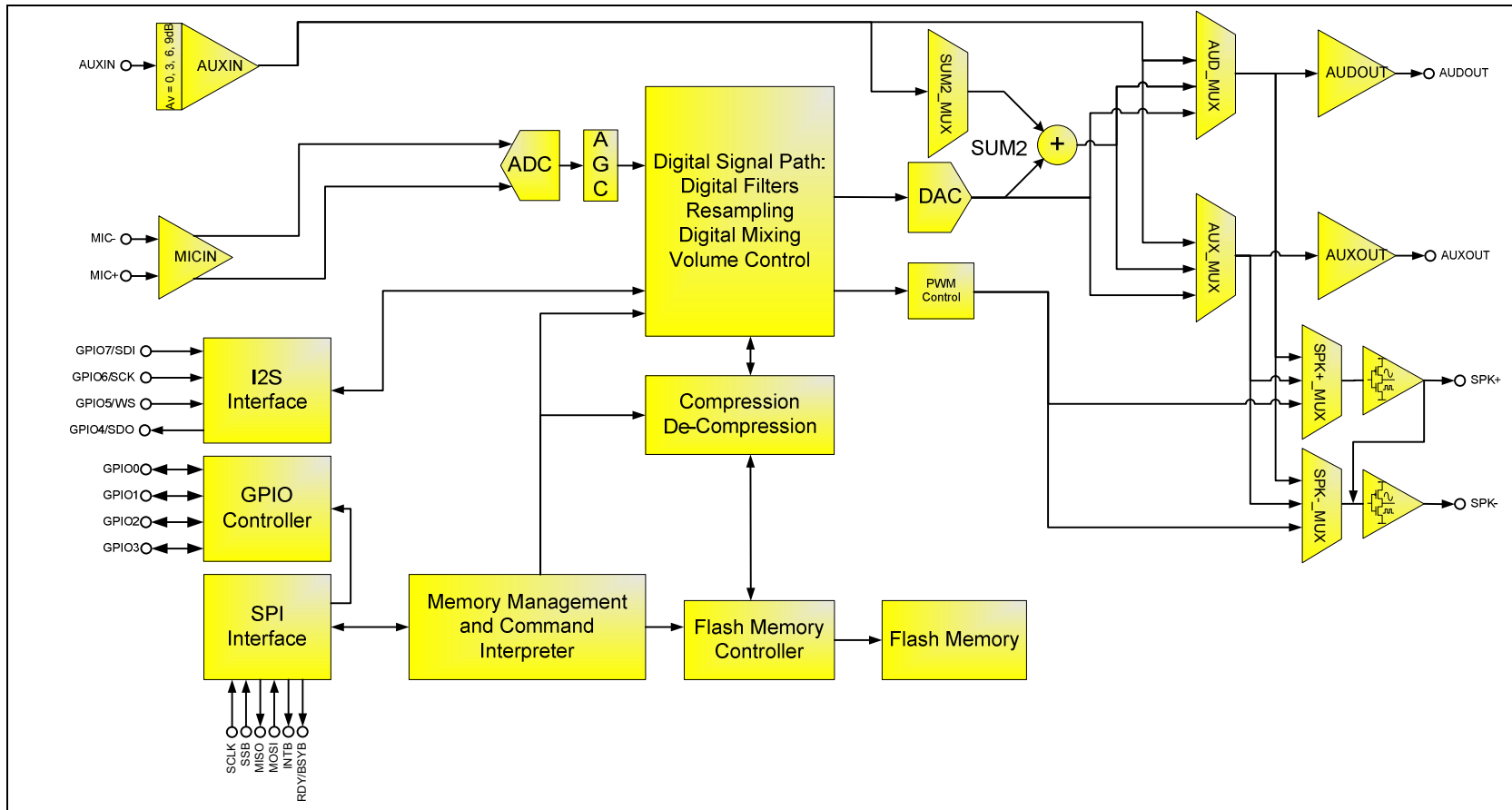


Figure 3-2 ISD15100 Block Diagram, MICIN Selected

Publication Release Date: May 6, 2011

Revision 1.3

# ISD15100 SERIES



## 4 PINOUT CONFIGURATION

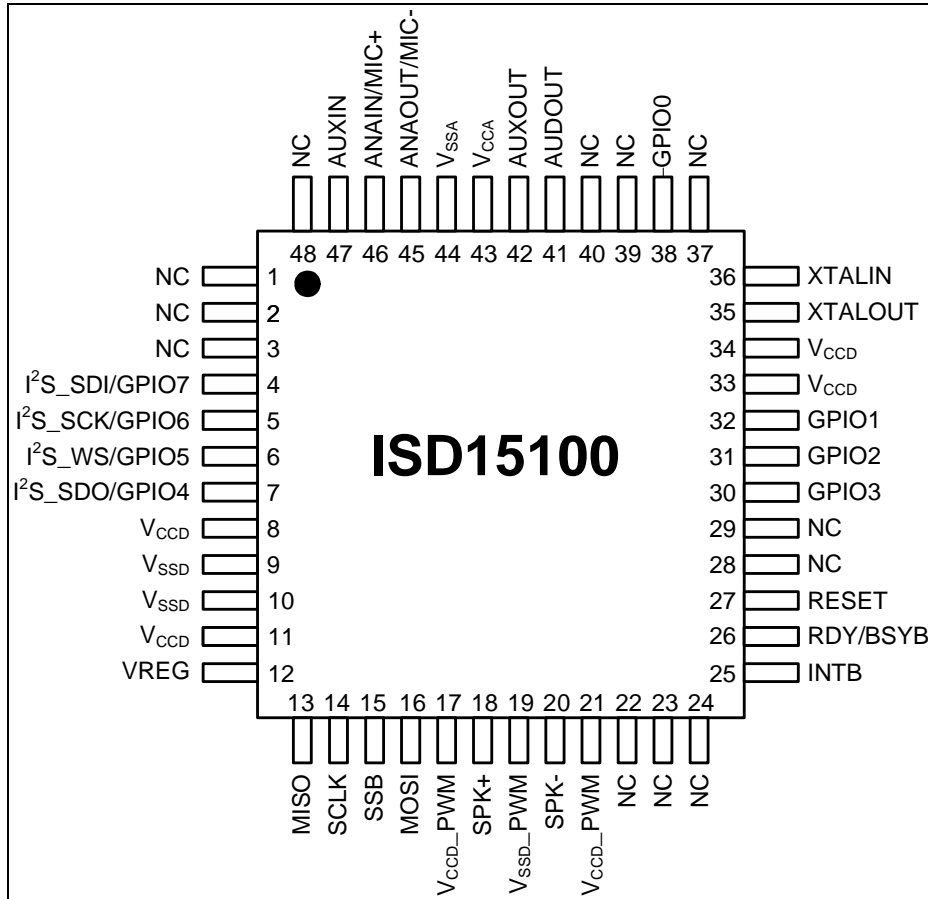


Figure 4-1 ISD15100 48-Lead LQFP Pin Configuration.

**ISD15100 SERIES****nuvoTon****5 PIN DESCRIPTION**

| Pin Number | Pin Name                       | I/O | Function  |
|------------|--------------------------------|-----|---|
| 1          | NC                             |     | This pin should be left unconnected.  |
| 2          | NC                             |     | This pin should be left unconnected.  |
| 3          | NC                             |     | This pin should be left unconnected.  |
| 4          | I <sup>2</sup> S_SDI/<br>GPIO7 | I   | Serial Data Input of the I <sup>2</sup> S interface (If I2S is not used, this pin should be grounded).<br>Or, can be configured as a GPIO pin.  |
| 5          | I <sup>2</sup> S_SCK/<br>GPIO6 | I/O | Clock input in slave mode or clock output in master mode. This pin can be configured as an external clock buffer if I <sup>2</sup> S is not used (If I2S is not used, this pin should be grounded).<br>Or, can be configured as a GPIO pin. |
| 6          | I <sup>2</sup> S_WS/<br>GPIO5  | I/O | Word Select (WS) input in slave mode or WS output in master mode (If I2S is not used, this pin should be grounded).<br>Or, can be configured as a GPIO pin.   |
| 7          | I <sup>2</sup> S_SDO/<br>GPIO4 | O   | Serial Data Output of the I <sup>2</sup> S Interface (If I2S is not used, this pin should be left unconnected).<br>Or, can be configured as a GPIO pin.   |
| 8          | V <sub>CCD</sub>               | I   | Digital power supply.   |
| 9          | V <sub>SSD</sub>               | I   | Digital Ground.   |
| 10         | V <sub>SSD</sub>               | I   | Digital Ground.   |
| 11         | V <sub>CCD</sub>               | I   | Digital power supply.   |
| 12         | VREG                           | O   | A 1.8V regulator to supply the internal logic. A 0.1uF capacitor should be connected to this pin for supply decoupling and stability.   |
| 13         | MISO                           | O   | Master-In-Slave-Out. Serial output from the ISD15100 to the host. This pin is in tri-state when SSB=1.  |
| 14         | SCLK                           | I   | Serial Clock input to the ISD15100 from the host.   |
| 15         | SSB                            | I   | Slave Select input to the ISD15100 from the host. When SSB is low device is selected and responds to commands on the SPI interface.   |
| 16         | MOSI                           | I   | Master-Out-Slave-In. Serial input to the ISD15100 from the host.  |
| 17         | V <sub>CCD_PWM</sub>           | I   | Digital Power for the PWM Driver.   |

Publication Release Date: May 6, 2011

- 8 -

Revision 1.3



**ISD15100 SERIES****nuvoTon**

| Pin Number | Pin Name              | I/O | Function   |
|------------|-----------------------|-----|--|
| 18         | SPK+                  | O   | PWM driver positive output. This SPK+ output, together with SPK- pin, provide a differential output to drive 8Ω speaker or buzzer. During power down this pin is in tri-state.<br>Or, can be configured as BTL which, together with SPK- pin, provide a differential voltage output.<br>Or, can independently switch to AUDOUT or AUXOUT.            |
| 19         | V <sub>SSD</sub> _PWM | I   | Digital Ground for the PWM Driver.   |
| 20         | SPK-                  | O   | PWM driver negative output. This SPK- output, together with SPK+ pin, provides a differential output to drive 8Ω speaker or buzzer. During power down this pin is tri-state.<br>Or, can be configured as BTL which, together with SPK+ pin, provide a differential voltage output.<br>Or, can independently switch to AUDOUT or AUXOUT.              |
| 21         | V <sub>CCD</sub> _PWM | I   | Digital Power for the PWM Driver.  |
| 22         | NC                    |     | This pin should be left unconnected.   |
| 23         | NC                    |     | This pin should be left unconnected.   |
| 24         | NC                    |     | This pin should be left unconnected.   |
| 25         | INTB                  | O   | Active low interrupt request pin. This pin is an open-drain output.  |
| 26         | RDY/BSYB              | O   | An output pin to report the status of data transfer on the SPI interface. "High" indicates that ISD15100 is ready to accept new SPI commands or data.  |
| 27         | RESET                 | I   | Applying power to this pin will reset the chip. (A high pulse of 50ms or more will reset the chip.)  |
| 28         | NC                    |     | This pin should be left unconnected.   |
| 29         | NC                    |     | This pin should be left unconnected.   |
| 30         | GPIO3                 | I/O | GPIO   |
| 31         | GPIO2                 | I/O | GPIO   |
| 32         | GPIO1                 | I/O | GPIO   |
| 33         | V <sub>CCD</sub>      | I   | Digital power supply pin.  |
| 34         | V <sub>CCD</sub>      | I   | Digital power supply pin.  |
| 35         | XTALOUT               | O   | Crystal interface output pin.  |
| 36         | XTALIN                | I   | The CLK_CFG register determines one of the following three configurations: (1) A crystal or resonator connected between the XTALOUT and XTALIN pins. (2) A resistor connected to GND as a reference current to the internal oscillator and left the XTALOUT unconnected. (3) An external clock input to the device and left the XTALOUT unconnected. |

Publication Release Date: May 6, 2011

- 9 -

Revision 1.3

**ISD15100 SERIES****nuvoTon**

| Pin Number | Pin Name         | I/O | Function  |
|------------|------------------|-----|---|
| 37         | NC               |     | This pin should be left unconnected.  |
| 38         | GPIO0            | I/O | GPIO  |
| 39         | NC               |     | This pin should be left unconnected.  |
| 40         | NC               |     | This pin should be left unconnected.  |
| 41         | AUDOUT           | O   | Audio Out. This pin can be either a voltage output or a current output configured by the internal registers via SPI command.<br>If AUDOUT is not used, this pin should be left unconnected.   |
| 42         | AUXOUT           | O   | Aux Out. This pin is an analog voltage output.<br>If AUXOUT is not used, this pin should be left unconnected.   |
| 43         | V <sub>CCA</sub> | I   | Analog power supply pin.  |
| 44         | V <sub>SSA</sub> | I   | Analog ground pin.  |
| 45         | ANAOUT/<br>MIC-  | O   | Variable gain analog output with the gain set by feedback resistance to ANAIN.<br>Or, can be configured as MIC- which, together with MIC+, provides a microphone differential input.<br>If ANAIN/ANAOUT is not used, this pin should be left unconnected. |
| 46         | ANAIN/<br>MIC+   | I   | Variable gain analog input.<br>Or, can be configured as MIC+ which, together with MIC-, provides a microphone differential input.<br>If ANAIN/ANAOUT is not used, this pin should be left unconnected.  |
| 47         | AUXIN            | I   | Auxiliary input with the gain set by SPI command<br>If AUXIN is not used, this pin should be left unconnected.  |
| 48         | NC               |     | This pin should be left unconnected.  |

*Publication Release Date: May 6, 2011**- 10 -**Revision 1.3*

**ISD15100 SERIES****nuvoTon****6 ELECTRICAL CHARACTERISTICS****6.1 ABSOLUTE MAXIMUM RATINGS****ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)<sup>[1]</sup>**

| CONDITIONS   | VALUES   |
|--|--|
| Junction temperature   | 130°C  |
| Storage temperature range                                      | -65°C to +150°C                                      |
| Voltage Applied to any pins                                    | (V <sub>SS</sub> - 0.3V) to (V <sub>CC</sub> + 0.3V) |
| Voltage applied to any pin (Input current limited to +/-20 mA) | (V <sub>SS</sub> - 1.0V) to (V <sub>CC</sub> + 1.0V) |
| Power supply voltage to ground potential                       | -0.3V to +5.0V                                       |

<sup>[1]</sup> Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

**6.2 OPERATING CONDITIONS****OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)**

| CONDITIONS                                       | VALUES   |
|--|--|
| Operating temperature range (Case temperature)   | -40°C to +85°C                                       |
| Supply voltage (V <sub>DD</sub> ) <sup>[1]</sup> | +2.7V to +3.6V                                       |
| Ground voltage (V <sub>SS</sub> ) <sup>[2]</sup> | 0V   |
| Input voltage (V <sub>DD</sub> ) <sup>[1]</sup>  | 0V to 3.6V   |
| Voltage applied to any pins                      | (V <sub>SS</sub> - 0.3V) to (V <sub>DD</sub> + 0.3V) |

NOTES: <sup>[1]</sup> V<sub>DD</sub> = V<sub>CCA</sub> = V<sub>CCD</sub> = V<sub>CCPWM</sub>

<sup>[2]</sup> V<sub>SS</sub> = V<sub>SSA</sub> = V<sub>SSD</sub> = V<sub>SSPWM</sub>

**6.3 DC PARAMETERS**

| PARAMETER               | SYMBOL                   | MIN                  | TYP <sup>[1]</sup> | MAX                 | UNITS | CONDITIONS   |
|-------------------------|--------------------------|----------------------|--------------------|---------------------|-------|--|
| Supply Voltage          | V <sub>DD</sub>          | 2.7                  |                    | 3.6                 | V     |  |
| Input Low Voltage       | V <sub>IL</sub>          | V <sub>SS</sub> -0.3 |                    | 0.3xV <sub>DD</sub> | V     |  |
| Input High Voltage      | V <sub>IH</sub>          | 0.7xV <sub>DD</sub>  |                    | V <sub>DD</sub>     | V     |  |
| Output Low Voltage      | V <sub>OL</sub>          | V <sub>SS</sub> -0.3 |                    | 0.3xV <sub>DD</sub> | V     | I <sub>OL</sub> = 1mA                                      |
| Output High Voltage     | V <sub>OH</sub>          | 0.7xV <sub>DD</sub>  |                    | V <sub>DD</sub>     | V     | I <sub>OH</sub> = -1mA                                     |
| INTB Output Low Voltage | V <sub>OH1</sub>         |                      |                    | 0.4                 | V     |  |
| Record Current          | I <sub>DD_Record</sub>   |                      |                    | 40                  | mA    | V <sub>DD</sub> = 3.6V, No load,<br>Sampling freq = 16 kHz |
| Playback Current        | I <sub>DD_Playback</sub> |                      |                    | 30                  | mA    |  |
| Standby Current         | I <sub>SB</sub>          |                      | 1                  | 10                  | μA    | V <sub>DD</sub> = 3.6V                                     |

Publication Release Date: May 6, 2011

- 11 -

Revision 1.3

## ISD15100 SERIES

nuvoTon

|                       |          |  |  |         |         |                |
|-----------------------|----------|--|--|---------|---------|----------------|
| Input Leakage Current | $I_{IL}$ |  |  | $\pm 1$ | $\mu A$ | Force $V_{DD}$ |
|-----------------------|----------|--|--|---------|---------|----------------|

Notes: <sup>[1]</sup> Conditions  $V_{DD}=3V$ ,  $T_A=25^{\circ}C$  unless otherwise stated

**ISD15100 SERIES****nuvoTon****6.4 AC PARAMETERS****6.4.1 Internal Oscillator**

| PARAMETER   | SYMBOL    | MIN  | TYP       | MAX  | UNITS | CONDITIONS   |
|---|-----------|------|-----------|------|-------|--|
| Internal Oscillator with internal reference               | $F_{INT}$ | -10% | 2.048 MHz | +10% | MHz   | V <sub>DD</sub> = 3V.<br>At room temperature   |
| Internal Oscillator with external resistor <sup>[1]</sup> | $F_{EXT}$ | -5%  | 2.048 MHz | +5%  | MHz   | With 1% precision resistor, 80k-ohm.<br>V <sub>DD</sub> = 3V.<br>At room temperature |

Notes:

<sup>[1]</sup> Characterization data shows that frequency deviation is +/- 5% across temperature and voltage ranges.**6.4.2 Inputs****ANAIN & MICIN**

| PARAMETER                  | SYMBOL        | MIN | TYP <sup>[1]</sup> | MAX | UNITS      | CONDITIONS                  |
|----------------------------|---------------|-----|--------------------|-----|------------|-----------------------------|
| ANAIN Input Voltage        | $V_{ANAIN}$   |     | 10-1000            |     | mV         | Peak-to-Peak <sup>[2]</sup> |
| ANAIN Feed Back Resistance | $R_{ANA(FB)}$ | 40  |                    | 100 | K $\Omega$ |                             |
| MICIN Input Voltage        | $V_{MICIN}$   |     | 5-500              |     | mV         | Peak-to-Peak <sup>[2]</sup> |

Notes: <sup>[1]</sup> Conditions V<sub>DD</sub>=3V, T<sub>AB</sub>=25°C unless otherwise stated<sup>[2]</sup> Depends on Gain Setting**AUXIN**

| PARAMETER                        | SYMBOL           | MIN  | TYP <sup>[1]</sup> | MAX  | UNITS      | CONDITIONS                      |
|----------------------------------|------------------|------|--------------------|------|------------|---------------------------------|
| AUXIN Input Voltage              | $V_{AUXIN}$      |      | 1000               |      | mV         | Peak-to-Peak <sup>[2]</sup>     |
| Gain from AUXIN to AUXOUT/ANAOUT | $A_{AUXIN GAIN}$ |      | 0 to 9             |      | dB         | 4 Gain Steps of 3db each        |
| AUXIN Gain Accuracy              | $A_{AUXIN (GA)}$ | -0.5 |                    | +0.5 | dB         |                                 |
| AUXIN Input Resistance           | $R_{AUXIN}$      |      | 20-40              |      | K $\Omega$ | Depending on AUXIN Gain Setting |

Notes: <sup>[1]</sup> Conditions V<sub>DD</sub>=3V, T<sub>A</sub>=25°C unless otherwise stated.<sup>[2]</sup> With 0db Gain setting.

Publication Release Date: May 6, 2011

**ISD15100 SERIES****nuvoTon****6.4.3 Outputs****AUXOUT**

| PARAMETER                | SYMBOL                        | MIN | TYP <sup>[1]</sup> | MAX | UNITS | CONDITIONS                |
|--------------------------|-------------------------------|-----|--------------------|-----|-------|---------------------------|
| SINAD, AUXIN to AUXOUT   | SINAD <sub>AUXIN_AUXOUT</sub> |     | 80                 |     | dB    | Load 5K <sup>[2][3]</sup> |
| SINAD, ANAIN to AUXOUT   | SINAD <sub>ANAIN_AUXOUT</sub> |     | 80                 |     | dB    | Load 5K <sup>[2][3]</sup> |
| PSRR                     | PSRR <sub>AUXOUT</sub>        |     | -40                |     | dB    | [4]                       |
| DC Bias                  | V <sub>BIAS_AUXOUT</sub>      |     |                    | 1.2 | V     |                           |
| Minimum Load Impedance   | R <sub>L(AUXOUT)</sub>        | 5   |                    |     | KΩ    |                           |
| Maximum Load Capacitance | C <sub>L(AUXOUT)</sub>        |     |                    | 0.1 | nF    |                           |

- Notes:
- <sup>[1]</sup> Conditions V<sub>DD</sub>=3V, T<sub>A</sub>=25°C unless otherwise stated.
  - <sup>[2]</sup> 1 Vpp 1KHz signal applied at AUXIN/ANAIN with 0db Gain setting.
  - <sup>[3]</sup> All measurements are C-message weighted.
  - <sup>[4]</sup> Measured with 1KHz, 100 mVpp sine wave applied to V<sub>CCA</sub> pins.

**AUDOUT**

| PARAMETER                               | SYMBOL                        | MIN | TYP <sup>[1]</sup> | MAX | UNITS | CONDITIONS                |
|---|-------------------------------|-----|--------------------|-----|-------|---------------------------|
| SINAD, AUXIN to AUDOUT <sup>[5]</sup>   | SINAD <sub>AUXIN_AUDOUT</sub> |     | 80                 |     | dB    | Load 5K <sup>[2][3]</sup> |
| SINAD, ANAIN to AUDOUT <sup>[5]</sup>   | SINAD <sub>ANAIN_AUDOUT</sub> |     | 80                 |     | dB    | Load 5K <sup>[2][3]</sup> |
| PSRR <sup>[5]</sup>                     | PSRR <sub>AUDOUT</sub>        |     | -40                |     | dB    | [4]                       |
| DC Bias <sup>[5]</sup>                  | V <sub>BIAS_AUDOUT</sub>      |     |                    | 1.2 | V     |                           |
| Minimum Load Impedance <sup>[5]</sup>   | R <sub>L(AUDOUT)</sub>        | 5   |                    |     | KΩ    |                           |
| Maximum Load Capacitance <sup>[5]</sup> | C <sub>L(AUDOUT)</sub>        |     |                    | 0.1 | nF    |                           |
| Output Current <sup>[6]</sup>           | I <sub>AUDOUT</sub>           | 0   | 3                  | 6   | mA    | [2][6]                    |

- Notes:
- <sup>[1]</sup> Conditions V<sub>CC</sub>=3V, T<sub>A</sub>=25°C unless otherwise stated.
  - <sup>[2]</sup> 1 Vpp 1KHz signal applied at AUXIN/ANAIN with 0db Gain setting.
  - <sup>[3]</sup> All measurements are C-message weighted.
  - <sup>[4]</sup> Measured with 1KHz, 100 mVpp sine wave applied to V<sub>CCA</sub> pins.
  - <sup>[5]</sup> Configured as AUDOUT(Voltage Output).
  - <sup>[6]</sup> Configured as AUDOUT(Current Output).

# ISD15100 SERIES



## SPEAKER OUTPUTS

| PARAMETER               | SYMBOL                       | MIN | TYP <sup>[1]</sup> | MAX | UNITS | CONDITIONS                  |
|-------------------------|------------------------------|-----|--------------------|-----|-------|-----------------------------|
| SNR, AUXIN to SPK+/SPK- | SNR <sub>AUXIN_SPK</sub>     |     | 60                 |     | dB    | Load 150Ω <sup>[2][3]</sup> |
| SNR, ANAIN to SPK+/SPK- | SNR <sub>ANAIN_SPK</sub>     |     | 60                 |     | dB    | Load 150Ω <sup>[2][3]</sup> |
| Output Power            | P <sub>OUT_SPK</sub> VCC=3.0 |     |                    | 360 | mW    | Load 8Ω <sup>[2]</sup>      |
| THD, AUXIN to SPK+/SPK- | THD %                        |     | <1%                |     |       | Load 8Ω <sup>[2]</sup>      |
| Minimum Load Impedance  | R <sub>L(SP)</sub>           | 4   | 8                  |     | Ω     |                             |

- Notes:
- <sup>[1]</sup> Conditions V<sub>CC</sub>=3V, T<sub>A</sub>=25°C unless otherwise stated.
  - <sup>[2]</sup> 1 Vpp 1KHz signal applied at AUXIN/ANAIN with 0db Gain setting.
  - <sup>[3]</sup> All measurements are C-message weighted.

### 6.4.4 SPI Timing

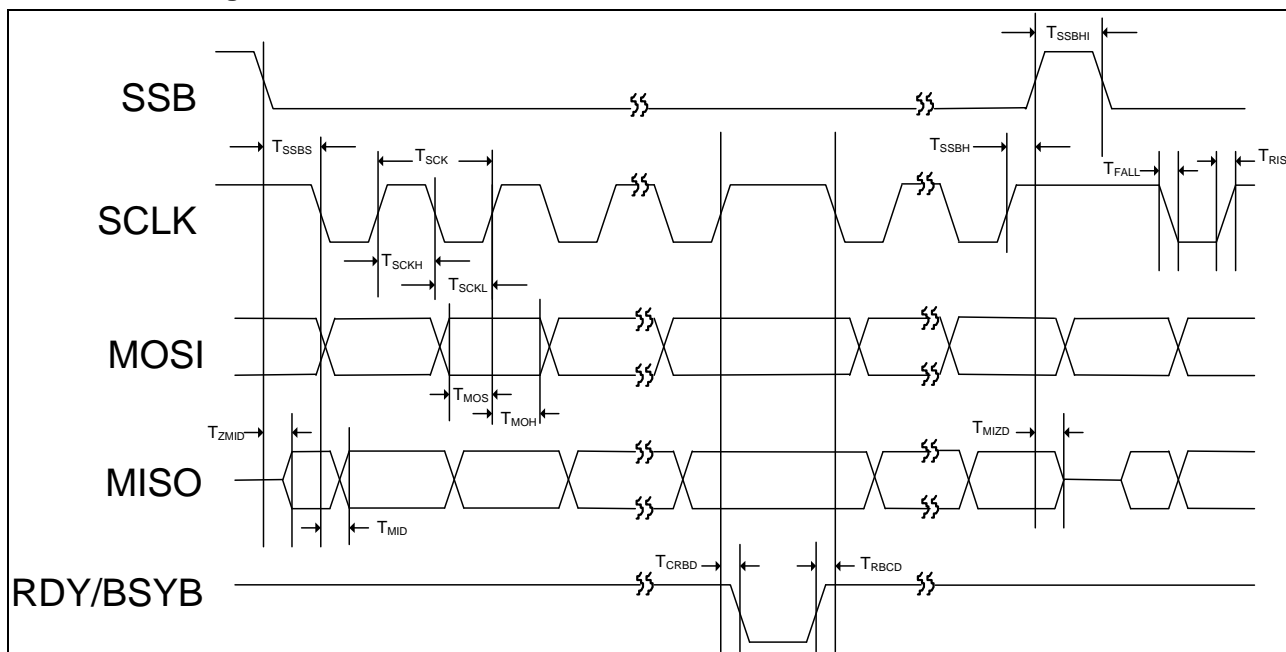


Figure 0-1 SPI Timing

| SYMBOL            | DESCRIPTION           | MIN | TYP | MAX | UNIT |
|-------------------|-----------------------|-----|-----|-----|------|
| T <sub>SCK</sub>  | SCLK Cycle Time       | 60  | --- | --- | ns   |
| T <sub>SCKH</sub> | SCLK High Pulse Width | 25  | --- | --- | ns   |
| T <sub>SCKL</sub> | SCLK Low Pulse Width  | 25  | --- | --- | ns   |

**ISD15100 SERIES****nuvoTon**

| SYMBOL             | DESCRIPTION  | MIN   | TYP | MAX  | UNIT |
|--------------------|--|-------|-----|------|------|
| T <sub>RISE</sub>  | Rise Time for All Digital Signals                                | ---   | --- | 10   | ns   |
| T <sub>FALL</sub>  | Fall Time for All Digital Signals                                | ---   | --- | 10   | ns   |
| T <sub>SSBS</sub>  | SSB Falling Edge to 1 <sup>st</sup> SCLK Falling Edge Setup Time | 30    | --- | ---  | ns   |
| T <sub>SSBH</sub>  | Last SCLK Rising Edge to SSB Rising Edge Hold Time               | 30 ns | --- | 50us | ---  |
| T <sub>SSBHI</sub> | SSB High Time between SSB Lows                                   | 20    | --- | ---  | ns   |
| T <sub>MOS</sub>   | MOSI to SCLK Rising Edge Setup Time                              | 15    | --- | ---  | ns   |
| T <sub>MOH</sub>   | SCLK Rising Edge to MOSI Hold Time                               | 15    | --- | ---  | ns   |
| T <sub>ZMID</sub>  | Delay Time from SSB Falling Edge to MISO Active                  | --    | --  | 12   | ns   |
| T <sub>MIZD</sub>  | Delay Time from SSB Rising Edge to MISO Tri-state                | --    | --  | 12   | ns   |
| T <sub>MID</sub>   | Delay Time from SCLK Falling Edge to MISO                        | ---   | --- | 12   | ns   |
| T <sub>CRBD</sub>  | Delay Time from SCLK Rising Edge to RDY/BSYB Falling Edge        | --    | --  | 12   | ns   |
| T <sub>RBCD</sub>  | Delay Time from RDY/BSYB Rising Edge to SCLK Falling Edge        | 0     | --  | --   | ns   |

*Publication Release Date: May 6, 2011**- 16 -**Revision 1.3*



# ISD15100 SERIES



## 6.4.5 I<sup>2</sup>S Timing

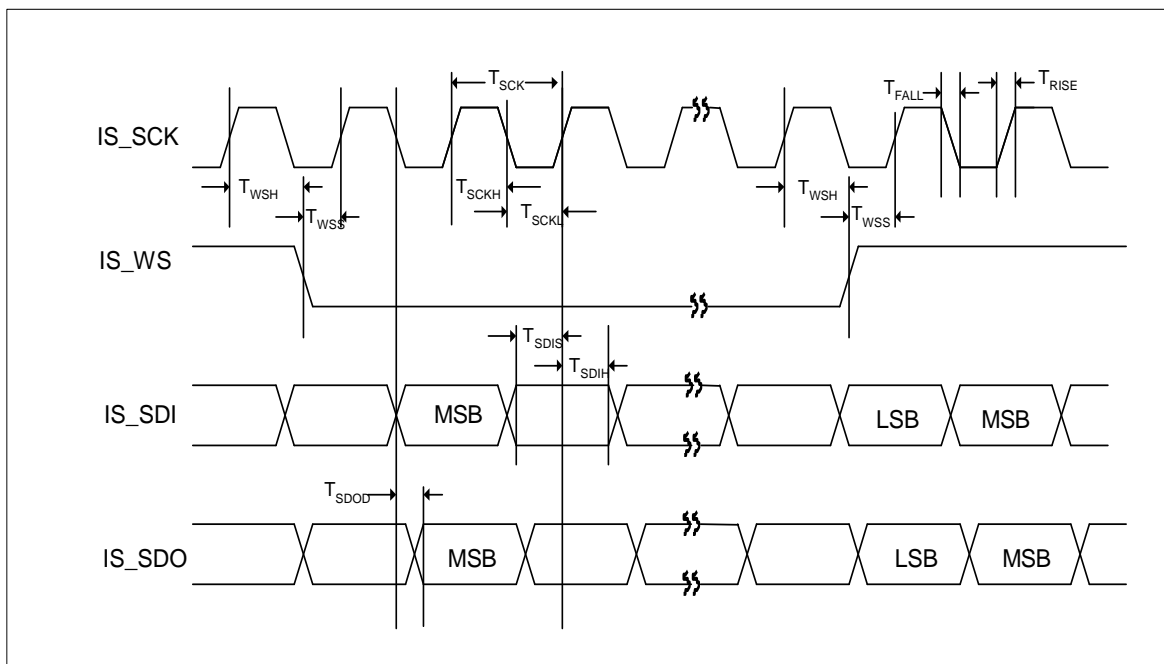


Figure 0-2 I<sup>2</sup>S Timing

| SYMBOL            | DESCRIPTION                                    | MIN | TYP | MAX | UNIT |
|-------------------|--|-----|-----|-----|------|
| T <sub>SCK</sub>  | IS_SCK Cycle Time                              | 60  | --- | --- | ns   |
| T <sub>SCKH</sub> | IS_SCK High Pulse Width                        | 25  | --- | --- | ns   |
| T <sub>SCKL</sub> | IS_SCK Low Pulse Width                         | 25  | --- | --- | ns   |
| T <sub>RISE</sub> | Rise Time for All Digital Signals              | --- | --- | 10  | ns   |
| T <sub>FALL</sub> | Fall Time for All Digital Signals              | --- | --- | 10  | ns   |
| T <sub>WSS</sub>  | WS to IS_SCK Rising Edge Setup Time            | 20  | --- | --- | ns   |
| T <sub>WSH</sub>  | IS_SCK Rising Edge to IS_WS Hold Time          | 20  | --- | --- | ns   |
| T <sub>SDIS</sub> | IS_SDI to IS_SCK Rising Edge Setup Time        | 15  | --- | --- | ns   |
| T <sub>SDIH</sub> | IS_SCK Rising Edge to IS_SDI Hold Time         | 15  | --- | --- | ns   |
| T <sub>SDOD</sub> | Delay Time from IS_SCLK Falling Edge to IS_SDO | --- | --- | 12  | ns   |

# ISD15100 SERIES



## 7 APPLICATION DIAGRAM

The following applications example is for references only. It makes no representation or warranty that such applications shall be suitable for the use specified. Each design has to be optimized in its own system for the best performance on voice quality, current consumption, functionalities and etc.

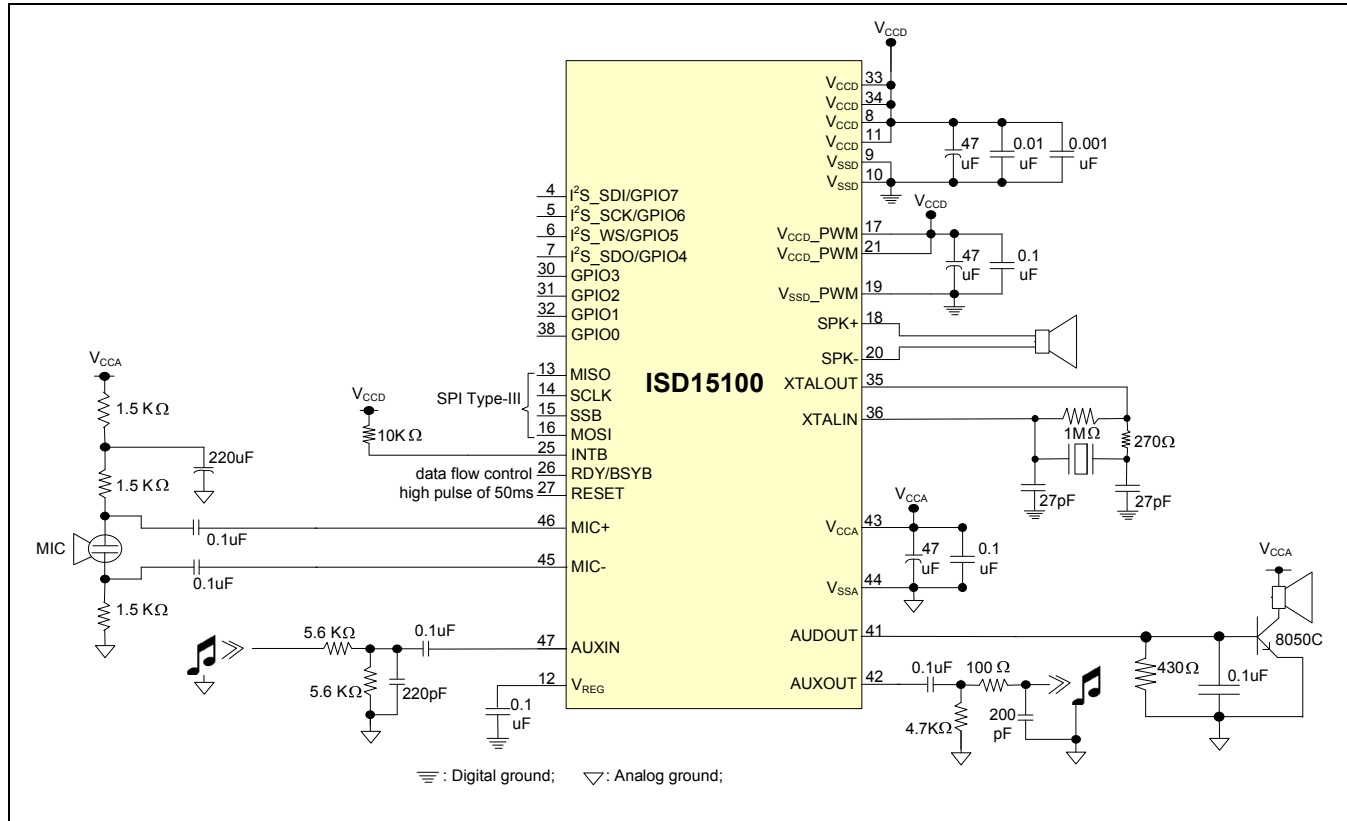


Figure 7-1 ISD15100 Application Diagram

Publication Release Date: May 6, 2011

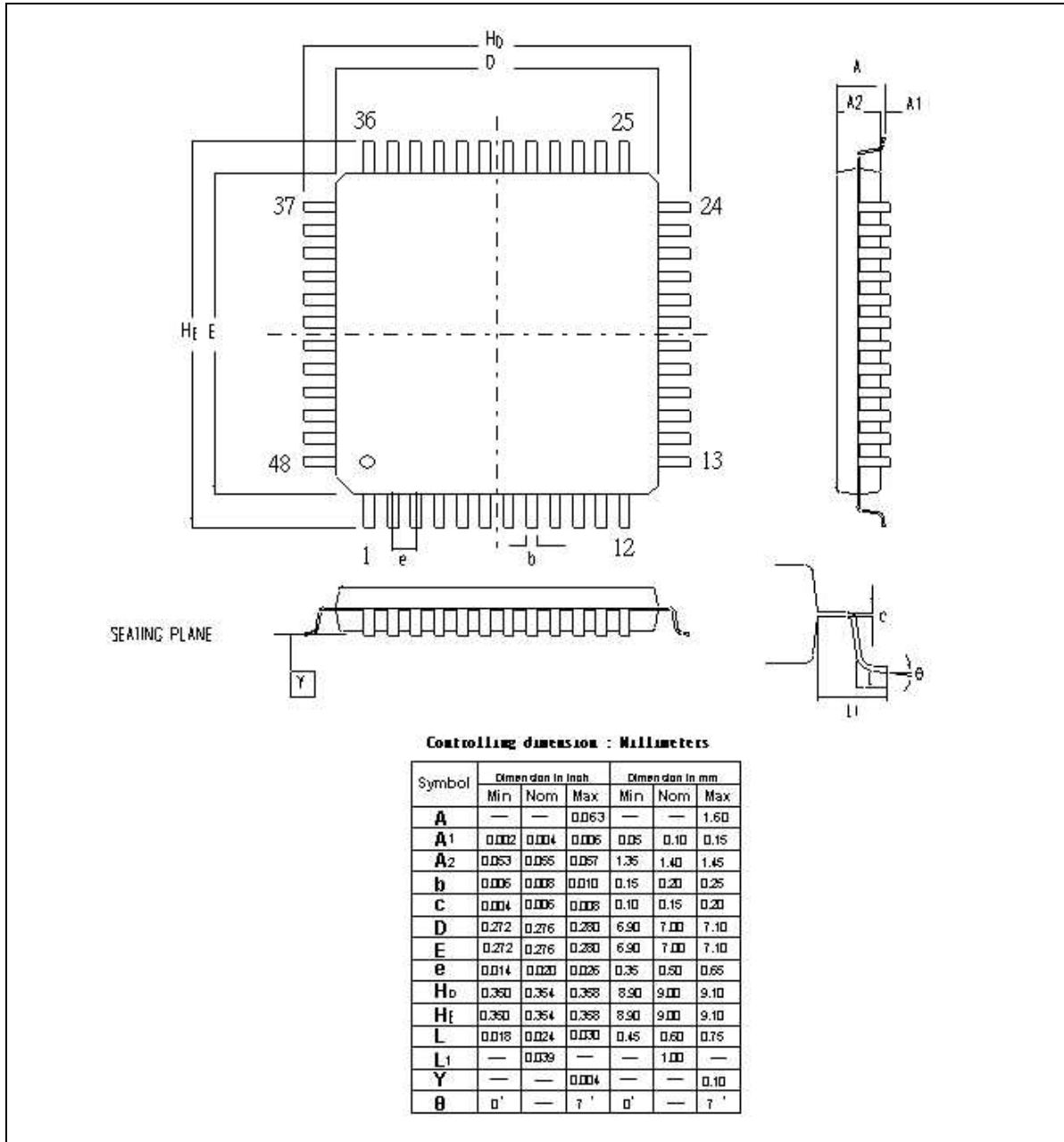
Revision 1.3

# ISD15100 SERIES



## 8 PACKAGE SPECIFICATION

### 8.1 48 LEAD LQFP(7X7X1.4MM FOOTPRINT 2.0MM)

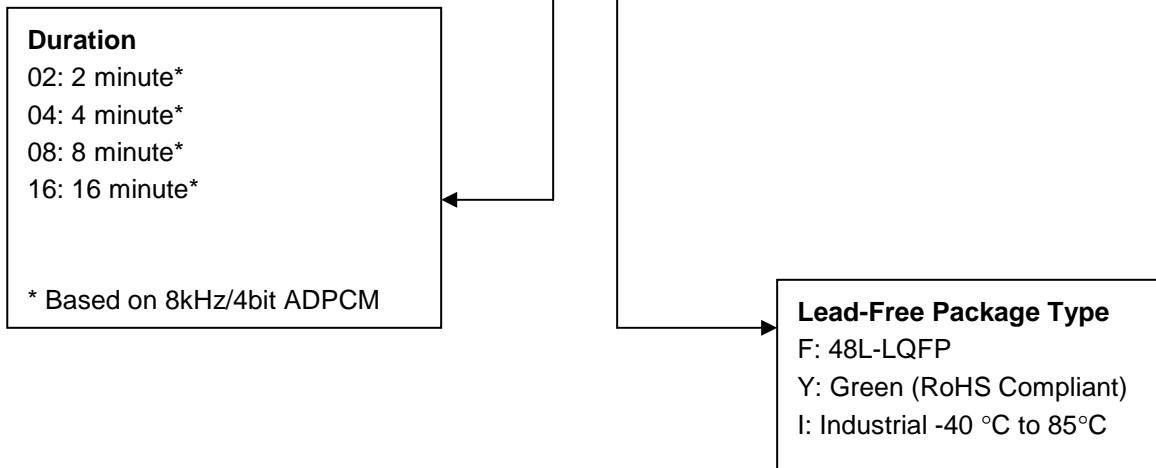


## ISD15100 SERIES

nuvoTon

### 9 ORDERING INFORMATION

#### I151xx FYI



*Publication Release Date: May 6, 2011*

- 20 -

*Revision 1.3*

# ISD15100 SERIES



---

## 10 REVISION HISTORY

| Version | Date         | Description  |
|---------|--------------|--|
| 0.71    | May 28, 2008 | Initial release. <ul style="list-style-type: none"><li>• Reset pulse: 50ms.</li><li>• Add a 270-ohm resistor between XTALOUT and crystal.</li><li>• Update spec of internal oscillator.</li><li>• Industrial temp.</li></ul>       |
| 0.75    | Sep 10, 2008 | Update: <ul style="list-style-type: none"><li>• SPI timing: <math>T_{SSBH}</math> maximum 50us.</li><li>• MICIN input signal: 500mV</li><li>• Revise Block Diagram; add BTL block.</li><li>• Revise Application Diagram.</li></ul> |
| 0.80    | Feb 10, 2009 | Update: <ul style="list-style-type: none"><li>• Remove the Preliminary watermark.</li><li>• Output low/high voltage.</li></ul>   |
| 0.82    | Nov 20, 2009 | Update Block Diagram.  |
| 1.0     | July 1, 2010 | Update crystal configuration.  |
| 1.3     | May 6, 2011  | Add Absolute Maximum Ratings.  |

*Publication Release Date: May 6, 2011*

- 21 -

*Revision 1.3*

## ISD15100 SERIES

**nuvoton**

Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Nuvoton customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nuvoton for any damages resulting from such improper use or sales.

The contents of this document are provided only as a guide for the applications of Nuvoton products. Nuvoton makes no representation or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to discontinue or make changes to specifications and product descriptions at any time without notice. No license, whether express or implied, to any intellectual property or other right of Nuvoton or others is granted by this publication. Except as set forth in Nuvoton's Standard Terms and Conditions of Sale, Nuvoton assumes no liability whatsoever and disclaims any express or implied warranty of merchantability, fitness for a particular purpose or infringement of any Intellectual property.

The contents of this document are provided "AS IS", and Nuvoton assumes no liability whatsoever and disclaims any express or implied warranty of merchantability, fitness for a particular purpose or infringement of any Intellectual property. In no event, shall Nuvoton be liable for any damages whatsoever (including, without limitation, damages for loss of profits, business interruption, loss of information) arising out of the use of or inability to use the contents of this documents, even if Nuvoton has been advised of the possibility of such damages.

Application examples and alternative uses of any integrated circuit contained in this publication are for illustration only and Nuvoton makes no representation or warranty that such applications shall be suitable for the use specified.

The 100-year retention and 100K record cycle projections are based upon accelerated reliability tests, as published in the Nuvoton Reliability Report, and are neither warranted nor guaranteed by Nuvoton.

This datasheet and any future addendum to this datasheet is(are) the complete and controlling ISD<sup>®</sup> ChipCorder<sup>®</sup> product specifications. In the event any inconsistencies exist between the information in this and other product documentation, or in the event that other product documentation contains information in addition to the information in this, the information contained herein supersedes and governs such other information in its entirety. This datasheet is subject to change without notice.

Copyright<sup>®</sup> 2005, Nuvoton Technology Corporation. All rights reserved. ChipCorder<sup>®</sup> and ISD<sup>®</sup> are trademarks of Nuvoton Technology Corporation. All other trademarks are properties of their respective owners.

### Headquarters

No. 4, Creation Rd. III  
Science-Based Industrial Park,  
Hsinchu, Taiwan  
TEL: 886-3-5770066  
FAX: 886-3-5665577  
<http://www.Nuvoton.com.tw/>

### Nuvoton Technology Corporation America

2727 North First Street, San Jose,  
CA 95134, U.S.A.  
TEL: 1-408-9436666  
FAX: 1-408-5441797  
<http://www.Nuvoton-usa.com/>

### Nuvoton Technology (Shanghai) Ltd.

27F, 299 Yan An W. Rd. Shanghai,  
200336 China  
TEL: 86-21-62365999  
FAX: 86-21-62356998

### Taipei Office

9F, No. 480, Pueiguang Rd.  
Neihu District  
Taipei, 114 Taiwan  
TEL: 886-2-81777168  
FAX: 886-2-87153579

### Nuvoton Technology Corporation Japan

7F Daini-ueno BLDG. 3-7-18  
Shinyokohama Kohokuku,  
Yokohama, 222-0033  
TEL: 81-45-4781881  
FAX: 81-45-4781800

### Nuvoton Technology (H.K.) Ltd.

Unit 9-15, 22F, Millennium City,  
No. 378 Kwun Tong Rd.,  
Kowloon, Hong Kong  
TEL: 852-27513100  
FAX: 852-27552064

Please note that all data and specifications are subject to change without notice.  
All the trademarks of products and companies mentioned in this datasheet belong to their respective owners.

*Publication Release Date: May 6, 2011*

*Revision 1.3*