



26 GHz, T FLIP-FLOP w/ RESET & PROGRAMMABLE OUTPUT VOLTAGE

Typical Applications

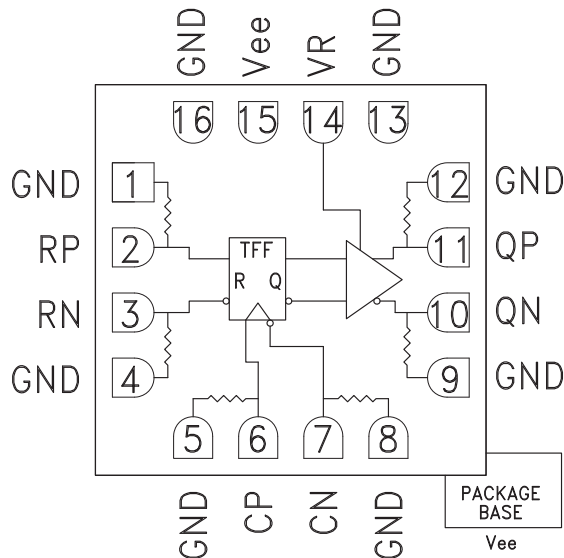
The HMC679LC3C is ideal for:

- Serial Data Transmission up to 26 Gbps
- High Speed Frequency Divider (up to 26 GHz)
- Broadband Test & Measurement
- RF ATE Applications

Features

- Supports Clock Frequencies up to 26 GHz
- Differential & Single-Ended Operation
- Fast Rise and Fall Times: 18 / 17 ps
- Low Power Consumption: 270 mW typ.
- Programmable Differential Output Voltage Swing: 600 - 1100 mV
- Propagation Delay: 95 ps
- Single Supply: -3.3V
- 16 Lead Ceramic 3x3mm SMT Package: 9mm²

Functional Diagram



General Description

The HMC679LC3C is a T Flip-Flop w/Reset designed to support clock frequencies as high as 26 GHz. During normal operation, with the reset pin not asserted, the output toggles from its prior state on the positive edge of the clock. This results in a divide-by-two function of the clock input. Asserting the reset pin forces the Q output low regardless of the clock edge state (asynchronous reset assertion). Reversing the clock inputs allows for negative-edge triggered applications. The HMC679LC3C also features an output level control pin, VR, which allows for loss compensation or for signal level optimization.

All input signals to the HMC679LC3C are terminated with 50Ω to ground on-chip, and may be either AC or DC coupled. Outputs can be connected directly to a 50Ω terminated system, while DC blocking capacitors may be used if the terminating system is 50Ω to a non-ground DC voltage. The HMC679LC3C operates from a single -3.3V DC supply and is available in a ceramic RoHS compliant 3x3 mm SMT package.

Electrical Specifications, $T_A = +25^\circ\text{C}$ $V_{ee} = -3.3\text{V}$

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		-3.6	-3.3	-3.0	V
Power Supply Current			82		mA
Maximum Clock Rate			26		GHz
Input High Voltage		-0.5		0.5	V
Input Low Voltage		-1.0		0.0	V
Input Return Loss	Frequency <13 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		550		mVpp
	Differential, peak-to-peak		1100		mVpp
Output High Voltage			-10		mV
Output Low Voltage			-570		mV



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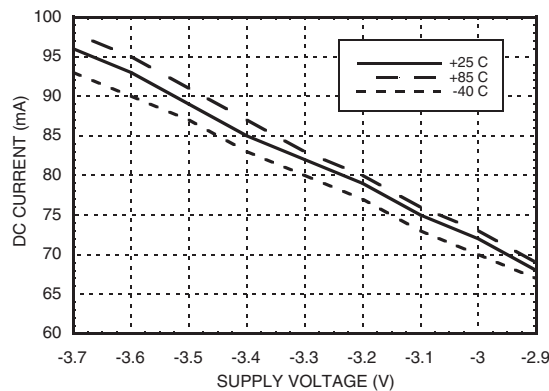
Electrical Specifications, (continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
Output Rise / Fall Time	Differential, 20% - 80%		18 / 17		ps
Output Return Loss	Frequency <13 GHz		10		dB
Random Jitter Jr	rms [1]			0.2	ps rms
Deterministic Jitter, Jd	peak-to-peak, 2 ¹⁵ -1 PRBS input [2]		2		ps, pp
Propagation Delay Clock to Q, td			95		ps
Propagation Delay Reset to Q, tdr			125		ps
Set Up & Hold Time, t _{SH}			6		ps

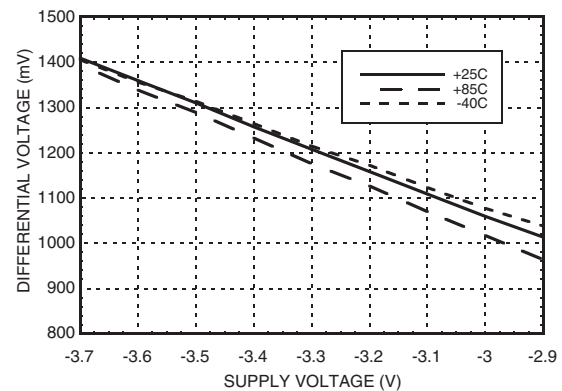
[1] Upper limit of random jitter, J_R, determined by measuring and integrating output phase noise with a sinusoidal input at 5, 10, and 13.5 GHz over temperature.

[2] TBD

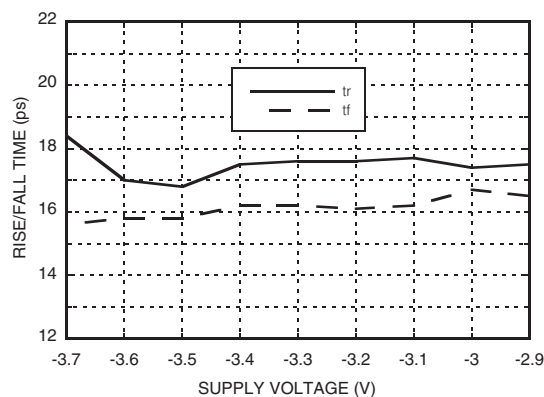
DC Current vs. Supply Voltage [1] [2]



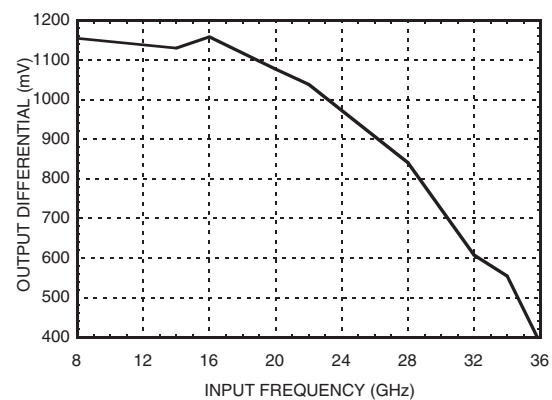
Output Differential vs. Supply Voltage [1][2]



Rise / Fall Time vs. Supply Voltage [3]



Output Differential vs. Input Frequency [1]



[1] VR = 0.0V

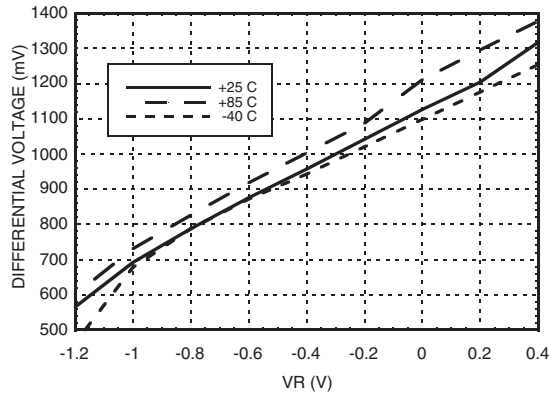
[2] Frequency = 13 GHz

[3] Frequency = 24 GHz

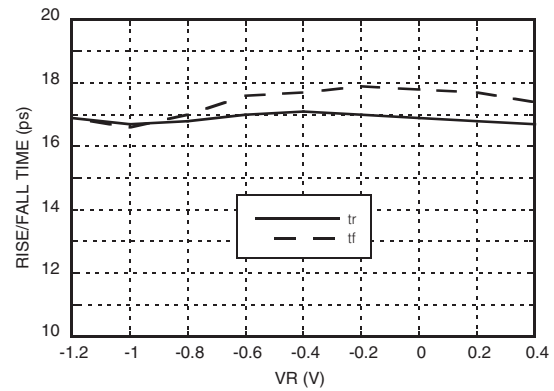


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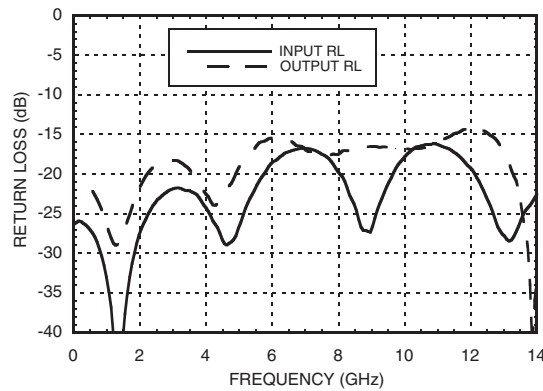
Output Differential vs. VR [2]



Rise / Fall Time vs. VR [3]



Input & Output Return Loss



[1] VR = 0.0V

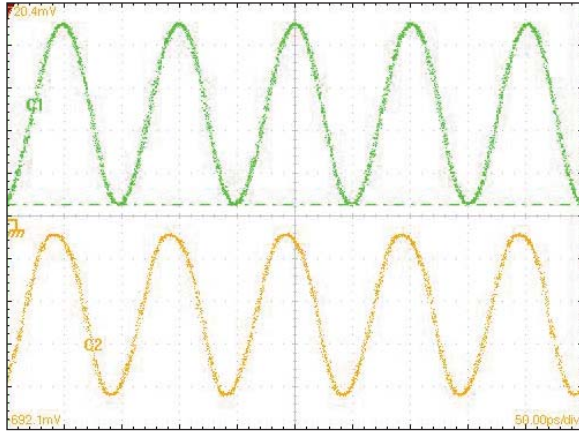
[2] Frequency = 13 GHz

[3] Frequency = 24 GHz



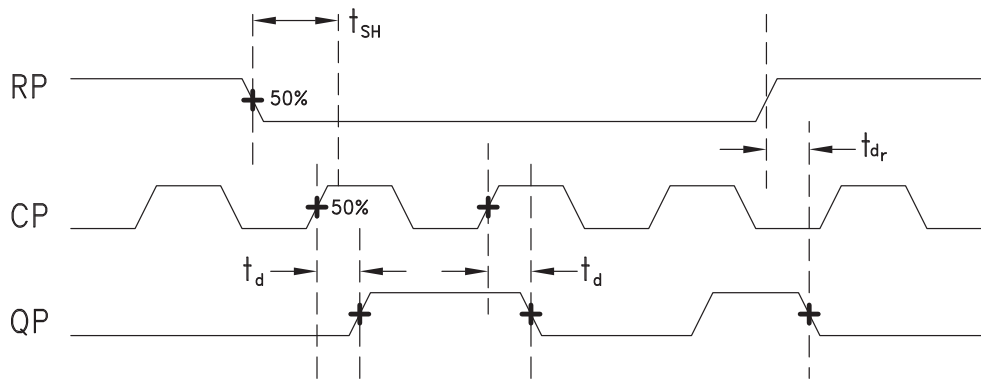
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Output Waveform



[1] Test Conditions:
Waveform generated with a CW signal source input at 20 GHz.
Diagram data presented on a Tektronix CSA 8000.

Timing Diagram



t_d = propagation delay, CK (clock) to Q
 t_{dr} = propagation delay, R (reset) to Q.

Truth Table

R	CK	Q	Q Next
0	L --> H	0	1
0	L --> H	1	0
1	X	0	0 (ASYNC)
1	X	1	0 (ASYNC)

Notes:
R = RP - RN
CK = CP - CN
Q = QP - QN

H = Positive voltage level
L = Negative voltage level



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Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75V to +0.5V
Input Signals	-2V to +0.5V
Output Signals	-1.5V to +1V
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C

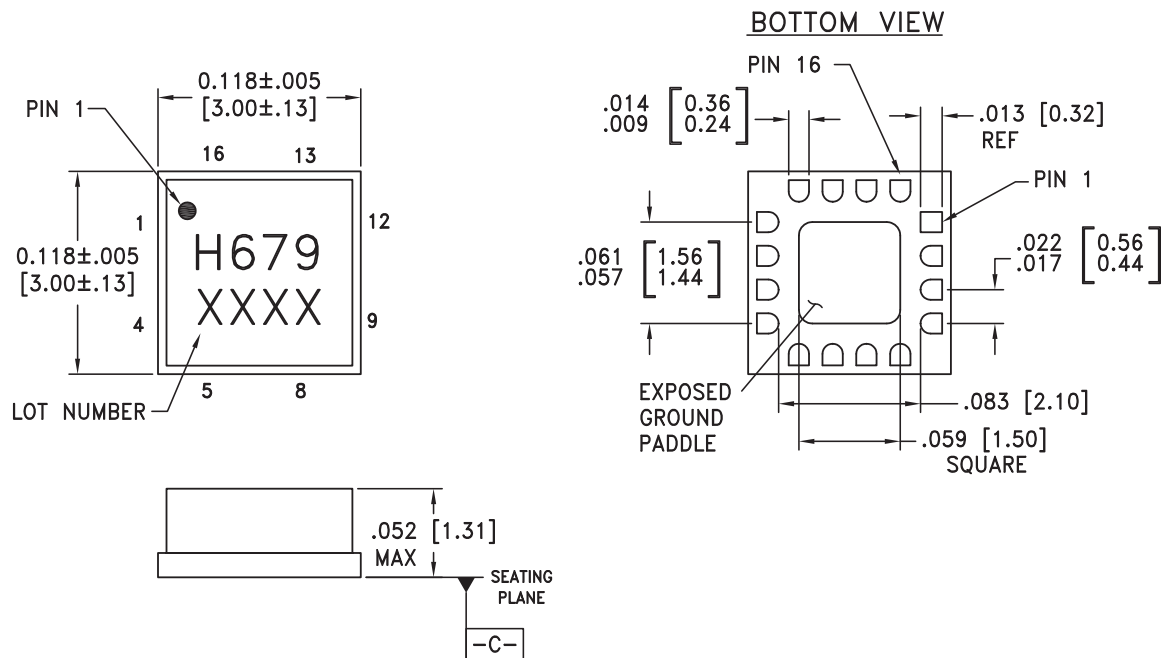


**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**

7

HIGH SPEED LOGIC - SMT

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. GROUND PADDLE MUST BE SOLDERED TO Vee.

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Pin Descriptions [1]

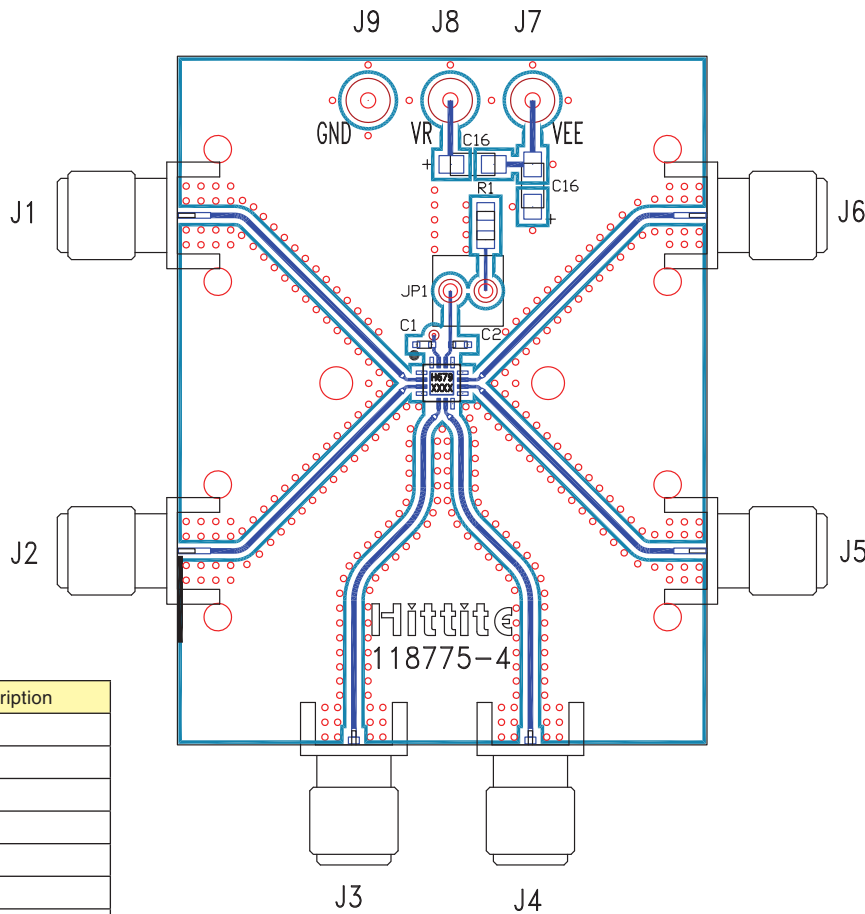
Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3	RP, RN	Reset Inputs	
6, 7	CP, CN	Clock Inputs	
10, 11	QN, QP	Data Output	
13, 16	GND	Supply Ground	
14	VR	Output level control. Output level may be adjusted by either applying a voltage to VR per "Output Differential vs. VR" plot, or by tying VR to GND with a resistor per the following equation: $V_o(R) = 1.2 / (2.1 + R)$, R in k Ω	
15, Package Base	Vee	Negative Supply	

[1] Contact HMC for alternate pinouts



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Evaluation PCB



Item	Description
J1	RP
J2	RN
J3	CP
J4	CN
J5	QN
J6	QP
J7	VR
J8	Vee

List of Materials for Evaluation PCB 118777 [1]

Item	Description
J1, J2, J5, J6	PCB Mount SMA RF Connectors
J3, J4	PCB Mount 2.92mm RF Connectors
J7 - J9	DC Pin
C1 - C2	100 pF Capacitor, 0402 Pkg.
C16 - C17	4.7 μF Capacitor, Tantalum
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC679LC3C
PCB [2]	118775 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed packaged base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.



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Application Circuit

