

20V N-Channel Enhancement-Mode MOSFET

SUNSTAR单片机专用电路 <http://www.icasic.com/> TEL: 0755-83387030 FAX:0755-83376182 E-MAIL:szss20@163.com

RDS(ON), Vgs@1.8V, Ids@2.0A = 75mΩ

RDS(ON), Vgs@2.5V, Ids@3.5A = 38mΩ

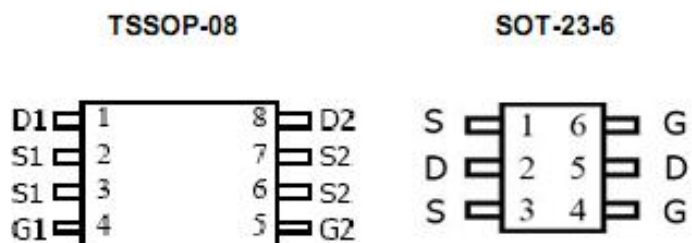
RDS(ON), Vgs@4.0V, Ids@4.5A = 30mΩ

RDS(ON), Vgs@4.5V, Ids@4.5A = 28mΩ

RDS(ON), Vgs@10V, Ids@5.0A = 25mΩ

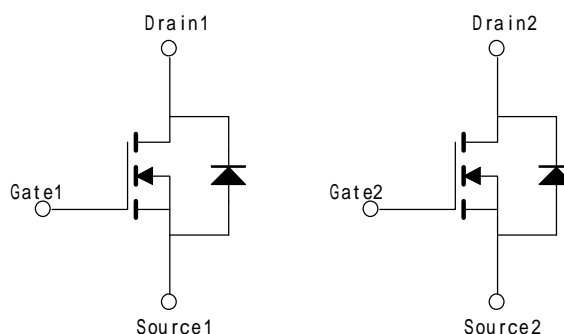
Features

- Ø Advanced trench process technology
- Ø High Density Cell Design For Ultra Low On-Resistance
- Ø High Power and Current handing capability
- Ø Ideal for Li ion battery pack applications



Top View

Internal Schematic Diagram



N-Channel MOSFET

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	20	V	
Gate-Source Voltage	V _{GS}	±12		
Continuous Drain Current ¹	I _D	6	A	
Pulsed Drain Current ²	I _{DM}	20		
Maximum Power Dissipation	P _D	TA = 25°C	2	W
		TA = 75°C	1.28	
Operating Junction and Storage Temperature Range	T _{j1} T _{stg}	-55 to 150	°C	
Junction-to-Ambient Thermal Resistance (PCB mounted) ³	R _{OUA}	62.5	°C/W	

Note: 1. Fused current that based on wire numbers and diameter

2. Repetitive Rating: Pulse width limited by the maximum junction temperature

3. 1-in² 2oz Cu PCB board

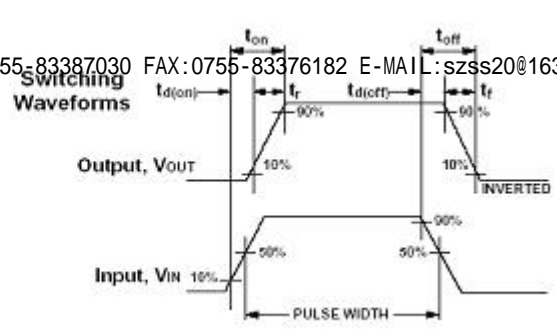
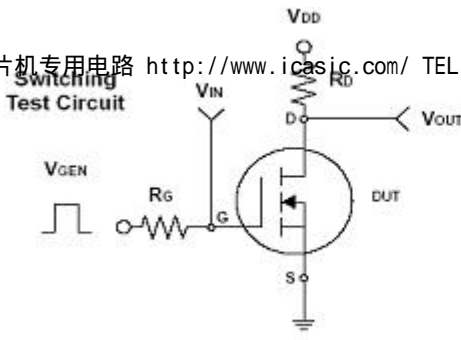
ELECTRICAL CHARACTERISTICS

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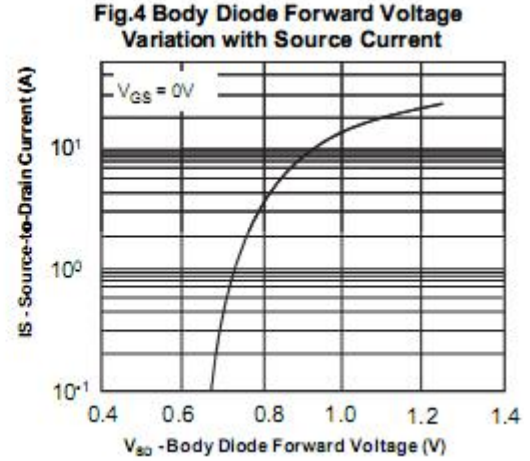
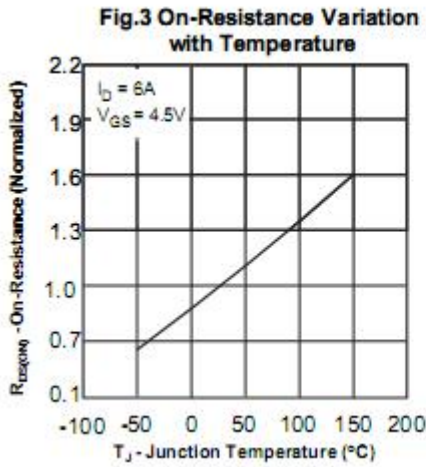
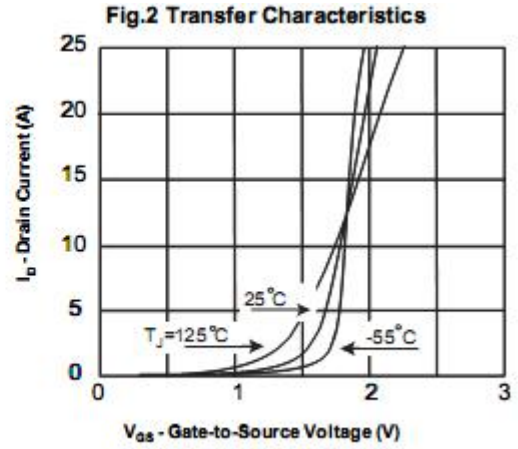
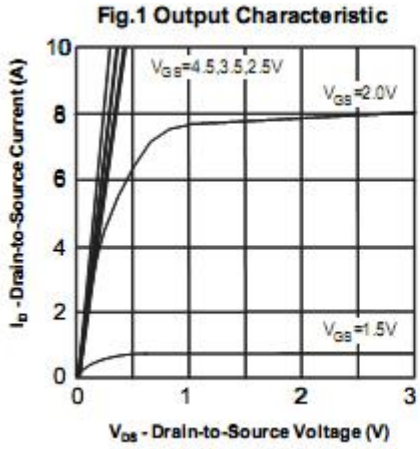
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 1.8V, I_D = 2.0A$		53.0	75.0	mΩ
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 2.5V, I_D = 3.5A$		30.0	38.0	
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 4.0V, I_D = 4.5A$		23.0	30.0	
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 4.5V, I_D = 4.5A$		22.0	28.0	
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 5.0A$		20.0	25.0	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{GS}, I_D = 250\mu A$	0.6	0.75	1	V
Zero Gate Voltage drain Current	I_{DSS}	$V_{GS} = 20V, V_{GS} = 0V$			1	uA
Gate Body Leakage	I_{GSS}	$V_{GS} = \pm 12V, V_{DS} = 0V$			±100	nA
Dynamic³						
Total Gate Charge	Q_G	$V_{DS} = 10V, I_D = 6A$ $V_{GS} = 4.5V$		6.24	8.11	nC
Gate-Source Charge	Q_{GS}			1.64	2.13	
Gate-Drain Charge	Q_{GB}			1.34	1.74	
Turn-On Delay Time	$T_{d(on)}$	$V_{DD} = 10V, I_D = 6A$ $I_D = 1A, V_{GS} = 4.5V$		10.4	20.8	ns
Turn-On Rise Time	T_r			4.4	8.8	
Turn-Off Delay Time	$T_{d(off)}$			27.36	54.72	
Turn-Off Fall Time	T_f			4.16	8.32	
Input Capacitance	C_{iss}	$V_{DS} = 8V, V_{GS} = 0V$ $f = 1.0MHz$		522.3		pF
Output Capacitance	C_{oss}			98.48		
Reverse Transfer Capacitance	C_{rss}			74.69		
Source-Drain Diode						
Max.Diode Forward Current	I_S				1.7	A
Diode Forward Voltage	V_{SD}	$I_S = 1.7A, V_{GS} = 0V$		0.74		V

Note: Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

3. Guaranteed by design; not subject to production testing



Typical Characteristics Curves (Ta=25°C, unless otherwise note)



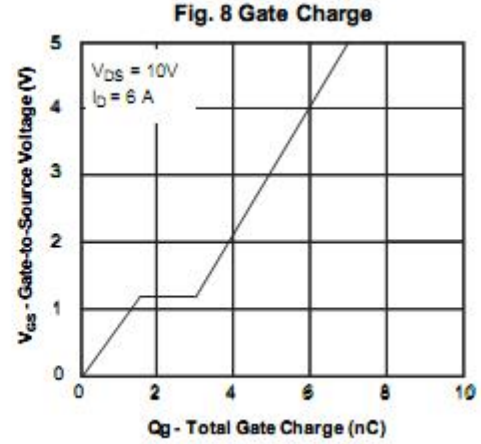
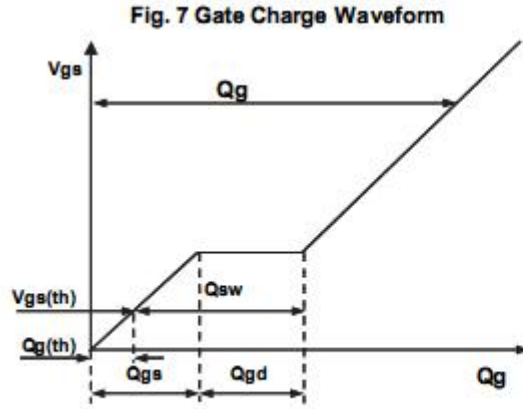
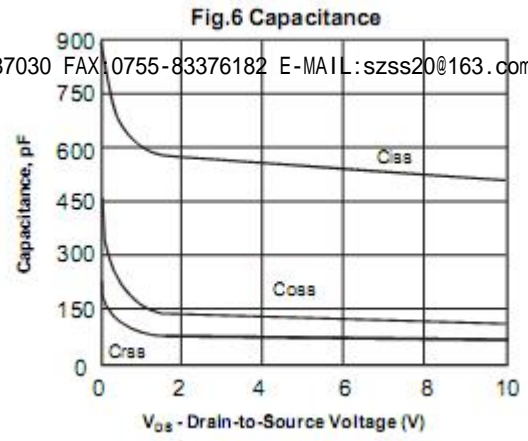
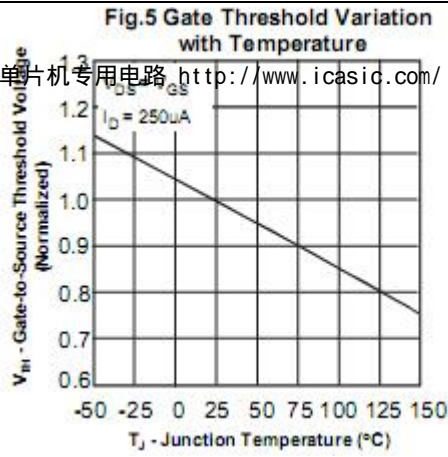


Fig.9 Maximum Safe Operating Area

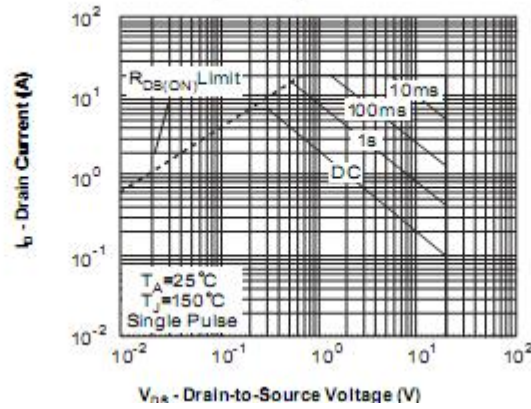
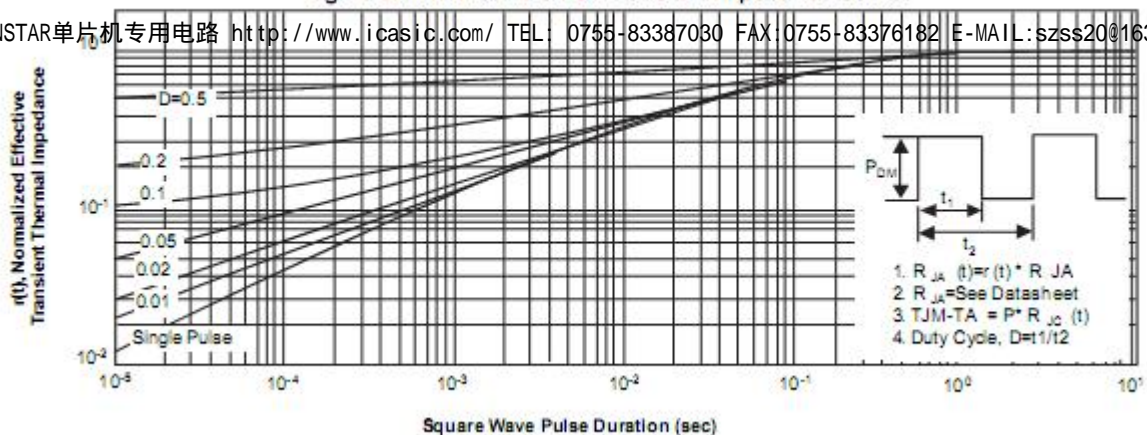


Fig. 10 Normalized Thermal Transient Impedance Curve



Features

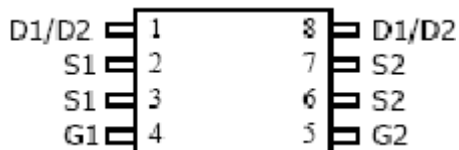
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- Ø High density cell design for ultra low On-Resistance;
- Ø High power and current handling capability;
- Ø Ideal for Li ion battery pack applications;

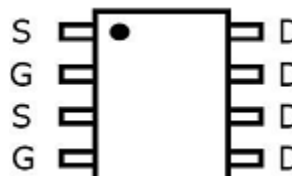
- Ø $V_{DS} = 20V$
- $R_{DS(ON)}, V_{gs}@2.5V, I_{ds}@3.3A = 30m\Omega$;
- $R_{DS(ON)}, V_{gs}@4.5V, I_{ds}@8.2A = 20m\Omega$;
- Ø Recommended Package: TSSOP-8/SO-8/SOT-23-6.

Package

TSSOP-08

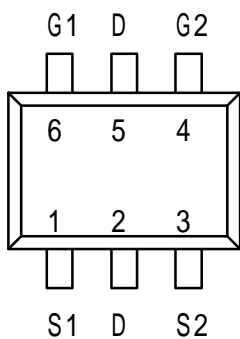


SOP-8

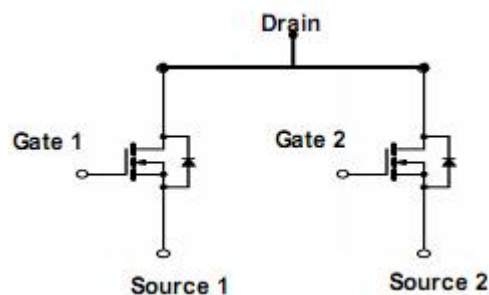


Top View

SOT-23-6



Internal Schematic Diagram



N-Channel MOSFET

Maximum Ratings and Thermal Characteristics ($T_a = 25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source voltage		V_{DS}	20	V
Gate-Source voltage		V_{GS}	± 12	
Continuous drain current		I_D	8.2	A
Pulsed drain current ¹⁾		I_{DM}	30	
Maximum power dissipation	$T_A = 25^\circ C$	P_D	2	W
	$T_A = 75^\circ C$		1.3	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to 150	$^\circ C$
Junction-to-Ambient thermal resistance (PCB mounted) ²⁾		$R_{\theta JA}$	62.5	$^\circ C/W$

Note: 1. Repetitive Rating: Pulse width limited by the maximum junction temperature

2. 1-in² 2oz Cu PCB board

Electrical Characteristics

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	20	--	--	V
Drain-Source On-Stage Resistance	$R_{DS(on)}$	$V_{GS} = 2.5V, I_D = 3.3A$	--	22.0	30.0	m Ω
Drain-Source On-Stage Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 8.2A$	--	16.0	20.0	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.6	--	1.5	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20V, V_{GS} = 0V$	--	--	1	μA
Gate Body Leakage	I_{GSS}	$V_{GS} = \pm 12V, I_D = 0\mu A$	--	--	± 100	nA
Forward Transconductance	g_{fs}	$V_{DS} = 15V, I_D = 8.2A$	--	29	--	S
Dynamic³⁾						
Total Gate Charge	Q_g	$V_{DS} = 10V, I_D = 8.2A$ $V_{GS} = 4.5V$	--	11	14.3	nC
Gate-Source Charge	Q_{gs}		--	2.5	3.25	
Gate-Drain Charge	Q_{gd}		--	3.2	4.16	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10V, R_G = 6\Omega$ $I_D = 1A, V_{GEN} = 4.5V$	--	45	90	ns
Turn-On Rise Time	t_r		--	50	100	
Turn-Off Delay Time	$t_{d(off)}$		--	35	70	
Turn-Off Fall Time	t_f		--	20	40	
Input Capacitance	C_{iss}	$V_{DS} = 8V, V_{GS} = 0V$ $f = 1.0MHz$	--	560	--	pF
Output Capacitance	C_{oss}		--	95	--	
Reverse Transfer Capacitance	C_{rss}		--	75	--	
Source-Drain Diode						
Max. Diode Forward Current	I_S	--	--	--	1.7	A
Diode Forward Voltage	V_{SD}	$I_S = 1.7A, V_{GS} = 0V$	--	--	1.2	V

Note: 1. Pulse test: Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

2. Guaranteed by design; not subject to production testing

