Application Note

Using the ACD0900 Downconverter MMIC for CATV

Rev 2

RELEVANT PRODUCTS

- ACD0900

INTRODUCTION

The ACD0900 downconverter MMIC is designed to be used as the second frequency converter in double conversion cable television tuners. The chip, fabricated in gallium arsenide, incorporates a high degree of integration, which significantly reduces the number of components required in the tuner. This eliminates the need for individual component tuning, thereby reducing manufacturing costs and improving tuner reliability. The devices are supplied in a modified 16 lead surface mount SOIC package, which allows designers to reduce the overall size of the tuner.

FUNCTIONAL DESCRIPTION

A functional block diagram of the ACD0900 device is shown in Figure 1. Each MMIC has three main sections: a Gilbert Cell (consisting of a low noise amplifier and a double balanced mixer), a phase splitter and an oscillator.

TUNER APPLICATIONS

A functional block diagram of a typical double conversion tuner is shown in Figure 2. Signals in the 50 to 860 MHz range are upconverted to a fixed IF frequency by the ACU series of devices. The upconverted signal passes through a bandpass filter, is amplified, and is presented to the RF input of the ACD0900 . This device then amplifies and mixes the signal down to a final IF frequency of 35 to 150 MHz.

A lowpass filter at the RF input is used to reduce the LO to RF leakage levels at the input of the tuner, and to prevent image signals from reaching the input of the ACU device. In the case where low frequency information is being retransmitted along the cable, a bandbass filter should be used.

The main purpose of the bandpass filter shown at the IF output of the upconverter is to provide coarse channel filtering. All of the input channels will appear

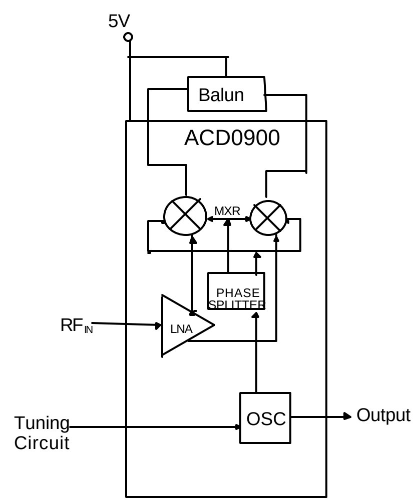


Figure 1: Block Diagram of ACD0900

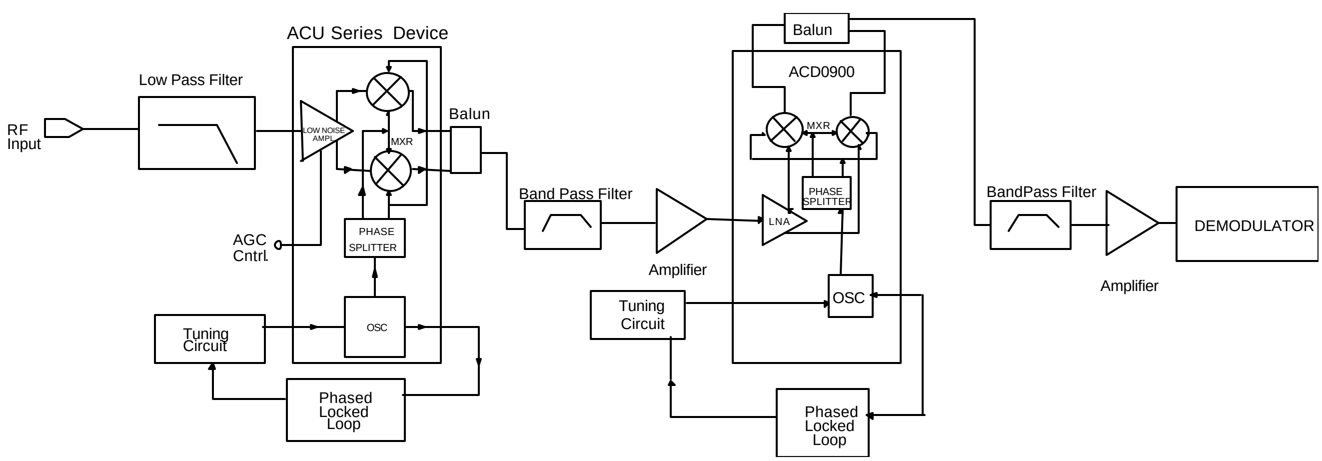


Figure 2: Double Conversion Tuner

at the output, and there has to be a means to eliminate as many channels as possible. This prevents overloading the IF amplifier and downconverter. The type of filter used (lumped, distributed or ceramic) will depend on cost and space constraints.

The bandpass filter shown at the output of the downconverter is used for precise channel selection, and should have a high Q and narrow bandwidth. Although any filter type can be used here, a SAW or ceramic filter will give the best performance, and trade offs between cost and performance must be considered.

ON CHIP OSCILLATOR

In order for the ACD0900 to convert input signals to the correct output frequency, the on-chip oscillator must be properly tuned. This is accomplished with an external resonator circuit, such as the one shown in Figure 3. The LO frequency is adjusted by applying a positive voltage to the cathode of the varactor via the terminal marked $V_{TUNE.}$ The voltage and LO frequency range will be a function of the type of varactor used, its distance from the LO port of the device (pin 11 for the ACD0900), and the value of L1. Varactors with a tuning curve similar to that shown in Figure 4 will work well with the ACD0900.

When using the 1SV245 varactor, the value of L1 should be chosen so that the required LO frequency can be achieved with a tuning voltage of 2.5 Volts. This will optimize the oscillator phase noise by allowing the varactor to operate with a lower series resistance and, therefore, a higher Q. Increasing L1 results in a lower LO frequency for a given voltage at the terminal marked V_{TUNE}. Decreasing the inductance results in a higher LO frequency for the same voltage.

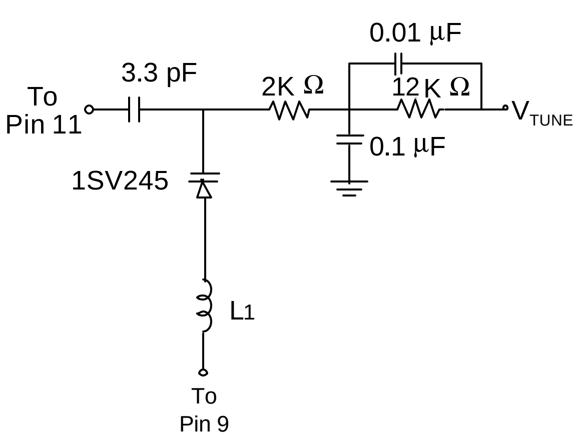
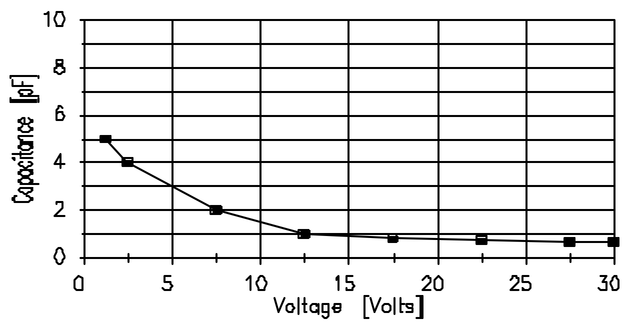


Figure 3: External Resonator Circuit

The resistors and the 0.01µF capacitor are selected as part of the phase locked loop, and their values need to be determined separately for each application.

Figure 4: Capacitance vs. Voltage 1SV245 Varactor



BALANCED VS. SINGLE ENDED OUTPUT

The ACD0900 provides a balanced IF output at pins 1 and 16. Although an appropriate conversion gain can be measured at each of these outputs, approximately 3 dB of improvement can be obtained with the use of a balun. In addition, the balun serves to improve distortion performance by cancelling the second order intermodulation products present at the output of the device.

A balun which works well for this application is shown in Figure 5. It is fabricated on a toroidal ferrite core having a permeability of 850, and is wound with four turns of 36 gauge trifilar wire. The purpose of the center tap is to provide bias to the IF outputs of the device. Dimensions for the ferrite core are shown in Figure 6.

LINEARITY ADJUSTMENT

A resistor connected from pin 7 to ground is used to adjust the mixer current, which gives the user some control over the linearity of the device. Using a 5.6Ω resistor guarantees that the device will meet the distortion specifications shown on the data sheet. If, however, better linearity is required, the value of this resistor can be decreased. The acceptable range of values is 3.9Ω to 8.2Ω.

TEST FIXTURE

A test fixture used to characterize the ACD0900 is shown in Figure 7. The layout shown is for 0.062 inch thick FR4, with a relative dielectric constant of 4.8. All ground hole vias should be plated through and should be a minimum of 30 mils (0.076mm) in diameter.

Proper component layout is also shown in Figure 7. Component leads should be kept as short as possible, and good RF quality chip capacitors and resistors should be used wherever possible. Special attention should be given to the layout of the tuning circuit, as this will greatly affect the local oscillator phase noise and tuning range of the oscillator. The layout of this circuit should be optimized for each particular application.

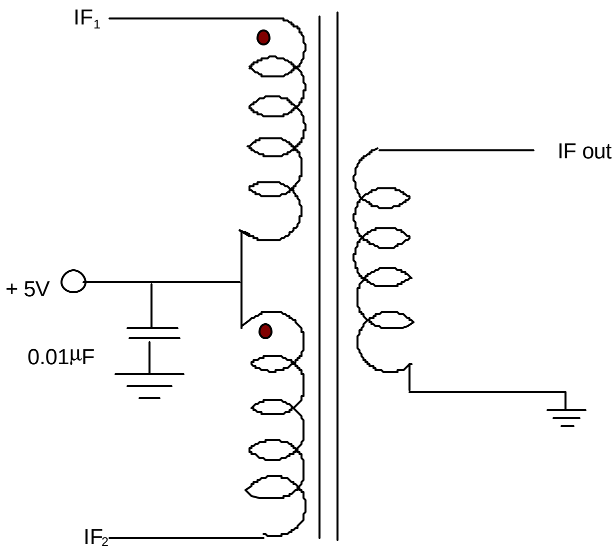


Figure 5: Balun Schematic

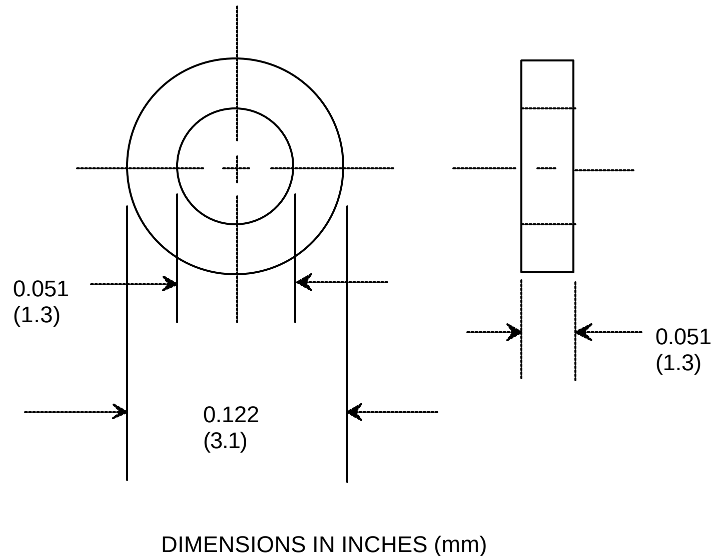
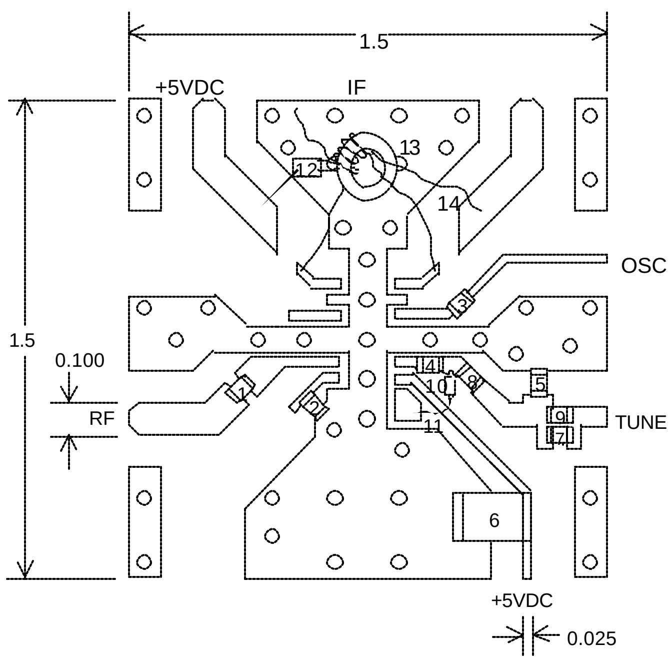


Figure 6: Core Dimensions



SYMBOL	DESCRIPTION	PART NUMBER
1,3	0.001uF CHIP CAP	VJ0805V102MXA
7,12	0.01uF CHIP CAP	VJ0805Y103KXA
5	0.1 µF CHIP CAP	VJ0805U104MXAAB
4	3.3pF CHIP CAP	VJ0805A3R3DXAAB
6	330 µF CHIP CAP	595D337X0010R2T
2	5.6 OHM RES.	5R6
8	2K OHM RES.	202
9	12K OHM RES.	123
10	VARACTOR	1SV245
11	WIRE, L = 0.250 inch	28 GAUGE
13	FERRITE CORE	H5C2T-3.1-1.3 -1.3
14	TRIFILAR WIRE	#36 108 TWISTS/FT

NOTES:
1. DRAWING & COMPONENTS NOT TO SCALE
2. SUBSTRATE MATERIAL: FR4 Er = 4.8
3. SUBSTRATE THICKNESS: 0.062 INCHES
4. CAPACITOR #12 IS STANDING ON END
5. PCB DIMENSIONS ARE IN INCHES

Figure 7: Test Fixture

TEST CIRCUIT

The recommended external circuitry for the ACD0900 is shown in Figure 8. This circuitry minimizes component count, while providing good performance.

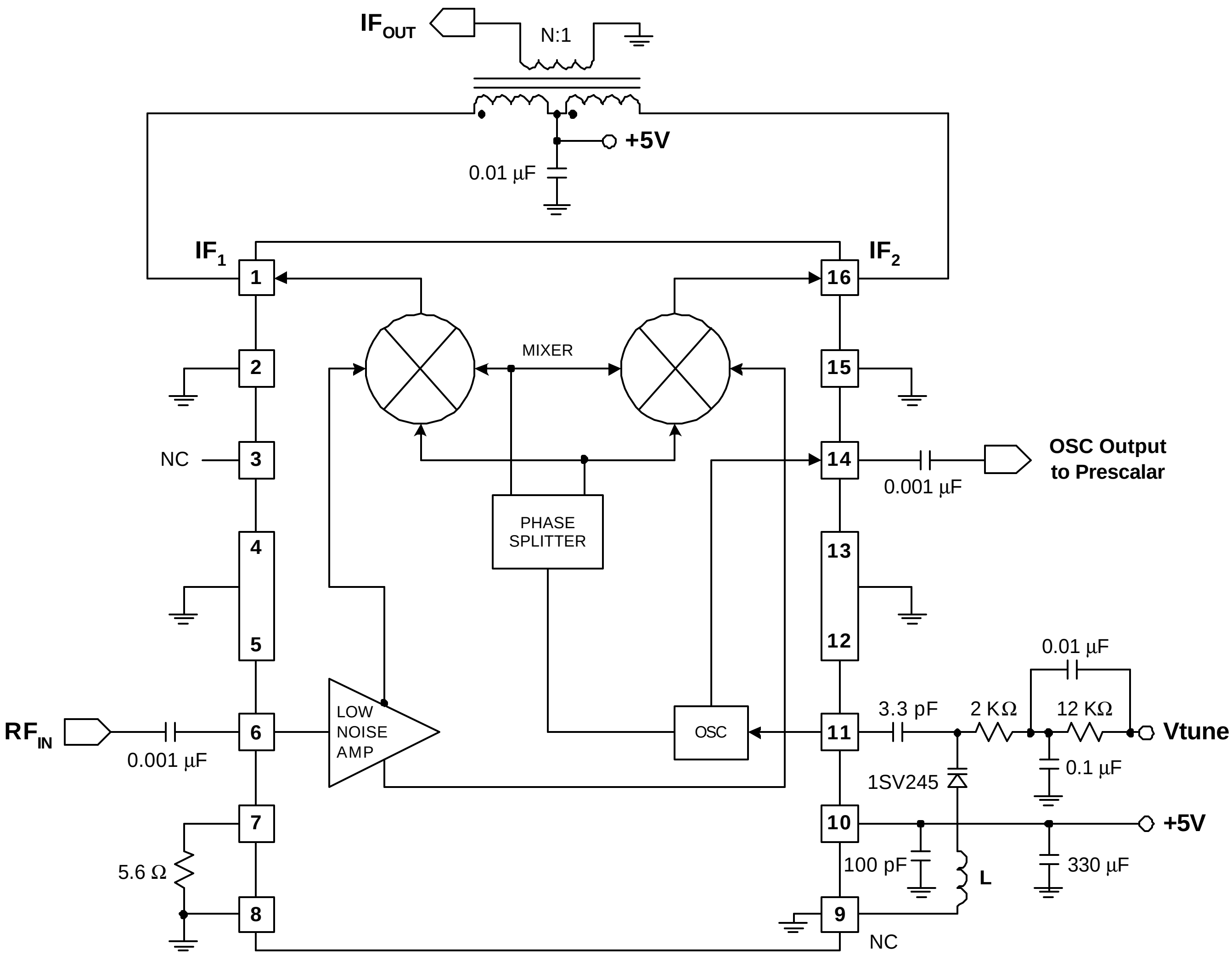


Figure 8: Test Circuit

HANDLING PRECAUTIONS

When handling the ACD0900, standard ESD prevention techniques should be followed. A wrist strap will give adequate protection against static build up, particularly in dry weather. Antistatic mats on work benches are recommended. In addition to wrist straps and antistatic mats, well grounded soldering irons should be used in work areas. In fact, any tool that can come in contact with the device should have a discharge path to ground.

The devices are based on a 0.5 micron MESFET process, and it is therefore important to maintain generally accepted electrostatic discharge (ESD) and overvoltage precautions when handling and biasing the devices. Microstrip lines used to bias the devices should be bypassed with RF quality capacitors as close to the device pins as possible. Zener diodes on these lines can provide added protection.

Device failures could be induced by intermittently short circuiting supply pins to ground, or by removing and reattaching DC supply leads with the power on. Failures can also result from transients set up on long supply leads. Supply leads should be kept as short as possible, and twisted wire or coaxial cable should be used with a regulated power supply.

THERMAL CONSIDERATIONS

It is important to provide a heat sink to prevent damage and to prolong the lifetime of the ACD0900. The device should be soldered directly to the PC board, and pins 4, 5, 12 and 13 should be soldered to as large a thermal mass as possible. This will result in adequate heat sinking, provided that the temperature at the four ground pins doesn't exceed +70 ^{0}C. Bringing any enclosure walls as close to the device as possible will help dissipate the heat.

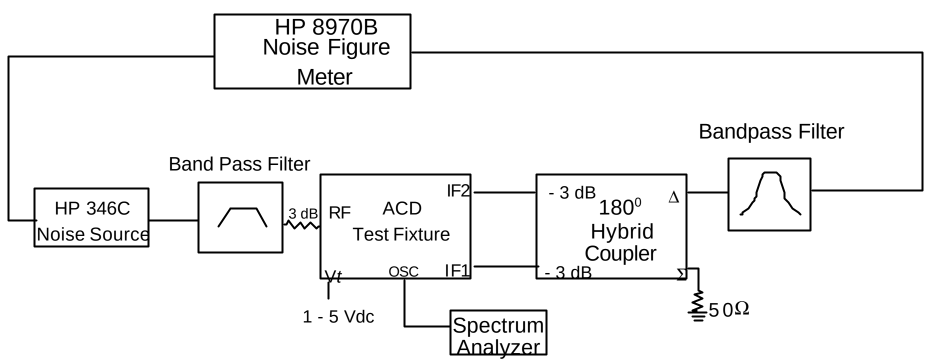


FIgure 9: Gain/ NF Measurement

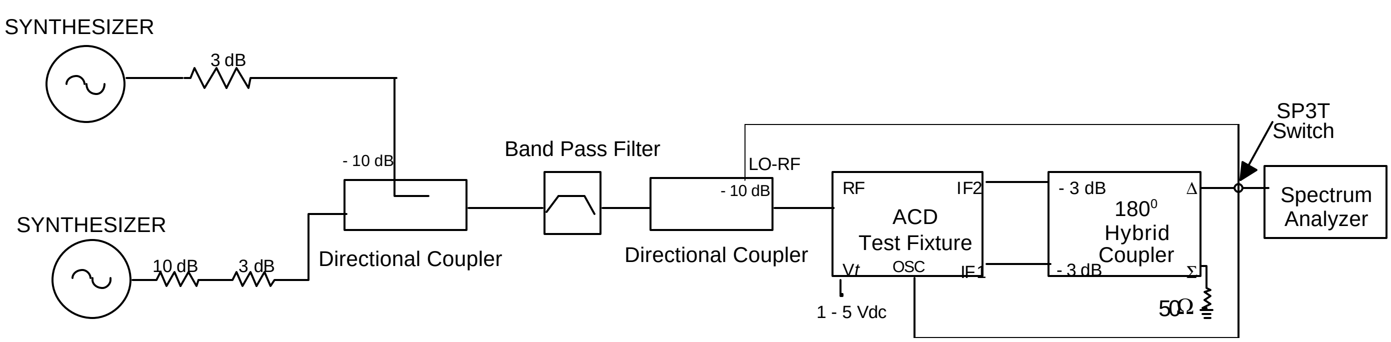


FIgure 10: IMD/ LO-RF/ Prescaler

Figures 9 and 10 show measurement setups which can be used to fully characterize the device.

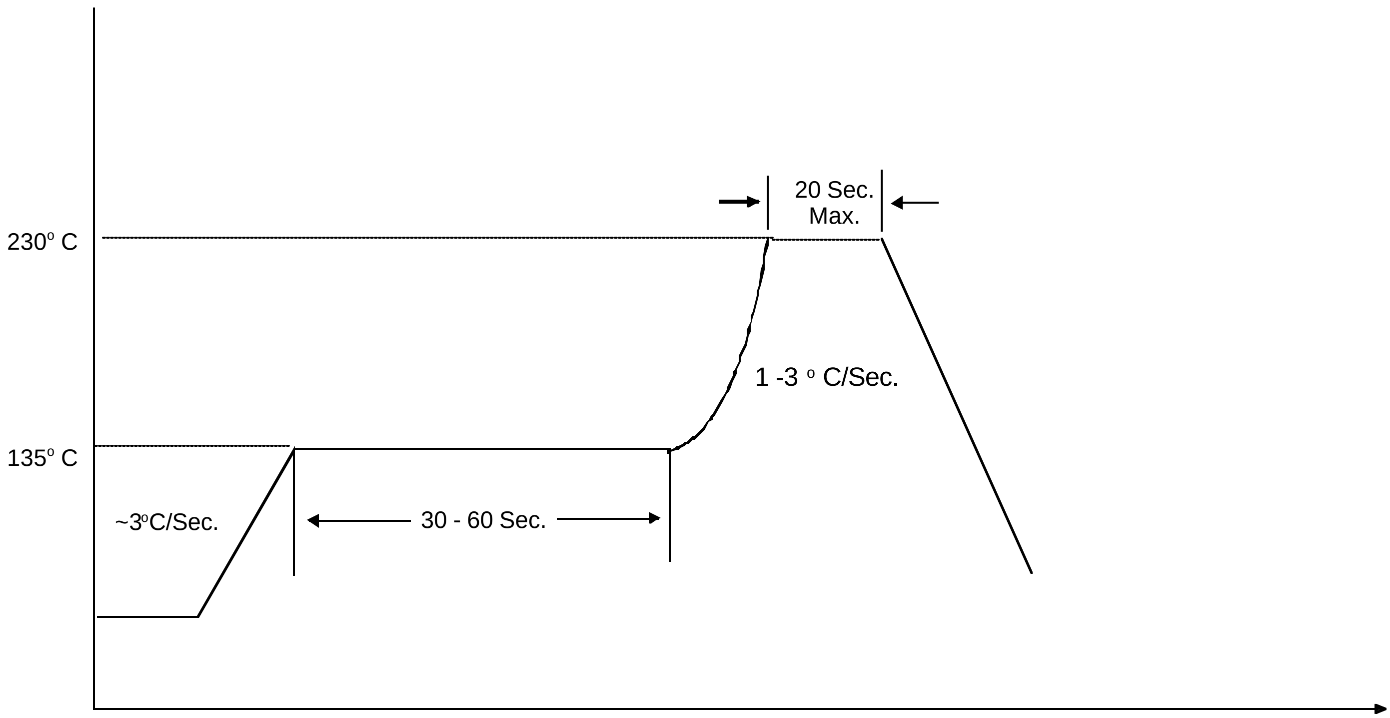


Figure 11: Temperature Profile for Surface Mount Assembly

NOTES

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