

Application Note

CDMA/AMPS 4mm x 4mm Power Amplifier Modules Rev 1

RELEVANT PRODUCTS

AWT6112

GENERAL DESCRIPTION

The 4mm x 4mm hetero-junction bipolar transistor (HBT) power amplifier modules designed for CDMA cellular handsets have an operating frequency band

from 824 MHz to 849 MHz and are designed to operate from a single lithium-ion (Li-ion) battery. The amplifier input and output are matched to provide optimum performance in a 50 Ω system; only minimal external components are required for proper RF bypassing. The tantalum capacitors, C8 and C9, are optional.

Table 1: Module Pin Description

PIN	NAME	DESCRIPTION	NOTES
1	Vref	Reference Voltage	+2.75 to +3.1 V for PA "on" 0 to +0.5 V for PA "shut down"
2	VMODE	Mode Control Voltage	+2.5 to +3.1 V for Low Bias Mode 0 to +0.5 V for High Bias Mode
4	RF⋈	RF Input	Use 50 Ω transmission line
5	Vcc	Supply Voltage	+3.2 to +4.2 V
6	Vcc	Supply Voltage	+3.2 to +4.2 V
8	RFоит	RF Output	Use 50 Ω transmission line
3, 7, 9, 10	GND	Ground	

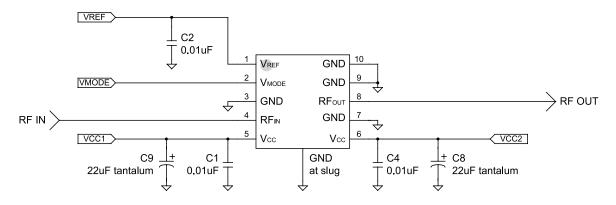


Figure 1. Evaluation Circuit

Note: Tantalum capacitors are not required in actual battery-operated applications.

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EVALUATION BOARD

The evaluation board, shown in Figure 2, was designed on GETEK material with 0.014" thickness:

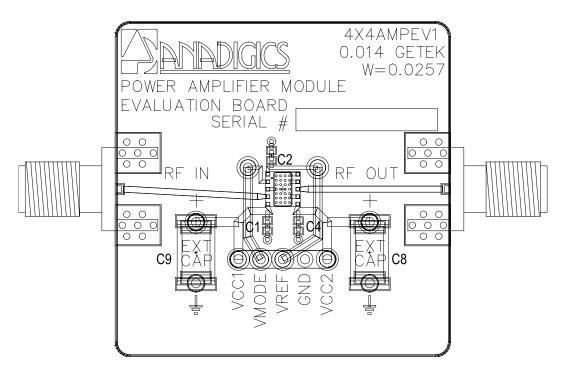


Figure 2: Evaluation Board Layout

Notes:

- 1. Copper trace width is 0.0257 +/- 0.001".
- 2. Relative dielectric constant is 4.37 at 1 GHz.
- 3. Dielectric thickness is 0.014 +/- 0.001".

Table 2: Evaluation Board Parts List

DESCRIPTION	VALUE	FUNCTION
C1	0.01μF	Bypass
C2	0.01μF	Bypass
C4	0.01μF	Bypass
C8	22μF, tant.	Bypass
C9	22μF, tant.	Bypass

Notes:

1. C3, C5, C6 and C7 not used.

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MINIMUM TEST BENCH REQUIREMENTS

The following minimum equipment is required for proper power amplifier evaluation:

- 1. Spectrum Analyzer
- 2. DC Power Supplies (3)
- 3. CDMA Function Generator
- 4. RF SAW (Surface Acoustic Wave) Filter
- 5. Isolator
- 6. RF Power Meter
- 7. Coupler(s)

TURN ON PROCEDURES

Upon receipt of the amplifier module, the characterization sheet should be reviewed for the appropriate bias conditions. Review the evaluation board drawing prior to connecting the bias pins. The order in which the supply, reference and control voltages are applied is offered as a recommendation only; the device will not be damaged if the sequence is altered. Do not exceed any maximum ratings for the device, per the product data sheet.

- 1. Connect the amplifier to 50 Ω RF input and output cables.
- 2. With all the DC supplies off, attach Vcc1, Vcc2, VREF and VMODE.
- 3. Set the VREF supply to +2.85 V, and observe a current draw of approximately 6.5 mA.
- 4. Set the Vcc1 and Vcc2 supplies to +3.4 V. Observe a current draw of approximately 90 mA from the Vcc supplies. (VMODE = 0 V, so the amplifier is in High Bias Mode.)
- 5. Apply an RF input power of 0 dBm. Adjust the input power until the appropriate output power level is obtained (+28 dBm in digital mode, +31 dBm in analog mode.)
- 6. Perform measurements.

LAYOUT CONSIDERATIONS

A sufficient number of plated through via holes should be placed under the module in order to channel the heat properly. In addition, contact should be made between the PA slug, located under the amplifier module, and the board. For hand assembly of the board, apply a sufficient amount of bonding paste, so that contact is made between the PA and ground. For large volume assembly, please refer to the Solder Reflow Report application note. For RF in/out, provide 50 Ω transmission lines.

OTHER RECOMMENDATIONS

For AMPS operation, the PA module achieves the analog mode full output power (+31 dBm) while operating in Low Bias Mode. This minimizes quiescent current (50 mA typical) and eliminates the need for mode switching between high and low power. In order to maximize performance in a CDMA system, both the Low and High Bias Modes should be used. Operation in the High Bias Mode allows the PA to exceed the system performance requirements at output power levels from +16 dBm to +28 dBm. For an output power less than +16 dBm, the Low Bias Mode should be used to minimize quiescent current while maintaining system performance. A logic low (0 V) at the VMODE pin places the PA in High Bias Mode, and a logic high (+3.0 V) at the VMODE pin places the PA in Low Bias Mode. Applying a logic low (0 V) to both the VREF and VMODE pins places the amplifier in shutdown (standby) mode.





ANADIGICS, Inc.

141 Mount Bethel Road Warren, New Jersey 07059, U.S.A.

Tel: +1 (908) 668-5000 Fax: +1 (908) 668-5132

URL: http://www.anadigics.com E-mail: Mktg@anadigics.com

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传真: 0755-83376182 (0) 13823648918 MSN: SUNS8888@hotmail.com

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深圳赛格展销部: 深圳华强北路赛格电子市场 2583 号 电话: 0755-83665529 25059422

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