Application Note

GSM850/GSM900/DCS/PCS
Quad Band Power Amplifier Module
With Integrated Power Control

Rev 0

RELEVANT PRODUCTS

- AWT6146

INTRODUCTION

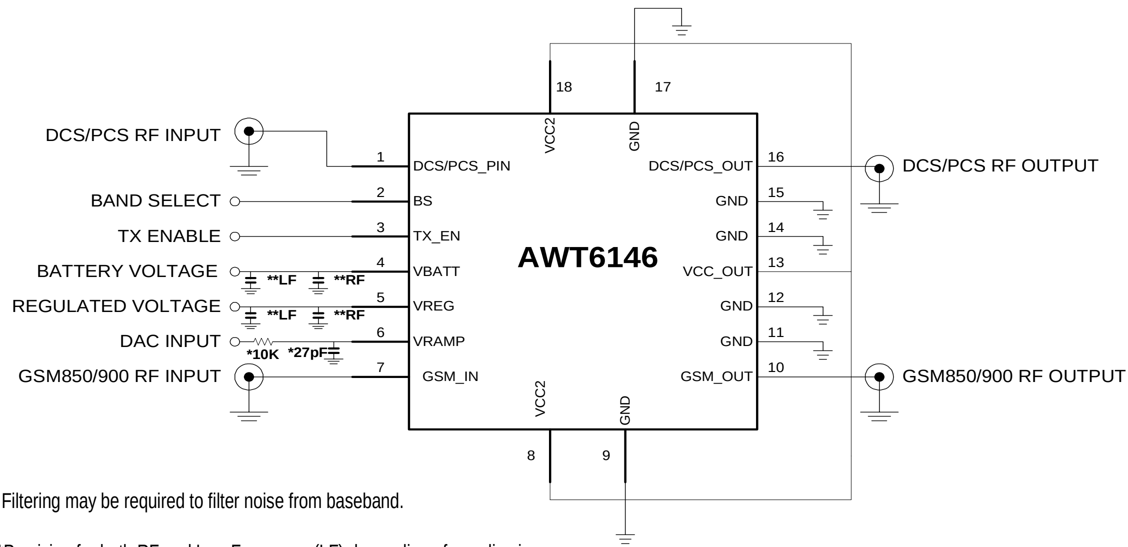
This power amplifier module is designed to support dual, tri and quad band applications. The module includes an integrated power control scheme that facilitates fast and easy production calibration and reduces the number of external components required to complete a power control function. This integrated control loop reduces the development time associated with optimizing loop filters to meet time mask and switching transient requirements, as it is completely self-contained.

The module size is a competitve 7mm x 7mm and with the few external components required, it is well suited for a small form factor transmit front-end solution.

GENERAL DESCRIPTION

The application circuit below shows the relative ease with which this amplifier can be designed into a GSM transmit front-end. All of the RF ports for this device are internally matched to 50Ω, with internal DC blocks provided at the RF ports.

The RF inputs can interface to transmit VCO's with the addition of simple attenuators. These can be used to set the input drive to the PA and is generally good practice to help minimise any possible load pulling effects at the VCO, PA interface. The RF outputs can interface directly to an antenna switch module to complete the front-end solution.



* Filtering may be required to filter noise from baseband.

**Provision for both RF and Low Frequency (LF) decoupling of supplies is recommended and consistent with good design practice. The values chosen depend on SRF of capacitors used, ground via inductance, capacitor location, and thus have layout dependency.

Figure 1: Application Schematic

DESCRIPTION (Continued)

The logical control inputs, TX_EN and BS, are both 1.8 V and 3 V logic compliant. The TX_EN is used to enable the amplifier typically with the TX burst. The BS is used to select which amplifier is enabled.

POWER CONTROL

The scheme used is a closed loop method that requires only the application of an analog voltage to the VRAMP pin to set the output power. This can be applied directly from a standard DAC output. The method used does not require any power or current sensing.

Setting the VRAMP voltage, in turn sets the collector voltages of the power amplifiers to a multiple of the VRAMP voltage using a pre-determined formula. This collector voltage is regulated in a voltage control loop as shown in Figure 2 below. The amplifier's bias is held constant while the collector voltage is adjusted to set the power. The relationship between the output power and collector voltage is represented by EQ 1.

$$P_{OUT}\,(\text{watts}) = \frac{(2V_{CC} - V_{SAT})^2}{(8.\,R_{LOAD})} \qquad \text{(EQ 1)}$$

where V_{CC}, V_{SAT} are the collector voltage and saturation voltage of the transistor respectively. This expression shows how the power variation due to VBATT is limited due to voltage control loop.

Under extreme conditons, as the battery voltage degrades, it is important to maintain the control loop bandwidth, so the collector voltage quickly follows VRAMP . This is done by adjusting VRAMP , such that:

$$\text{VRAMP} \leq 0.39 * \text{VBATT} - 0.17 \leq 1.5\text{V} \qquad \text{(EQ2)}$$

The effect of the loop bandwidth slowing can be seen most clearly in the switching transients measurement.

This adjustment can be incorporated in the software of the final application, so that performance is enhanced under low voltage conditions.

Another advantage of this control scheme is the improved noise performance due to individual stages being held in compression, thus improving the overall receive band noise performance.

HIGH FREQUENCY DECOUPLING

It is generally good practice to provide for high frequency bypassing on the supply lines of an RF module like the VBATT and VREG. Effective high frequency bypassing requires the component be placed as close as possible to the devices and provide as direct a path ground as possible with preferably a via connection to the board ground.

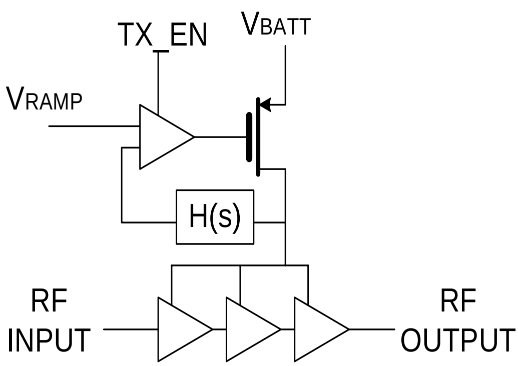


Figure 2: Voltage Control Loop

TIMING

In order to meet the GSM power time template and switching transients, the sequence of events outlined in figure 5 is recommended. The timing between VREG and BS is not critical, they just need to be enabled and settled prior to TX_EN going high (approx 2us).

The timing of the TX_EN is critical to ensure the application has sufficient margin for meeting the burst timing requirement.

The PA "forward isolation 1" parameter and the T/R switch isolation ensure the template is met outside the burst. The PA "forward isolation 2" parameter ensures the time template is met during the burst with sufficient margin.

The ramp profile should be as close as possible to a raised cosine waveform to achieve the spectral efficiency needed for meeting switching transient requirements.

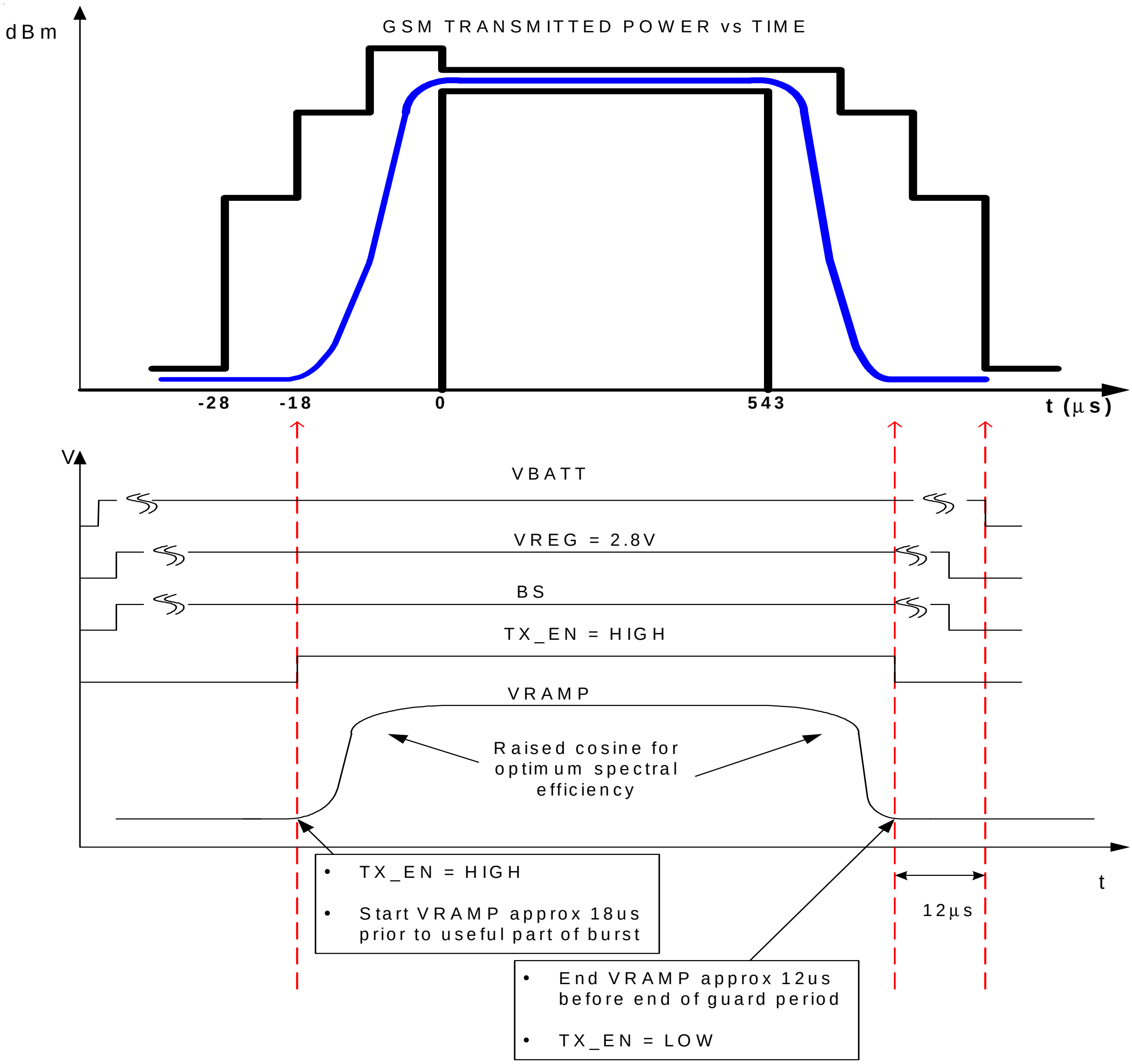


Figure 5: Timing recommendations

EVALUATION BOARD

The evaluation board is a multilayer board using GETEK substrate which is similar to FR4 but has a more controlled dielectric constant. The board thickness is 1.57mm.

All the routing is on the top layer (1) of a 4 layer board with a distance of 0.36mm to the ground plane, which is on layer 2. All RF routing has been sized to present a 50Ω impedance.

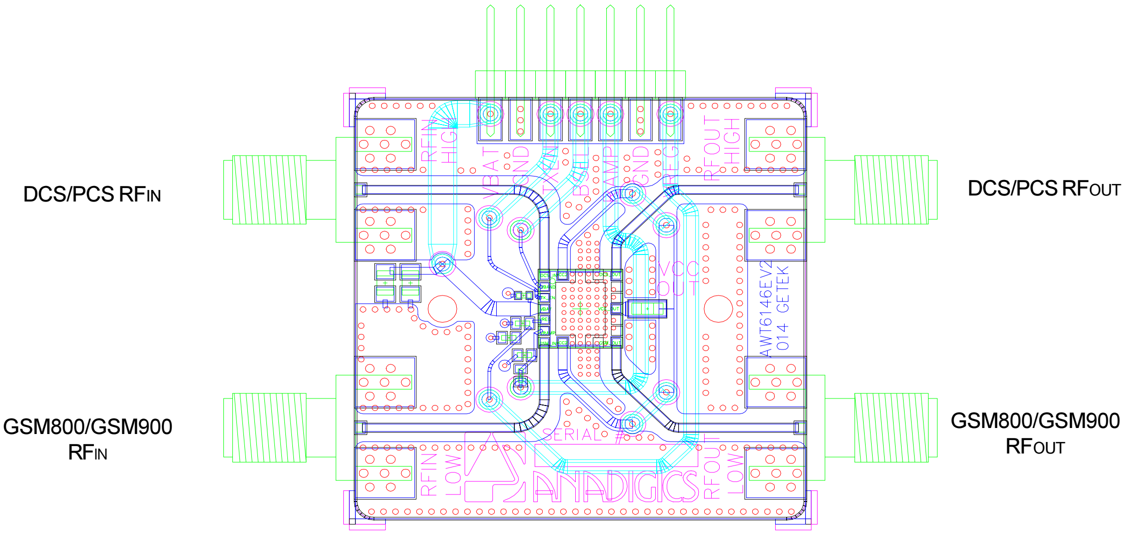


Figure 6: AWT6146 Evaluation Board

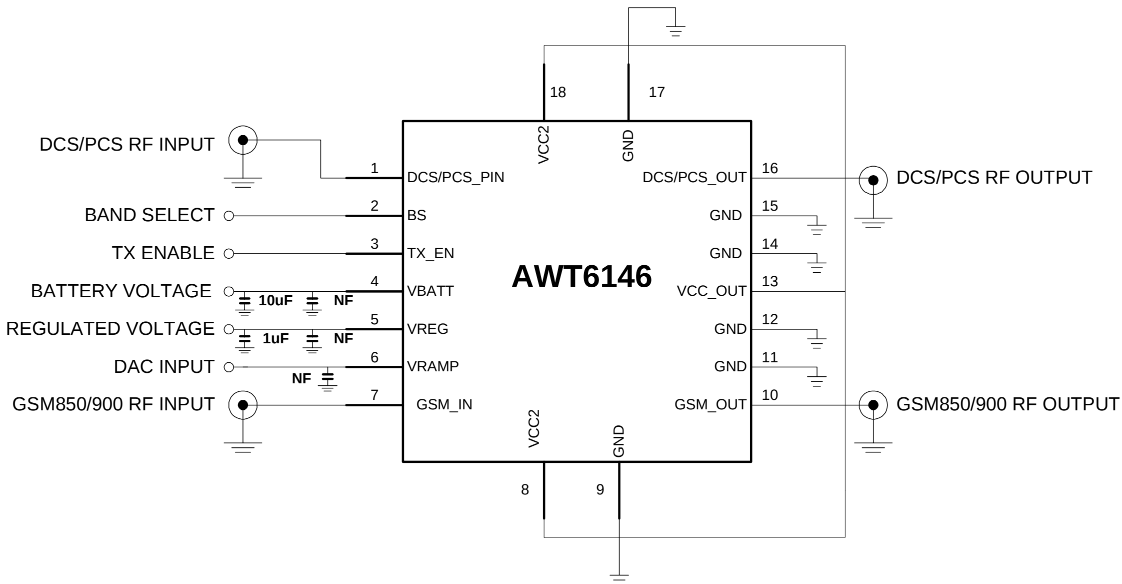
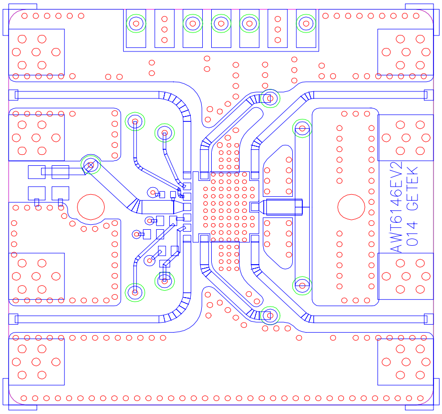
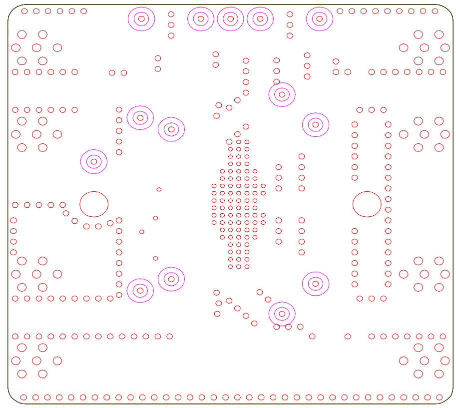


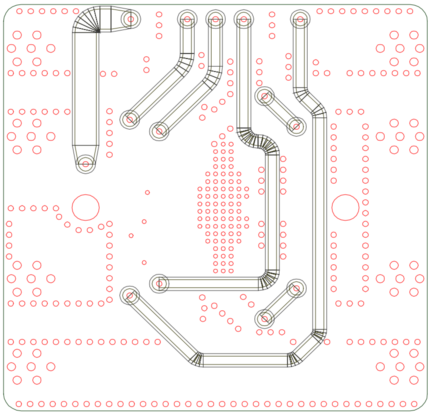
Figure 7: AWT6146 Evaluation Board Schematic



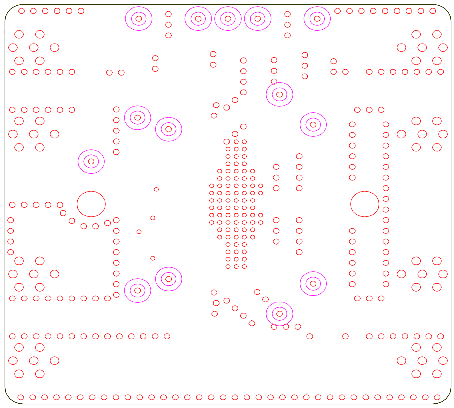
Layer 1



Layer 2



Layer 3



Layer 4

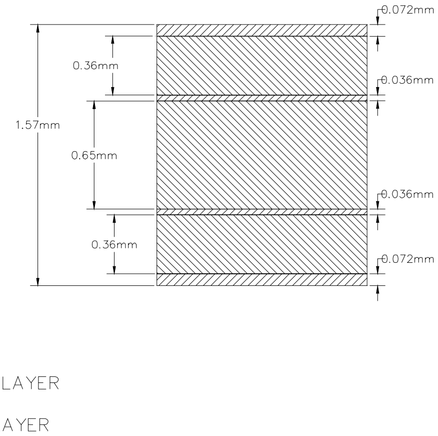


Figure 8: Evaluation Board Layout and Structure

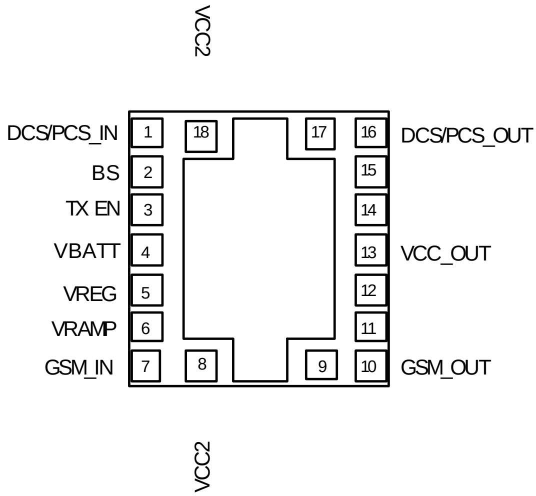
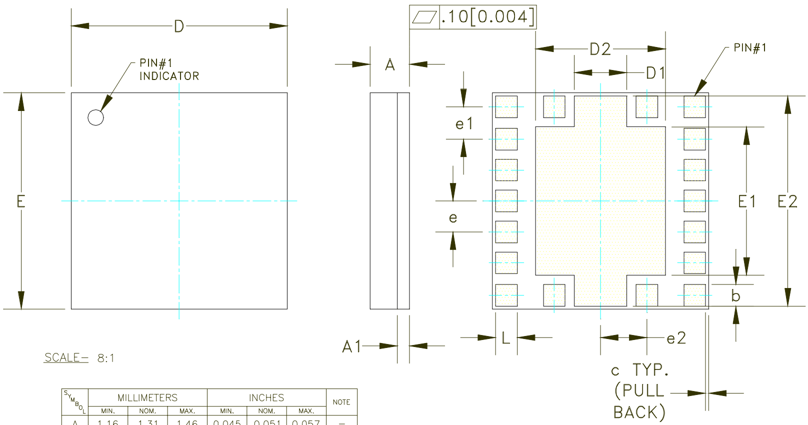


Figure 9: Pinout (X- Ray View)

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	DCS/PCS_IN	DCS/PCS RF Input	10	GSM_OUT	GSM850/900 RF Output
2	BS	Band Select Logic Input	11	GND	Ground
3	TX_EN	TX Enable Logic Input	12	GND	Ground
4	VBATT	Battery Supply Connection	13	VCC_OUT	Control Voltage Output which must be connected to VCC2, no decoupling
5	VREG	Regulated Supply Connection	14	GND	Ground
6	VRAMP	Analog Signal used to control the output power	15	GND	Ground
7	GSM_IN	GSM850/900 RF Input	16	DCS/PCS_OUT	DCS/PCS RF Output
8	VCC2	VCC Control Input for GSM850/900 Pre-amplifier	17	GND	Ground
9	GND	Ground	18	VCC2	VCC Control Input for DCS/PCS Pre-amplifier

Table 1: Pinout Description

PACKAGE OUTLINE



SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	1.16	1.31	1.46	0.045	0.051	0.057	–
A1	–	0.30	–	–	0.012	–	–
b	–	0.70	–	–	0.027	–	–
c	–	0.10	–	–	0.004	–	–
D	6.88	7.00	7.12	0.270	0.275	0.280	–
D1	–	1.70	–	–	0.067	–	–
D2	–	4.19	–	–	0.165	–	–
E	6.88	7.00	7.12	0.270	0.275	0.280	–
E1	–	4.80	–	–	0.189	–	–
E2	–	6.78	–	–	0.267	–	–
e	–	1.00	–	–	0.039	–	8X
e1	–	1.05	–	–	0.041	–	4X
e2	–	1.50	–	–	0.059	–	4X
L	–	0.70	–	–	0.027	–	–

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. –
–
–
–

Figure 10: Package Outline

NOTES

NOTES

NOTES

NOTES

ANADIGICS, Inc.
141 Mount Bethel Road
Warren, New Jersey 07059, U.S.A.
Tel: +1 (908) 668-5000
Fax: +1 (908) 668-5132

URL: http://www.anadigics.com
E-mail: Mktg@anadigics.com

IMPORTANT NOTICE

ANADIGICS, Inc. reserves the right to make changes to its products or to discontinue any product at any time without notice. The product specifications contained in Advanced Product Information sheets and Preliminary Data Sheets are subject to change prior to a product's formal introduction. Information in Data Sheets have been carefully checked and are assumed to be reliable; however, ANADIGICS assumes no responsibilities for inaccuracies. ANADIGICS strongly urges customers to verify that the information they are using is current before placing orders.

WARNING

ANADIGICS products are not intended for use in life support appliances, devices or systems. Use of an ANADIGICS product in any such application without written consent is prohibited.