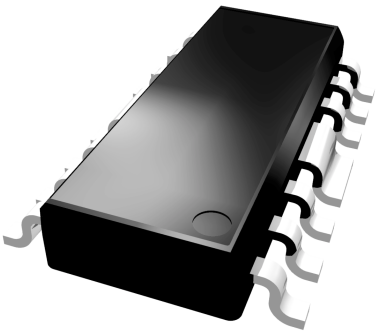
ADC20013

950-2050 MHz DBS Tuner IC

Data Sheet - Rev 2.9

FEATURES

- Monolithic DBS Tuner IC
- On Chip Oscillator
- 6 dB Noise Figure
- 11 dB Conversion Gain
- Single + 5V Supply
- Small Size
- Low Cost
- High Reliability
- Surface Mount Package



S3 Package
Modified 16 Pin SOIC

PRODUCT DESCRIPTION

The ANADIGICS DBS (Direct Broadcast Satellite) Tuner IC is intended for use in high volume, low cost manufacturing of compact DBS tuners for satellite receivers and integrated satellite ready TV/VTR receivers.

The ADC20013 Tuner IC provides DBS tuner manufacturers the ability to produce, in high volumes, tuners with low component count, minimal tuning, small size, high reliability and exceptional price-performance ratios. The ADC20013 offers a high degree of functionality in a very small and user friendly configuration.

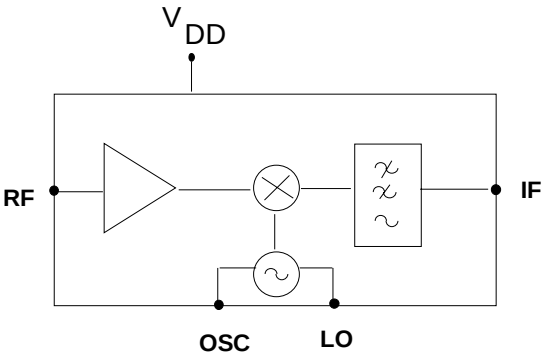


Figure 1: Functional Block Diagram

ELECTRICAL CHARACTERISTICS

Table 1: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
V_{DD}/V_{IF}	0	+7	VDC
V_{LO}	-5	+0.5	VDC
V_{RF}	-10	+0.5	VDC
V_{OSC}	-5	+0.5	VDC
Storage Temperature	-55	+100	°C
Input Power RF		+10	dBm
Input Power LO		+17	dBm

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 2: Operating Ranges

PARAMETER		MIN	TYP	MAX	UNIT
Frequency					
	RF	950	-	2050	MHz
	LO	1430	-	2530	MHz
	IF	-	480	-	MHz
V_{DD}		-	+5	-	VDC
Case Temperature		-55	-	+85	°C

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 3: Electrical Specifications

(T_A = 25 °C; V_{DD} = + 5V)

PARAMETER	MIN	TYP	MAX	UNIT
Conversion Gain(6)	6	11	-	dB
SSB Noise Figure(6)	-	6.5	11	dB
Third Order IMD(4) (-20 dBm Tones, 5 MHz Apart)	-	- 40	-35	dBc
Second Order IMD (-20 dBm Input Level)	-	- 25	- 20	dBc
LO Leakage (1),(2) RF Port IF Port	 - -	 - 30 0	 - 25 3	 dBm dBm
LO Output Level for PLL(3)	-8	- 4	-	dBm
Tuning Voltage (1) (VT)	1	-	20	Volts
VCO Phase Noise(5) 10 kHz Offset 100 kHz Offset	 - -	 - 70 - 100	 - 65 - 95	 dBc/Hz dBc/Hz
Input Impedance(7)	-	-	-	-
Output Impedance(7)	-	-	-	-
Power Supply Current	-	60	85	mA

Notes:

(1) Measured in ANADIGICS test fixture with Toshiba 1SV186 off-chip-varactor.

(2) Includes external coupling through test fixture.

(3) Oscillator output for external PLL. (Pin 14)

(4) Measured at 1450 & 1750 MHz.

(5) Measured using PLL (LBW =1KHz, Reference = 1.25 MHz, Step Size = 10 MHz).

(6) Measured in ANADIGICS test setup.

(7) See Smith charts.

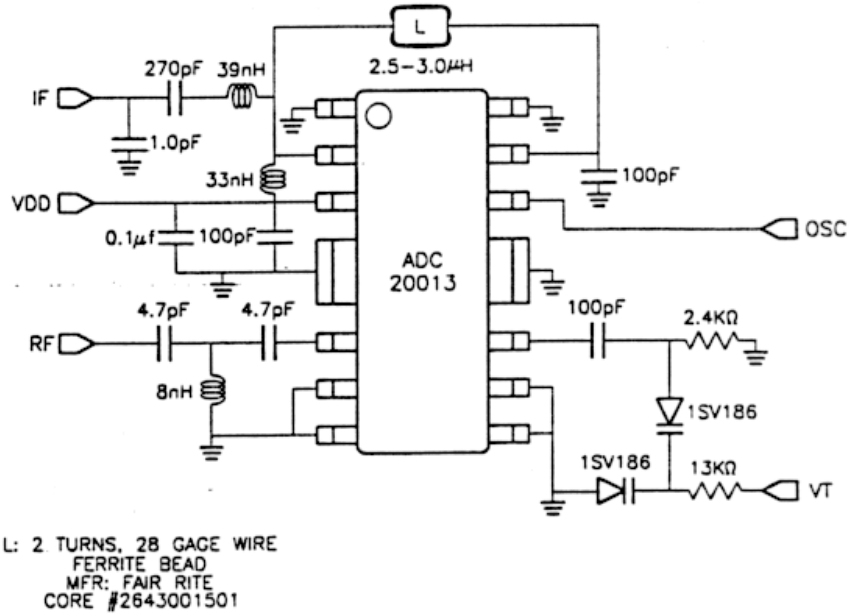


Figure 2: Test Circuit

PERFORMANCE DATA

Figure 3: Conversion Gain and Noise Figure vs Frequency

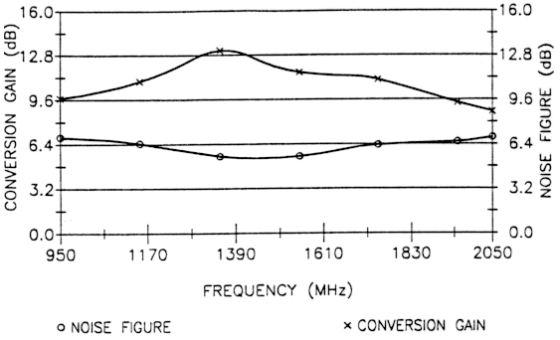


Figure 4: Oscillator Tuning Curve

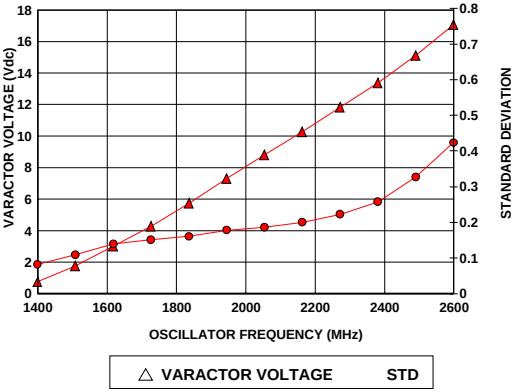


Figure 5: Third Order IMD RF Input Power Level -20dBm/Tone

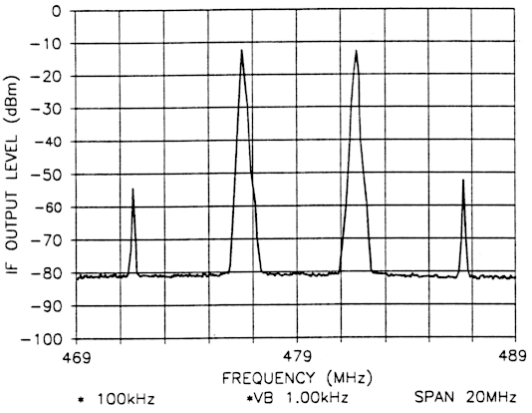


Figure 6: VCO Phase Noise

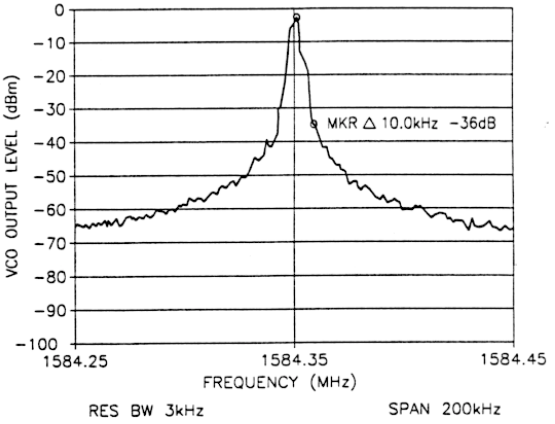
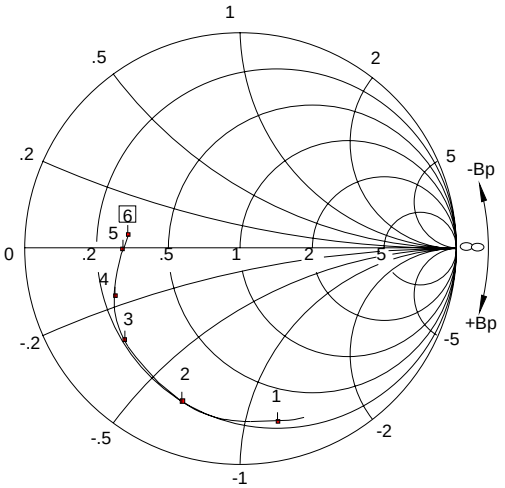


Figure 7: Input Impedance Data (RF)

1. IMPEDANCE REFERENCE AT PIN 6
2. VCO ON Vt = 3.20 VOLTS
3. Vdd = + 5 VOLTS
4. USE EXTERNAL BIAS TEE FOR IF

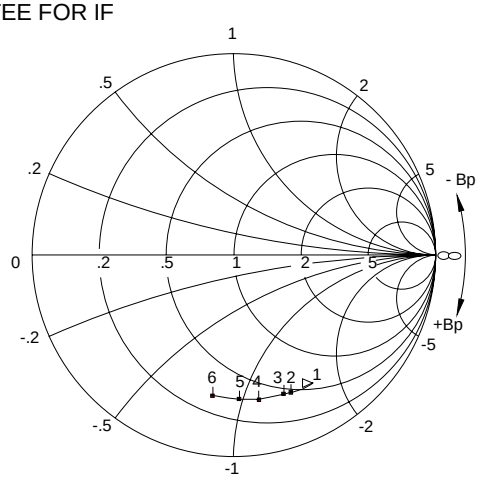


MEASURED IN 50 Ω SYSTEM

1	0.950 GHz 8.40 Ω - 61.53 j Ω
2	1.250 GHz 8.12 Ω -34.53 j Ω
3	1.550 GHz 10.13 Ω - 19.90 j Ω
4	1.750 GHz 12.75 Ω - 8.70 j Ω
5.	1.900 GHz 15.23 Ω - 3.03 jΩ
6.	2.050 GHz 16.33 Ω - 0.27 j Ω

Figure 8: Output Impedance Data (IF)

1. IMPEDANCE REFERENCE AT PIN 2
2. VCO ON Vt = 3.20 VOLTS
3. Vdd = + 5 VOLTS
4. USE EXTERNAL BIAS TEE FOR IF

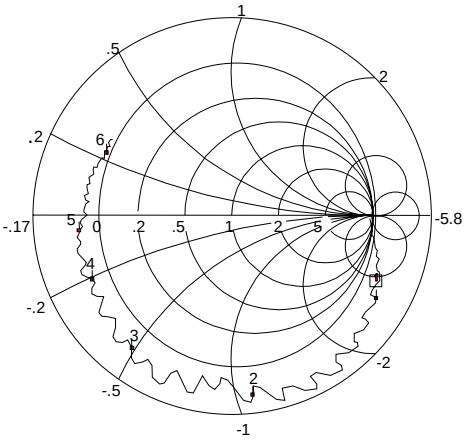


MEASURED IN 50 Ω SYSTEM

1	0.40 GHz 26.8 Ω - 82.8 j Ω
2	0.48 GHz 22.2 Ω - 70.0 j Ω
3	0.50 GHz 21.4 Ω - 67.5 j Ω
4	0.60 GHz 18.1 Ω - 56.2 j Ω
5.	0.70 GHz 15.9 Ω - 48.7 jΩ
6.	0.80 GHz 14 Ω - 41.2 j Ω

Figure 9: LO Impedance Data

1. IMPEDANCE REFERENCE AT PIN 11
2. Vdd = + 5 VOLTS



1 500.0 MHz
- 60.83 Ω
- 169.80 j Ω

2 1000.0 MHz
-15.15 Ω
-54.41 j Ω

3 1430.0 MHz
- 5.71 Ω
- 24.62 j Ω

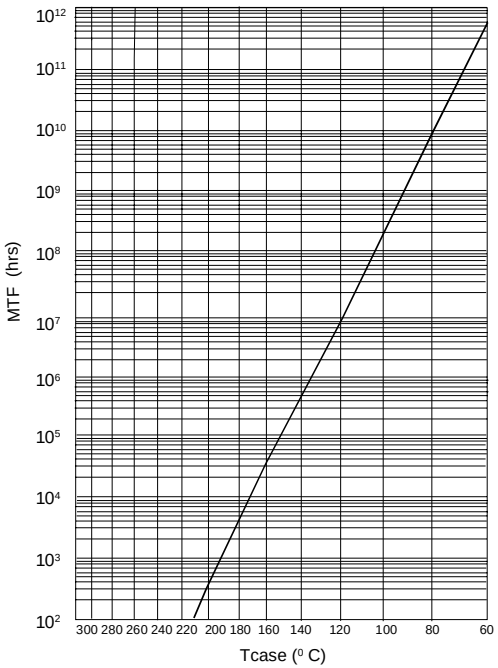
4 1700.0 MHz
- 2.80 Ω
- 12.02 j Ω

5. 1922.0 MHz
- 2.83 Ω
- 4.25 j Ω

6. 2768.0 MHz
0.54 Ω
-11.31 j Ω

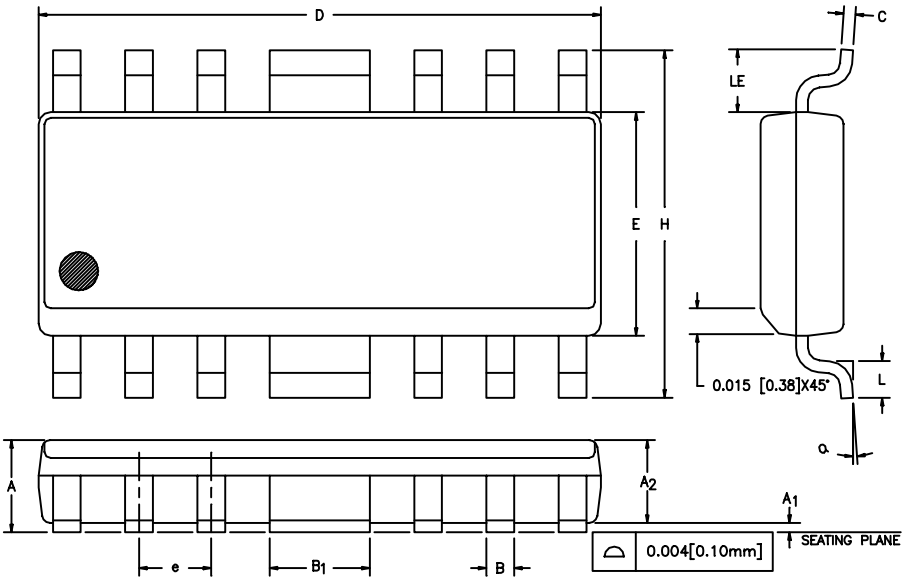
MEASURED IN 50 Ω SYSTEM

Figure 10: MTF vs. Tcase



$\theta_{JC} \simeq 60^{0}$ C/W

PACKAGE OUTLINE



SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.058	0.068	1.47	1.73	
A_1	0.004	0.010	0.10	0.25	
A_2	0.055	0.065	1.40	1.65	
B	0.013	0.020	0.33	0.50	
B_1	0.062	0.070	1.58	1.78	
C	0.008	0.010	0.20	0.25	4
D	0.380	0.400	9.66	10.16	2
E	0.150	0.160	3.81	4.06	3
e	0.050 BSC		1.27 BSC		
H	0.226	0.244	5.74	6.20	
L	0.016	0.040	0.41	1.02	
LE	0.030	—	0.76	—	
α	0°	8°	0°	8°	

NOTES:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE ±0.005 [0.13mm].
5. LEAD THICKNESS AFTER PLATING TO BE 0.013 [0.33mm] MAXIMUM.

Figure 11: S3 Package Outline - Modified 16 Pin SOIC

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ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ADC20013S3CTR	-55 to +85°C	Modified 16 Pin SOIC	3500 Piece Tape and Reel
ADC20013S3C	-55 to +85°C	Modified 16 Pin SOIC	Plastic Tubes (50 pcs. per tube)

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