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Agilent Technologies

# Optically Coupled 20 mA Current Loop Receiver

## Technical Data

**HCPL-4200**

### Features

- **Data Output Compatible with LSTTL, TTL and CMOS**
- **20 K Baud Data Rate at 1400 Metres Line Length**
- **Guaranteed Performance over Temperature (0°C to 70°C)**
- **Guaranteed On and Off Thresholds**
- **LED is Protected from Excess Current**
- **Input Threshold Hysteresis**
- **Three-State Output Compatible with Data Buses**
- **Internal Shield for High Common Mode Rejection**
- **Safety Approval**
  UL Recognized -3750 V rms, for 1 Minute
  CSA Approved
- **Optically Coupled 20 mA Current Loop Transmitter, HCPL-4100, Also Available**

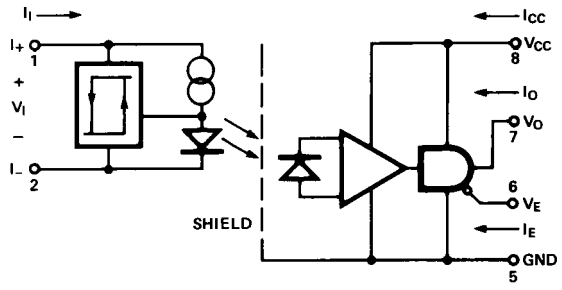
### Applications

- **Isolated 20 mA Current**
- **Loop Receiver in:**
  Computer Peripherals
  Industrial Control Equipment
  Data Communications Equipment

### Description

The HCPL-4200 optocoupler is designed to operate as a receiver in equipment using the 20 mA Current Loop. 20 mA current loop systems conventionally signal a logic high state by transmitting 20 mA of loop current (MARK), and signal a logic low state by allowing no more than a few milliamperes of loop current (SPACE). Optical coupling of the signal from the 20 mA current loop to the logic output breaks ground loops and provides for a very high common mode rejection. The HCPL-4200 aids in the design process by providing guaranteed thresholds for logic high state and logic low state for the current loop, providing an LSTTL, TTL, or CMOS compatible logic interface, and providing guaranteed common mode rejection. The buffer circuit on the current loop side of the HCPL-4200 provides typically 0.8 mA of hysteresis which increases the immunity to common mode and differential mode noise. The buffer also provides a controlled amount of LED drive current which takes into account any LED light output degradation. The internal shield allows a guaranteed 1000 V/µs common mode transient immunity.

### Functional Diagram




TRUTH TABLE (POSITIVE LOGIC)*

| $I_I$ | $V_E$ | $V_O$ |
|---|---|---|
| H | H | Z |
| L | H | Z |
| H | L | H |
| L | L | L |

*CURRENT LOOP CONVENTION –
H = MARK: $I_I \geq 12$ mA,
L = SPACE: $I_I \leq 3$ mA,
Z = OFF (HIGH IMPEDANCE) STATE.

A 0.1 µF bypass capacitor connected between pins 8 and 5 is recommended.

*CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

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## Ordering Information

Specify part number followed by Option Number (if desired).

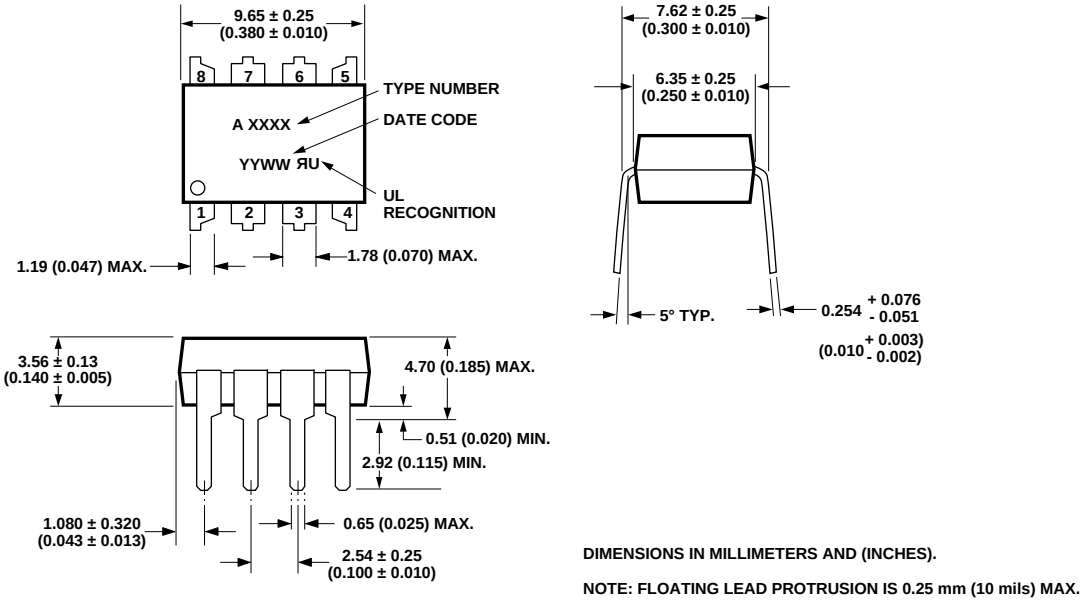
HCPL-4200# XXXX

- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 K min)
- XXXE = Lead Free Option

Option data sheets available. Contact your Agilent sales representative or authorized distributor for information.

Remarks: The notation "#" is used for existing products, while (new) products launched since 15th July 2001 and lead free option will use "–"

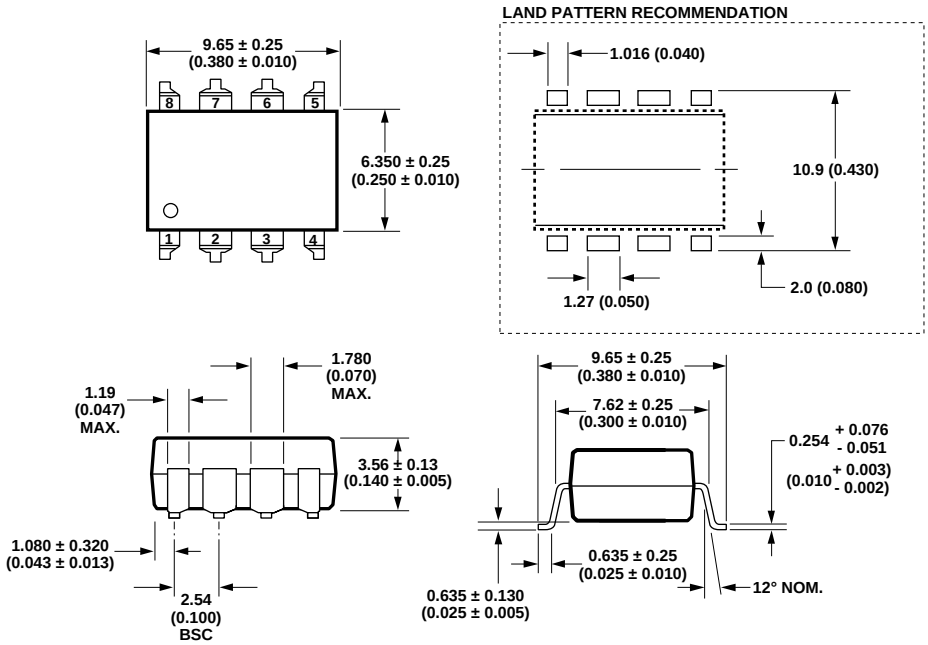
## Package Outline Drawings – 8 Pin DIP Package (HCPL-4200)




DIMENSIONS IN MILLIMETERS AND (INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

### 8 Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-4200)




DIMENSIONS IN MILLIMETERS (INCHES).

LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

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## Solder Reflow Thermal Profile

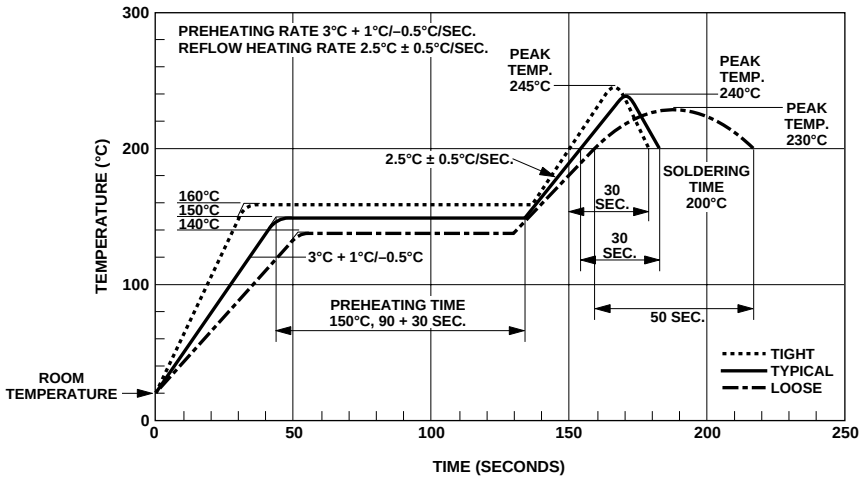
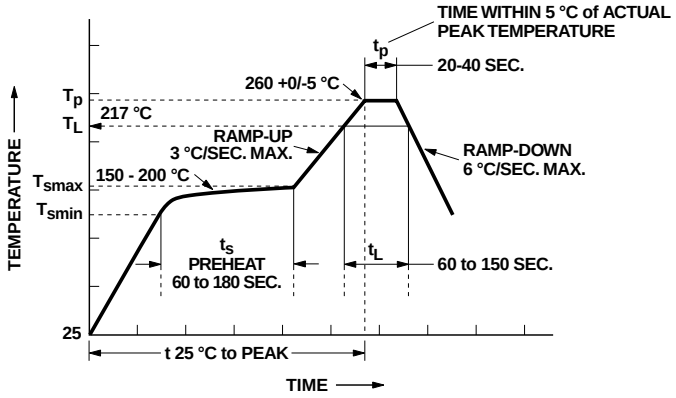



**Figure 1a. Solder Reflow Thermal Profile.**

## Recommended Pb-Free IR Profile




NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
$T_{smax}$ = 200 °C, $T_{smin}$ = 150 °C

**Figure 1b. Pb-Free IR Profile.**

## Regulatory Information

The HCPL-4200 has been approved by the following organizations:

### UL

Recognized under UL 1577, Component Recognition Program, File E55361.

### CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

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## Insulation and Safety Related Specifications

| Parameter | Symbol | Value | Units | Conditions |
|---|---|---|---|---|
| Min. External Air Gap (External Clearance) | L(IO1) | 7.1 | mm | Measured from input terminals to output terminals, shortest distance through air |
| Min. External Tracking Path (External Creepage) | L(IO2) | 7.4 | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Min. Internal Plastic Gap (Internal Clearance) | | 0.08 | mm | Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity |
| Tracking Resistance (Comparative Tracking Index) | CTI | 200 | volts | DIN IEC 112/VDE 0303 PART 1 |
| Isolation Group | | IIIa | | Material Group (DIN VDE 0110, 1/89, Table 1) |

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

## Absolute Maximum Ratings

(No Derating Required up to 70°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature .... 260°C for 10 s (1.6 mm below seating plane)
Supply Voltage – $V_{CC}$ ..... 0 V to 20 V
Average Input Current - $I_I$ ..... -30 mA to 30 mA
Peak Transient Input Current - $I_I$ ..... 0.5 A[1]
Enable Input Voltage – $V_E$ ..... -0.5 V to 20 V
Output Voltage – $V_O$ ..... -0.5 V to 20 V
Average Output Current – $I_O$ ..... 25 mA
Input Power Dissipation – $P_I$ ..... 90 mW[2]
Output Power Dissipation – $P_O$ ..... 210 mW[3]
Total Power Dissipation – P ..... 255 mW[4]
Infrared and Vapor Phase Reflow Temperature
(Option #300) ..... see Fig. 1, Thermal Profile

## Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 20 | Volts |
| Forward Input Current (SPACE) | $I_{SI}$ | 0 | 2.0 | mA |
| Forward Input Current (MARK) | $I_{MI}$ | 14 | 24 | mA |
| Operating Temperature | $T_A$ | 0 | 70 | °C |
| Fan Out | N | 0 | 4 | TTL Loads |
| Logic Low Enable Voltage | $V_{EL}$ | 0 | 0.8 | Volts |
| Logic High Enable Voltage | $V_{EH}$ | 2.0 | 20 | Volts |

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## DC Electrical Specifications

For 0°C ≤ $T_A$ ≤ 70°C, 4.5 V ≤ $V_{CC}$ ≤ 20 V, $V_E$ = 0.8 V, all typicals at $T_A$ = 25°C and $V_{CC}$ = 5 V unless otherwise noted. See note 13.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| Mark State Input Current | $I_{MI}$ | 12 | | | mA | | 2, 3, 4 | |
| Mark State Input Voltage | $V_{MI}$ | | 2.52 | 2.75 | Volts | $I_I$ = 20 mA $V_E$ = Don't Care | 4, 5 | |
| Space State Input Current | $I_{SI}$ | | | 3 | mA | | 2, 3, 4 | |
| Space State Input Voltage | $V_{SI}$ | | 1.6 | 2.2 | Volts | $I_I$ = 0.5 to 2.0 mA $V_E$ = Don't Care | 2, 4 | |
| Input Hysteresis Current | $I_{HYS}$ | 0.3 | 0.8 | | mA | | 2 | |
| Logic Low Output Voltage | $V_{OL}$ | | | 0.5 | Volts | $I_{OL}$ = 6.4 mA $I_I$ = 3 mA (4 TTL Loads) | 6 | |
| Logic High Output Voltage | $V_{OH}$ | 2.4 | | | Volts | $I_{OH}$ = -2.6 mA, $I_I$ = 12 mA | 7 | |
| Output Leakage Current ($V_{OUT}$ > $V_{CC}$) | $I_{OHH}$ | | | 100 | µA | $V_O$ = 5.5 V $I_I$ = 20 mA $V_{CC}$ = 4.5 V | | |
| | | | | 500 | µA | $V_O$ = 20 V | | |
| Logic High Enable Voltage | $V_{EH}$ | 2.0 | | | Volts | | | |
| Logic Low Enable Voltage | $V_{EL}$ | | | 0.8 | Volts | | | |
| Logic High Enable Current | $I_{EH}$ | | | 20 | µA | $V_E$ = 2.7 V | | |
| | | | | 100 | µA | $V_E$ = 5.5 V | | |
| | | | 0.004 | 250 | µA | $V_E$ = 20 V | | |
| Logic Low Enable Current | $I_{EL}$ | | | -0.32 | mA | $V_E$ = 0.4 V | | |
| Logic Low Supply Current | $I_{CCL}$ | | 4.5 | 6.0 | mA | $V_{CC}$ = 5.5 V $I_I$ = 0 mA $V_E$ = Don't Care | | |
| | | | 5.25 | 7.5 | mA | $V_{CC}$ = 20 V | | |
| Logic High Supply Current | $I_{CCH}$ | | 2.7 | 4.5 | mA | $V_{CC}$ = 5.5 V $I_I$ = 20 mA $V_E$ = Don't Care | | |
| | | | 3.1 | 6.0 | mA | $V_{CC}$ = 20 V | | |
| High Impedance State Output Current | $I_{OZL}$ | | | -20 | µA | $V_O$ = 0.4 V $V_E$ = 2 V, $I_I$ = 20 mA | | |
| | $I_{OZH}$ | | | 20 | µA | $V_O$ = 2.4 V | | |
| | | | | 100 | µA | $V_O$ = 5.5 V | | |
| | | | | 500 | µA | $V_O$ = 20 V | | |
| Logic Low Short Circuit Output Current | $I_{OSL}$ | 25 | | | mA | $V_O$ = $V_{CC}$ = 5.5 V $I_I$ = 0 mA | | 5 |
| | | 40 | | | mA | $V_O$ = $V_{CC}$ = 20 V | | |
| Logic High Short Circuit Output Current | $I_{OSH}$ | -10 | | | mA | $V_{CC}$ = 5.5 V $I_I$ = 20 mA $V_O$ = GND | | 5 |
| | | -25 | | | mA | $V_{CC}$ = 20 V | | |
| Input Capacitance | $C_{IN}$ | | 120 | | pF | f = 1 MHz, $V_I$ = 0 V dc, Pins 1 and 2 | | |

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## Switching Specifications

For 0°C ≤ $T_A$ ≤ 70°C, 4.5 V ≤ $V_{CC}$ ≤ 20 V, $V_E$ = 0.8 V, all typicals at $T_A$ = 25°C and $V_{CC}$ = 5 V unless otherwise noted. See note 13.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time to Logic High Output Level | $t_{PLH}$ | | 0.23 | 1.6 | µs | $V_E$ = 0 V, $C_L$ = 15 pF | 8, 9, 10 | 7 |
| Propagation Delay Time to Logic Low Output Level | $t_{PHL}$ | | 0.17 | 1.0 | µs | $V_E$ = 0 V, $C_L$ = 15 pF | 8, 9, 10 | 8 |
| Propagation Delay Time Skew | $t_{PLH} - t_{PHL}$ | | 60 | | ns | $I_I$ = 20 mA, $C_L$ = 15 pF | 8, 9, 10 | |
| Output Enable Time to Logic Low Level | $t_{PZL}$ | | 25 | | ns | $I_I$ = 0 mA, $C_L$ = 15 pF | 12, 13, 15 | |
| Output Enable Time to Logic High Level | $t_{PZH}$ | | 28 | | ns | $I_I$ = 20 mA, $C_L$ = 15 pF | 12, 13, 14 | |
| Output Disable Time to Logic Low Level | $t_{PLZ}$ | | 60 | | ns | $I_I$ = 0 mA, $C_L$ = 15 pF | 12, 13, 15 | |
| Output Disable Time to Logic High Level | $t_{PHZ}$ | | 105 | | ns | $I_I$ = 20 mA, $C_L$ = 15 pF | 12, 13, 14 | |
| Output Rise Time (10-90%) | $t_r$ | | 55 | | ns | $V_{CC}$ = 5 V, $C_L$ = 15 pF | 8, 9, 11 | 9 |
| Output Fall Time (90-10%) | $t_f$ | | 15 | | ns | $V_{CC}$ = 5 V, $C_L$ = 15 pF | 8, 9, 11 | 10 |
| Common Mode Transient Immunity at Logic High Output Level | $\|CM_H\|$ | 1,000 | 10,000 | | V/µs | $V_{CM}$ = 50 V (peak) $I_I$ = 12 mA, $T_A$ = 25°C | 16 | 11 |
| Common Mode Transient Immunity at Logic Low Output Level | $\|CM_L\|$ | 1,000 | 10,000 | | V/µs | $V_{CM}$ = 50 V (peak) $I_I$ = 3 mA, $T_A$ = 25°C | 16 | 12 |

## Package Characteristics

For 0°C ≤ $T_A$ ≤ 70°C, unless otherwise specified. All typicals at $T_A$ = 25°C.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Fig. | Notes |
|---|---|---|---|---|---|---|---|---|
| Input-Output Momentary Withstand Voltage* | $V_{ISO}$ | 3750 | | | V rms | RH ≤ 50%, t = 1 min, $T_A$ = 25°C | | 6, 14 |
| Resistance, Input-Output | $R_{I-O}$ | | $10^{12}$ | | ohms | $V_{I-O}$ = 500 V dc | | 6 |
| Capacitance, Input-Output | $C_{I-O}$ | | 1.0 | | pF | f = 1 MHz, $V_{I-O}$ = 0 V | | 6 |

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table (if applicable), your equipment level safety specification, or Agilent Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

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**Notes:**

1. ≤ 1 µs pulse width, 300 pps.
2. Derate linearly above 70°C free air temperature at a rate of 1.6 mW/°C. Proper application of the derating factors will prevent IC junction temperatures from exceeding 125°C for ambient temperatures up to 85°C.
3. Derate linearly above 70°C free air temperature at a rate of 3.8 mW/°C.
4. Derate linearly above 70°C free air temperature at a rate of 4.6 mW/°C.
5. Duration of output short circuit time shall not exceed 10 ms.
6. The device is considered a two terminal device, pins 1, 2, 3, and 4 are connected together and pins 5, 6, 7, and 8 are connected together.
7. The $t_{PLH}$ propagation delay is measured from the 10 mA level on the leading edge of the input pulse to the 1.3 V level on the leading edge of the output pulse.
8. The $t_{PHL}$ propagation delay is measured from the 10 mA level on the trailing edge of the input pulse to the 1.3 V level on the trailing edge of the output pulse.
9. The rise time, $t_r$, is measured from the 10% to the 90% level on the rising edge of the output logic pulse.
10. The fall time, $t_f$, is measured from the 90% to the 10% level on the falling edge of the output logic pulse.
11. Common mode transient immunity in the logic high level is the maximum (negative) $dV_{CM}/dt$ on the trailing edge of the common mode pulse, $V_{CM}$, which can be sustained with the output voltage in the logic high state (i.e., $V_O \geq 2$ V).
12. Common mode transient immunity in the logic low level is the maximum (positive) $dV_{CM}/dt$ on the leading edge of the common mode pulse, $V_{CM}$, which can be sustained with the output voltage in the logic low state (i.e., $V_O \leq 0.8$ V).
13. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.
14. In accordance with UL 1577, each optocoupler momentary withstand is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ µA).

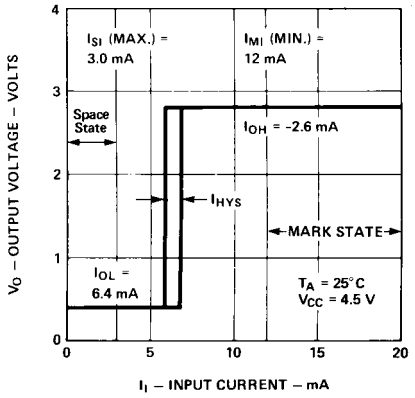


**Figure 2. Typical Output Voltage vs. Loop Current.**

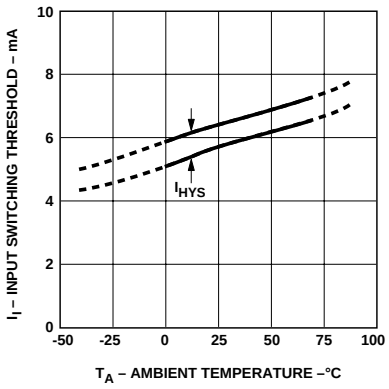


**Figure 3. Typical Current Switching Threshold vs. Temperature.**

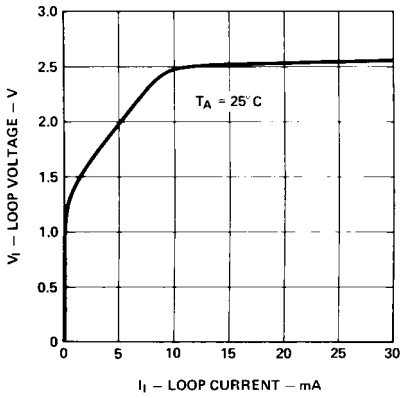


**Figure 4. Typical Input Loop Voltage vs. Input Current.**

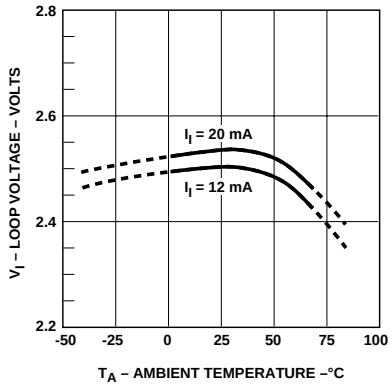


**Figure 5. Typical Input Voltage vs. Temperature.**

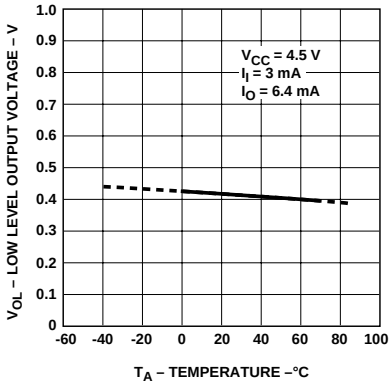


**Figure 6. Typical Logic Low Output Voltage vs. Temperature.**

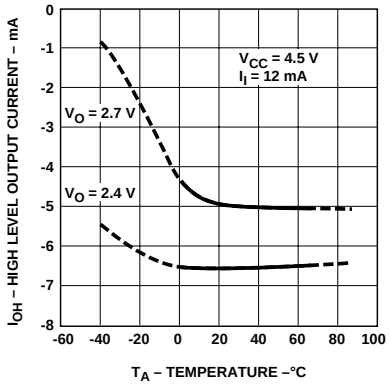


**Figure 7. Typical Logic High Output Current vs. Temperature.**

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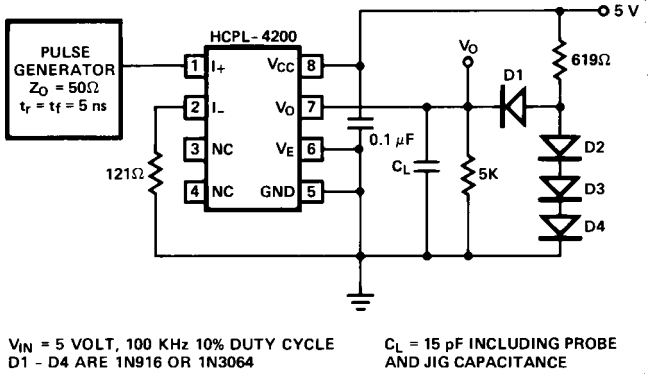


**Figure 8. Test Circuit for $t_{PHL}$, $t_{PLH}$, $t_r$, and $t_f$.**

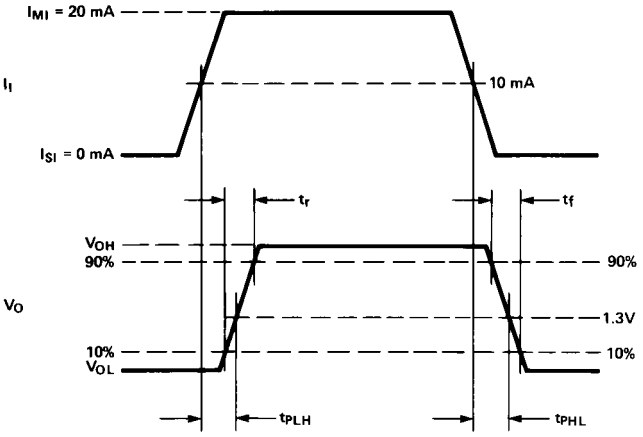


**Figure 9. Waveforms for $t_{PHL}$, $t_{PLH}$, $t_r$, and $t_f$.**

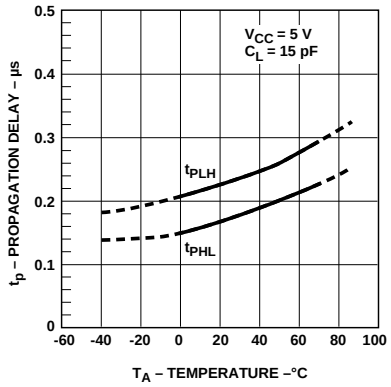


**Figure 10. Typical Propagation Delay vs. Temperature.**

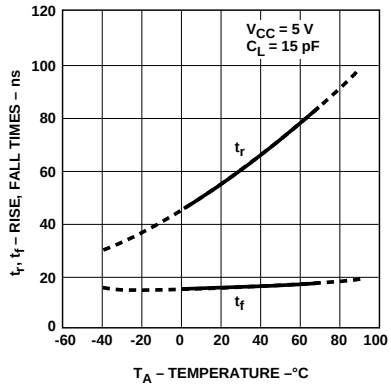


**Figure 11. Typical Rise, Fall Time vs. Temperature.**

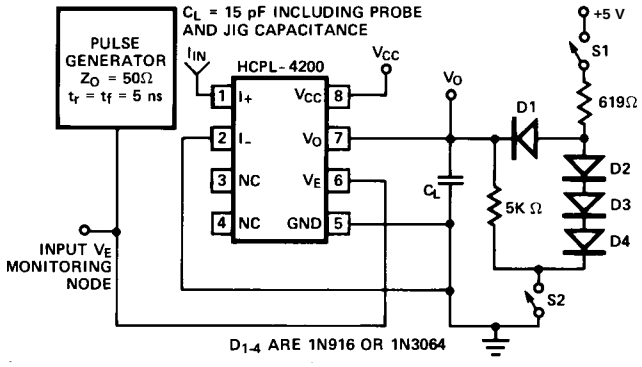


**Figure 12. Test Circuit for $t_{PZH}$, $t_{PZL}$, $t_{PHZ}$, and $t_{PLZ}$.**

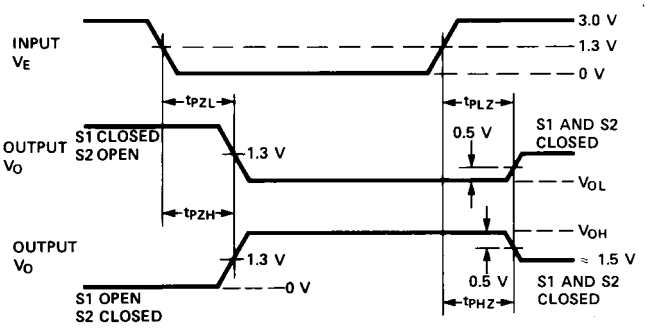


**Figure 13. Waveforms for $t_{PZH}$, $t_{PZL}$, $t_{PHZ}$, and $t_{PLZ}$.**

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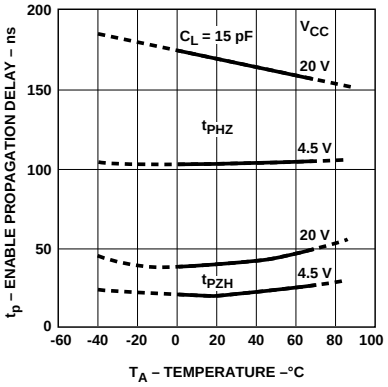


**Figure 14. Typical Logic High Enable Propagation Delay vs. Temperature.**

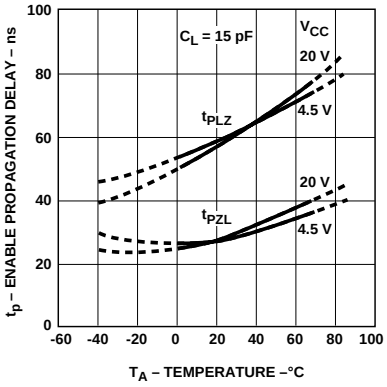


**Figure 15. Typical Logic Low Enable Propagation Delay vs. Temperature.**

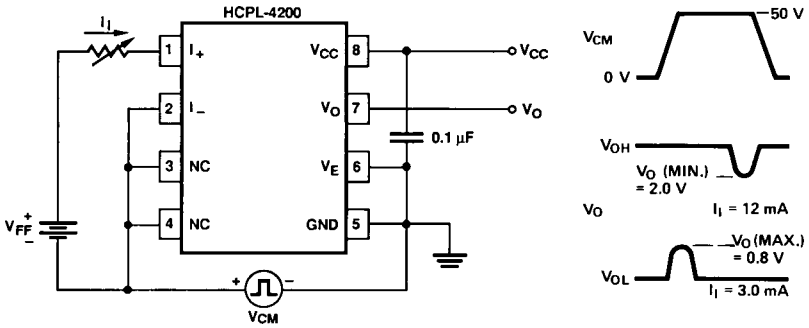


**Figure 16. Test Circuit for Common Mode Transient Immunity.**

## Applications

Data transfer between equipment which employs current loop circuits can be accomplished via one of three configurations: simplex, half duplex or full duplex communication. With these configurations, point-to-point and multidrop arrangements are possible. The appropriate configuration to use depends upon data rate, number of stations, number and length of lines, direction of data flow, protocol, current source location and voltage compliance value, etc.

### Simplex

The simplex configuration, whether point to point or multi-drop, gives unidirectional data flow from transmitter to receiver(s). This is the simplest configuration for use in long line length (two wire), for high data rate, and low current source compliance level applications. Block diagrams of simplex point-to-point and multidrop arrangements are given in Figures 17a and 17b respectively for the HCPL-4200 receiver optocoupler.

For the highest data rate performance in a current loop, the configuration of a non-isolated active transmitter (containing current source) transmitting data to a remote isolated receiver(s) should be used. When the current source is located at the transmitter end, the loop is charged approximately to $V_{MI}$ (2.5 V). Alternatively, when the current source is located at the receiver end, the loop is charged to the full compliance voltage level. The lower the charged voltage level the faster the data rate will be. In the configurations of Figures 17a and 17b, data rate is independent of the current source voltage compliance level. An adequate compliance level of current source must be available for voltage drops across station(s) during the MARK state in multi-drop applications or for long line length. The maximum compliance level is determined by the transmitter breakdown characteristic.

A recommended non-isolated active transmitter circuit which can be used with the HCPL-4200 in point-to-point or in multidrop 20 mA current loop applications is given in Figure 18. The current source is controlled via a standard TTL 7407 buffer to provide high output impedance of current source in both the ON

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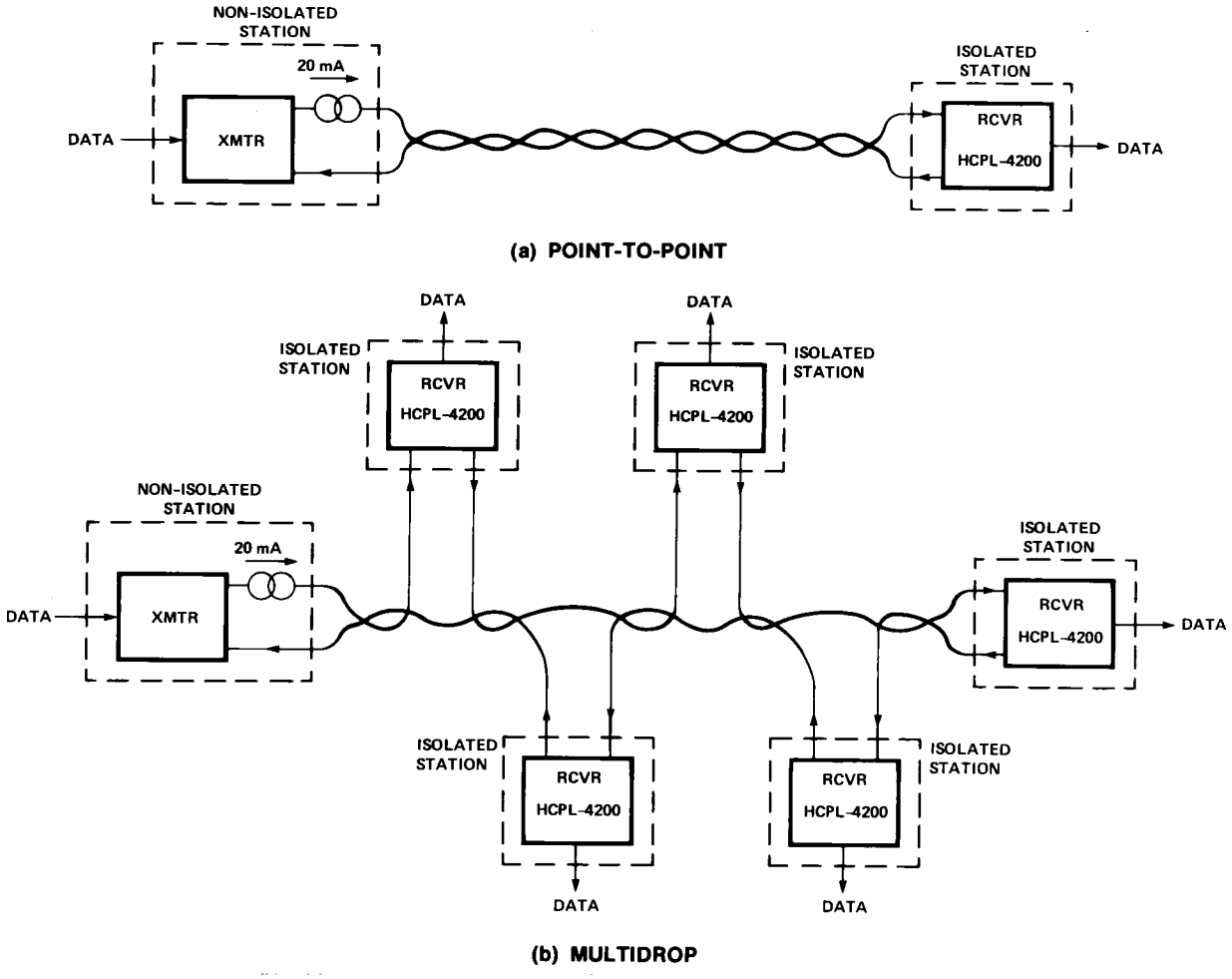


**Figure 17. Simplex Current Loop System Configurations for (a) Point-to-Point, (b) Multidrop.**

and OFF states. This non-isolated active transmitter provides a nominal 20 mA loop current for the listed values of $V_{CC}$, R2 and R3 in Figure 18.

Length of current loop (one direction) versus minimum required DC supply voltage, $V_{CC}$, of the circuit in Figure 18 is graphically illustrated in Figure 19. Multidrop configurations will require larger $V_{CC}$ than Figure 19 predicts in order to account for additional station terminal voltage drops.

Typical data rate performance versus distance is illustrated in Figure 20 for the combination of a non-isolated active transmitter and HCPL-4200 optically coupled current loop receiver shown in Figure 18. Curves are shown for 10% and 25% distortion data rate. 10% (25%) distortion data rate is defined as that rate at which 10% (25%) distortion occurs to output bit interval with respect to input bit interval. An input Non-Return-to-Zero (NRZ) test waveform of 16 bits (0000001011111101) was used for data rate distortion measurements. Data rate is independent of current source supply voltage, $V_{CC}$.

The cable used contained five pairs of unshielded, twisted, 22 AWG wire (Dearborn #862205). Loop current is 20 mA nominal. Input and output logic supply voltages are 5 V dc.

## Full Duplex

The full duplex point-to-point communication of Figure 21 uses a four wire system to provide simultaneous, bidirectional data communication between local and remote equipment. The basic application uses two simplex point-to-point loops which have two separate, active, non-isolated units at one common end of the loops. The other end of each loop is isolated.

As Figure 21 illustrates, the combination of Agilent current loop optocouplers, HCPL-4100 transmitter and HCPL-4200

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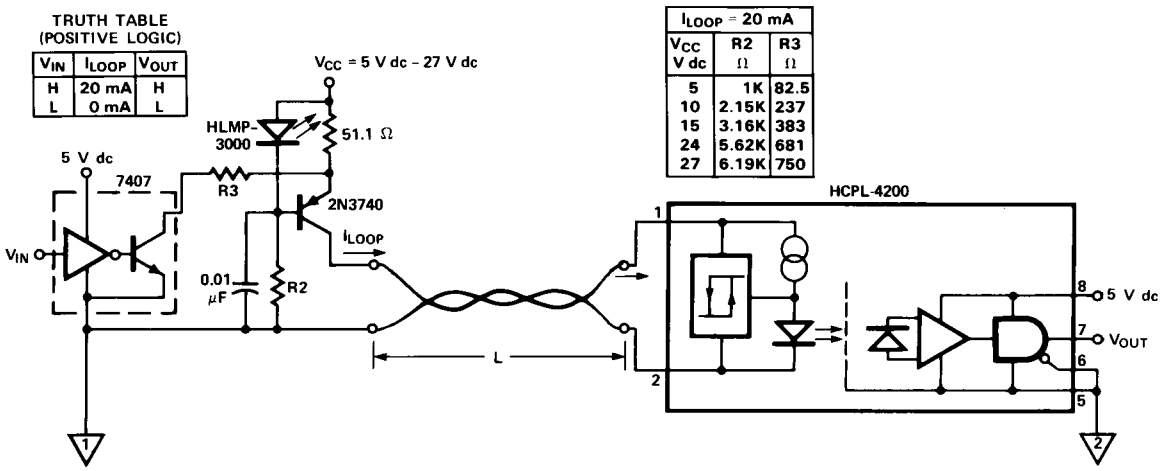


**Figure 18. Recommended Non-Isolated Active Transmitter with HCPL-4200 Isolated Receiver for Simplex Point-to-Point 20 mA Current Loop.**

receiver, can be used at the isolated end of current loops. Cross talk and common mode coupling are greatly reduced when optical isolation is implemented at the same end of both loops, as shown. The full duplex data rate is limited by the non-isolated active receiver current loop. Comments mentioned under simplex configuration apply to the full duplex case. Consult the HCPL-4100 transmitter optocoupler data sheet for specified device performance.

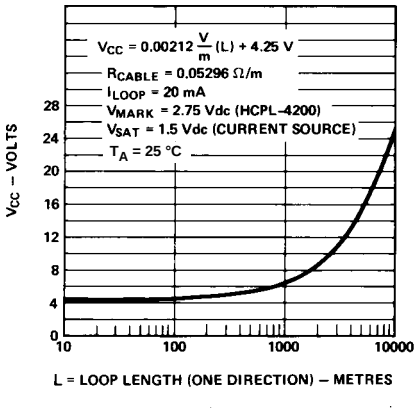


**Figure 19. Minimum Required Supply Voltage, $V_{CC}$, vs. Loop Length for Current Loop Circuit of Figure 19.**

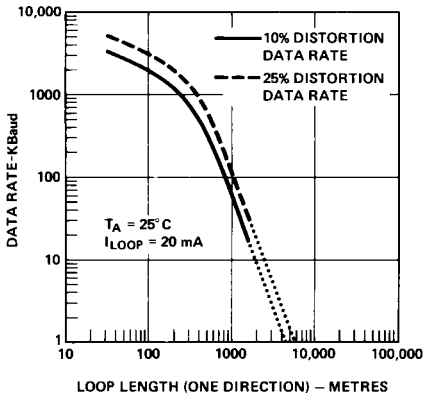


**Figure 20. Typical Data Rate vs. Distance.**

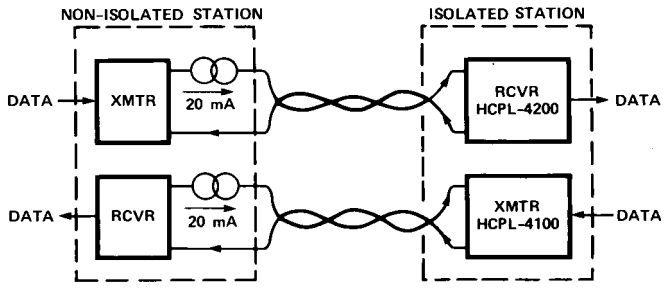


**Figure 21. Full Duplex Point-to-Point Current Loop System Configuration.**

## Half Duplex

The half duplex configuration, whether point-to-point or multidrop, gives non-simultaneous bidirectional data flow from transmitters to receivers shown in Figures 22a and 22b. This configuration allows the use of two wires to carry data back and forth between local and remote units. However, protocol must be used to determine which specific transmitter can operate at any given time. Maximum data rate for a half duplex system is limited by the loop current charging time. These considerations were explained in the Simplex configuration section.

Figures 22a and 22b illustrate half duplex application for the combination of HCPL-4100/-4200 optocouplers. The unique and complementary designs of the HCPL-4100 transmitter and HCPL-4200 receiver optocouplers provide many designed-in benefits. For example, total optical isolation at one end of the current loop is easily accomplished, which results in substantial removal of common mode influences, elimination of ground potential

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differences and reduction of power supply requirements. With this combination of HCPL-4100/-4200 optocouplers, specific current loop noise immunity is provided, i.e., minimum SPACE state current noise immunity is 1 mA, MARK state noise immunity is 8 mA.

Voltage compliance of the current source must be of an adequate level for operating all units in the loop while not exceeding 27 V dc, the maximum breakdown voltage for the HCPL-4100. Note that the HCPL-4100 transmitter will allow loop current to conduct when input $V_{CC}$ power is off. Consult the HCPL-4100 transmitter optocoupler data sheet for specified device performance.

For more information about the HCPL-4100/-4200 optocouplers, consult Application Note 1018.

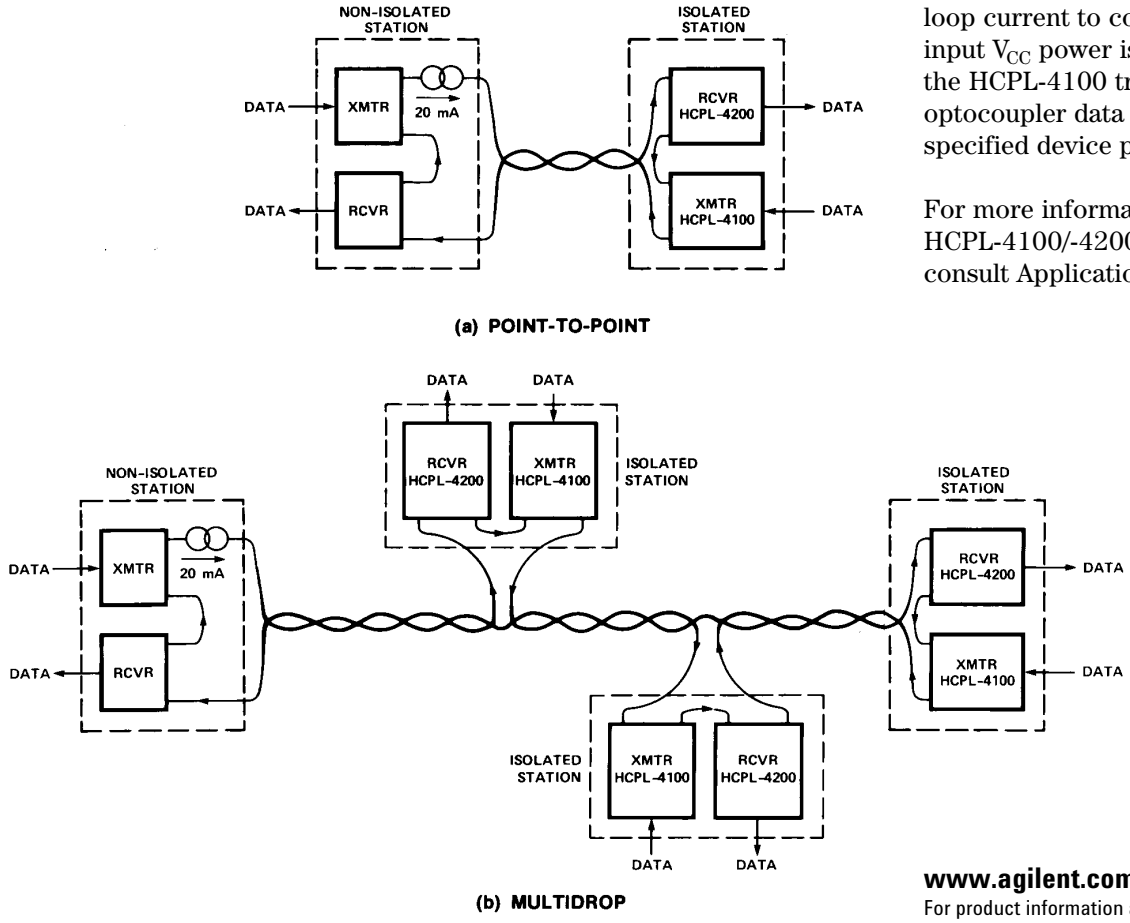


**Figure 22. Half Duplex Current Loop System Configurations for (a) Point-to-Point, (b) Multidrop.**

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