HCPL-0738

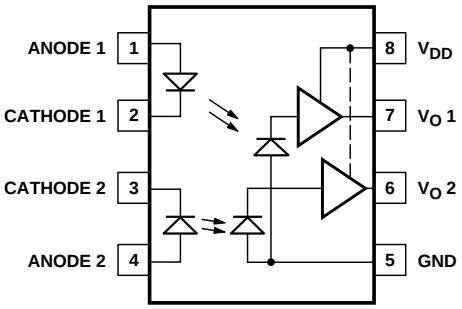
High Speed CMOS Optocoupler

Data Sheet

Description

The HCPL-0738 is a dual-channel 15 MBd CMOS optocoupler in SOIC-8 package. The HCPL-0738 optocoupler utilizes the latest CMOS IC technology to achieve out-standing performance with very low power consumption. Basic building blocks of HCPL-0738 are high speed LEDs and CMOS detector ICs. Avago also offers the same performance in the single channel version, HCPL-0708. Each detector incorporates an integrated photodiode, a high speed transimpedance amplifier, and a voltage comparator with an output driver.

Functional Diagram



Truth Table

LED	V_O, Output
OFF	H
ON	L

Note: A 0.1 µF bypass capacitor must be connected between pins 5 and 8.

Features

- **15 ns typical pulse width distortion**
- **40 ns maximum prop. delay skew**
- **20 ns typical prop. delay**
- **High speed: 15 MBd typical**
- **+ 5 V CMOS compatibility**
- **10 kV / mS minimum common mode rejection**
- **–40 to 100°C temperature range**
- **Safety and regulatory approvals**
  - UL recognized (3750 V rms for 1 minute per UL 1577)
  - CSA component acceptance notice #5.
  - IEC / EN / DIN EN 60747-5-2 approved for HCPL-0738 Option 060

Applications

- **PDP (plasma display panel)**
- **Digital field bus isolation: DeviceNet, SDS, Profibus**
- **Multiplexed data transmission**
- **Computer peripheral interface**
- **Microprocessor system interface**
- **DC / DC converter**

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Selection Guide

Small Outline SO-8
HCPL-0738

Ordering Information

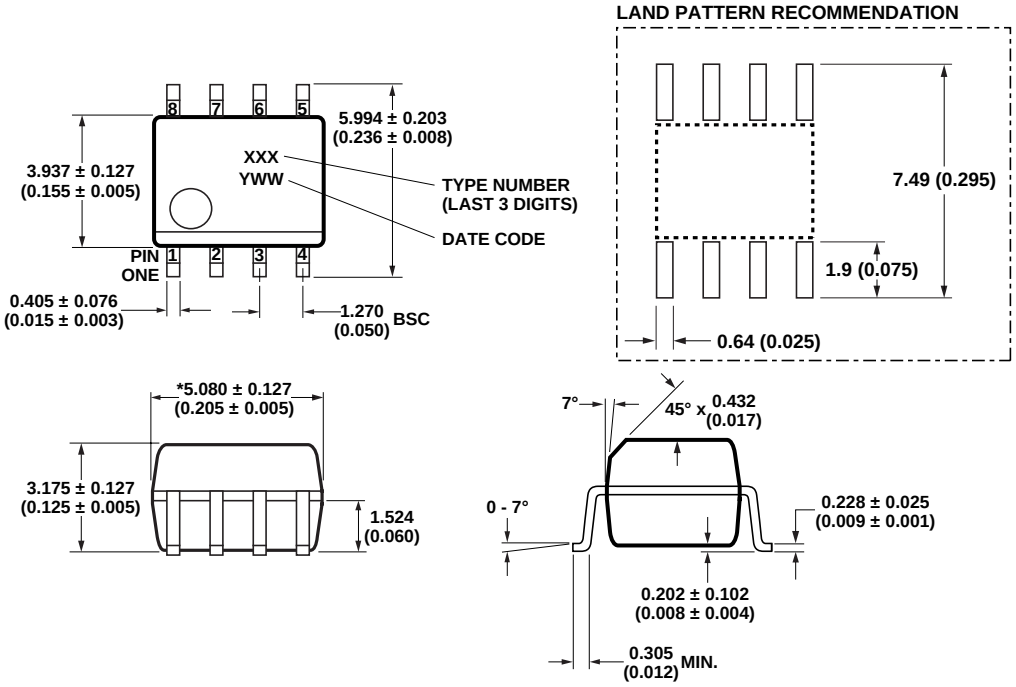
Specify Part Number followed by Option Number (if desired).

Example
HCPL-0738 -060 = IEC/EN/DIN EN 60747-5-2 Option
HCPL-0738 -500 = Tape and Reel Packaging Option
HCPL-0738-XXXE = Lead Free Option

No Option Code contains 100 units per tube. Option 500 contains 1500 units per reel. Option data sheets available. Contact Avago Technologies sales representative or authorized distributor.

Package Outline Drawing

HCPL-0738 Outline Drawing (Small Outline SO-8 Package)

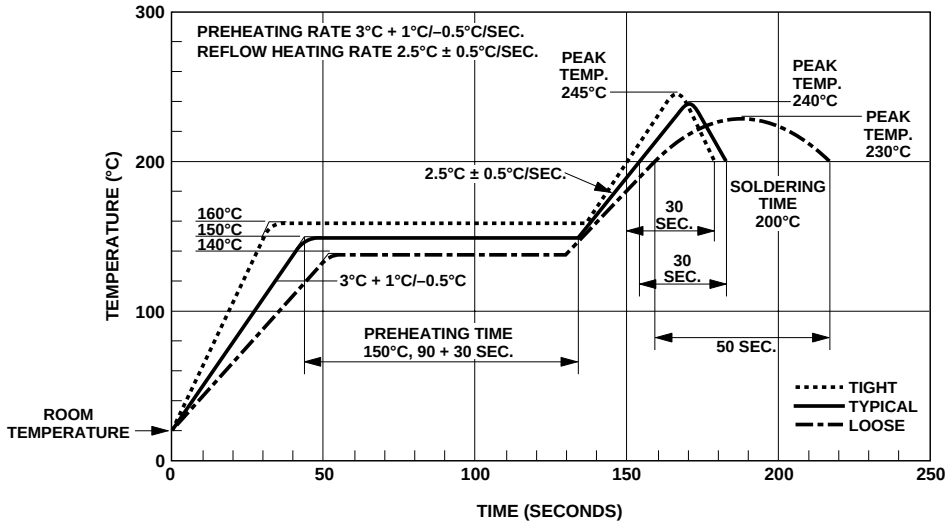


*TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

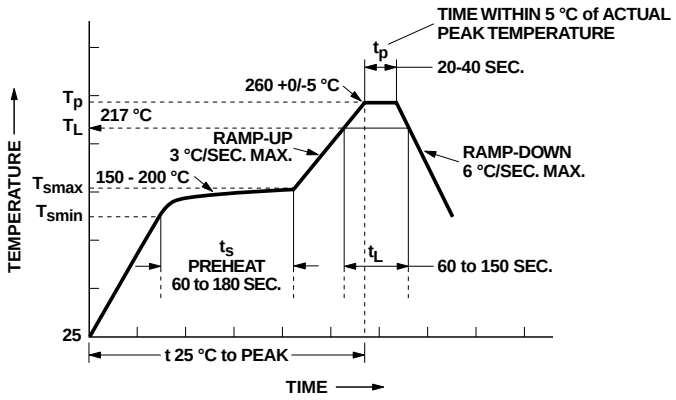
DIMENSIONS IN MILLIMETERS AND (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Solder Reflow Temperature Profile



Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Regulatory Information
The HCPL-0738 has been approved by the following organizations:

UL
Recognized under UL 1577, component recognition program, File E55361.

CSA
Approved under CSA Component Acceptance Notice #5, File CA88324.

IEC / EN / DIN EN 60747-5-2
Approved under:
IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01
(Option 060 only)

Insulation and Safety Related Specifications (approval pending)

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(I01)	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Insulation thickness between emitter and detector; also known as distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	≥ 175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

All Avago data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Storage Temperature	T_S	–55	125	°C
Ambient Operating Temperature	T_A	–40	100	°C
Supply Voltage	V_{DD}	0	6.0	Volts
Output Voltage	V_O	–0.5	V_{DD} + 0.5	Volts
Average Forward Input Current	I_F	—	20	mA
Average Output Current	I_O	—	2	mA
Lead Solder Temperature	260°C for 10 seconds, 1.6 mm below seating plane			
Solder Reflow Temperature Profile	See Solder Reflow Thermal Profile section			

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Ambient Operating Temperature	T_A	–40	100	°C
Supply Voltages	V_{DD}	4.5	5.5	V
Input Current (ON)	I_F	10	16	mA

Electrical Specifications
Over recommended temperature (T_A = –40°C to +100°C) and 4.5 V ≤ V_{DD} ≤ 5.5 V.
All typical specifications are at T_A = 25°C, V_{DD} = +5 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input Forward Voltage	V_F	1.3	1.5	1.8	V	I_F = 12 mA	1	
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA		
Logic High Output Voltage	V_{OH}	4.0	5		V	I_F = 0, I_O = –20 µA		
Logic Low Output Voltage	V_{OL}		0.01	0.1	V	I_F = 12 mA, I_O = 20 µA		
Input Threshold Current	I_{TH}		4.5	8.2	mA	I_{OL} = 20 µA	2	
Logic Low Output Supply Current	I_{DDL}		10	18.0	mA	I_F = 12 mA	4	
Logic High Output Supply Current	I_{DDH}		8	15.0	mA	I_F = 0 mA	3	

Switching Specifications
Over recommended temperature (T_A = –40°C to +100°C) and 4.5 V ≤ V_{DD} ≤ 5.5 V.
All typical specifications are at T_A = 25°C, V_{DD} = +5 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Propagation Delay Time to Logic Low Output	t_{PHL}	20	35	60	ns	I_F = 12 mA, C_L = 15 pF CMOS Signal Levels	5	1
Propagation Delay Time to Logic High Output	t_{PLH}	11	20	60	ns	I_F = 12 mA, C_L = 15 pF CMOS Signal Levels	5	1
Pulse Width	PW	100			ns			
Pulse Width Distortion	|PWD|	0	15	30	ns	I_F = 12 mA, C_L = 15 pF CMOS Signal Levels	5	2
Propagation Delay Skew	t_{PSK}			40	ns	I_F = 12 mA, C_L = 15 pF CMOS Signal Levels		3
Output Rise Time (10% – 90%)	t_R		20		ns	I_F = 0 mA, C_L = 15 pF CMOS Signal Levels		
Output Fall Time (90% – 10%)	t_F		25		ns	I_F = 12 mA, C_L = 15 pF CMOS Signal Levels		
Common Mode Transient Immunity at Logic High Output	|CM_H|	10	15		kV/µS	V_{CM} = 1000 V, T_A = 25°C, I_F = 0 mA		4
Common Mode Transient Immunity at Logic Low Output	|CM_L|	10	15		kV/µS	V_{CM} = 1000 V, T_A = 25°C, I_F = 12 mA		5

Package Characteristics

All typicals at $T_A = 25^\circ C$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Insulation	I_{I-O}			1	μA	45% RH, t = 5 s V_{I-O} = 3 kV DC, $T_A = 25^\circ C$
Input-Output Momentary Withstand Voltage	V_{ISO}	3750			V rms	RH ≤ 50%, t = 1 min., $T_A = 25^\circ C$
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V DC
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, $T_A = 25^\circ C$

Notes:

1. t_{PHL} propagation delay is measured from the 50% level on the rising edge of the input pulse to the 2.5 V level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the falling edge of the input pulse to the 2.5 V level of the rising edge of the V_O signal.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$.
3. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
4. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.
5. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.

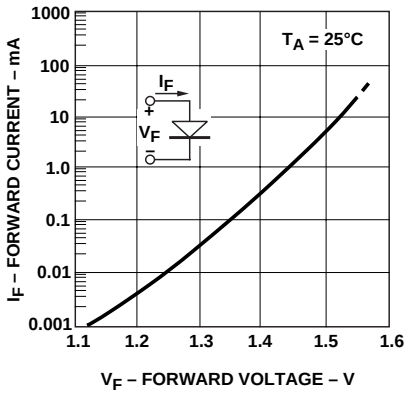


Figure 1. Typical input diode forward characteristic.

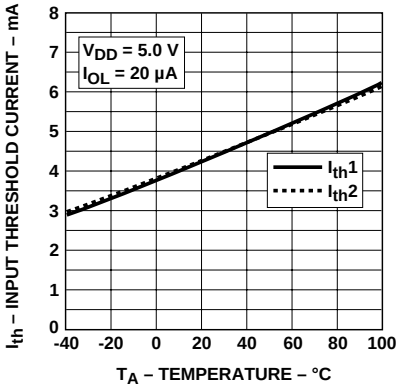


Figure 2. Typical input threshold current vs. temperature.

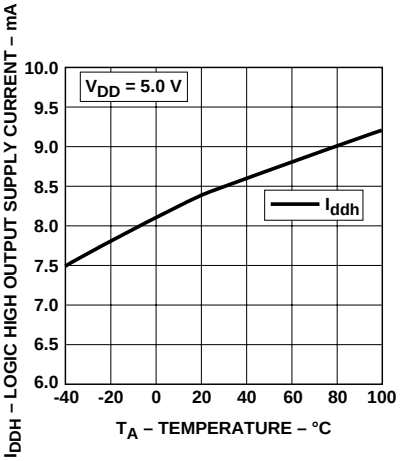


Figure 3. Typical logic high O/P supply current vs. temperature.

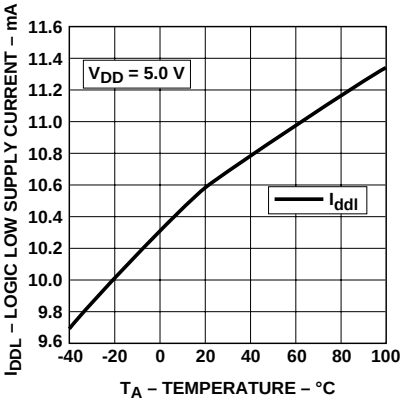


Figure 4. Typical logic low O/P supply current vs. temperature.

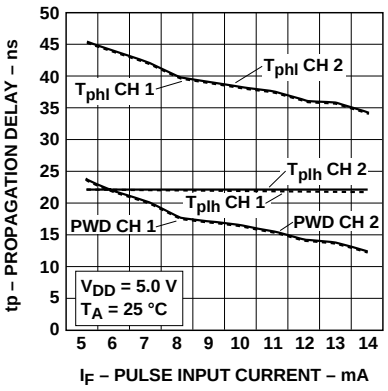


Figure 5. Typical switching speed vs. pulse input current.

Application Information

Bypassing and PC Board Layout

The HCPL-0738 optocoupler is extremely easy to use. No external interface circuitry is required because the HCPL-0738 uses high-speed CMOS IC technology allowing CMOS logic to be connected directly to the inputs and outputs.

As shown in Figure 6, the only external component required for proper operation is the bypass capacitor. Capacitor values should be between 0.01 µF and 0.1 µF. For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm.

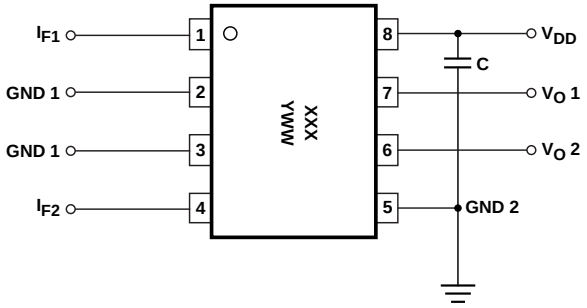


Figure 6. Recommended printed circuit board layout.

Propagation Delay, Pulse-Width Distortion, and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high.

Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 7).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of

the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same supply voltage, output load, and operating temperature). As illustrated in Figure 8, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 8 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 7 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, and power supply ranges.

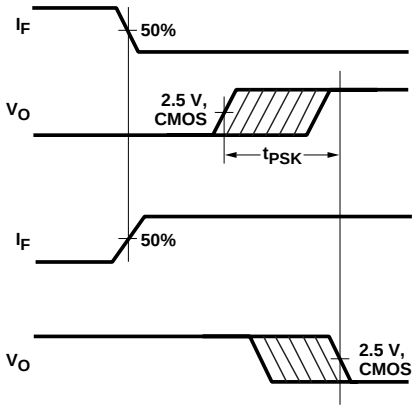


Figure 7. Propagation delay skew waveform.

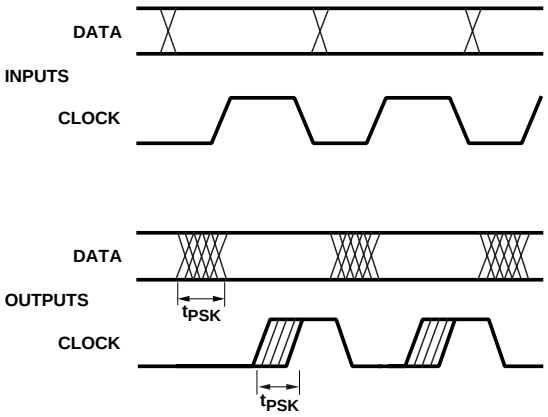


Figure 8. Parallel data transmission example.

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AV01-0032EN February 8, 2006

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