

High CMR, High Speed Optocouplers

Technical Data

HCPL-4504
HCPL-J454
HCPL-0454
HCNW4504

Features

- **Short Propagation Delays for TTL and IPM Applications**
- **15 kV/μs Minimum Common Mode Transient Immunity at $V_{CM} = 1500$ V for TTL/Load Drive**
- **High CTR at $T_A = 25^\circ\text{C}$**
 >25% for HCPL-4504/0454
 >23% for HCNW4504
 >19% for HCPL-J454
- **Electrical Specifications for Common IPM Applications**
- **TTL Compatible**
- **Guaranteed Performance from 0°C to 70°C**
- **Open Collector Output**
- **Safety Approval UL Recognized**
 - 3750 V rms / 1min. for HCPL-4504/0454/J454
 - 5000 V rms / 1min. for HCPL-4504 Option020 and HCNW4504

CSA Approved
IEC/EN/DIN EN 60747-5-2
Approved

- $V_{IORM} = 560$ Vpeak for HCPL-0454 Option060
- $V_{IORM} = 630$ Vpeak for HCPL-4504 Option060

- $V_{IORM} = 891$ Vpeak for HCPL-J454
- $V_{IORM} = 1414$ Vpeak for HCNW4504

Applications

- **Inverter Circuits and Intelligent Power Module (IPM) interfacing** - High Common Mode Transient Immunity (> 10 kV/μs for an IPM load/drive) and ($t_{PLH} - t_{PHL}$) Specified (See Power Inverter Dead Time section)
- **Line Receivers** - Short Propagation Delays and Low Input-Output Capacitance
- **High Speed Logic Ground Isolation - TTL/TTL, TTL/CMOS, TTL/LSTTL**

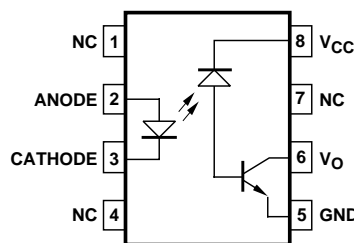
- **Replaces Pulse Transformers** - Save Board Space and Weight
- **Analog Signal Ground Isolation** - Integrated Photodetector Provides Improved Linearity over Phototransistors

Description

The HCPL-4504 and HCPL-0454 contain a GaAsP LED while the HCPL-J454 and HCNW4504 contain an AlGaAs LED. The LED is optically coupled to an integrated high gain photo detector.

The HCPL-4504 series has short propagation delays and high CTR. The HCPL-4504 series also has a guaranteed propagation delay difference ($t_{PLH} - t_{PHL}$). These

Functional Diagram



TRUTH TABLE

| LED | V_O |
|-----|-------|
| ON | LOW |
| OFF | HIGH |

A 0.1 μF bypass capacitor between pins 5 and 8 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

features make the HCPL-4504 series an excellent solution to IPM inverter dead time and other switching problems. The CTR, propagation delay, and CMR are specified both for TTL and IPM conditions which are provided for ease of application. These single channel, diode-transistor optocouplers are available in 8-Pin DIP, SO-8, and Widebody

package configurations. An insulating layer between a LED and an integrated photodetector provide electrical insulation between input and output. Separate connections for the photodiode bias and output-transistor collector increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base collector capacitance.

Selection Guide

| Package Type | Standard 8-Pin DIP (300 Mil) | White Mold 8-Pin DIP (300 Mil) | Small Outline SO8 | Widebody (400 Mil) |
|----------------------------------|--|--------------------------------|--|----------------------------|
| Part Number | HCPL-4504 | HCPL-J454 | HCPL-0454 | HCNW4504 |
| IEC/EN/DIN EN 60747-5-2 Approval | $V_{IORM} = 630 V_{peak}$ (Option 060) | $V_{IORM} = 891 V_{peak}$ | $V_{IORM} = 560 V_{peak}$ (Option 060) | $V_{IORM} = 1414 V_{peak}$ |

Ordering Information

Specify Part number followed by Option Number (if desired)

Example

HCPL-4504 #XXXX

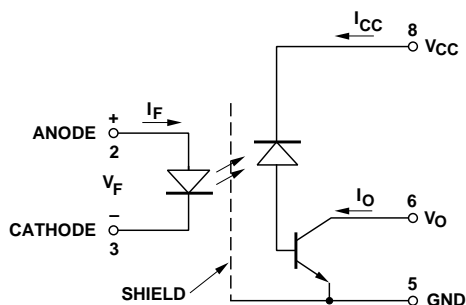
- _____ 020 = UL 5000 Vrms/1minute Option* for HCPL-4504 Only.
- _____ 060 = IEC/EN/DIN EN 60747-5-2 Option* for HCPL-4504/0454.
- _____ 300 = Gull-Wing Lead Option for HCPL-4504/J454, HCNW4504.
- _____ 500 = Tape and Reel Packaging Option.
- _____ XXXE = Lead Free Option

Option data sheets available. Contact Agilent sales representative or authorized distributor for information.

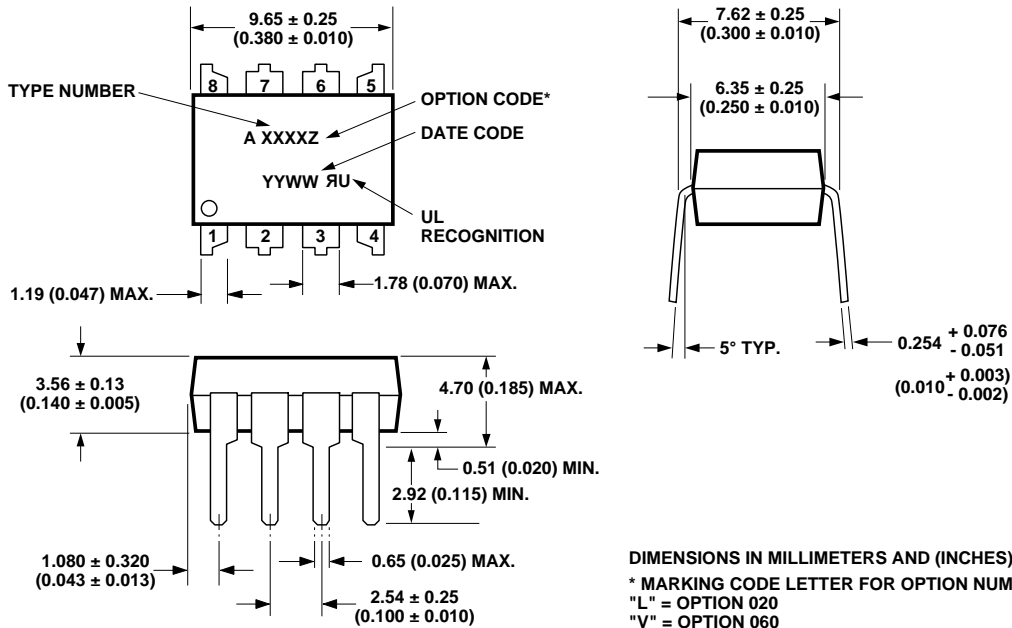
*Combination of Option 020 and Option 060 is not available.

Remarks: The notation “#” is used for existing products, while (new) products launched since 15th July 2001 and lead free option will use “-”

Schematic



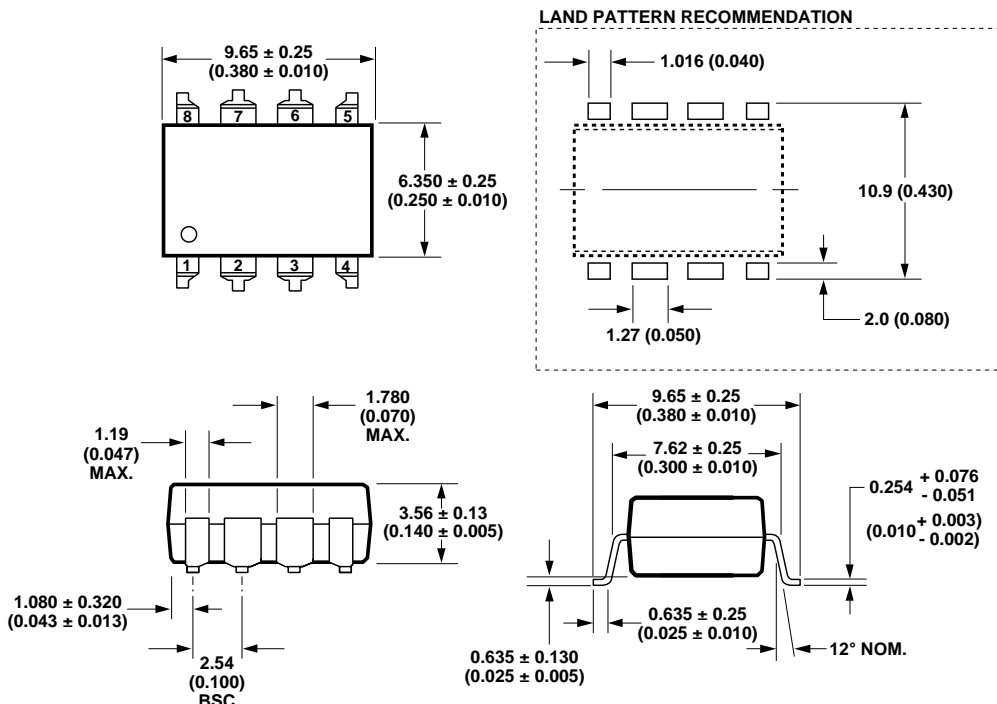
Package Outline Drawings HCPL-4504 Outline Drawing



DIMENSIONS IN MILLIMETERS AND (INCHES).
 * MARKING CODE LETTER FOR OPTION NUMBERS
 "L" = OPTION 020
 "V" = OPTION 060
 OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

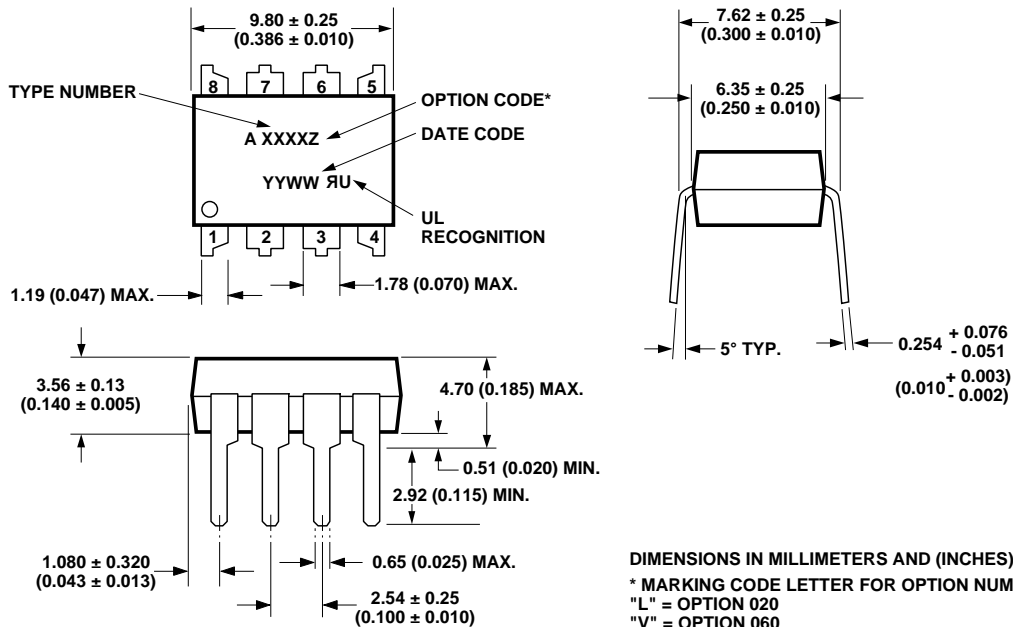
HCPL-4504 Gull Wing Surface Mount Option 300 Outline Drawing



DIMENSIONS IN MILLIMETERS (INCHES).
 LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

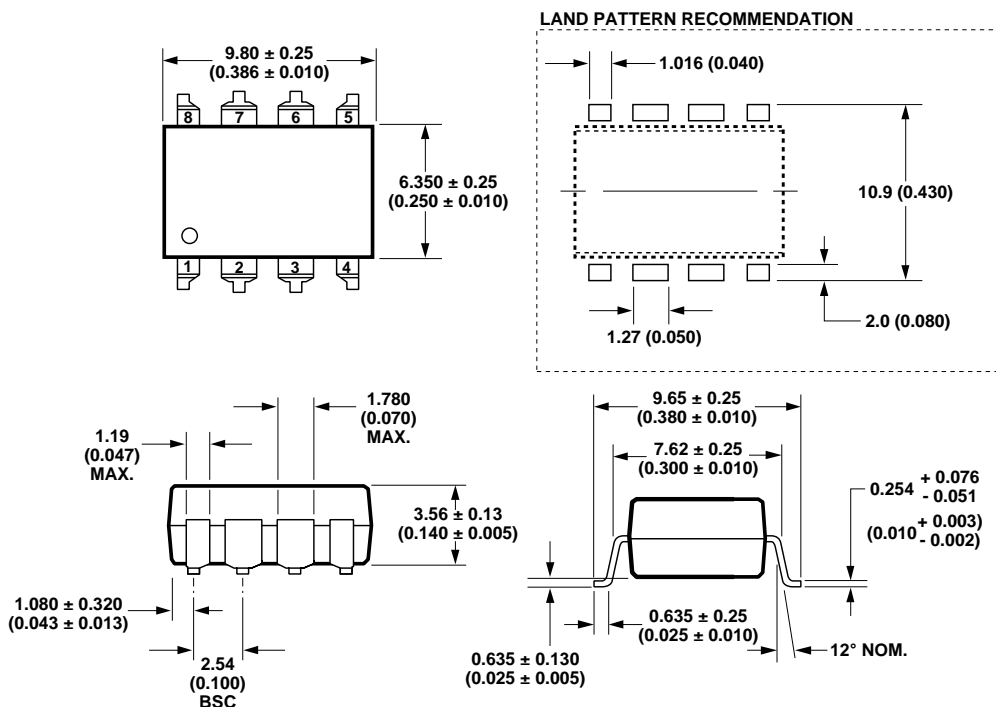
Package Outline Drawings HCPL-J454 Outline Drawing



DIMENSIONS IN MILLIMETERS AND (INCHES).
* MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

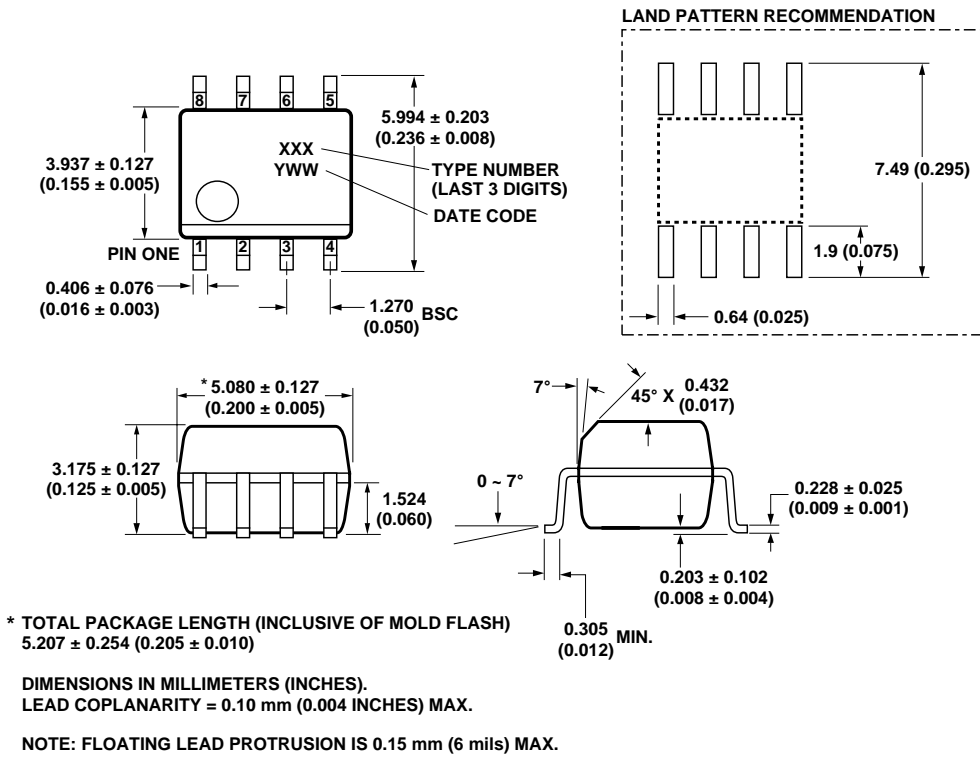
HCPL-J454 Gull Wing Surface Mount Option 300 Outline Drawing



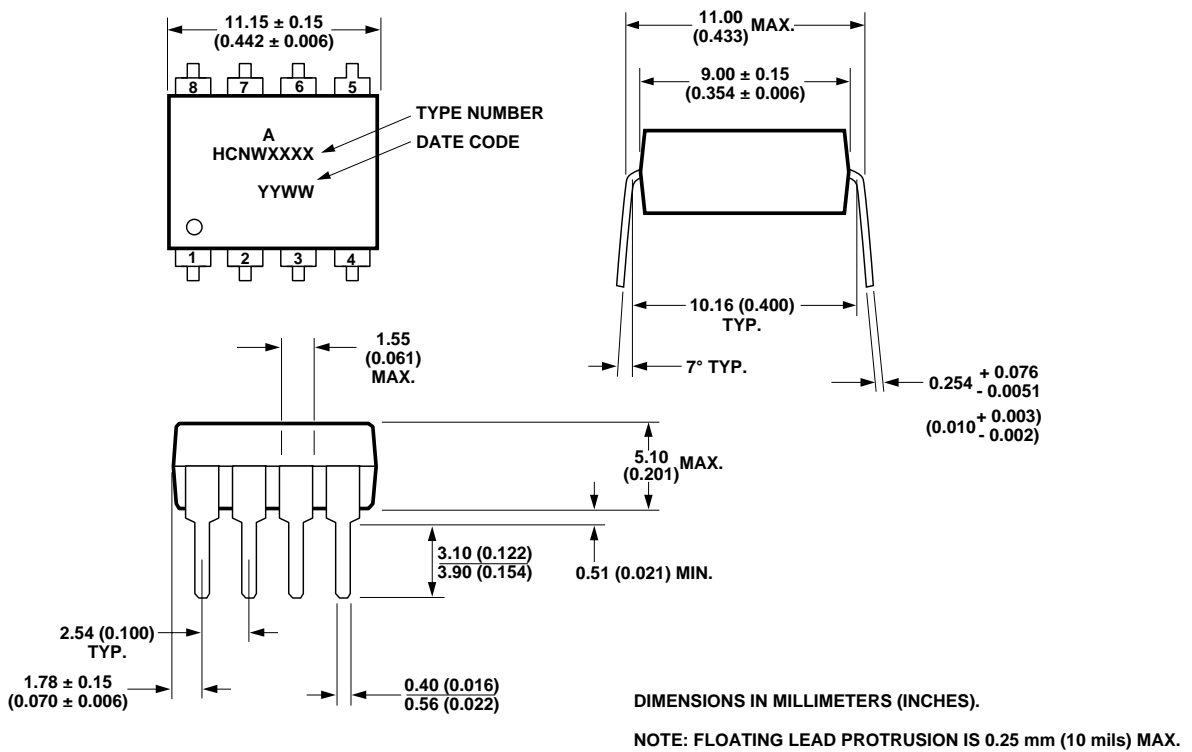
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

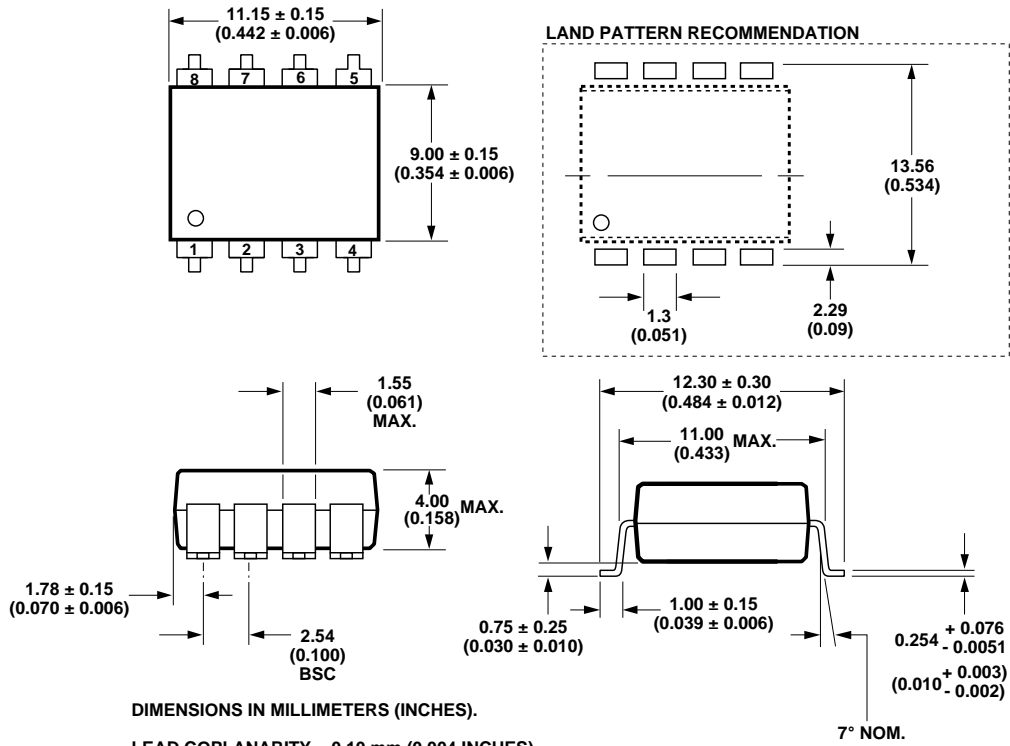
HCPL-0454 Outline Drawing (8-Pin Small Outline Package)



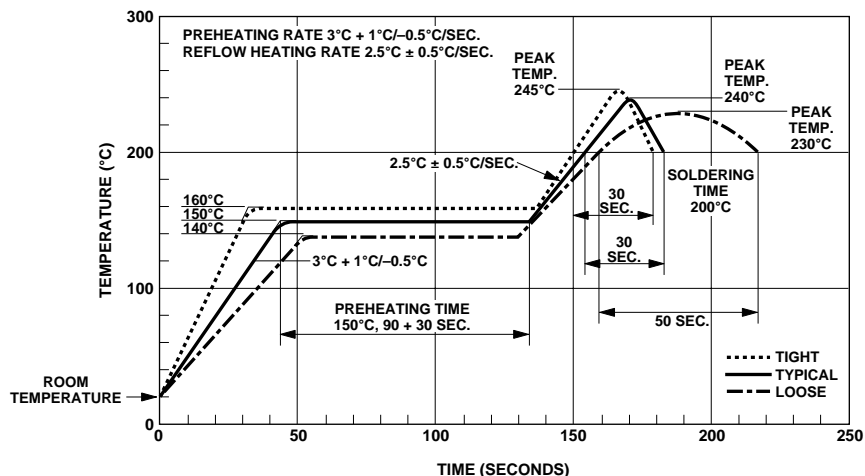
HCNW4504 Outline Drawing (8-Pin Widebody Package)



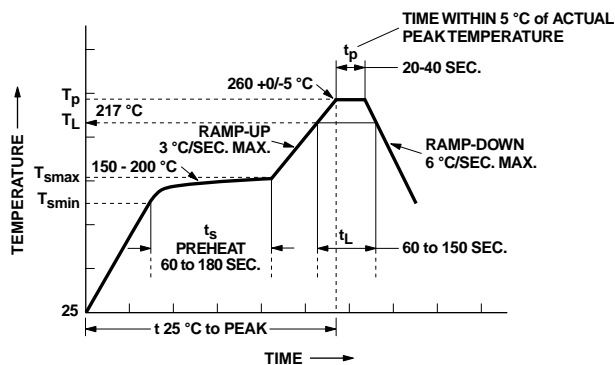
HCNW4504 Gull Wing Surface Mount Option 300 Outline Drawing



Solder Reflow Temperature Profile



Recommended Pb-Free IR Profile



NOTES:
 THE TIME FROM 25°C TO PEAK TEMPERATURE = 8 MINUTES MAX.
 $T_{smax} = 200^{\circ}\text{C}$, $T_{smin} = 150^{\circ}\text{C}$

Regulatory Information

The devices contained in this data sheet have been approved by the following agencies:

| Agency/Standard | HCPL-4504 | HCPL-J454 | HCPL-0456 | HCNW4504 |
|---|-----------|-----------|-----------|----------|
| Underwriters Laboratories (UL) UL1577 Recognized under UL1577, Component Recognition Program, Category FPQU2, File E55361 | ✓ | ✓ | ✓ | ✓ |
| Canadian Standards Association (CSA) Component Acceptance Notice #5 File CA88324 | ✓ | ✓ | ✓ | ✓ |
| IEC/EN/DIN EN 60747-5-2 Approved under: IEC 60747-5-2:1997 + A1:2002 EN 60747-5-2:2001 + A1:2002 DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01 | ✓ | ✓ | | ✓ |

Insulation and Safety Related Specifications

| Parameter | Symbol | Value | | | | Units | Conditions |
|---|--------|-----------|-----------|-----------|----------|-------|--|
| | | HCPL-4504 | HCPL-J454 | HCPL-0454 | HCNW4504 | | |
| Minimum External Air Gap (External Clearance) | L(101) | 7.1 | 7.4 | 4.9 | 9.6 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (External Creepage) | L(102) | 7.4 | 8.0 | 4.8 | 10.0 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | | 0.08 | 0.5 | 0.08 | 1.0 | mm | Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity. |
| Minimum Internal Tracking (Internal Creepage) | | NA | NA | NA | 4.0 | mm | Measured from input terminals to output terminals, along internal cavity. |
| Tracking Resistance (Comparative Tracking Index) | CTI | ≥ 175 | ≥ 175 | ≥ 175 | ≥ 200 | Volts | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | IIIa | IIIa | IIIa | IIIa | | Material Group (DIN VDE 0110, 1/89, Table 1) |

All Agilent data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements.

However, once mounted on a printed circuit board, minimum

creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and

ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics

| Description | Symbol | HCPL-0454 OPTION 060 | HCPL-4504 OPTION 060 | HCPL-J454 | HCNW4504 | Unit |
|--|----------------|-------------------------|-------------------------|--------------------------------|-------------------------------|-------------|
| Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 150 V rms for rated mains voltage ≤ 300 V rms for rated mains voltage ≤ 450 V rms for rated mains voltage ≤ 600 V rms for rated mains voltage ≤ 1000 V rms | | I-IV I-III | I-IV I-IV I-III | I-IV I-IV I-III I-III | I-IV I-IV I-IV I-III | |
| Climatic Classification | | 55/100/21 | 55/100/21 | 55/100/21 | 55/85/21 | |
| Pollution Degree (DIN VDE 0110/1.89) | | 2 | 2 | 2 | 2 | |
| Maximum Working Insulation Voltage | V_{IORM} | 560 | 630 | 891 | 1414 | V_{peak} |
| Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ sec, Partial Discharge < 5 pC | V_{PR} | 1050 | 1181 | 1670 | 2652 | V_{peak} |
| Input to Output Test Voltage, Method a* $V_{IORM} \times 1.5 = V_{PR}$, Type and Sample Test, $t_m = 60$ sec, Partial Discharge < 5 pC | V_{PR} | 840 | 945 | 1336 | 2121 | V_{peak} |
| Highest Allowable Overvoltage* (Transient Overvoltage, $t_{ini} = 10$ sec) | V_{IOTM} | 4000 | 6000 | 6000 | 8000 | V_{peak} |
| Safety Limiting Values - Maximum Values Allowed in the Event of a Failure, also see Thermal Derating curve | | | | | | |
| Case Temperature | T_S | 150 | 175 | 175 | 150 | $^{\circ}C$ |
| Input Current | $I_{S,INPUT}$ | 150 | 230 | 400 | 400 | mA |
| Output Power | $P_{S,OUTPUT}$ | 600 | 600 | 600 | 700 | mW |
| Insulation Resistance at T_S , $V_{IO} = 500$ V | R_S | $\geq 10^9$ | $\geq 10^9$ | $\geq 10^9$ | $\geq 10^9$ | Ω |

*Refer to the optocoupler section of the Designer's Catalog, under regulatory information (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

NOTE: These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

NOTE: Insulation Characteristics are per IEC/EN/DIN EN 60747-5-2.

NOTE: Surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

| Parameter | Symbol | Device | Min. | Max. | Units | Note |
|---|----------------|-------------------------------------|---|------|-------|------|
| Storage Temperature | T_S | | -55 | 125 | °C | |
| Operating Temperature | T_A | HCPL-4504 HCPL-0454 HCPL-J454 | -55 | 100 | °C | |
| | | HCNW4504 | -55 | 85 | | |
| Average Forward Input Current | $I_{F(AVG)}$ | | | 25 | mA | 1 |
| Peak Forward Input Current (50% duty cycle, 1 ms pulse width) | $I_{F(PEAK)}$ | HCPL-4504 HCPL-0454 | | 50 | mA | 2 |
| | | HCPL-J454 HCNW4504 | | 40 | | |
| Peak Transient Input Current ($\leq 1 \mu s$ pulse width, 300 pps) | $I_{F(TRANS)}$ | HCPL-4504 HCPL-0454 | | 1 | A | |
| | | HCPL-J454 HCNW4504 | | 0.1 | | |
| Reverse LED Input Voltage (Pin 3-2) | V_R | HCPL-4504 HCPL-0454 | | 5 | V | |
| | | HCPL-J454 HCNW4504 | | 3 | | |
| Input Power Dissipation | P_{IN} | HCPL-4504 HCPL-0454 | | 45 | mW | 3 |
| | | HCPL-J454 HCNW4504 | | 40 | | |
| Average Output Current (Pin 6) | $I_{O(AVG)}$ | | | 8 | mA | |
| Peak Output Current | $I_{O(PEAK)}$ | | | 16 | mA | |
| Supply Voltage (Pin 8-5) | V_{CC} | | -0.5 | 30 | V | |
| Output Voltage (Pin 6-5) | V_O | | -0.5 | 20 | V | |
| Output Power Dissipation | P_O | | | 100 | mW | 4 |
| Lead Solder Temperature (Through-Hole Parts Only) 1.6 mm below seating plane, 10 seconds Up to seating plane, 10 seconds | T_{LS} | HCPL-4504 HCPL-J454 | | 260 | °C | |
| | | HCNW4504 | | 260 | | |
| Reflow Temperature Profile | T_{RP} | HCPL-0454 and Option 300 | See Package Outline Drawings section | | | |

Electrical Specifications (DC)Over recommended temperature ($T_A = 0^\circ\text{C}$ to 70°C) unless otherwise specified. See note 12.

| Parameter | Symbol | Device | Min. | Typ.* | Max. | Units | Test Conditions | | Fig. | Note | | | |
|--|---------------------------------|-----------|------|-------|--------------------------|----------------------------|---|---|---|------------|----|--------------------------------|--|
| Current Transfer Ratio | CTR | HCPL-4504 | 25 | 32 | 60 | % | $T_A = 25^\circ\text{C}$ | $V_O = 0.4\text{ V}$ | $I_F = 16\text{ mA}$, $V_{CC} = 4.5\text{ V}$ | 1, 2, 4 | 5 | | |
| | | HCPL-0454 | 21 | 34 | | | | $V_O = 0.5\text{ V}$ | | | | | |
| | | HCPL-J454 | 19 | 37 | 60 | | $T_A = 25^\circ\text{C}$ | $V_O = 0.4\text{ V}$ | | | | | |
| | | | 13 | 39 | | | | $V_O = 0.5\text{ V}$ | | | | | |
| | | HCNW4504 | 23 | 29 | 60 | | $T_A = 25^\circ\text{C}$ | $V_O = 0.4\text{ V}$ | | | | | |
| | | 19 | 31 | 63 | | $V_O = 0.5\text{ V}$ | | | | | | | |
| | CTR | HCPL-4504 | 26 | 35 | 65 | % | $T_A = 25^\circ\text{C}$ | $V_O = 0.4\text{ V}$ | $I_F = 12\text{ mA}$, $V_{CC} = 4.5\text{ V}$ | 1, 2, 4 | 5 | | |
| | | HCPL-0454 | 22 | 37 | | | | $V_O = 0.5\text{ V}$ | | | | | |
| | | HCPL-J454 | 21 | 43 | 65 | | $T_A = 25^\circ\text{C}$ | $V_O = 0.4\text{ V}$ | | | | | |
| | | | 16 | 45 | | | | $V_O = 0.5\text{ V}$ | | | | | |
| HCNW4504 | | 25 | 33 | 65 | $T_A = 25^\circ\text{C}$ | | $V_O = 0.4\text{ V}$ | | | | | | |
| | 21 | 35 | 68 | | $V_O = 0.5\text{ V}$ | | | | | | | | |
| Logic Low Output Voltage | V_{OL} | HCPL-4504 | | 0.2 | 0.4 | V | $T_A = 25^\circ\text{C}$ | $I_O = 4.0\text{ mA}$ | $I_F = 16\text{ mA}$, $V_{CC} = 4.5\text{ V}$ | | | | |
| | | HCPL-0454 | | 0.5 | | | | $I_O = 3.3\text{ mA}$ | | | | | |
| | | HCPL-J454 | | 0.2 | 0.4 | | $T_A = 25^\circ\text{C}$ | $I_O = 3.6\text{ mA}$ | | | | | |
| | | | | | 0.5 | | | $I_O = 3.0\text{ mA}$ | | | | | |
| | | HCNW4504 | | 0.2 | 0.4 | | $T_A = 25^\circ\text{C}$ | $I_O = 3.6\text{ mA}$ | | | | | |
| | | | | | 0.5 | | | $I_O = 3.0\text{ mA}$ | | | | | |
| Logic High Output Current | I_{OH} | | | 0.003 | 0.5 | μA | $T_A = 25^\circ\text{C}$ | $V_O = V_{CC} = 5.5\text{ V}$ | $I_F = 0\text{ mA}$ | 5 | | | |
| | | | | 0.01 | 1 | | $T_A = 25^\circ\text{C}$ | $V_O = V_{CC} = 15\text{ V}$ | | | | | |
| | | | | | 50 | | | | | | | | |
| | | | | | | | | | | | | | |
| Logic Low Supply Current | I_{CCL} | HCPL-4504 | | 50 | 200 | μA | $I_F = 16\text{ mA}$, $V_O = \text{Open}$, $V_{CC} = 15\text{ V}$ | | | | 12 | | |
| | | HCPL-0454 | | | | | | | | | | | |
| | | HCNW4504 | | | | | | | | | | | |
| | | HCPL-J454 | | 70 | | | | | | | | | |
| Logic High Supply Current | I_{CCH} | | | 0.02 | 1 | μA | $T_A = 25^\circ\text{C}$ | $I_F = 0\text{ mA}$, $V_O = \text{Open}$, $V_{CC} = 15\text{ V}$ | | | 12 | | |
| | | | | | 2 | | | | | | | | |
| Input Forward Voltage | V_F | HCPL-4504 | | 1.5 | 1.7 | V | $T_A = 25^\circ\text{C}$ | $I_F = 16\text{ mA}$ | 3 | | | | |
| | | HCPL-0454 | | | 1.8 | | | | | | | | |
| | | HCPL-J454 | | 1.45 | 1.59 | | 1.85 | | | | | $T_A = 25^\circ\text{C}$ | |
| | | | | 1.35 | | | 1.95 | | | | | | |
| Input Reverse Breakdown Voltage | BV_R | HCPL-4504 | | 5 | | V | $I_R = 10\text{ }\mu\text{A}$ | | | | | | |
| | | HCPL-0454 | | | | | | | | | | | |
| | | HCPL-J454 | | 3 | | | | | | | | $I_R = 100\text{ }\mu\text{A}$ | |
| | | HCNW4504 | | | | | | | | | | | |
| Temperature Coefficient of Forward Voltage | $\frac{\Delta V_F}{\Delta T_A}$ | HCPL-4504 | | -1.6 | | $\text{mV}/^\circ\text{C}$ | $I_F = 16\text{ mA}$ | | | | | | |
| | | HCPL-0454 | | | | | | | | | | | |
| | | HCPL-J454 | | -1.4 | | | | | | | | | |
| | | HCNW4504 | | | | | | | | | | | |
| Input Capacitance | C_{IN} | HCPL-4504 | | 60 | | pF | $f = 1\text{ MHz}$, $V_F = 0\text{ V}$ | | | | | | |
| | | HCPL-0454 | | | | | | | | | | | |
| | | HCPL-J454 | | 70 | | | | | | | | | |
| | | HCNW4504 | | | | | | | | | | | |

*All typicals at $T_A = 25^\circ\text{C}$.

AC Switching Specifications

Over recommended temperature ($T_A = 0^\circ\text{C}$ to 70°C) unless otherwise specified.

| Parameter | Symbol | Device | Min. | Typ. | Max. | Units | Test Conditions | Fig. | Note | |
|---|-------------------|-----------|------|------|------|-------------------------|--|--|-------------|-------|
| Propagation Delay Time to Logic Low at Output | t_{PHL} | | | 0.2 | 0.3 | μs | $T_A = 25^\circ\text{C}$ | Pulse: $f = 20\text{ kHz}$, Duty Cycle = 10%, $I_F = 16\text{ mA}$, $V_{CC} = 5.0\text{ V}$, $R_L = 1.9\text{ k}\Omega$, $C_L = 15\text{ pF}$, $V_{THHL} = 1.5\text{ V}$ | 6, 8, 9 | 9 |
| | | | | | 0.5 | | | | | |
| | | HCPL-J454 | 0.05 | 0.5 | 1.0 | | $T_A = 25^\circ\text{C}$ | Pulse: $f = 10\text{ kHz}$, Duty Cycle = 50%, $I_F = 12\text{ mA}$, $V_{CC} = 15.0\text{ V}$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{THHL} = 1.5\text{ V}$ | 6, 10-14 | 10 |
| | | Others | 0.1 | | | | | | | |
| Propagation Delay Time to Logic High at Output | t_{PLH} | | | 0.3 | 0.5 | μs | $T_A = 25^\circ\text{C}$ | Pulse: $f = 20\text{ kHz}$, Duty Cycle = 10%, $I_F = 16\text{ mA}$, $V_{CC} = 5.0\text{ V}$, $R_L = 1.9\text{ k}\Omega$, $C_L = 15\text{ pF}$, $V_{THLH} = 1.5\text{ V}$ | 6, 8, 9 | 9 |
| | | | | | 0.7 | | | | | |
| | | | 0.3 | 0.8 | 1.1 | μs | $T_A = 25^\circ\text{C}$ | Pulse: $f = 10\text{ kHz}$, Duty Cycle = 50%, $I_F = 12\text{ mA}$, $V_{CC} = 15.0\text{ V}$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{THLH} = 2.0\text{ V}$ | 6, 10-14 | 10 |
| | | 0.2 | | 1.4 | | | | | | |
| Propagation Delay Difference Between Any 2 Parts | $t_{PLH}-t_{PHL}$ | | -0.4 | 0.3 | 0.9 | μs | $T_A = 25^\circ\text{C}$ | Pulse: $f = 10\text{ kHz}$, Duty Cycle = 50%, $I_F = 12\text{ mA}$, $V_{CC} = 15.0\text{ V}$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{THHL} = 1.5\text{ V}$, $V_{THLH} = 2.0\text{ V}$ | 6, 10-14 | 17 |
| | | | -0.7 | | 1.3 | | | | | |
| Common Mode Transient Immunity at Logic High Level Output | $ CM_H $ | | 15 | 30 | | $\text{kV}/\mu\text{s}$ | $T_A = 25^\circ\text{C}$ $V_{CM} = 1500\text{ V}_{P-P}$ | $V_{CC} = 5.0\text{ V}$, $R_L = 1.9\text{ k}\Omega$, $C_L = 15\text{ pF}$, $I_F = 0\text{ mA}$ | 7 | 7, 9 |
| | $ CM_H $ | | 15 | 30 | | $\text{kV}/\mu\text{s}$ | | $V_{CC} = 15.0\text{ V}$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$, $I_F = 0\text{ mA}$ | 7 | 8, 10 |
| Common Mode Transient Immunity at Logic Low Level Output | $ CM_L $ | | 15 | 30 | | $\text{kV}/\mu\text{s}$ | $T_A = 25^\circ\text{C}$ $V_{CM} = 1500\text{ V}_{P-P}$ | $V_{CC} = 5.0\text{ V}$, $R_L = 1.9\text{ k}\Omega$, $C_L = 15\text{ pF}$, $I_F = 16\text{ mA}$ | 7 | 7, 9 |
| | $ CM_L $ | HCPL-J454 | 15 | 30 | | $\text{kV}/\mu\text{s}$ | | $V_{CC} = 15.0\text{ V}$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$, $I_F = 12\text{ mA}$ | 7 | 8, 10 |
| | $ CM_L $ | Others | 10 | | | | | $V_{CC} = 15.0\text{ V}$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$, $I_F = 16\text{ mA}$ | 7 | 8, 10 |
| | $ CM_L $ | | 15 | 30 | | $\text{kV}/\mu\text{s}$ | | $V_{CC} = 15.0\text{ V}$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$, $I_F = 16\text{ mA}$ | 7 | 8, 10 |

*All typicals at $T_A = 25^\circ\text{C}$.

Package Characteristics

Over recommended temperature ($T_A = 0^\circ\text{C}$ to 25°C) unless otherwise specified.

| Parameter | Sym. | Device | Min. | Typ.* | Max. | Units | Test Conditions | Fig. | Note | |
|---|-----------|-------------------------|-----------|-----------|------|----------|--|------|--------------|--------------------------|
| Input-Output Momentary Withstand Voltage† | V_{ISO} | HCPL-4504 | 3750 | | | V rms | RH ≤ 50%, t = 1 min., $T_A = 25^\circ\text{C}$ | | 6, 13, 16 | |
| | | HCPL-0454 | | | | | | | 6, 14, 16 | |
| | | HCPL-J454 | 3750 | | | | | | 6, 11, 15 | |
| | | HCPL-4504 Option 020 | 5000 | | | | | | 6, 15, 16 | |
| Input-Output Resistance | R_{I-O} | HCPL-4504 | | 10^{12} | | Ω | $V_{I-O} = 500\text{ Vdc}$ | | 6 | |
| | | HCPL-0454 | | | | | | | | |
| | | HCPL-J454 | | | | | | | | |
| | | HCNW4504 | 10^{12} | 10^{13} | | | | | | $T_A = 25^\circ\text{C}$ |
| | | | 10^{11} | | | | $T_A = 100^\circ\text{C}$ | | | |
| Capacitance (Input-Output) | C_{I-O} | HCPL-4504 | | 0.6 | | pF | f = 1 MHz | | 6 | |
| | | HCPL-0454 | | | | | | | | |
| | | HCPL-J454 | | 0.8 | | | | | | |
| | | HCNW4504 | | 0.5 | 0.6 | | | | | |

*All typicals at $T_A = 25^\circ\text{C}$.

†The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics Table (if applicable), your equipment level safety specification or Agilent Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

- Derate linearly above 70°C free-air temperature at a rate of $0.8\text{ mA}/^\circ\text{C}$ (8-Pin DIP).
Derate linearly above 85°C free-air temperature at a rate of $0.5\text{ mA}/^\circ\text{C}$ (SO-8).
- Derate linearly above 70°C free-air temperature at a rate of $1.6\text{ mA}/^\circ\text{C}$ (8-Pin DIP).
Derate linearly above 85°C free-air temperature at a rate of $1.0\text{ mA}/^\circ\text{C}$ (SO-8).
- Derate linearly above 70°C free-air temperature at a rate of $0.9\text{ mW}/^\circ\text{C}$ (8-Pin DIP).
Derate linearly above 85°C free-air temperature at a rate of $1.1\text{ mW}/^\circ\text{C}$ (SO-8).
- Derate linearly above 70°C free-air temperature at a rate of $2.0\text{ mW}/^\circ\text{C}$ (8-Pin DIP).
Derate linearly above 85°C free-air temperature at a rate of $2.3\text{ mW}/^\circ\text{C}$ (SO-8).
- CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F , times 100.
- Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
- Under TTL load and drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM} , to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0\text{ V}$). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8\text{ V}$).
- Under IPM (Intelligent Power Module) load and LED drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM} , to assure that the output will remain in a Logic High state (i.e., $V_O > 3.0\text{ V}$). Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a Logic Low state (i.e., $V_O < 1.0\text{ V}$).
- The $1.9\text{ k}\Omega$ load represents 1 TTL unit load of 1.6 mA and the $5.6\text{ k}\Omega$ pull-up resistor.
- The $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$ load represents an IPM (Intelligent Power Module) load.
- See Option 020 data sheet for more information.
- Use of a $0.1\text{ }\mu\text{F}$ bypass capacitor connected between Pins 5 and 8 is recommended.
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 4500\text{ V rms}$ for 1 second (leakage detection current limit, $I_{i-o} \leq 5\text{ }\mu\text{A}$).
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 4500\text{ V rms}$ for 1 second (leakage detection current limit, $I_{i-o} \leq 5\text{ }\mu\text{A}$).
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 6000\text{ V rms}$ for 1 second (leakage detection current limit, $I_{i-o} \leq 5\text{ }\mu\text{A}$).
- This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.
- The difference between t_{PLH} and t_{PHL} between any two devices (same part number) under the same test condition. (See Power Inverter Dead Time and Propagation Delay Specifications section.)

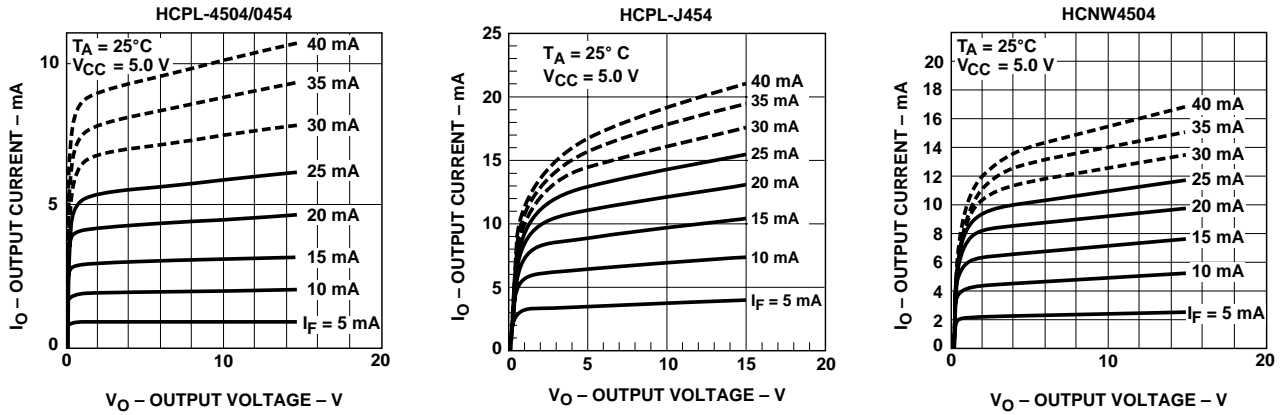


Figure 1. DC and Pulsed Transfer Characteristics.

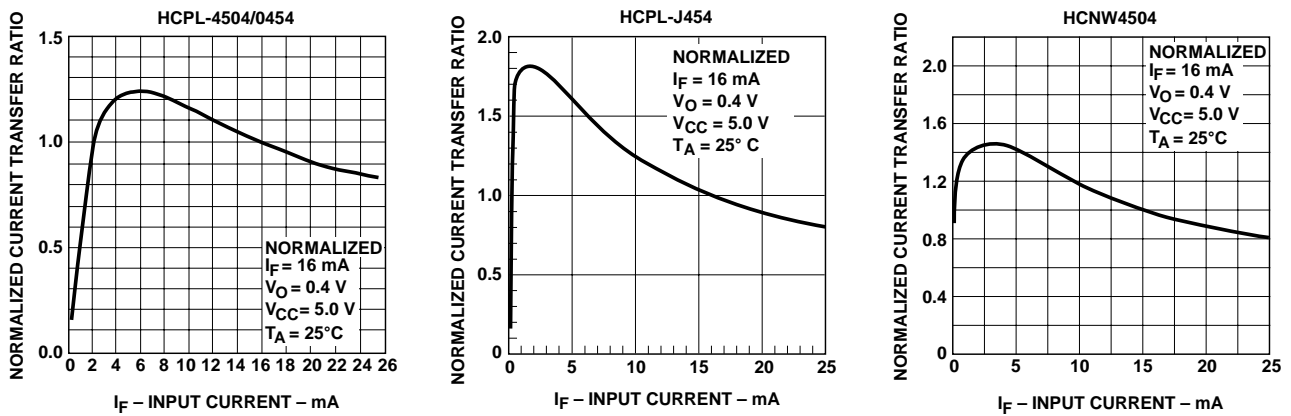


Figure 2. Current Transfer Ratio vs. Input Current.

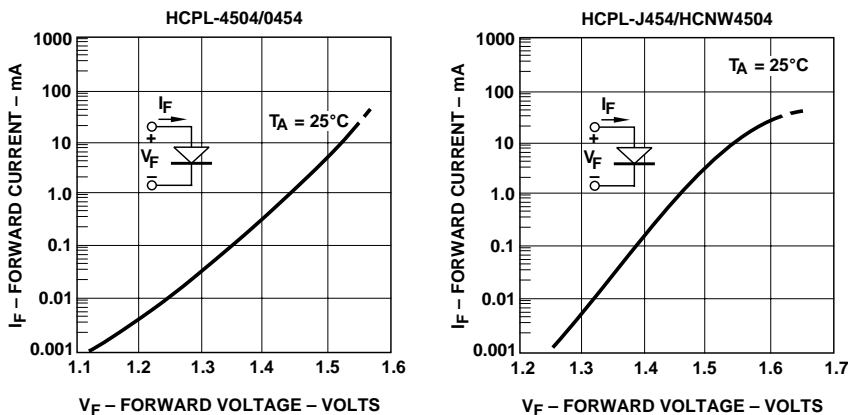


Figure 3. Input Current vs. Forward Voltage.

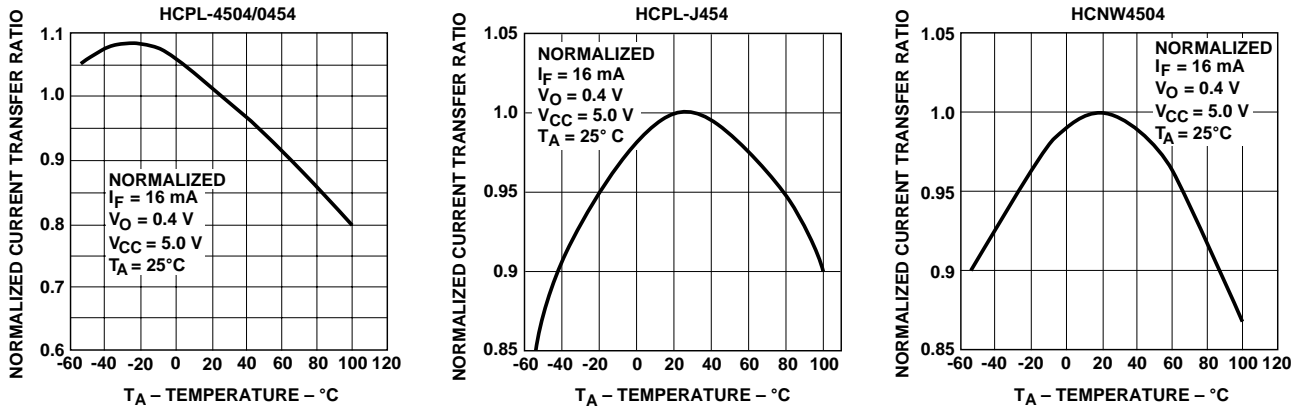


Figure 4. Current Transfer Ratio vs. Temperature.

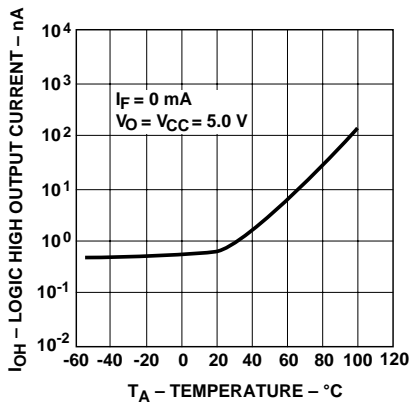


Figure 5. Logic High Output Current vs. Temperature.

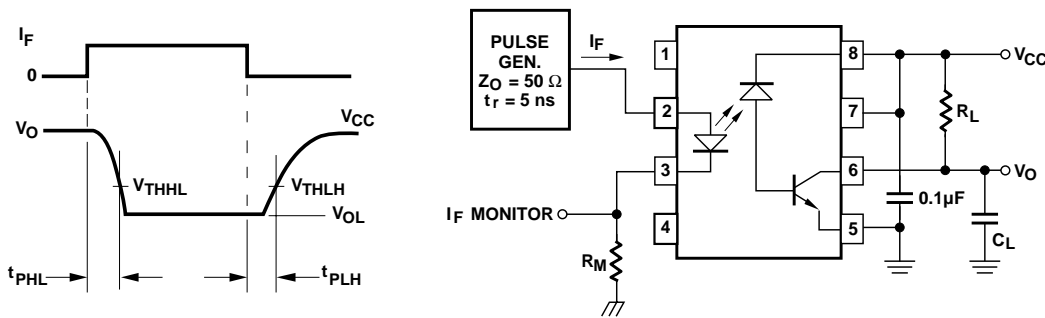


Figure 6. Switching Test Circuit.

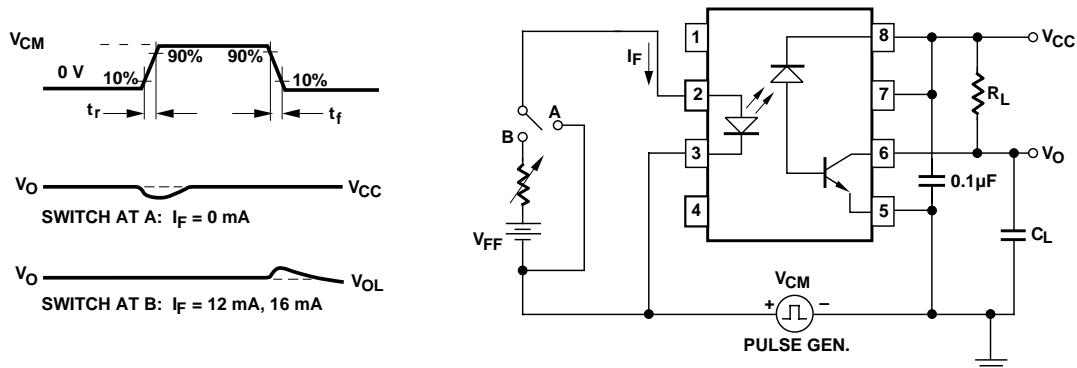


Figure 7. Test Circuit for Transient Immunity and Typical Waveforms.

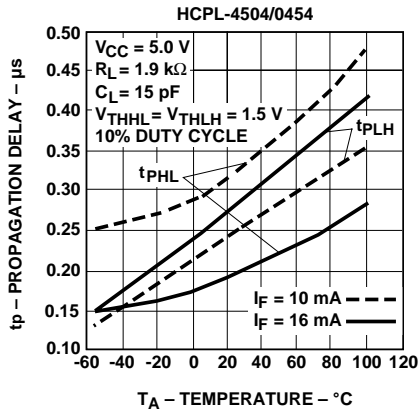


Figure 8. Propagation Delay Time vs. Temperature.

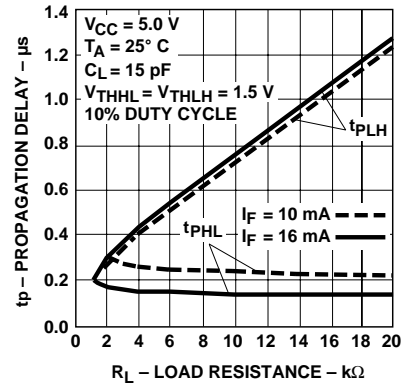
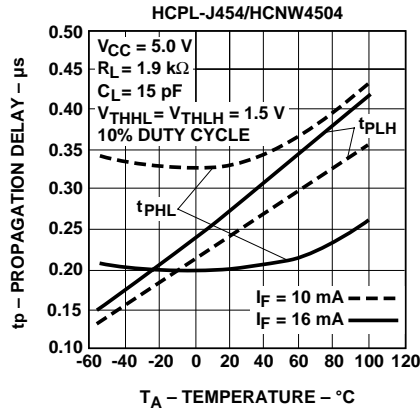


Figure 9. Propagation Delay Time vs. Load Resistance.

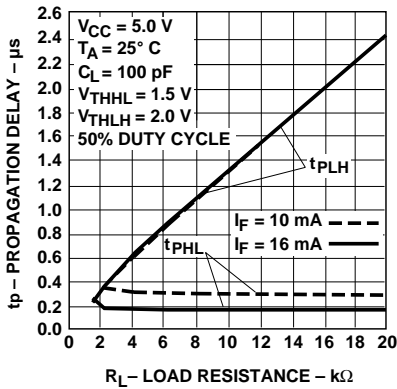


Figure 10. Propagation Delay Time vs. Load Resistance.

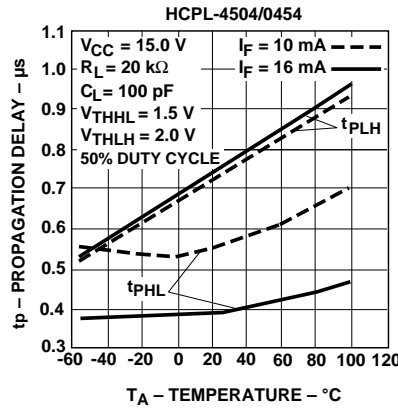
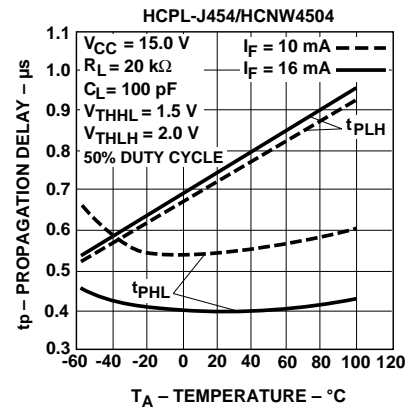


Figure 11. Propagation Delay Time vs. Temperature.



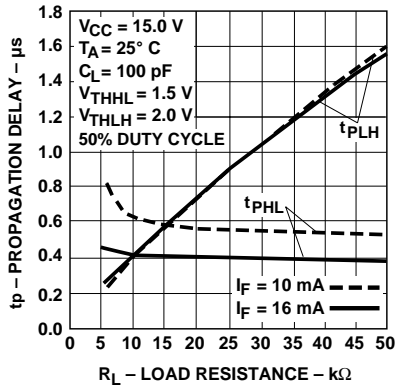


Figure 12. Propagation Delay Time vs. Load Resistance.

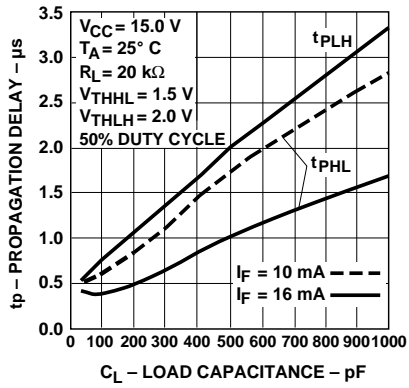


Figure 13. Propagation Delay Time vs. Load Capacitance.

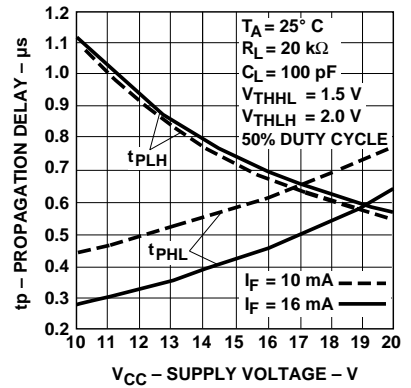


Figure 14. Propagation Delay Time vs. Supply Voltage.

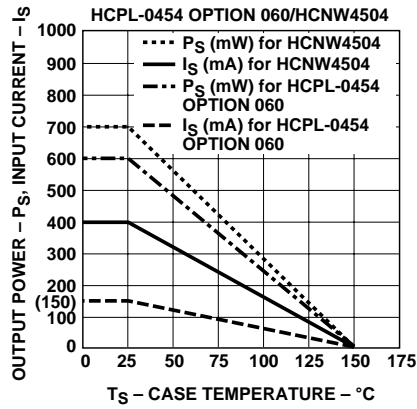
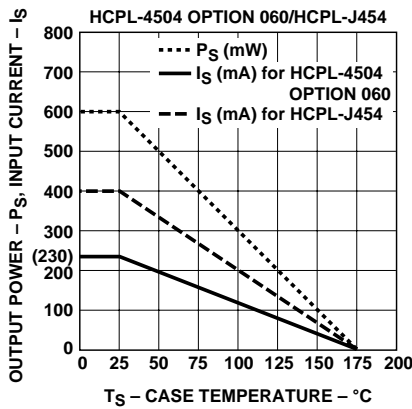


Figure 15. Thermal Derating Curve, Dependence of Safety Limiting Valve with Case Temperature per IEC/EN/DIN EN 60747-5-2.

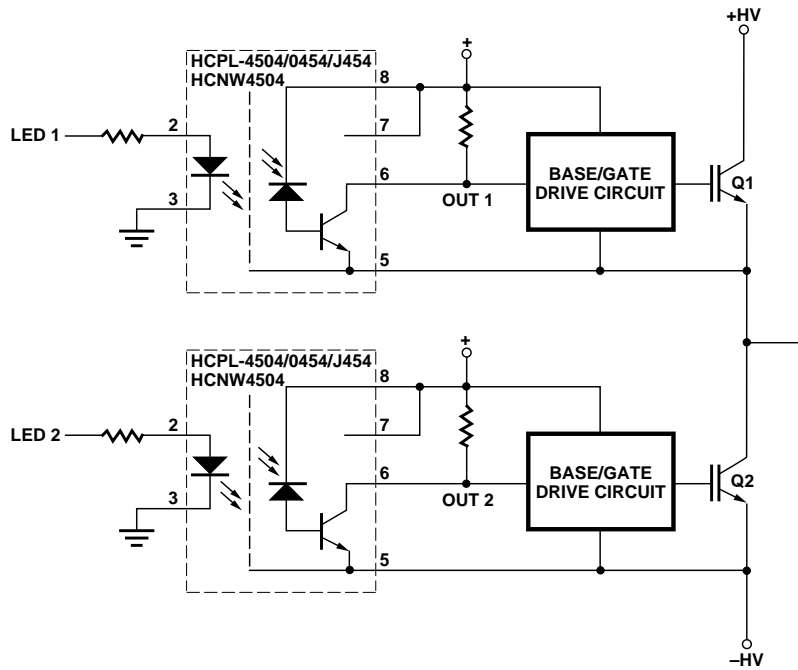


Figure 16. Typical Power Inverter.

Power Inverter Dead Time and Propagation Delay Specifications

The HCPL-4504/0454/J454 and HCNW4504 include a specification intended to help designers minimize “dead time” in their power inverter designs. The new “propagation delay difference” specification ($t_{PLH} - t_{PHL}$) is useful for determining not only how much optocoupler switching delay is needed to prevent “shoot-through” current, but also for determining the best achievable worst-case dead time for a given design.

When inverter power transistors switch (Q1 and Q2 in Figure 17), it is essential that they never conduct at the same time. Extremely large currents will flow if there is any overlap in their conduction during switching transitions, potentially damaging the transistors and even the surrounding circuitry. This “shoot-through” current is eliminated by delaying the turn-on of one transistor (Q2) long enough to ensure that the opposing transistor (Q1) has completely turned off. This delay introduces a small amount of “dead time” at the output of the inverter during which both transistors are off during switching transitions. Minimizing this dead time is an important design goal for an inverter designer.

The amount of turn-on delay needed depends on the propagation delay characteristics of the optocoupler, as well as the characteristics of the transistor base/gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the base/gate drive circuit can be analyzed in the

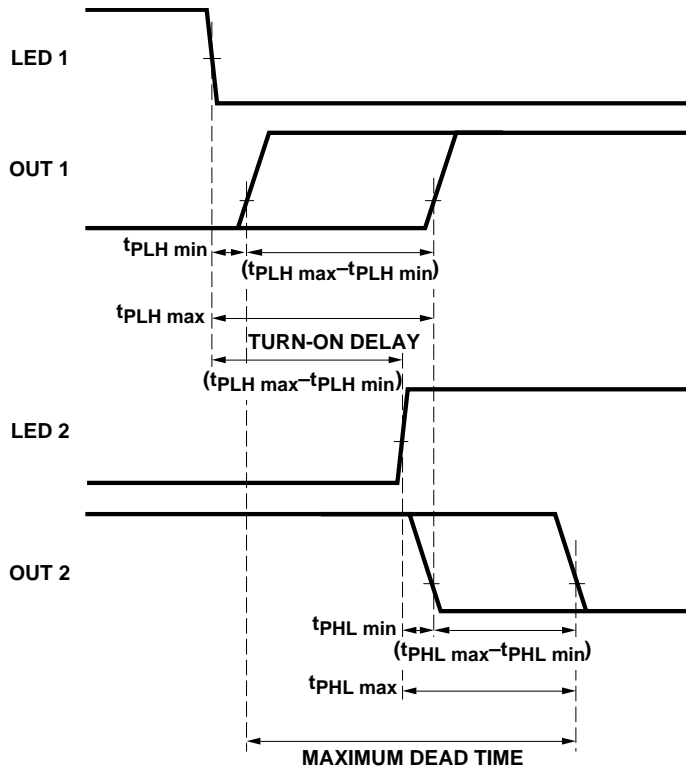


Figure 17. LED Delay and Dead Time Diagram.

same way), it is important to know the minimum and maximum turn-on (t_{PHL}) and turnoff (t_{PLH}) propagation delay specifications, preferably over the desired operating temperature range. The importance of these specifications is illustrated in Figure 17. The waveforms labeled “LED1”, “LED2”, “OUT1”, and “OUT2” are the input and output voltages of the optocoupler circuits driving Q1 and Q2 respectively. Most inverters are designed such that the power transistor turns on when the optocoupler LED turns on; this ensures that both power transistors will be off in the event of a power loss in the control circuit. Inverters can also be designed such that the power transistor turns off when the optocoupler LED turns on; this type of design, however, requires additional fail-safe circuitry to turn off the power transistor if an over-current condition is detected. The timing illustrated in Figure 17 assumes that the power transistor turns on when the optocoupler LED turns on.

The LED signal to turn on Q2 should be delayed enough so that an optocoupler with the very fastest turn-on propagation delay (t_{PHLmin}) will never turn on before an optocoupler with the very slowest turn-off propagation delay (t_{PLHmax}) turns off. To ensure this, the turn-on of the optocoupler should be delayed by an amount no less than ($t_{PLHmax} - t_{PHLmin}$), which also happens to be the

maximum data sheet value for the propagation delay difference specification, ($t_{PLH} - t_{PHL}$). The HCPL-4504/0454/J454 and HCNW4504 specify a maximum ($t_{PLH} - t_{PHL}$) of 1.3 μ s over an operating temperature range of 0-70°C.

Although ($t_{PLH} - t_{PHL}$)_{max} tells the designer how much delay is needed to prevent shoot-through current, it is insufficient to tell the designer how much dead time a design will have. Assuming that the optocoupler turn-on delay is exactly equal to ($t_{PLH} - t_{PHL}$)_{max}, the minimum dead time is zero (i.e., there is zero time between the turnoff of the very slowest optocoupler and the turn-on of the very fastest optocoupler).

Calculating the maximum dead time is slightly more complicated. Assuming that the LED turn-on delay is still exactly equal to ($t_{PLH} - t_{PHL}$)_{max}, it can be seen in Figure 17 that the maximum dead time is the sum of the maximum difference in turn-on delay plus the maximum difference in turnoff delay,

$$[(t_{PLHmax} - t_{PLHmin}) + (t_{PHLmax} - t_{PHLmin})].$$

This expression can be rearranged to obtain

$$[(t_{PLHmax} - t_{PHLmin}) - (t_{PHLmin} - t_{PHLmax})],$$

and further rearranged to obtain

$$[(t_{PLH} - t_{PHL})_{max} - (t_{PLH} - t_{PHL})_{min}],$$

which is the maximum minus the minimum data sheet values of ($t_{PLH} - t_{PHL}$). The difference between the maximum and minimum values depends directly on the total spread in propagation delays and sets the limit on how good the worst-case dead time can be for a given design. Therefore, optocouplers with tight propagation delay specifications (and not just shorter delays or lower pulse-width distortion) can achieve short dead times in power inverters. The HCPL-4504/0454/J454 and HCNW4504 specify a minimum ($t_{PLH} - t_{PHL}$) of -0.7 μ s over an operating temperature range of 0-70°C, resulting in a maximum dead time of 2.0 μ s when the LED turn-on delay is equal to ($t_{PLH} - t_{PHL}$)_{max}, or 1.3 μ s.

It is important to maintain accurate LED turn-on delays because delays shorter than ($t_{PLH} - t_{PHL}$)_{max} may allow shoot-through currents, while longer delays will increase the worst-case dead time.



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