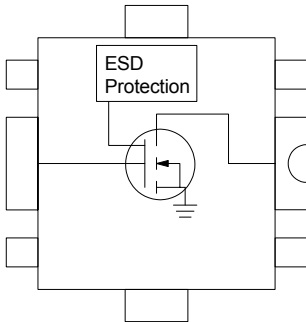




## Product Description

Sirenza Microdevices' **SLD-1026Z** is a robust 3 Watt high performance LDMOS transistor designed for operation from 10 to 2700MHz. It is an excellent solution for applications requiring high linearity and efficiency at a low cost. The SLD-1026Z is typically used in the design of driver stages for power amplifiers, repeaters, and RFID applications. The power transistor is fabricated using Sirenza's latest, high performance LDMOS II process. This product features a RoHS/WEEE Compliant package with matte tin finish, designated by the 'Z' suffix.

## Functional Schematic Diagram



Backside Paddle = Ground

## RF Specifications

Symbol	Parameter	Unit	Min	Typ	Max
Frequency	Frequency of Operation	MHz	10	-	2700
Gain	3 Watt CW, 902-928MHz	dB		19	
Efficiency	Drain Efficiency at 3 Watt PEP, 915MHz	%		32	
IRL	Input Return Loss, 3 Watt Output Power, 915MHz	dB		-12	
Linearity	3 <sup>rd</sup> Order IMD at 3 Watt PEP (Two Tone), 915MHz	dBc		-28	
	1dB Compression ( $P_{1dB}$ ), 915MHz	Watt		3.5	
$R_{TH}$	Thermal Resistance (Junction-to-Case)	°C/W		17	

**Test Conditions**  $V_{DS} = 28.0V$ ,  $I_{DQ} = 50mA$ ,  $T_{Flange} = 25^{\circ}C$

## DC Specifications

Symbol	Parameter	Unit	Min	Typical	Max
$g_m$	Forward Transconductance @ 30mA $I_{DS}$	mA / V		150	
$V_{GS}$ Threshold	$I_{DS}=3mA$ , $V_{DS}=28V$	Volts		4.2	
$V_{DS}$ Breakdown	1mA $V_{DS}$ current	Volts		65	
$C_{iss}$	Input Capacitance (Gate to Source) $V_{GS}=0V$ $V_{DS}=28V$	pF		5.2	
$C_{rss}$	Reverse Capacitance (Gate to Drain) $V_{GS}=0V$ $V_{DS}=28V$	pF		0.2	
$C_{oss}$	Output Capacitance (Drain to Source) $V_{GS}=0V$ $V_{DS}=28V$	pF		3.2	
$R_{DSon}$	Drain to Source Resistance, $V_{GS}=10V$ $V_{DS}=250mV$	$\Omega$		3.0	

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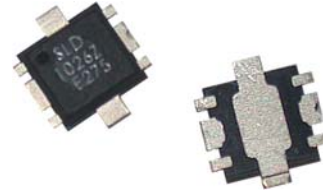
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EDS-104157 Rev A

Preliminary

## SLD-1026Z



### 3 Watt Discrete LDMOS Device Plastic Surface Mount Package



Proprietary SOF-26 Package

## Product Features

- 3 Watt Output  $P_{1dB}$
- Single Polarity Supply Voltage
- High Gain: 19 dB at 915 MHz
- High Efficiency: 44% at 3W CW
- XeMOS II LDMOS
- Proprietary Low Thermal Resistance Package  
Hand Solderable and Easy Rework
- Integrated ESD Protection, Class 1B

## Applications

- Base Station PA driver
- Repeaters
- RFID
- Military Communication
- GSM/CDMA



Preliminary

SLD-1026Z 3 Watt LDMOS FET

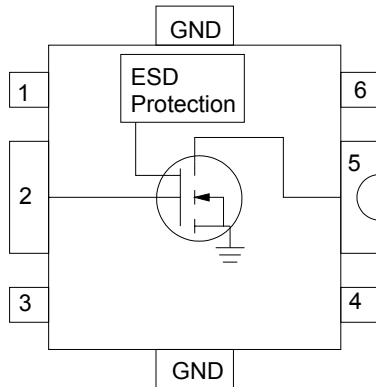
## Quality Specifications

Parameter	Description	Rating
ESD Rating	Human Body Model	1B

## Pin Description

Pin #	Function	Description
1, 3	NC	These pins are not connected internal to the package. Bus them to pin 2 as shown in the app circuit.
2	Gate	Transistor RF input and gate bias voltage. The gate bias voltage must be temperature compensated to maintain constant bias current over the operating temperature range. Care must be taken to protect against video transients that exceed the maximum input power or voltage.
4, 6	NC	These pins are not connected internal to the package. Bus them to pin 5 as shown in the app circuit.
5	Drain	Transistor RF output and drain bias voltage. Typical voltage 28V.
GND	Source, Gnd	These pins are DC connected to the backside paddle. They provide good thermal connection to the backside paddle for hand soldering and rework. Many thermal and electrical GND vias are recommended as shown in the landing pattern.

## Pin Diagram



### Note 1:

Gate voltage must be applied to  $V_{GS}$  lead concurrently or after application of drain voltage to prevent potentially destructive oscillations. Bias voltages should never be applied to the transistor unless it is properly terminated on both input and output.

### Note 2:

The required  $V_{GS}$  corresponding to a specific  $I_{DQ}$  will vary from device to device due to the normal die-to-die variation in threshold voltage with LDMOS transistors.

### Note 3:

The threshold voltage ( $V_{GSTH}$ ) of LDMOS transistors varies with device temperature. External temperature compensation may be required. See Sirenza application notes AN-067 LDMOS Bias Temperature Compensation.

## Absolute Maximum Ratings

Parameters	Value	Unit
Drain Voltage ( $V_{DS}$ )	35	Volts
Gate Voltage ( $V_{GS}$ )	20	Volts
RF Input Power	+30	dBm
Load Impedance for Continuous Operation Without Damage	10:1	VSWR
Output Device Channel Temperature	+150	°C
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-40 to +150	°C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.

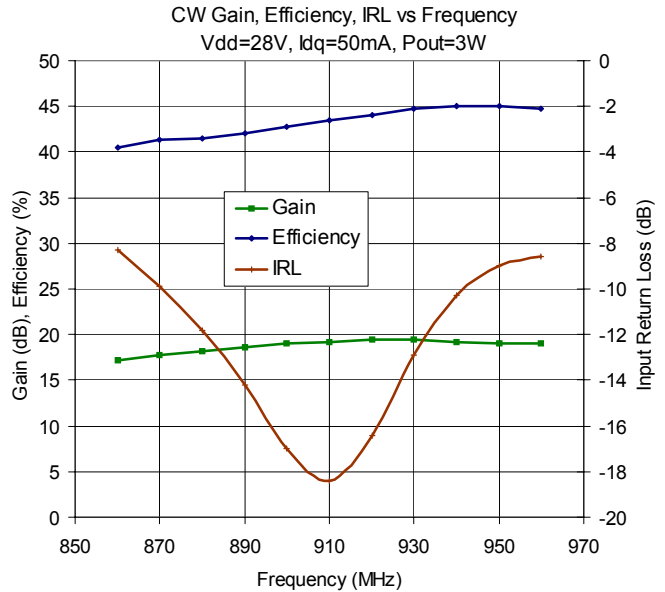
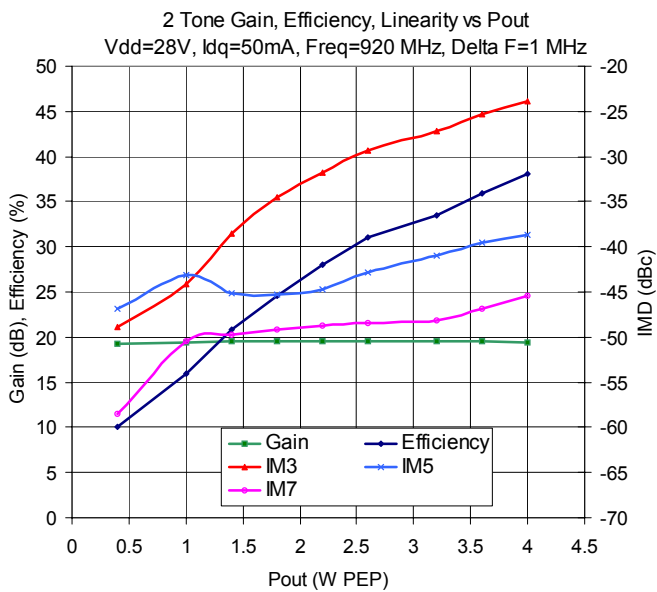
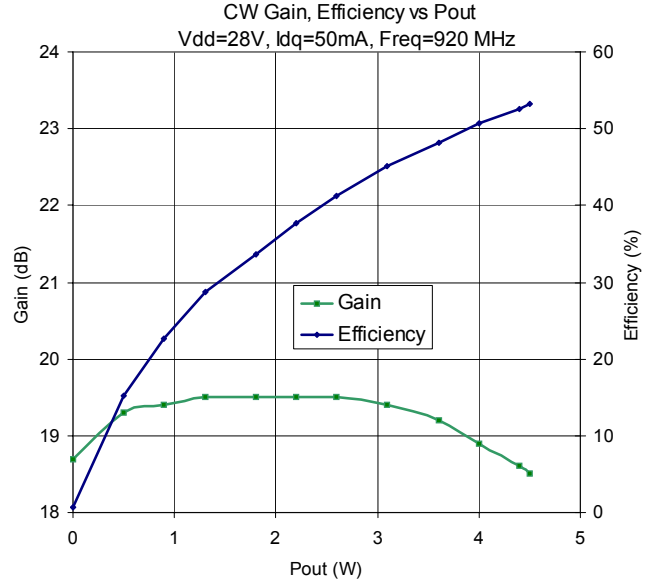
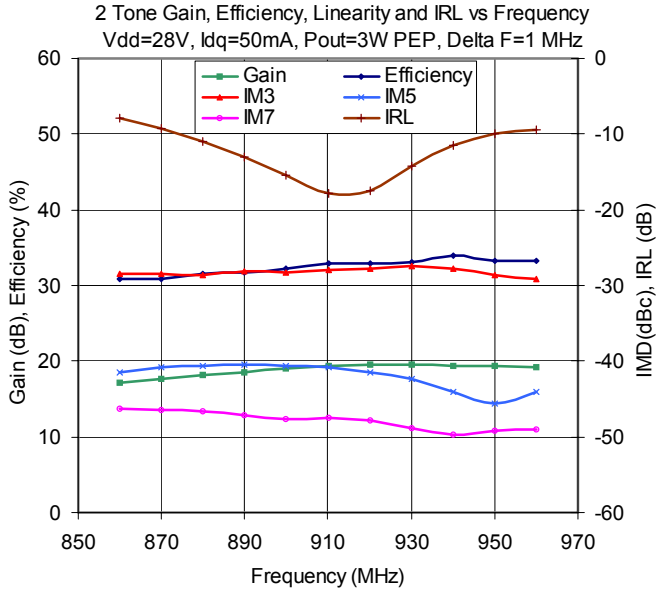


### Caution: ESD Sensitive

Appropriate precaution in handling, packaging and testing devices must be observed.



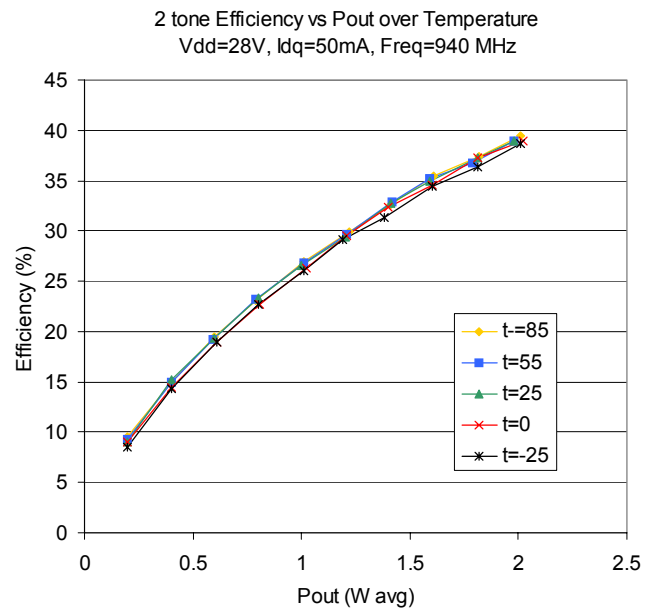
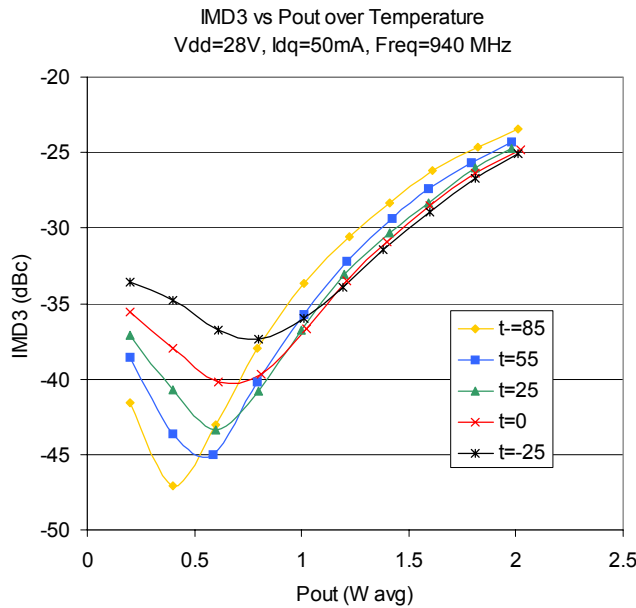
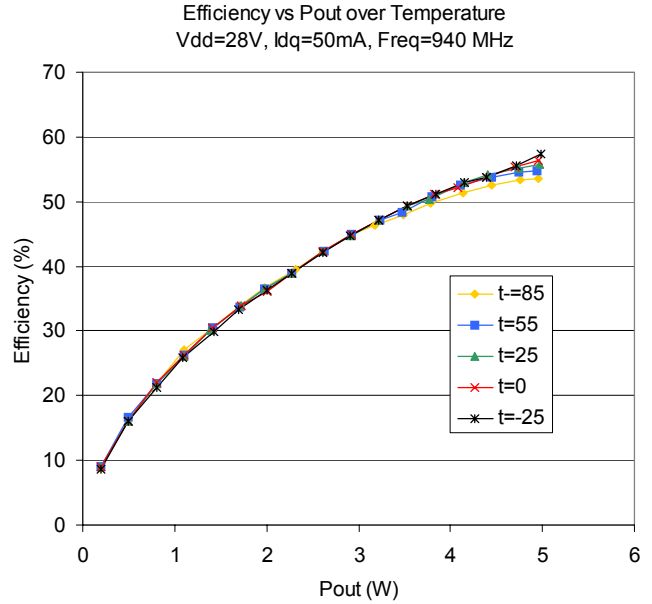
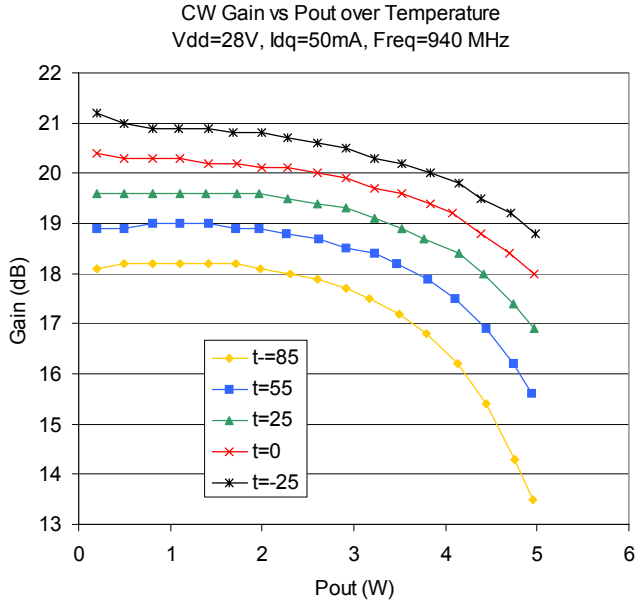
### Typical Performance Curves in 900 MHz Application Circuit



To receive Gerber files, DXF drawings, and assembly recommendations for the test board with fixture, contact applications support at [support@sirenza.com](mailto:support@sirenza.com).



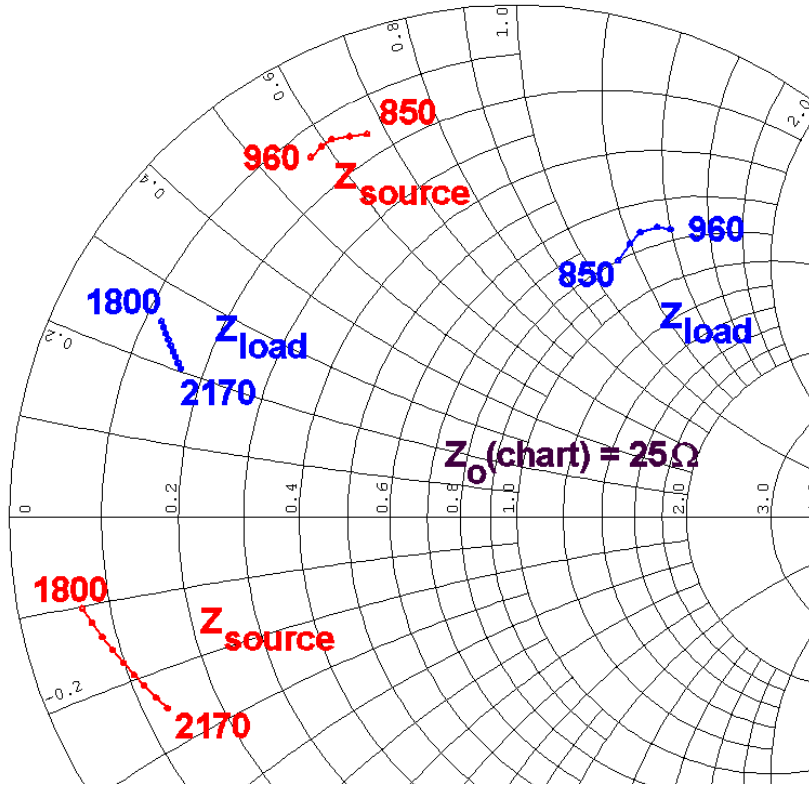
### Typical Performance Curves in 900 MHz Application Circuit - Data over Temperature



To receive Gerber files, DXF drawings, and assembly recommendations for the test board with fixture, contact applications support at [support@sirenza.com](mailto:support@sirenza.com).



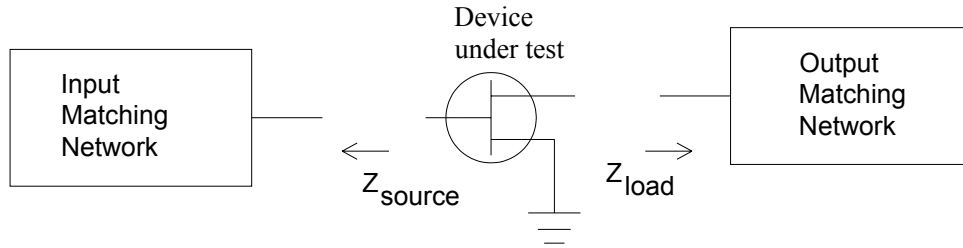
Impedance data



**Preliminary**  
**SLD-1026Z 3 Watt LDMOS FET**

**Impedance Data**

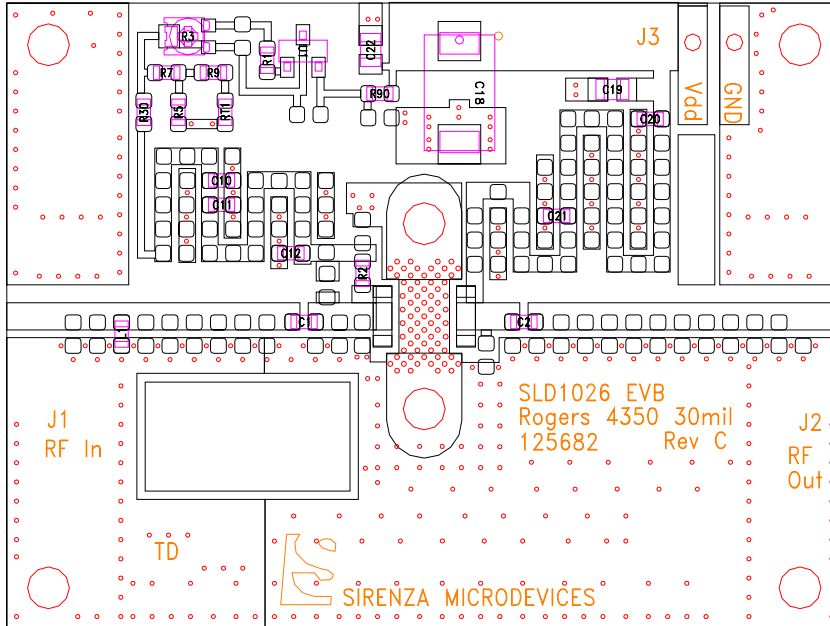
Frequency (MHz)	Z <sub>source</sub>	Z <sub>load</sub>
850	4.0 + j 16.7	20.0 + j 28.0
880	3.7 + j 16.0	18.8 + j 30.0
910	3.4 + j 15.3	18.0 + j 31.5
940	3.4 + j 14.8	18.0 + j 33.5
960	3.5 + j 14.2	18.6 + j 35.0
1800	1.7 - j 2.6	3.0 + j 6.3
1840	1.9 - j 3.0	3.15 + j 6.15
1880	2.1 - j 3.5	3.3 + j 6.0
1930	2.3 - j 3.9	3.45 + j 5.8
1960	2.5 - j 4.4	3.6 + j 5.7
1990	2.7 - j 4.9	3.75 + j 5.55
2110	2.85 - j 5.3	3.9 + j 5.4
2140	3.1 - j 5.8	4.05 - j 5.25
2170	3.25 - j 6.2	4.2 - j 5.1



Z<sub>source</sub> and Z<sub>load</sub> are the optimal impedances presented to the SLD-1026Z when operating at 28V, Idq=50mA, Pout=3W PEP



**900 MHz Application Circuit**



**Bill of Materials - 900 MHz Application Circuit**

Reference Designation	Description	Mfg	Mfg part #
C1	CAP 9.2PF250V 5% 0603	ATC	600S9R2JT250XT
C2	CAP 68PF250V 5% 0603	ATC	600S680JT250XT
C21	CAP 56PF250V 5% 0603	ATC	600S560JT250XT
L1	IND, 18 nH 5% 0603	Coilcraft	0603CS-180XJB
C10	CAP 0.1 UF 16V 10% 0603	AVX	0603YG104ZA2A
C11, C20	CAP 1000 PF 50V 10% 603	AVX	06035C102KAT2A
C12	CAP 68PF 250V 5% 603 LF	ATC	600S680JT250XT
C18	CAP 10 UF 35V 20% TAN T ELECT	Kemet	T494D106M035AS
C19, C22	CAP 0.1 UF 50V 10% 805	Panasonic	ECJ2YB1H104K
J1, J2	Connector SMA END 0.037	Johnson	142-0751-821
J3	Connector MTA SMD R/A 2 PIN	Amp	640455-2
R1	RES 324 1/16W 1% 603	Panasonic	ERJ-3EKF3240V
R2	RES 2.7 Ohm 0603	Panasonic	ECR-104493-2R7
R3	POT TRIM 500 OHM 2MM	Panasonic	EVM-2WSX80B52
R30	RES 49.9 1/16W 1% 603	Panasonic	ERJ-EKF49R9V
R5	RES 130 1/16W 1% 603	Panasonic	ERJ-3EKF1300V
R7	RES 210 1/16W 1% 603	Phillips	9C06031A2100FKHFT
R9	RES 0 1/16W 5% 603	Panasonic	ERJ-3GSY0R00V
R90	RES 1.0K 1/16W 1% 603	Panasonic	ERJ-3EKF1001V
RT1	THERMISTOR 100K 5% 603	Panasonic	ERT-J1VV104J
U1	IC VOLT REG 100 MA 5 V SOT-23	National	LM3480IM3-5.0
6 Screws	SCREW #2-56 PHILIPS PAN HEAD	various	-
6 Washers	WASHER #2 FLAT SS	various	-
PCB	PCB, 30 mils thick Dk=3.48	Rogers	4350
Heatsink	machined aluminum	various	-

To receive Gerber files, DXF drawings, and assembly recommendations for the test board with fixture, contact applications support at [support@sirenza.com](mailto:support@sirenza.com).

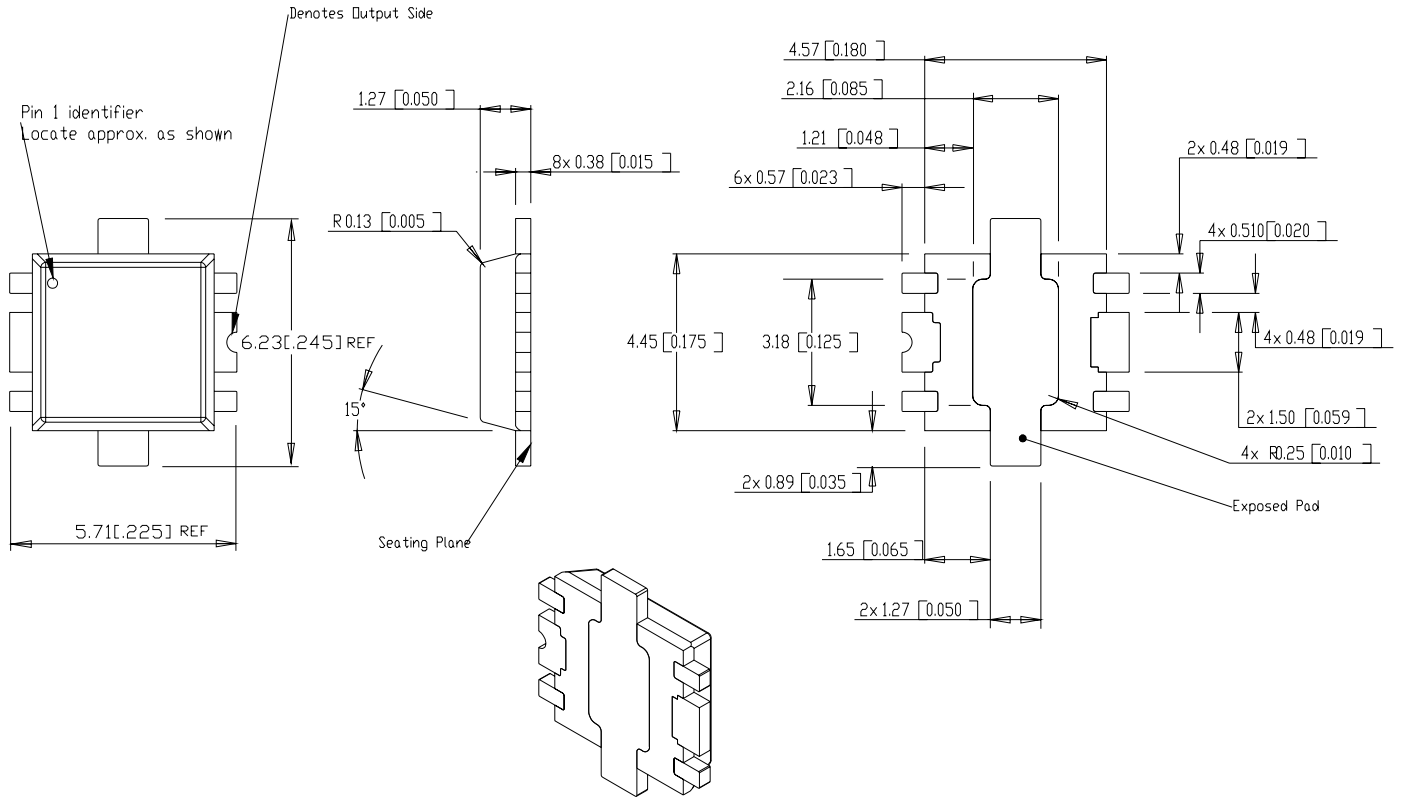
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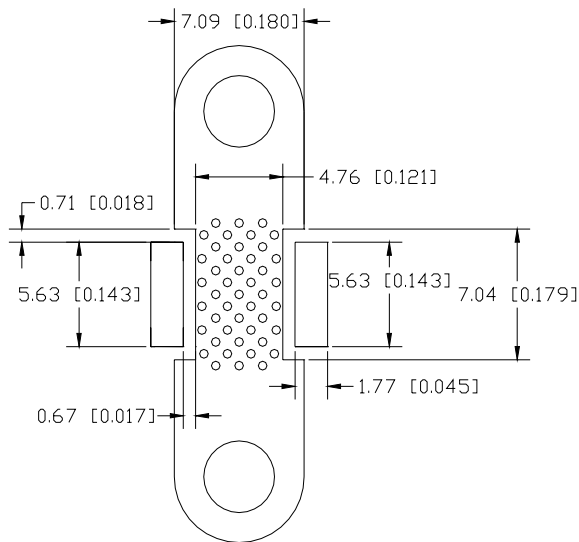
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EDS-104157 Rev A



**Package Outline (dimensions in mm [in]):**



**Recommended Metal Land Pattern (dimensions in mm [in]):**



**Part Number Ordering Information**

Part Number	Devices Per Reel	Reel Size
SLD-1026Z	500	7"

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