

VF230V

Voltage Controlled Oscillators LVPECL/LVDS 3.3V

5X7 mm Surface Mount

750 KHz to 800 MHz

Features

- High speed – Low jitter LVPECL or LVDS output with tristate
- Small SMD package (5X7 mm)
- Stability options of 50 and 25ppm
- Commercial or industrial temperature range
- Rugged, hermetic package for automated assembly
- ROHS Compatible

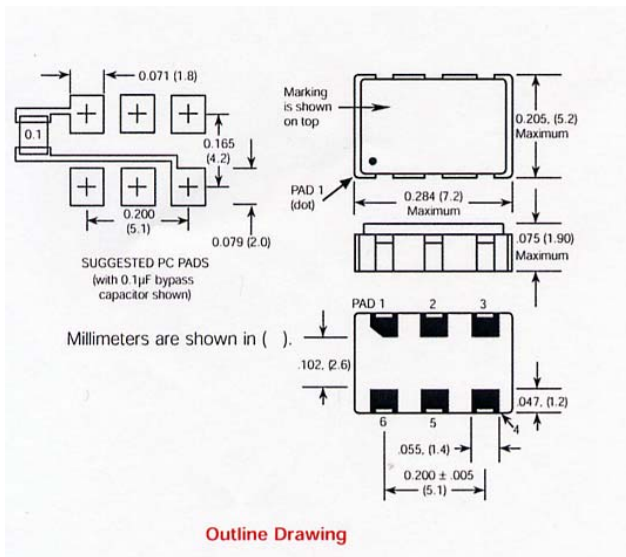
Typical Applications

Telecom/networking systems that require low jitter clocks

- ✓ DSL,
- ✓ Gigabit Ethernet,
- ✓ Fibre channel
- ✓ Optical networking

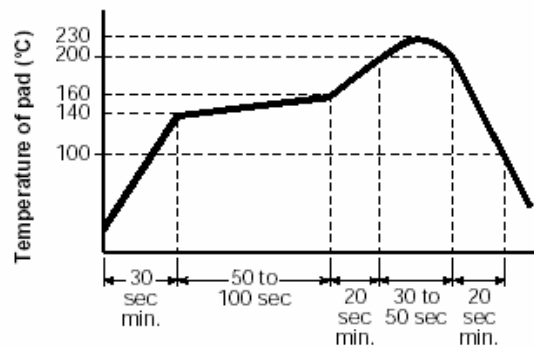
Description

Valpey Fisher's 230V surface mount VCXO provides waveforms for clocking LVPECL and LVDS circuits. The 5X7mm footprint package provides the performance of larger oscillators with a level of board space reduction achieved. ASIC technology is used to accomplish size reduction and enhance performance and reliability. Low jitter output signals are generated. The wide range of frequencies offered, many stability options, and industrial temperature range availability, make this model the solution for many applications. A tristate function is included to allow for easy automated testing of assemblies. Tape and reel packaging is standard.



CONNECTIONS

PIN 1	V _c (Control Voltage)
Pin 2	OE (Output Enable)
PIN 3	Ground
PIN 4	Output 1: Q
PIN 5	Output 2: Q
PIN 6	+V _{DD}



VF230V**Voltage Controlled Oscillators LVPECL/LVDS 3.3V****5X7 mm Surface Mount****750 KHz to 800 MHz****ELECTRICAL SPECIFICATIONS****Frequency Range** 750 KHz to 800 MHz**Frequency Stability**

Includes calibration at 25°C, operating temperature, change of input voltage, change of load, shock and vibration 100, 50, 25 or 20 ppm

	MIN	TYP	MAX	UNITS
Input Voltage, V_{DD}	3.15	3.3	3.45	volts
Jitter				
Period jitter RMS				
19.44MHz		5		ps
77.76MHz		8		ps
155.52MHz		9		ps
622.08MHz		10		ps
Integrated jitter RMS				
12 KHz to 20 MHz @ 155.52MHz		3	5	ps
Symmetry at (V_{DD}-1.3) V_{DC} (PECL)	40	50	60	percent
At (1.25 V_{DC}) (LVDS)	40	50	60	percent

Aging

First year	3	ppm
After first year	1	ppm/yr

Tristate**Input Requirements for Pin 1:**

“1”: On-Pin 1 may float or 2.8V min
 “0”: Tristate-Pin 1 requires 0.4V max

Typical Phase Noise (dBc/Hz)	10Hz	100Hz	1KHz	10KHz	100KHz
Oscillator Frequency					
19.44MHz	-60	-90	-112	-140	-140
106.25MHz	-60	-90	-112	-127	-125
155.52MHz	-60	-90	-112	-125	-123
622.08MHz	-60	-90	-109	-110	-109

	MIN	TYP	MAX	UNITS
Input Impedance, Z_{in}		50		kΩ
Control Voltage, V_c (V)	0.3	1.65	3	volts
(also available)	0	1.65	3	volts
Center Frequency, (V_{co})		1.65		volts
Linearity		5	15	%
Pullability (APR)		100	150	

See ordering information

(Include initial tolerance, deviation over temperature, shock, vibration supply voltage and aging).

ENVIRONMENTAL SPECIFICATIONS**Temperature**

*Operating 0° to 70°C

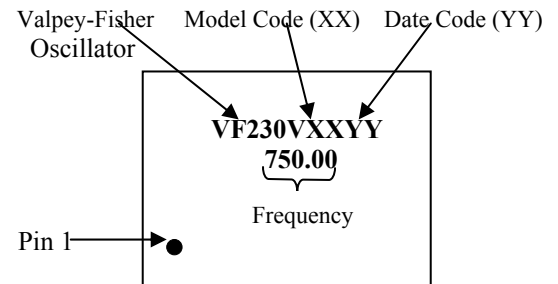
Storage -55° to +125°C

Shock- 1000 Gs, 0.35 ms, ½ sine wave, 3 shocks in each plane**Vibration-** 10-2000 Hz of .06" d.a. or 20 Gs, whichever is less**Humidity-** Resistant to 85° R.H. at 85°C**MECHANICAL SPECIFICATIONS****Leak-** MIL STD 883, Method 1014, Condition A1**Case-** Ceramic with hermetic resistance-welded metal lid**Pads-** Solderable gold over nickel**Marking-** Epoxy ink or laser engraved**Resistance to solvents-** MIL STD 202, Method 215

*Operating -40 to +85°C also available.

MARKING SPECIFICATION

The format for the marking is:



VF230V

Voltage Controlled Oscillators LVPECL/LVDS 3.3V

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750 KHz to 800 MHz

PECL Output Models

Electrical Specifications

	MIN	TYP	MAX	UNITS
RL = 50 Ω to (V _{DD} - 2V) (see figure)				
Output High Voltage, V _{OH}		V _{DD} -1.025		V
Output Low Voltage, V _{OL}			V _{DD} -1.620	V
Input Current, PECL				
0.75 – 24 MHz			25	mA
24 – 160 MHz			65	mA
160 – 800 MHz			100	mA
Switching Characteristics				
Clock Rise Time, tr @20/80%		0.3	0.35	ns
Clock Fall Time, tf @80/20%		0.3	0.35	ns

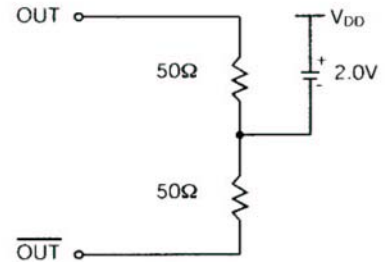


Fig 1.
PECL Levels Test Circuit

LVDS Output Models

Electrical Specifications

	MIN	TYP	MAX	UNITS
RL = 100 Ω (see figure)				
Output Differential Voltage, V _{OD}	247	355	454	mV
Output High Voltage, V _{OH}		1.4	1.6	V
Output Low Voltage, V _{OL}	0.9	1.1		V
Offset Voltage, V _{OS}	1.125	1.2	1.375	V
Input Current, LVDS				
0.75 – 24 MHz			25	mA
24 – 96 MHz			45	mA
96 – 800 MHz			80	mA
Switching Characteristics				
Differential Clock Rise Time, tr		0.3	0.4	ns
Differential Clock Fall Time, tf		0.3	0.4	ns

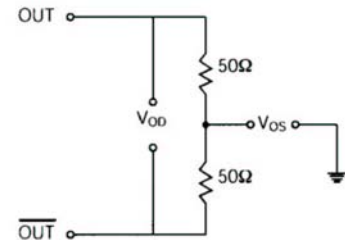


Fig 2.
LVDS Test Load

HOW TO ORDER

For part Number, put package type before model number, and add frequency in MHz, for example:

VF230V	<u>A</u>	<u>A</u>	<u>T</u>	<u>A</u>	<u>A</u>	<u>125</u> Frequency	<u>M</u> M=MHz K=KHz
Frequency Stability		Temperature Range	Tristate	Output Logic	Pullability		
A=+/-50 ppm	} 0.3-1.65-3V 0-1.65-3.3V	A=0 to +70°C	T=Tristate	A=45/55%LVDS	A=+/- 100ppm		
B=+/-25ppm		B=-40 to +85°C	N=Non Tristate	B=40/60%LVDS	B=+/-150ppm		
C=+/-50ppm				C=45/55%PECL			
D=+/-25ppm				D=40/60%PECL			

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