CMOS SOS Switches Offer Useful Features, High Integration

Understanding the basic theory and characteristics underlying CMOS SOS switch technology opens the door to numerous RF and microwave applications.

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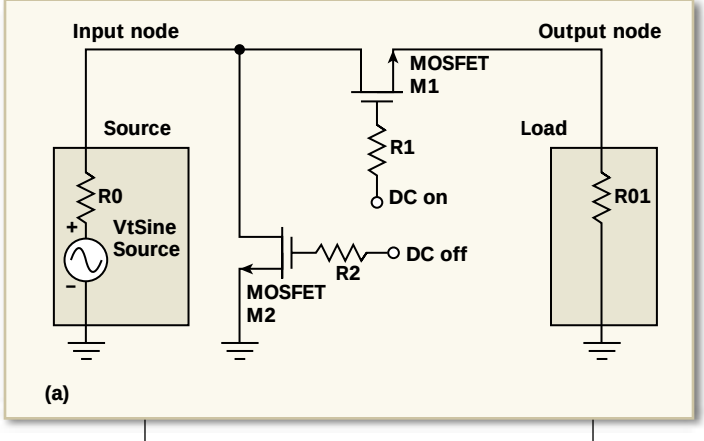
Switching RF and microwave signals is a fundamental function in all radio applications. Accordingly, there are a great variety of switch products and forms, from the basic single pole, single throw (SPST) to a large crosspoint matrix. This article explains basic RF semiconductor switch functionality and reviews switch parameters and limitations. It examines the basic theory of an RF switch and the trade-offs between power handling, insertion loss, and isolation.

Although there are diode-type switches, the focus here is on complementary-metal-oxide-semiconductor (CMOS) metal-oxide-semiconductor field-effect-transistor (MOSFET) types, the main technology for wireless applications. Switches can also be classified as reflective and absorptive, but this article addresses only the reflective type.

Most high-frequency switches use gallium-arsenide (GaAs) technology. Peregrine Semiconductor's Ultra-Thin-Silicon (UTSi) Technology enables the realization of quality RF switches using dielectric isolation between UTSi MOSFETs that are fabricated in CMOS. UTSi is a Si-CMOS process that is fabricated on a sapphire insulator, known as Si-on-sapphire (SOS). This enables the manufacture of simple to highly integrated RF switches with modest-to-high-power capability (+10 to +37 dBm). Stacking devices allows UTSi RF switches to handle any practical power level. The complete isolation afforded by UTSi makes this switch impossible to fabricate in conventional Si-CMOS, bipolar CMOS (BiCMOS), and Si-germanium (SiGe) technologies. UTSi switches can be further integrated with complex digital CMOS control and other components in order to realize excellent on-chip isolation and insertion loss over a broad range of frequencies and supply voltages.



1a. The basic MOSFET SPST switch consists of two devices (M1 and M2) that either pass or block an RF input signal depending on the bias voltages that control M1 and M2.

Simple mathematical expressions can be used to describe the operation of MOS-

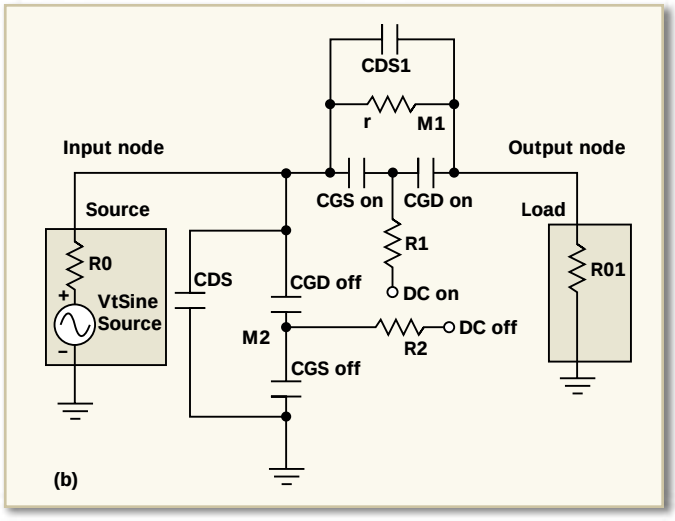
FET switches. An SPST switch schematic is shown in **Fig. 1a**. An RF signal presented at the input node is either blocked from or passed through to the output node, depending on the DC bias of MOSFETs M1 and M2. Actual values of DC bias depend on the polarity and threshold of the MOSFETs. Resistor R0 isolates the bias from the AC signal and is essential for optimal switch action. The on- and off-states of the switch are explained using **Figs. 1b and c.**

Figure 1b illustrates the equivalent small-signal values of MOSFETs M1 and M2 when the RF switch is on. M1 is primarily resistive, with a through coupling of r, while M2 is primarily capacitive, with coupling to ground through capacitors CGS off, CGD off, and CDS. The importance of the gate resistor R1 is clearly illustrated. If R1 is too small, the gate node of M1 would be held at the DC bias voltage, resulting in negative feedback via capacitors CGS on and CGD on. This feedback has the effect of increasing r, resulting in larger Ohmic loss. A small value of R2 prevents the voltage dividing action of M2 capacitors CGS off and CGD off, reducing the 1-dB compression point up to 6 dB (as explained later). R, therefore, needs to be large enough so that RF signals feeding onto the gate node are AC isolated from the DC bias. That is:

$$f_{min} = 5 / \pi RC_{offp}\sqrt{2} \qquad (1)$$

where:

R = the series resistor of the gate node **(Fig. 1b),** and f_{min} = the minimum frequency at which the switch can operate. Since R is much larger than 50 Ω, C_{offp} for M2 is the parallel value of CGS off and CGD off (the off-capacitance was chosen since it results in the largest f_{min}). It is important to realize that Eq. 1 is based on simple resistive-capacitive (RC) calculations and has no lower limit due to semiconductor material limitations. By contrast, GaAs switches may have switching speed limitations as a result of slow states that may be present in the GaAs.



1b. The equivalent small-signal parameters of M1 and M2 in Fig. 1a show the dominant characteristics of each device. M1 is primarily resistive while M2 is capacitive.

The insertion loss of the switch is the difference between the maximum available power at the input and the power delivered to the output. At low frequencies, most of the power is lost across r, resulting in the following expression for insertion loss:

$$IL = 10LOG_{10}\left[\left(1+\frac{r}{2R0}\right)^2 + \left(\frac{\omega C_{offs}(R0+r)}{2}\right)^2\right](in\ dB) \qquad (2a)$$

where:

R0 = the impedance of the source and load (50 Ω),

r = the resistance of M1 when the switch is on, and

C_{offs} = the series value of CGS off and CGD off in parallel with CDS of M2.

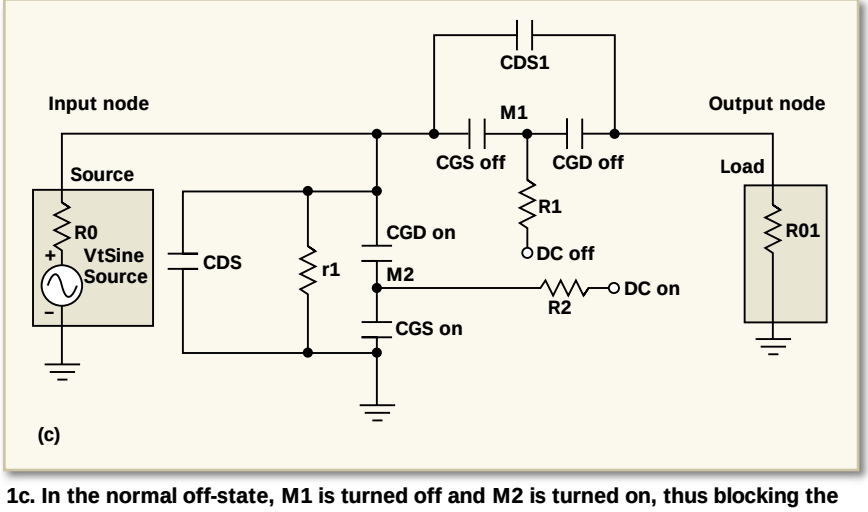
Equation 2a becomes invalid when the capacitive reactance of M2 becomes comparable to r. However, Eq. 2a can serve as a guide in estimating insertion loss. Usually, r is much less than R0 in real switches. Equation 2a is simplified as follows:

$$IL \approx \frac{10r}{R01n(10)} \approx 0.087r \qquad (2b)$$

within 5 percent at low frequencies $\omega \times C \times R0 \leq 0.1$ for $r < 10\ \Omega$ and R0 = 50 Ω

Thus, at low frequencies, a 3-Ω value for r will result in approximately one-quarter-of-a-decibel insertion loss.

The small-signal equivalent circuit for the off-state of the switch in Fig. 1a is provided in Fig. 1c. For simplification, M1 and M2 are chosen identically, so



1c. In the normal off-state, M1 is turned off and M2 is turned on, thus blocking the input signal from the output node. M2 serves to increase the input-to-output isolation of the switch.

the values of capacitance and resistance are identical to those in Fig. 1b. However, for an actual circuit design, M1 and M2 may have different sizing for overall performance optimization.

In the off state, M1 has the role of blocking the input from the output. When turned off, M1 is primarily capacitive with feedthrough of the input determined by the series/parallel values of CGD off, CGS off, and CDS. Feedthrough of the signal is undesirable and is related to the isolation of output to input when the switch is turned off. To reduce the magnitude of the feedthrough (i.e., increase the isolation), M2 comes into play.

M2 is turned on when M1 is turned off. In this condition, M2 is primarily a resistor with value r. By design, this value is much less than the characteristic impedance of the RF source, so r greatly reduces the voltage at the input of M1. When the value of r is much less than R0 and the feedthrough capacitive reactance of M2, isolation can be easily calculated. Isolation for the off-switch is the difference between the maximum available power at the input to power at the output. The circuit analysis results in the following equation for isolation:

$$IS = -10LOG_{10}\left[4r^2\omega^2{C_{offs}}^2 \Big/ \left(1+\frac{r}{R0}\right)^2 + \omega^2{C_{offs}}^2R0^2\left(1+\frac{2r}{R0}\right)\right] \quad (3a)$$

For the condition r <0.1 R0, and $\omega r C_{ons} < 0.1$,
where:

ω = the frequency of the RF input,

R0 = the impedance of the source (50 Ω),

C_{offs} = the feedthrough capacitance of M1 in the off condition,

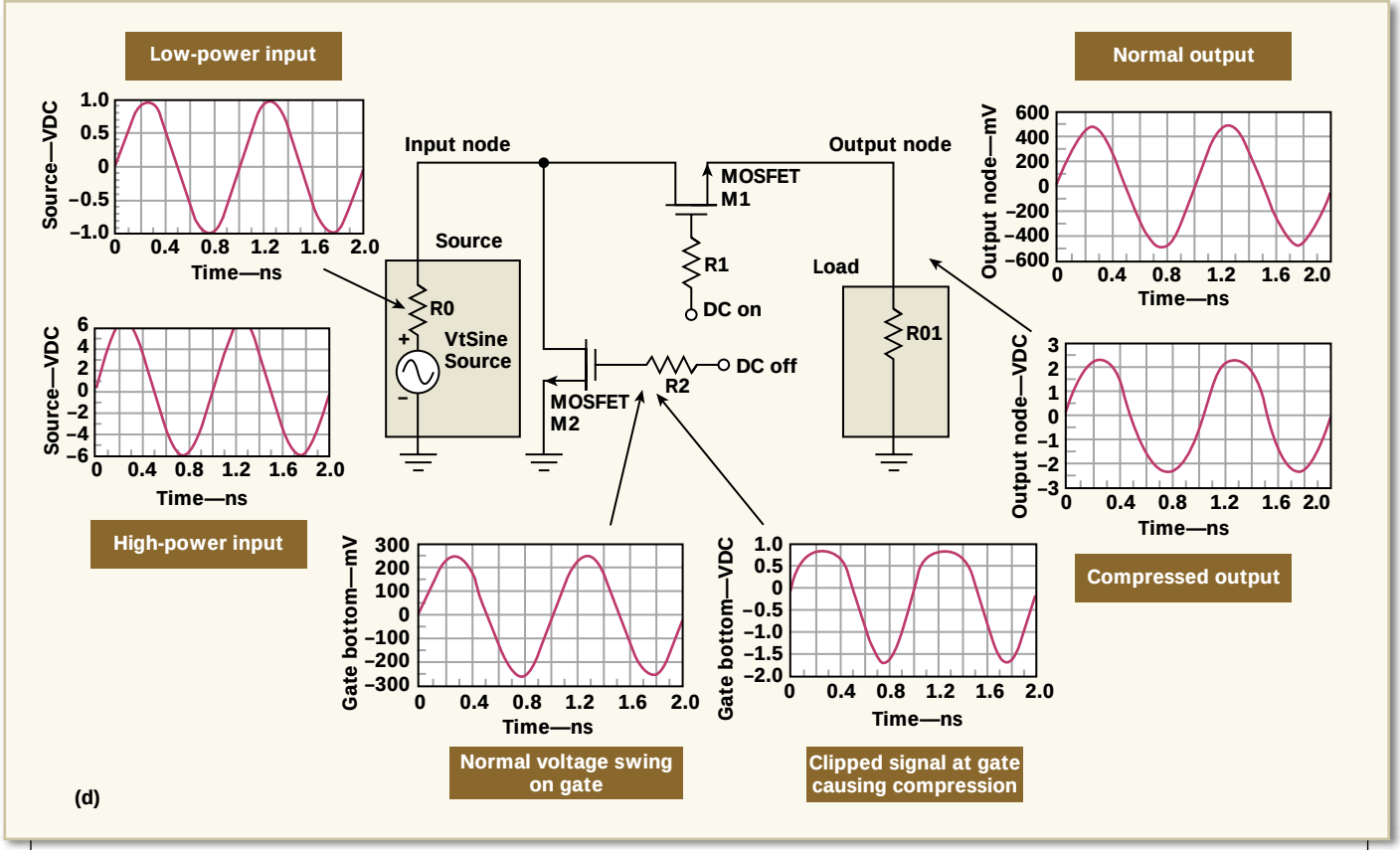
r = the on resistance of M2 in the on condition, and

C_{ons} = the shunt capacitance of M2 in the on condition. Equation 3a is derived by assuming that the coupling to ground is primarily through r. For small values of frequencies and r, the equation for isolation can be further simplified:

$$IS = -20LOG_{10}(2r\omega Ct) \quad (3b)$$

for the condition, r <0.1 R0, and $\omega r C_s < 0.1$ and $\omega R0 C_{offs} < 0.1$

Eqs. 2b and 3b can now be used to estimate values of r and C_t if target insertion loss and isolation are known. For an insertion loss of 0.6 dB, r must be less than 7 Ω in a 50-Ω system. For the same switch, a target isolation of 35 dB at 1-GHz C_{offs} must be less than 0.25 pF. Usually, the values of C_{offs} and r cannot be decoupled and both are determined by the geometry of the device. Thus, the limits of insertion loss and isolation of the switch in Fig. 1a can be determined for a particular device



1d. Various types of compression result in the circuit shown in Fig. 1a, depending on the bias voltages at the gates of M1 and M2. A compressed output is caused by the turning on of the shunt switch (M2), thereby diverting the input signal from appearing at the output node.

geometry. Usually, the product of r and C_t are independent of the MOSFET width, so fundamental isolation of the switch is also independent of MOSFET width.

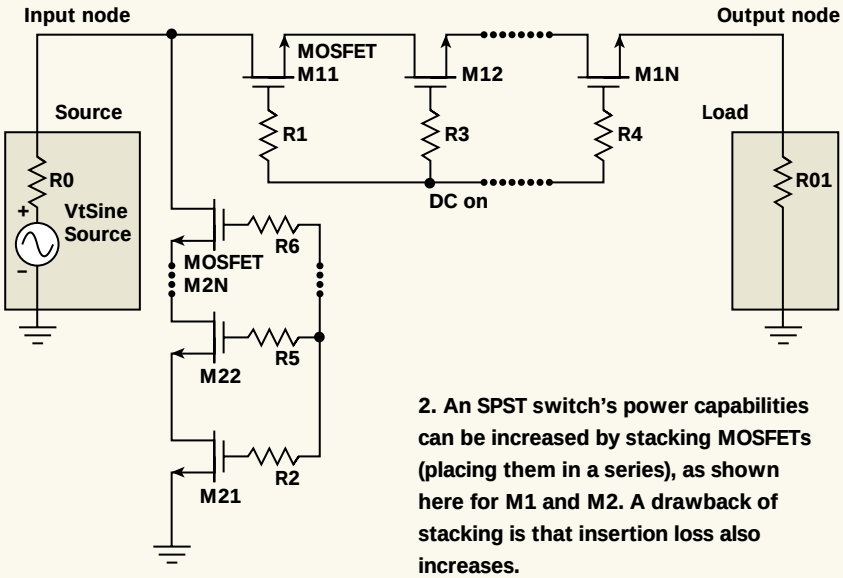
Switch Compression

In addition to insertion loss and isolation, another important parameter of RF switches is their ability to handle large input power when the switch is turned on, so that the insertion loss is not a function of power at a fixed frequency. Many applications require that power transmitted through an on switch should not be distorted. If two tones that are closely spaced in frequency are passed through a switch at the same time, nonlinearity of the switch can produce intermodulation (IM) and create a false tone in adjacent channels. If these channels are reserved for information signals, power in these false tones must be as small as possible. A measure of the power in these false tones is known as the input third-order intercept point (IP3). Switches with large IP3 values produce little power in adjacent channels, which is important in applications such as antenna switches. IP3 is usually 17 to 20 dB larger than the largest input power a switch can handle without distortion.

An indicator of a switch's ability to handle power is known as the 1-dB compression point (P1dB). It is defined as the input power at which the insertion loss has increased by 1 dB from its low-power value.

$$IL(P1dB) - IL(P \rightarrow -\infty) = 1.0\ dB \qquad (4)$$

To understand what causes compression, voltage levels at various nodes are drawn for the simple switch in Fig. 1a in the on-state and presented in **Fig. 1d.** The source is represented by a sine wave with a peak-to-peak amplitude of 2 V_o. DC levels required to turn the MOSFETs on and off are V_{on} and V_{off}, respectively. A normal, uncompressed signal is shown on the output node, as well as curves showing the compression modes at the output. To understand how compression occurs, operation of the MOSFET must be understood.



2. An SPST switch's power capabilities can be increased by stacking MOSFETs (placing them in a series), as shown here for M1 and M2. A drawback of stacking is that insertion loss also increases.

MOSFETs require a gate-to-source bias that exceeds the threshold voltage, V_t, to turn on. Likewise, the gate-to-source bias must be less than V_t for the switch to be off. V_t is positive in "type-N" MOSFETs and negative for "type-P" MOSFETs. For the switch in Fig. 1a, "type-N" MOSFETs were chosen. The source of an "type-N" MOSFET is the node with the lowest potential.

The reason for the first type of compression can now be explained using the previous concepts. If a transient voltage on M2, shown in Fig. 1c, results in turning on M2 during part of the cycle, input power will be routed to ground and lost to the output. This loss of power becomes larger for larger input powers and will cause compression. P1dB for this case can be estimated.

Assuming CGD and CGS are similar or the same in value, only half of the transient voltage change on the input node will appear at the gate node of M2. Eventually, the negative swing of the input will dip below the potential of the gate, as well as below ground (thus becoming the source). When this difference becomes V_t, M2 begins to turn on and compression begins. P1dB from this effect is:

$$P1dB_{VT} = 10LOG_{10}\left(\frac{2(V_t - V_{off})^2}{R0}\right) + 30\ (in\ dBm) \qquad (5)$$

where:

$P1dB_{VT}$ = the onset of compression for the switch in Fig. 1a.

This compression is caused by the turning on of a normally off gate in the shunt leg of the switch. Suppose V_t is approximately +0.7 VDC and V_{off} is cho-

Power capability versus insertion-loss trade-offs

Number in stack	Vth (VDC)	V_{on}/ V_{off}	IL at 1 GHz	IS at 1 GHz	IL at 2 GHz	IS at 2 GHz	IL at 4 GHz	IS at 4 GHz	Onset of comp. (dBm)
1	0.7	3.0/0	0.16	41	0.24	35	0.55	30	13
3	0	3.0/ –3.0	0.39	41	0.40	35	0.43	29	31
6	0	3.0/ –3.0	0.75	42	0.75	36	0.76	30	37

C_{offs} = 0.5 pF
r = 1.5 Ω

sen to be 0 VDC. Substituting in Eq. 5, compression will begin at approximately +13 dBm. A negative value for V_{off} of −1 VDC will increase the compression to approximately +21 dBm. For the circuit in Fig. 1d, compression can be greatly increased by using a negative supply to turn off the devices. Note that for normal low input power, half of the source voltage is dropped across the output load. With low input power, the potential on shunt MOSFET gate never exceeds +0.7 VDC, thus ensuring that it does not turn on. At high-power input, the voltage swing on the output is much less than half of the source voltage, indicating that the compression is occurring. The compression is caused by the extreme swing in gate voltage on shunt MOSFET, which turns it on during the positive half of the input cycle (Fig. 1d).

The second type of compression occurs when the source and drain of M2 break down at excessive voltages. For submicron Si-on-insulator (SOI) devices, this voltage may be approximately only +1 VDC above the supply. Clipping occurs at the two extremes of the large transient input voltage. If the source-to-drain breakdown voltage is V_{bk}, the onset of compression from this effect is:

$$P1dBbk = 10LOG_{10}\left(\frac{V_{bk}^{\,2}}{2R0}\right) + 30\ (in\ dBm) \qquad (6)$$

where:

V_{bk} = the source-to-drain breakdown, and

$P1dB_{bk}$ = the estimate of compression for a switch where the source and drain of the off leg break down at large input voltage excursions. For example, suppose the switch in Fig. 1a has the following characteristics:

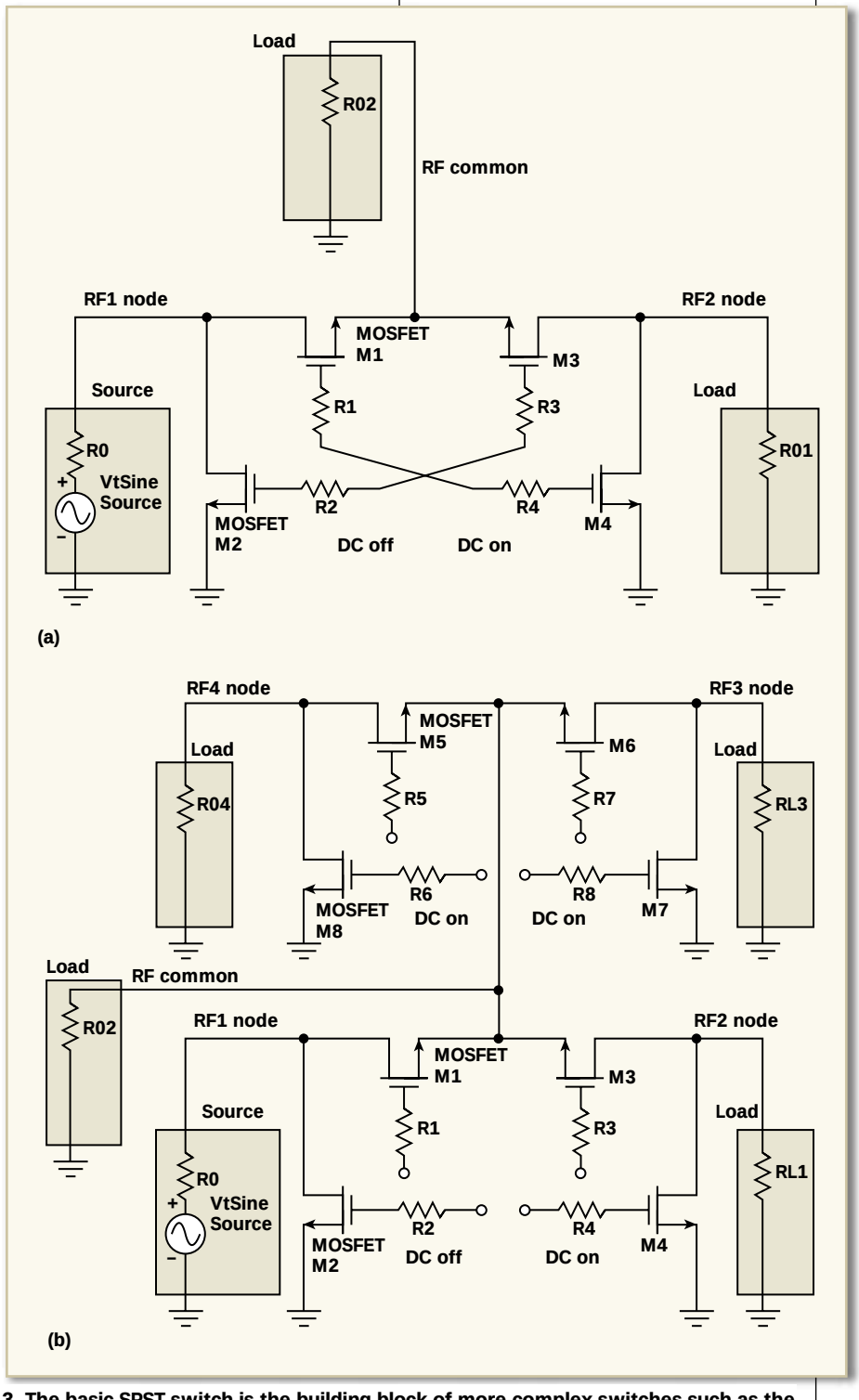
V_{off} = −3.0 VDC,

V_t = +0.7 VDC, and

V_{bk} = +4.0 VDC,

What will cause compression and what will its value be? To answer that, Eqs. 5 and 6 are used to calculate $P1dB_{vt}$ = +27 dBm and $P1dB_{bk}$ = +25 dBm. Since $P1dB_{bk} < P1dB_{vt}$ for this example, the cause of compression will be source-to-drain breakdown and compression will be approximately +25 dBm.

Equations 5 and 6 set clear limits on the power-handling capabilities of the switch as shown in Fig. 1a. For power levels above +22 to +25 dBm, there may be a limit set by source-to-drain



3. The basic SPST switch is the building block of more-complex switches such as the SPDT type shown here. Stacking can also be used here to increase power-handling capability (a). A more complex switch than that shown in Fig. 3a is the SP4T type that appears here. In this example, RF1 is turned on. Integrating devices of this complexity in ICs is not complex using UTSi technology (b).

breakdown. If not, the difficulty of producing negative supplies below $-V_{dd}$ (-3 VDC) demands other circuit solutions. Also, there is the very real issue of placing too much electrical-field stress across a gate oxide. If the simple switch can stand off, by +30 dBm for example, at with a negative supply of -3 VDC, the gate oxide will experience up to +8 VDC. For a 100-Ågate oxide, this will pose a reliability problem.

Figure 2 is a SPST switch with N MOSFETs placed in series (or stacked) for the through and shunt legs. This switch has the advantage of increased power-handling capability, which is traded off against increased insertion loss. Layout of stacked devices is simple and does not require any contacts at the diffusion connection of the MOSFETs, thus device-area penalty is moderate. Each gate has its own resistor R that AC-isolates the MOSFETs from DC bias.

Using small-signal analysis similar to that used in Fig. 1a, the insertion loss for the on-state of a stacked SPST switch is derived. In general, stacked devices will have less off capacitance (by 1/N) and greater resistance than a single device. Thus, the insertion loss becomes:

$$IL(N) = 10LOG_{10}\left\{\left(1+\frac{Nr}{2R0}\right)^2 + \left[\frac{\omega C_{offs}(R0+Nr)}{2N}\right]^2\right\} \qquad (7)$$

where:

IL(N) = the calculated insertion loss of the stacked switch in Fig. 2.

For small values of r, doubling it will double the insertion loss at low frequencies, while at higher frequencies, feedthrough through capacitor C_{offs} to ground will begin to increase IL further.

The calculation of the isolation of stacked devices is made in a similar fashion as insertion loss. Since the net value of capacitance for the off-leg is proportional to 1/N and the on-value of resistance in the on-leg is proportional to N, Eq. 7 predicts that the isolation of a stacked switch will be insensitive to the number of stacked devices (at least to zero order). Including the effect of N thereby creates:

$$IS = -10 \times LOG_{10}\left[4r^2\omega^2 C_{offs}{}^2 / \left(1+\frac{Nr}{R0}\right)^2 + \frac{\omega^2 C_{offs}{}^2 R0^2}{N^2}\left(1+\frac{2Nr}{R0}\right)^2\right] \qquad (8)$$

for $N_r < 0.R0$, $\omega r C_{onp} < 0.1$

where:

C_{offs} = the capacitance of a single through device in the off-state and r = the resistance of a single shunt device in the on-state.

The Table illustrates that stacking devices and the ability to generate negative onboard voltage sources enables the realization of high-power, high-isolation, and low-insertion loss switches in UTSi technology. With actual packaged parts, inductances and mutual coupling become the limiting factors in isolation and insertion loss. When a part is packaged, care must be taken in order to achieve proper matching, so the final part can approach the theoretical limits of the technology. A balance between target costs and final packaged switch characteristics must be made. However, values that are outlined in the table are more easily realized in highly integrated applications where RF switching is only required between two on-chip locations. In these applications, point- to-point inductances are much smaller than those in wirebonded parts.

The process that is used to build this type of SPST switch lends itself to high levels of integration. Since the process is based on standard CMOS process flows, digital interfaces can be created with little impact on area, design time, or yield. For example, matrix switches that have three-wire serial-to-parallel interfaces are simple to implement, and, when combined with NAND-NAND-type logic, complex control can now be integrated on-chip. SPST switches can be combined into more complex switch functions, including single-pole, double-throw (SPDT) and single-pole, four-throw (SP4T) configurations as shown in **Figs. 3a and b.** Again, digital control with correct digital-to-RF buffering is easily integrated. Gate resistors, which are located near RF switch components, provide excellent isolation. For high-power applications, negative supply generators are integrated by using standard techniques. These techniques require low frequency and low-current oscillators. With proper layout, they are isolated from RF. Sidebands from the negative supply generators are too small to be measured in the laboratory.

The availability of low threshold voltages enables the realization of low-voltage parts in UTSi. For example, switches can operate below +2 VDC with trade-offs in RF characteristics. For +1-VDC applications, onboard voltage triplers can be used to realize the full potential of a switch as shown in the table with a trade-off in chip area. Low-frequency digital interfaces are affected little by low-voltage applications. As RF integrated solutions move toward lower voltages, such as in Bluetooth applications, UTSi switches can still be used with modest trade-offs in performance. MRF

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