PEREGRINE SEMICONDUCTOR

AN4: Application Note

Using the PE3291 in CDMA Applications

Features

- Dual PLL, 1.2 GHz/550 MHz IF capability
- Fractional ratios of 2, 4, 8, 16 or 32
- Fractional spurs typically less than -81 dBc at a step size of 10 or 50 kHz
- Very low operating power
- Standby current typically 5 uA
- 3 wire serial port programming

Introduction

The PE3291 fractional-N PLL is a dual VHF/UHF integrated frequency synthesizer with fractional ratios of 2, 4, 8, 16 and 32. Its low power, low phase noise and low spur content make the part well suited for use in high volume CDMA cellular wireless applications using slotted mode for extended battery life. The PE3291 incorporates a temperature-stable fractional spur compensation scheme to reduce comparison frequency spurious output. FlexiPower™ allows further reductions of power consumption to as little as 4 mW with a dual supply. Serial programming and patented spur compensation techniques make the part as easy to use as an integer-N PLL. The PE3291 contains a 16/17 modulus prescaler (PLL2) and a 32/33 modulus prescaler (PLL1).

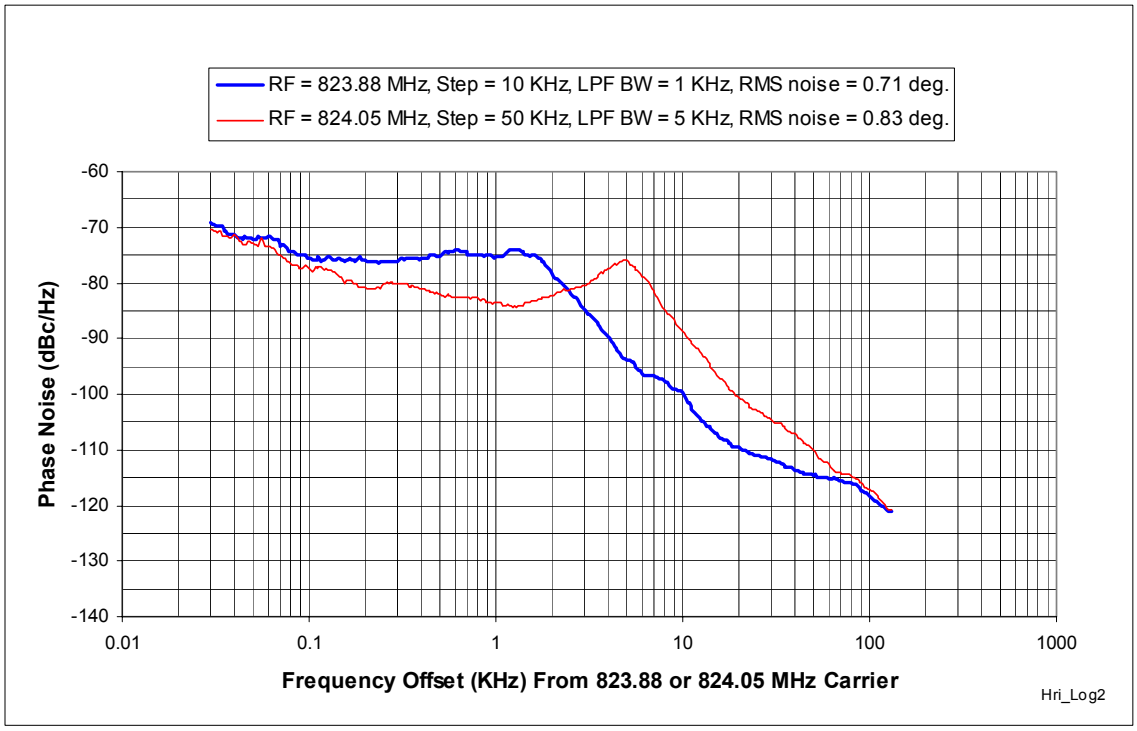
Product Features

- Dual PLL, 1.2 GHz/550 MHz IF capability
- Fractional ratios of 2, 4, 8, 16 or 32
- Fractional spurs typically less than -81 dBc at a step size of 10 or 50 kHz
  - No tuning or adjustment required
  - Stable across voltage, temperature and frequency
- 824 MHz with 10 kHz channel spacing
  - -75 dBc/Hz at 1 kHz offset; less than 0.7 degree integrated phase error
- 824 MHz with 50 kHz channel spacing
  - -83 dBc/Hz at 1 kHz offset
- Very low operating power
  - < 8 mW from a 3-volt supply
  - < 4.0 mW from a 1.0-volt and 3-volt supply
- Standby current typically 5 uA
- 3-wire serial port programming

Improved Phase Noise at Small / Medium Step Size

Improvement of phase noise inside the loop filter bandwidth is achieved using the fractional-N architecture of the PE3291. Standard integer-N PLLs require large values of N for small step sizes at high frequencies, leading to higher phase noise inside the loop. The PE3291 is capable of a maximum division of 524,256. This gives a minimum step size of 2.289 kHz for a 1.2 GHz output. Common step sizes of 10 kHz and 50 kHz for CDMA application are easily obtainable in the 1 GHz region. Figure 1 shows PE3291 phase noise from 10 Hz to 1 MHz offset from 823.88 MHz or 824.05 MHz carrier with a step size 10.08 or 50 kHz, respectively.

Figure 1. PE3291 Phase Noise



As shown in Table 1, the PE3291 performance exceeds the typical CDMA handset requirements:

Table 1. Comparison of PE3291 Performance and CDMA Requirements

	Phase Noise at 1 kHz offset (dBc/Hz)	Spurs (dBc)	Lock up time for a 20 MHz frequency step (ms)	Operating Power (mW)
CDMA Requirement	-70	-80	20	Not available
PE3291 at step 10 kHz	-75	-80	3.8	< 4 mW
PE3291 at step 50 kHz	-83	-80	1.1	< 4 mW

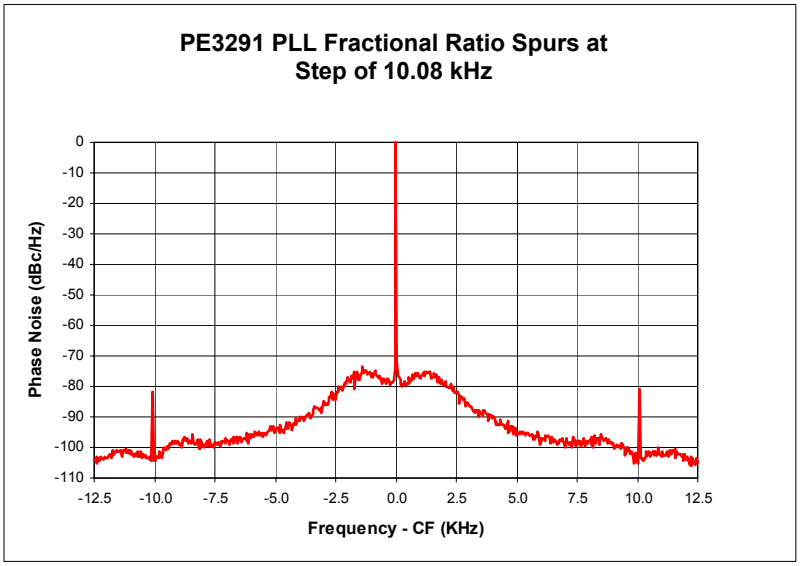
Excellent fractional spurious output suppression that is stable across temperature, voltage, and frequency with no adjustments or tuning.

The PE3291 is generally capable of suppressing fractional spurious outputs to -80 dBc or less at a step of 10 kHz with a 1 kHz bandwidth loop filter, or at a step of 50 kHz with a 5 kHz bandwidth loop filter. Figure 2 shows one example of fractional spurs. Here the center frequency is 823.88 MHz, step 10 kHz, loop filter bandwidth 1 kHz, span 25 kHz, RBW and VBW 10 Hz. As shown in Figure 2, the fractional spurious output is -80 dBc or less.

The classic method of fractional spurious output compensation requires a compensating current to balance the errors in the phase detector. To suppress the fractional spurs by 20 dB requires a balance current that tracks the charge pump error to within 1%. In practice, it is difficult to maintain 1% regulation of a sub nano-ampere current source across temperature and voltage. Also, the calculated current is correct for only one frequency -- a 1% frequency change will result in a 1% balance current error.

The Peregrine PE3291 uses an accumulate and average method to reduce the fractional spurious outputs. The outputs from the charge pump are stored on a 50 pF capacitor (100 pF on the IF side). The stored current on the capacitor is transferred to the loop filter by opening a pass gate each time the fractional accumulator returns to the base state. For a fractional ratio of 32 the pass gate will open after each 32 cycles of the phase detector and the main fractional spur will have an offset of 1/32 of the comparison frequency fc (usually the channel spacing). If the value for F is 2, 6, 10, 14, 18, 22, 26 or 30, the resulting fractional ratio will be 16 and the main spur will be at an offset of fc/16. For F = 4, 12, 20 or 28, fractional ratio will be 8. For F= 8 or 24, fractional ratio is 4. Fractional ratio is 2 for F=16.

Figure 2. PE3291 PLL 1 Fractional Ratio Spurs at Step of 10.08 kHz



Industry leading low power consumption (PE3291) and even lower power consumption (FlexiPower ®)

The PE3291 uses a typical power of 6.3 mW when operating at the maximum speed on PLL1 (RF at 950 MHz, IF at 300 MHz). Power consumption drops even further when the speed is reduced. The internal biasing is controlled by the programming software.

The PE3291 can further reduce power consumption if an external voltage is used to supply the prescalers. Typical operation (RF at 950 MHz, IF at 550 MHz) can be achieved on 5.8 mW, while reduced speed operation (RF at 450 MHz, IF at 300 MHz) uses 3.9 mW.

The ability to run at reduced power consumption with lower synthesized LO frequencies may lead to a preference for low side injection architectures.

Design Considerations

When designing for best phase noise the preferred choice of fractional ratio is the highest practical value. This tends to lead to high comparison frequencies.

As an example, a 10 kHz step size has a 320 kHz comparison frequency as the preferred choice. This may lead to restrictions in the choice of reference frequency. The 30, 15, 10, 7.5, 6 and 3 kHz series of channel spacings come from a 960 kHz comparison frequency or integer division of 960 kHz. The 25, 12.5, 6.25, and 3.125 kHz channel spacings come from an 800 kHz comparison frequency. Reference frequencies which are a multiple of 4.8 MHz allow access to both series of comparison frequency (14.4 and 19.2 MHz are the most common ones).

The minimum value of N may become a limiting factor for some of the larger channel spacings used in CDMA (i.e. 50 kHz). Values of N less than 1024 for PLL1 (256 for PLL2) may not be achievable. This is due both to the use of fractional ratio and to the 32/33 prescaler used in the RF main divider chain (16/17 in the IF chain). As an example, when using an 800 kHz comparison frequency with 25 kHz steps, the lowest frequency before missing steps appear is 819.2 MHz. Between 818.4 MHz and 819.2 MHz none of the fractional values of N can be accessed.

Loop filter considerations

The loop filter components can be calculated using the standard PLL loop filter equations for either second-order or third-order passive loop filters driven by a charge pump. These equations available on Peregrine's website at www.peregrine-semi.com (click on the Loop Filter Calc Button under the PE3291 product page). Note that the comparison frequency and the channel spacing are not the same in a fractional-N PLL. The proper number to use in the equations is the comparison frequency, as this determines how often the charge pump adds current to the averaging capacitor and thus sets the rate at which the charge pump drives the loop filter.

The channel spacing is determined by the comparison frequency divided by the fractional ratio. An 800 kHz comparison frequency and a fractional ratio of 32 give a step size of 25 kHz. The step size is the proper number to use in choosing the loop filter bandwidth. It sets how often the integrating capacitor charge is output to the loop filter and how long the delay is between loop phase error detection and the corrective output to the loop filter. For best stability the loop filter bandwidth should be a maximum of 10% of the step size. For a 25 kHz step size this would be a 2.5 kHz loop natural frequency.

Lock-up time

The lock-up time is a function of frequency step, loop filter bandwidth, quality of capacitors in the loop filter, and sensitivity of VCO. Temperature-stable, high-Q capacitors should be used in the loop filter. A high gain VCO usually has a faster lock time, as well as higher phase noise. The PE3291 has lock times comparable to other standard integer-N PLLs used with the same step size. When designing for best lock time, use the widest loop bandwidth practical. In general, a loop bandwidth that is 20% of the step size is about the maximum that is practical while maintaining acceptable loop stability. F=1 will yield the slowest lock times, and is also a worst-case condition for fractional spurious output amplitude. Setting the increment value of the fractional accumulator to 1 implements the full fractional ratio of 32. Setting the fractional ratio to 16 (F=2, 6, 10, 14, 18, 22, 26 or 30) will double the stability by halving the time between fractional spur suppression integrator cycles.

When designing for best lock time, Peregrine finds that the second-order loop filter gives the best results. When there is a difficult combined specification for both lock time and spurious outputs, a third-order filter may lead to the best solution.

Figures 3 and 4 show PE3291 PLL1 lock time of 20 MHz frequency shift from 814.2 to 834.2 MHz with step 10.08 kHz and loop filter bandwidth 1 kHz, in a coarse and fine frequency scale, respectively. The lock time from 814.2 MHz to within 1 kHz of 834.2 MHz was 3.82 ms. Figures 5 and 6 show the same 20 MHz frequency shift from 814.05 MHz to 834.05 MHz, but with step size of 50 kHz and loop filter bandwidth 5 kHz. The lock time was decreased to 1.1 ms.

VCO considerations

The PE3291 is a 3-volt device. Available control voltage from the device is 0.5 to 2.5 volts. VCOs requiring higher tuning voltage may be used, but the upper limit of the tuning range will be reduced unless an active filter (op-amp) with wider range is incorporated into the loop. In general, use the narrowest practical tuning range which meets the output frequency requirements of the system. The resulting lower VCO gain (KVCO) will result in lower conversion of charge pump current to spurious frequency output from the VCO. The lower tuning range VCO will also generally have a higher operating Q factor, and contribute less phase noise to the total frequency synthesizer output.

Figure 3. PE3291 PLL 1 Lock Time in 10 kHz Step and 1 kHz Loop Filter Bandwidth

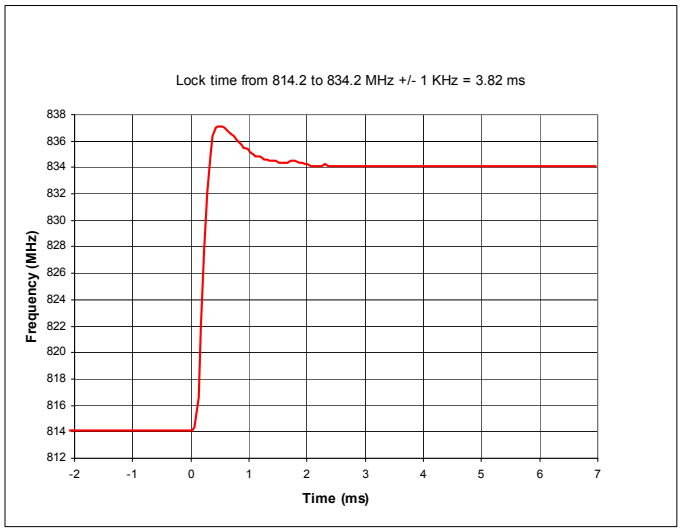


Figure 4. PE3291 PLL 1 Lock Time in 10 kHz Step and 1 kHz Loop Filter Bandwidth in Fin Frequency Scale

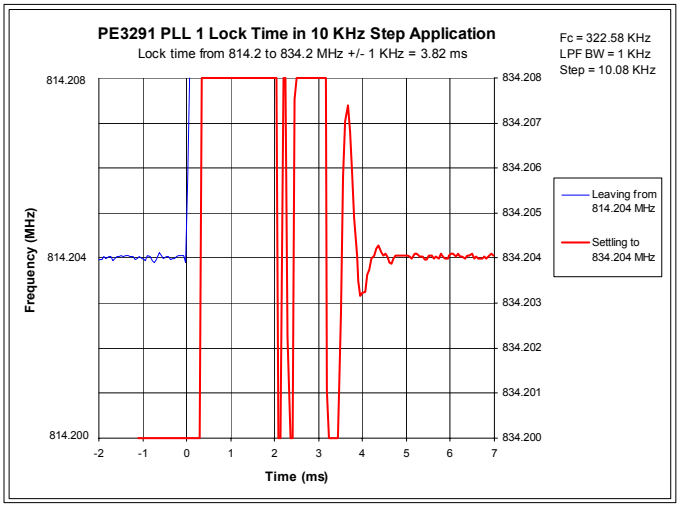


Figure 5. PE3291 PLL 1 Lock Time in 50 kHz Step and 5 kHz Loop Filter Bandwidth

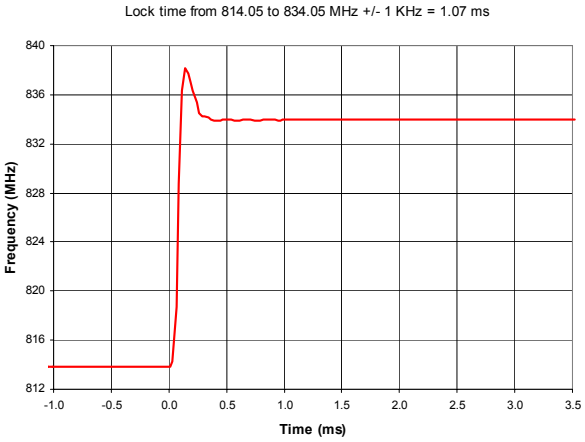
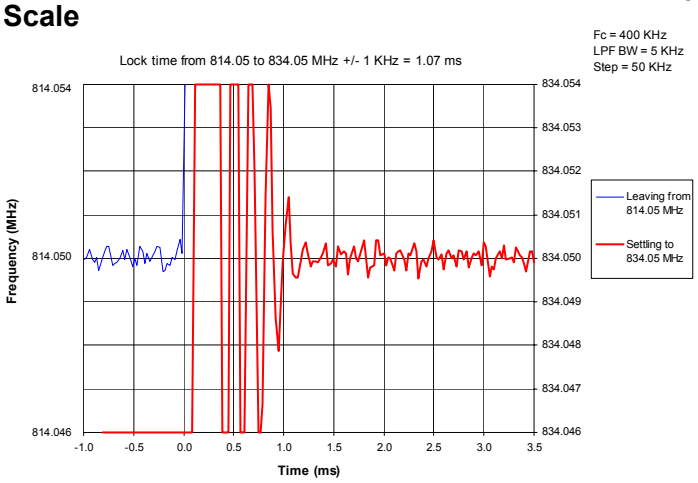


Figure 6. PE3291 PLL 1 Lock Time in 50 kHz Step and 5 kHz Loop Filter Bandwidth in Fin Frequency Scale



Minimizing Power Consumption

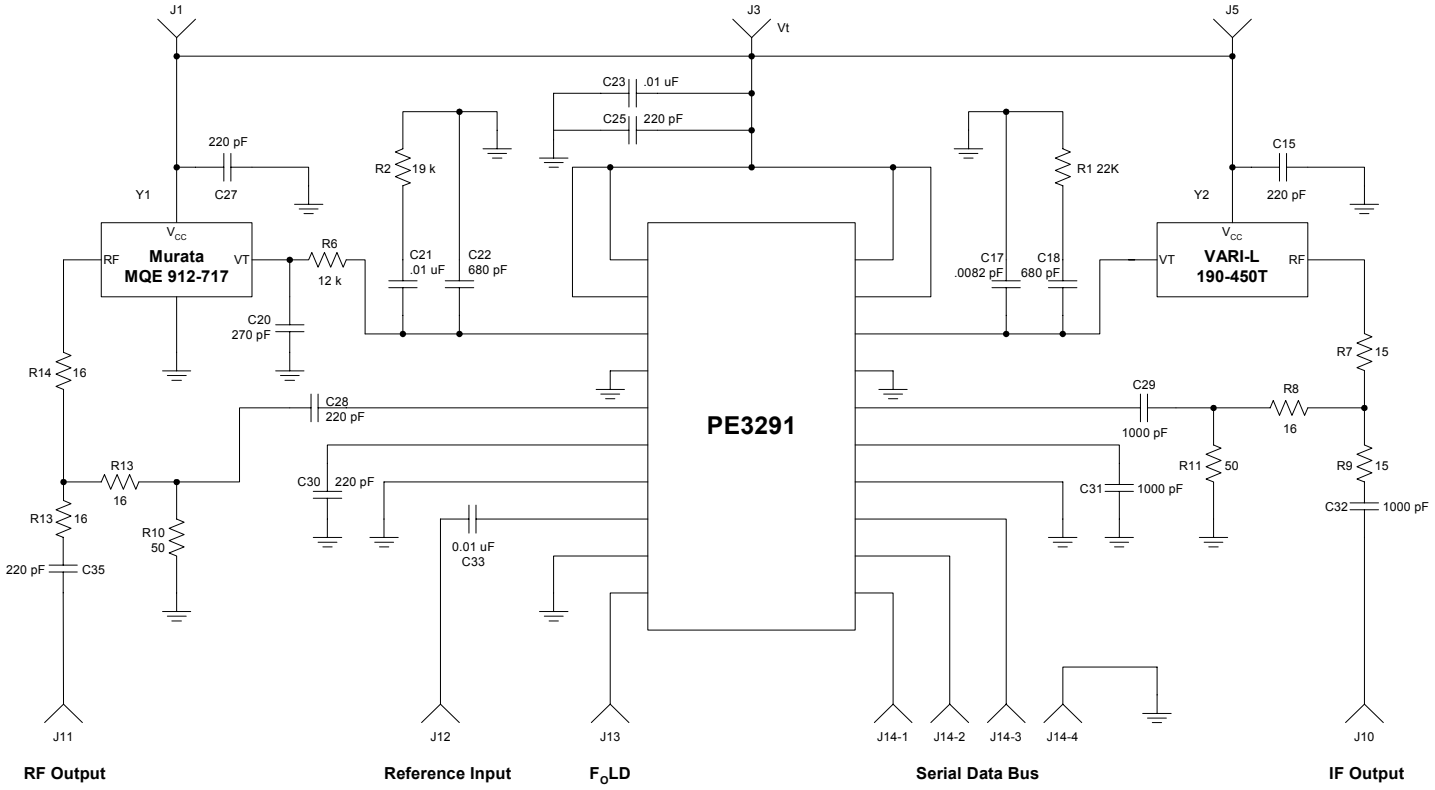
Programmable biasing and external access to the prescaler power supply points have been incorporated into the PE3291 to allow the user maximum flexibility in reducing the total power consumption of the device within the limits of meeting the requirements of the system. When working with a single 3-volt supply, the current consumption can be reduced if the RF frequency is below 700 MHz, or the IF frequency is below 300 MHz, by using the software commands to set one or both PLLs to low power. When multiple voltages are available, further power reduction is possible by custom tuning the current usage to the required frequency by reducing the voltage that supplies the prescaler.

The data sheet example shows a 900 MHz/300 MHz output using 9.9 mW (PLL1 high power, PLL2 low power). Using a 1.8-volt external supply reduces the power consumption to 7.9 mW. If the frequency requirement is reduced to 700 MHz/300 MHz the device will use 7.5 mW from a single 3-volt supply (low power/low power) or 5.5 mW from a split 3.0-volt / 1.4-volt supply.

Programming the PE3291

The PE3291 is programmed via a 3-wire serial bus using 3 volt CMOS logic levels. If a 5-volt microprocessor is used as the program source, an appropriate resistive voltage divider can be used as a level shifter. The Data, Clock and Enable pins are CMOS inputs. Pull-down resistors are recommended on these high impedance inputs if the driving microprocessor cannot provide a continuous pull-down on the programming lines. The Enable line is particularly critical, as a glitch on this line will reload a data buffer.

Figure 7. Schematic Diagram



The example circuit of Figure 7 has the following specifications and performance:

- Y1 = Murata MQE001-836
- KVCO = 12 MHz/V
- Output Frequency = 824 MHz
- Comparison Frequency = 320 kHz
- Channel Spacing = 10 kHz (fractional ratio = 16)
- Loop Filter =
    - kHz Loop natural frequency
    - Third-order loop filter
    - 2 dB third-order section
    - 55 degrees phase margin
- Phase Noise = -75 dBc/Hz at 500 kHz offset (Figure 1)
- Fractional Spur = -81 dBc at 10 kHz offset (Figure 2)
- Lock Time = less than 4 ms to within 1 kHz (Figures 3 and 4)

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