PEREGRINE SEMICONDUCTOR

AN12: Application Note

Design Considerations for Using the PE323x/PE333x in Fractional-N or Sigma-Delta Designs

Features

- Excellent phase noise performance
- Excellent spurious noise performance
- Dual-latch architecture

Introduction

It has been demonstrated in various performance-critical applications that the PE323x and PE333x devices exhibit exceptionally good phase noise and spurious signal suppression. This fact, combined with their dual-latch architecture that enables ping-pong loading of the main divide counter, makes these PLLs well suited as the core for fractional-N or sigma-delta implementation. This application note addresses several issues key to a successful design in these types of applications.

During the design of the PE323x and PE333x PLL cores, emphasis was placed on maximizing frequency performance while maintaining the strong phase noise and spurious noise performance of the devices. Due to this design optimization for integer-N operation, the usable counter values and ranges for fractional-N or sigma-delta applications were affected.

Using standard integer-N synthesis, the A-counter is only limited by A= (0-15), and A≤ M+1. However, in order to have seamless operation in fractional-N or sigma-delta operation, the A-counter cannot equal 0 at any time. This limitation is due to a design optimization of the A-counter to increase the overall speed of the PLL. When the A-count changes to or from “0” to another count value, there is an additional timing delay of one comparison cycle. This can cause the device to give inconsistent results, and in some cases will cause the PLL to fail to lock in fractional-N or sigma-delta designs.

One way to overcome this A-counter limitation is to re-map the M and A count values. For example, if M=10, and A=0, the same output frequency can be programmed using M=9 and A=10. As long as all other counter rules are observed, the M-counter can be decremented by one and the A-count changed from 0 to 10 to synthesize the same frequency.

In addition to the limitation that A≠0 and A≤M+1 in a fractional-N or sigma-delta application, there is also a change to the minimum total N count of the PLL. In order to obtain contiguous channels of operation, N must be greater than 100 (N≥101) based upon the equation N= 10(M+1) +A.

Table 1. PE323x/333x Valid Counter Ranges for Fractional Operation

Interface Mode	A–Counter	R–Counter	M–Counter	Total N–Count
Parallel	1≤A≤10	0≤R≤63	9≤M≤511	101≤N≤5130
Serial	1≤A≤10	0≤R≤63	9≤M≤511	101≤N≤5130
Direct	1≤A≤10	0≤R≤15	9≤M≤127	101≤N≤1290

Sales Offices

United States

Peregrine Semiconductor Corp.
6175 Nancy Ridge Drive
San Diego, CA 92121
Tel 1-858-455-0660
Fax 1-858-455-0770

Japan

Peregrine Semiconductor K.K.
5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: 03-3507-5755
Fax: 03-3507-5601

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches
Tel 33-1-47-41-91-73
Fax 33-1-47-41-91-73

Australia

Peregrine Semiconductor Australia
8 Herb Elliot Ave.
Homebush, NSW 2140
Australia
Tel: 011-61-2-9763-4111
Fax: 011-61-2-9746-1501

For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

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