



PE4305

50 Ω RF Digital Attenuator
5-bit, 15.5 dB, DC – 4.0 GHz

Features

- Attenuation: 0.5 dB steps to 15.5 dB
- Flexible parallel and serial programming interfaces
- Latched or direct mode
- Unique power-up state selection
- Positive CMOS control logic
- High attenuation accuracy and linearity over temperature and frequency
- Very low power consumption
- Single-supply operation
- 50 Ω impedance
- Pin compatible with PE430x series
- Packaged in a 20 Lead 4x4 mm QFN

Product Description

The PE4305 is a high linearity, 5-bit RF Digital Step Attenuator (DSA) covering a 15.5 dB attenuation range in 0.5 dB steps, and is pin compatible with the PE430x series. This 50-ohm RF DSA provides both parallel (latched or direct mode) and serial CMOS control interface, operates on a single 3-volt supply and maintains high attenuation accuracy over frequency and temperature. It also has a unique control interface that allows the user to select an initial attenuation state at power-up. The PE4305 exhibits very low insertion loss and low power consumption. This functionality is delivered in a 4x4 mm QFN footprint.

The PE4305 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram

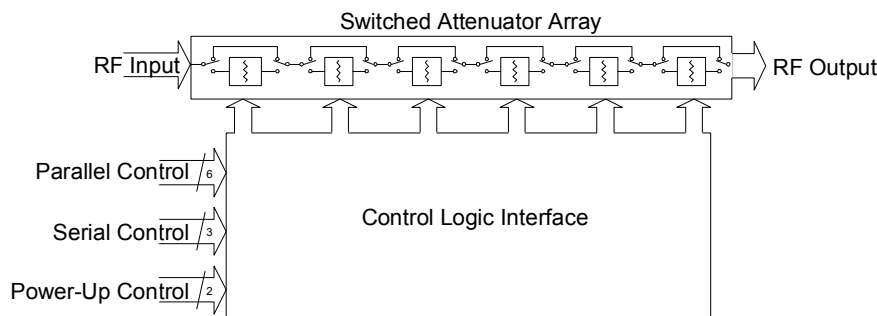


Figure 2. Package Type

4x4 mm 20-Lead QFN



Table 1. Electrical Specifications @ +25°C, V_{DD} = 3.0 V

Parameter	Test Conditions	Frequency	Minimum	Typical	Maximum	Units
Operation Frequency			DC		4000	MHz
Insertion Loss ²		DC - 2.2 GHz	-	1.5	2.25	dB
Attenuation Accuracy	Any Bit or Bit Combination	DC - 2.2 GHz	-	-	±(0.25 + 3% of atten setting) not to exceed ± 0.4 dB	dB
1 dB Compression ³		1 MHz - 2.2 GHz	30	34	-	dBm
Input IP ₃ ^{1,2}	Two-tone inputs +18 dBm	1 MHz - 2.2 GHz	-	52	-	dBm
Return Loss		DC - 2.2 GHz	15	20	-	dB
Switching Speed	50% control to 0.5 dB of final value		-	-	1	μs

Notes: 1. Device Linearity will begin to degrade below 1Mhz

2. See Max input rating in Table 3 & Figures on Pages 2 to 4 for data across frequency.

3. Note Absolute Maximum in Table 3.

Typical Performance Data @ 25°C, V_{DD} = 3.0 V

Figure 3. Insertion Loss

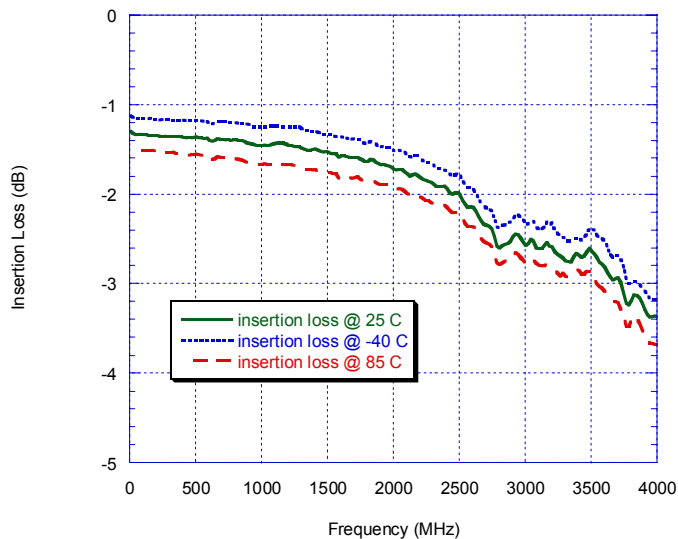


Figure 4. Attenuation at Major steps

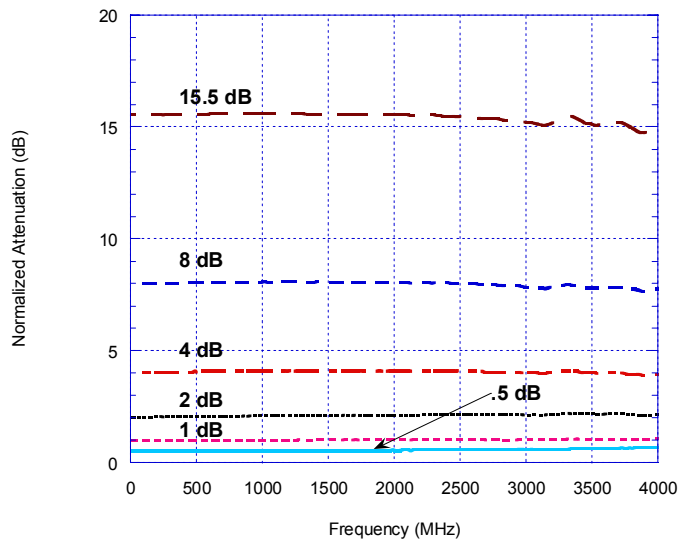


Figure 5. Input Return Loss at Major Attenuation Steps

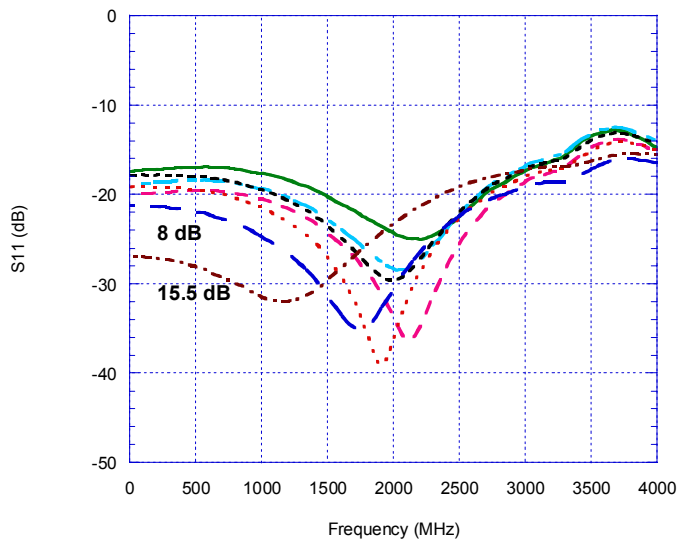
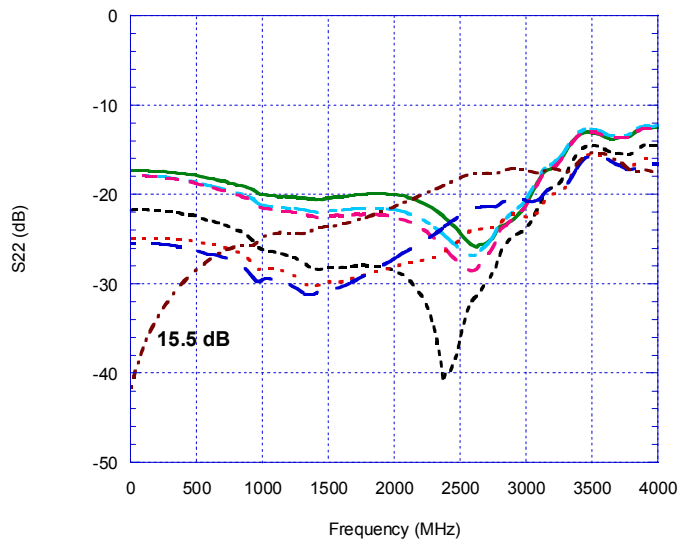


Figure 6. Output Return Loss at Major Attenuation Steps



Typical Performance Data @ 25°C, V_{DD} = 3.0 V

Figure 7. Attenuation Error Vs. Frequency

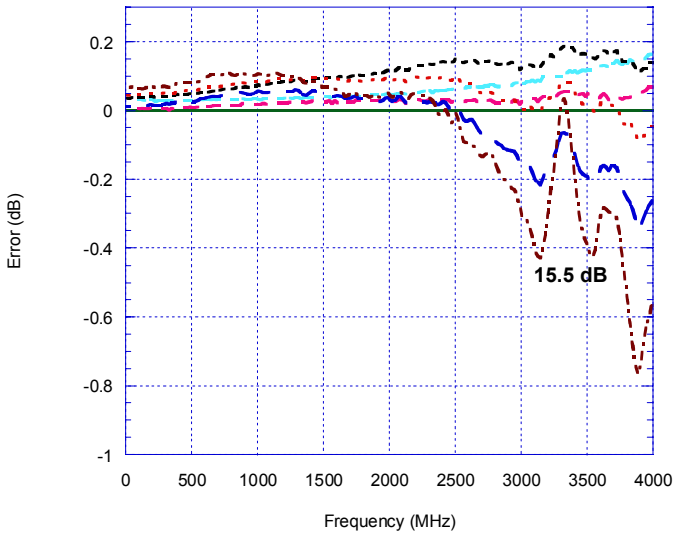


Figure 8. Attenuation Error Vs. Attenuation Setting at 10 MHz and 510 MHz

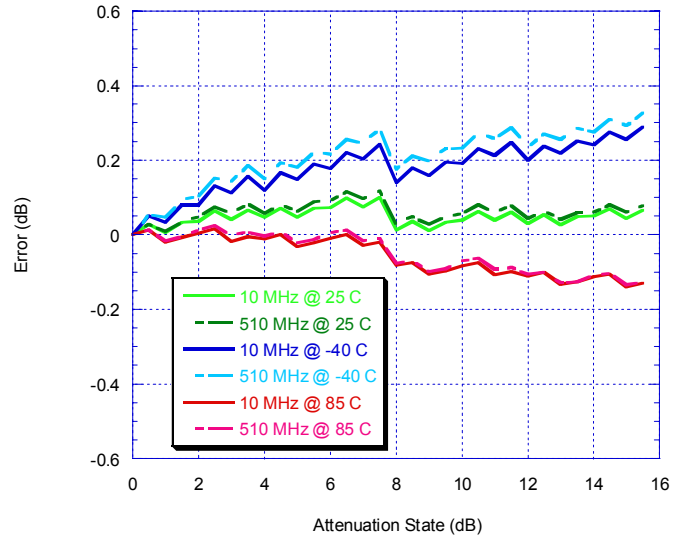


Figure 9. Attenuation Error Vs. Attenuation Setting 1010 MHz and 1210 MHz

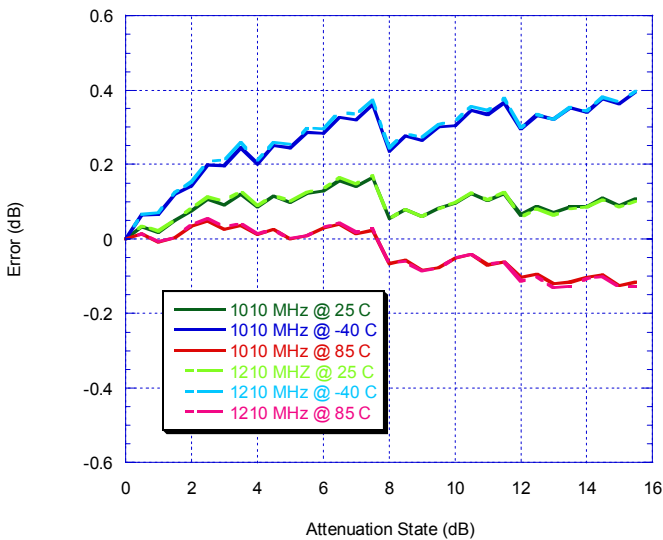
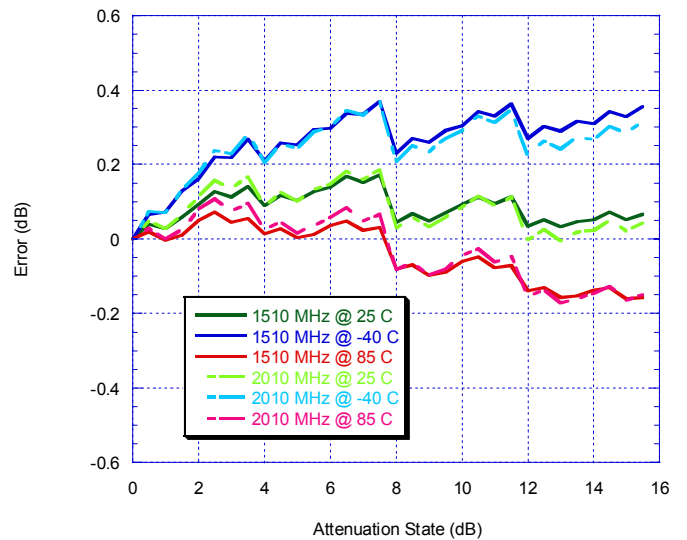


Figure 10. Attenuation Error Vs. Attenuation Setting at 1510 MHz and 2010 MHz



Note: Positive attenuation error indicates higher attenuation than target value

Typical Performance Data @ 25°C, V_{DD} = 3.0 V

Figure 11. Attenuation Error vs. Attenuation Setting at 2010 MHz and 2510 MHz

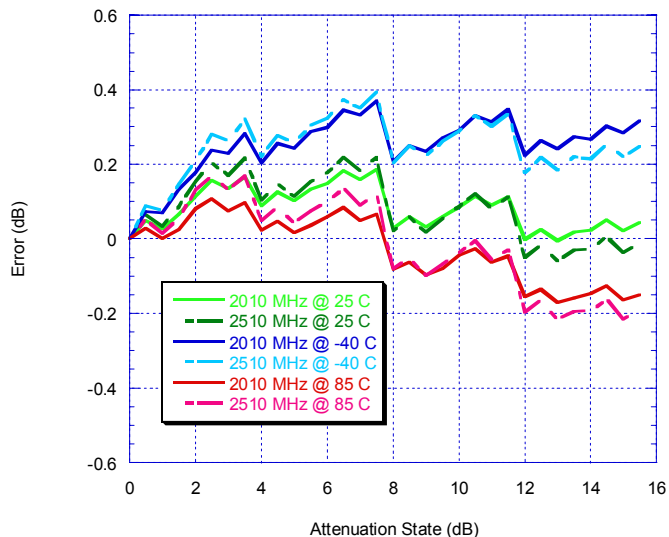


Figure 12. 1 dB Compression vs. Frequency

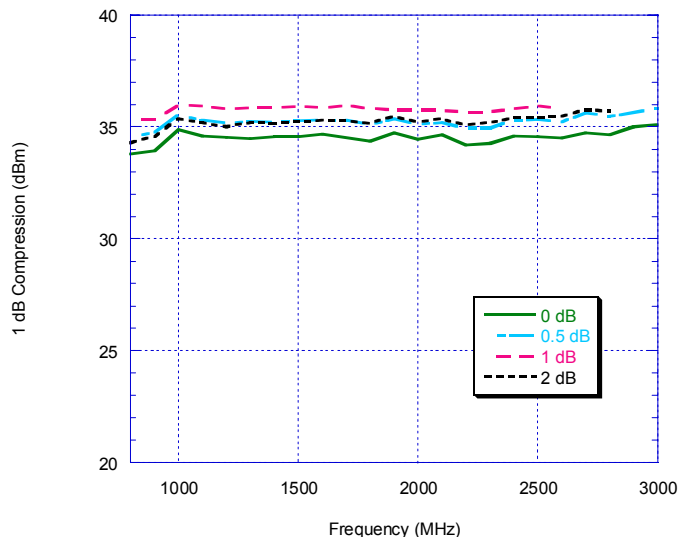
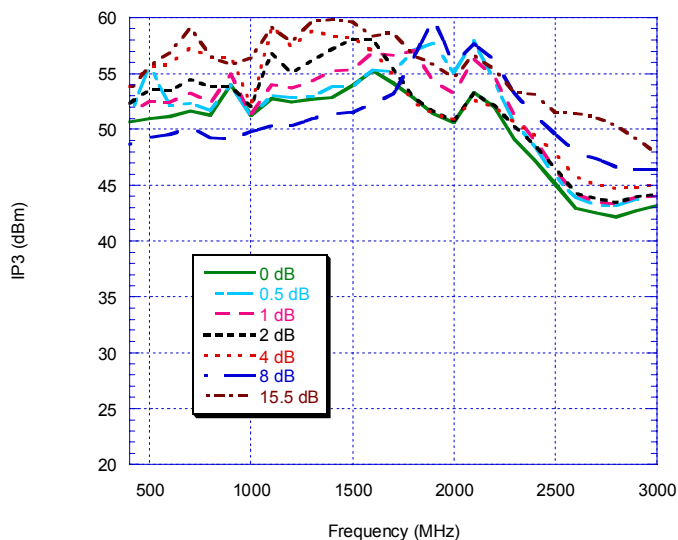


Figure 13. Input IP3 vs. Frequency



Note: Positive attenuation error indicates higher attenuation than target value

Figure 14. Pin Configuration (Top View)

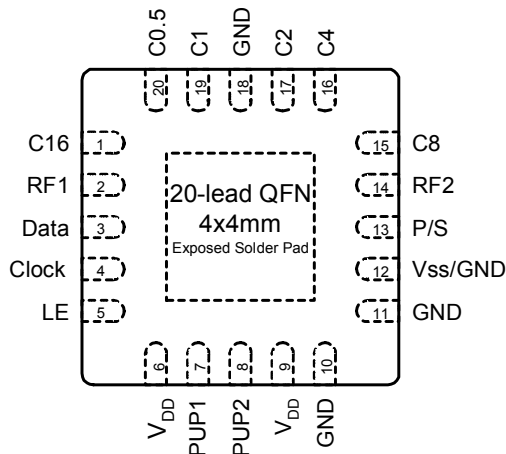


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	N/C	No connect. Can be connected to any bias.
2	RF1	RF port (Note 1).
3	Data	Serial interface data input (Note 4).
4	Clock	Serial interface clock input.
5	LE	Latch Enable input (Note 2).
6	V _{DD}	Power supply pin.
7	N/C	No connect. Can be connected to any bias.
8	PUP2	Power-up selection bit.
9	V _{DD}	Power supply pin.
10	GND	Ground connection.
11	GND	Ground connection.
12	V _{ss} /GND	Negative supply voltage or GND connection (Note 3)
13	P/S	Parallel/Serial mode select.
14	RF2	RF port (Note 1).
15	C8	Attenuation control bit, 8 dB.
16	C4	Attenuation control bit, 4 dB.
17	C2	Attenuation control bit, 2 dB.
18	GND	Ground connection.
19	C1	Attenuation control bit, 1 dB.
20	C0.5	Attenuation control bit, 0.5 dB.
Paddle	GND	Ground for proper operation

Note 1: Both RF ports must be held at 0 VDC or DC blocked with an external series capacitor.

2: Latch Enable (LE) has an internal 100 kΩ resistor to VDD.

3: Connect pin 12 to GND to enable internal negative voltage generator. Connect pin 12 to VSS (-VDD) to bypass and disable internal negative voltage generator.

4: Place a 10 kΩ resistor in series, as close to pin as possible to avoid frequency resonance. See "Resistor on Pin 3" paragraph.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V _{DD}	Power supply voltage	-0.3	4.0	V
V _I	Voltage on any input	-0.3	V _{DD} +0.3	V
T _{ST}	Storage temperature range	-65	150	°C
P _{IN}	Input power (50Ω)		+30	dBm
V _{ESD}	ESD voltage (Human Body Model)		500	V

Table 4. Operating Ranges

Parameter	Min	Typ	Max	Units
V _{DD} Power Supply Voltage	2.7	3.0	3.3	V
I _{DD} Power Supply Current			100	μA
Digital Input High	0.7xV _{DD}			V
Digital Input Low			0.3xV _{DD}	V
Digital Input Leakage			1	μA
Input Power			+24	dBm
Temperature range	-40		85	°C

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rate specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Switching Frequency

The PE4305 has a maximum 25 kHz switching rate.

Resistor on Pin 3

A 10 kΩ resistor on the input to Pin 3 (see Figure 16) will eliminate package resonance between the RF input pin and the digital input. Specified attenuation error versus frequency performance is dependent upon this condition.

Programming Options

Parallel/Serial Selection

Either a parallel or serial interface can be used to control the PE4305. The P/S bit provides this selection, with P/S=LOW selecting the parallel interface and P/S=HIGH selecting the serial interface.

Parallel / Direct Mode Interface

The parallel interface consists of five CMOS-compatible control lines that select the desired attenuation state, as shown in Table 5.

The parallel interface timing requirements are defined by Figure 18 (Parallel Interface Timing Diagram), Table 9 (Parallel Interface AC Characteristics), and switching speed (Table 1).

For parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per Figure 18) to latch new attenuation state into device.

For direct programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct Mode is ideal for manual control of the device (using hardware, switches, or jumpers).

Table 5. Truth Table

P/S	C8	C4	C2	C1	C0.5	Attenuation State
0	0	0	0	0	0	Reference Loss
0	0	0	0	0	1	0.5 dB
0	0	0	0	1	0	1 dB
0	0	0	1	0	0	2 dB
0	0	1	0	0	0	4 dB
0	1	0	0	0	0	8 dB
0	1	1	1	1	1	15.5 dB

Note: Not all 32 possible combinations of C0.5-C8 are shown in table

Serial Interface

The PE4305's serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. The latch is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be

serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The start bit (B5) of the data should always be low to prevent an unknown state in the device. The timing for this operation is defined by Figure 17 (Serial Interface Timing Diagram) and Table 8 (Serial Interface AC Characteristics).

Power-up Control Settings

The PE4305 always assumes a specifiable attenuation setting on power-up. This feature exists for both the Serial and Parallel modes of operation, and allows a known attenuation state to be established before an initial serial or parallel control word is provided.

When the attenuator powers up in Serial mode (P/S=1), the five control bits are set to whatever data is present on the five parallel data inputs (C0.5 to C8). This allows any one of the 32 attenuation settings to be specified as the power-up state.

When the attenuator powers up in Parallel mode (P/S=0) with LE=0, the control bits are automatically set to one of two possible values. These two values are selected by the power-up control bit, PUP2, as shown in Table 6 (Power-Up Truth Table, Parallel Mode).

Table 6. Power-Up Truth Table, Parallel Interface Mode

P/S	LE	PUP2	Attenuation State
0	0	0	Reference Loss
0	0	1	8 dB
0	1	X	Defined by C0.5-C8

Note: Power up with LE=1 provides normal parallel operation with C0.5-C8, and PUP2 is not active

Evaluation Kit

The Digital Attenuator Evaluation Kit board was designed to ease customer evaluation of the PE4305 DSA.

J9 is used in conjunction with the supplied DC cable to supply VDD, GND, and -VDD. If use of the internal negative voltage generator is desired, then connect -VDD (black banana plug) to ground. If an external -VDD is desired, then apply -3V.

J1 should be connected to the LPT1 port of a PC with the supplied control cable. The evaluation software is written to operate the DSA in serial mode, so switch 7 (P/S) on the DIP switch SW1 should be ON with all other switches off. Using the software, enable or disable each attenuation setting to the desired combined attenuation. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

To evaluate the Power Up options, first disconnect the control cable from the evaluation board. The control cable must be removed to prevent the PC port from biasing the control pins.

During power up with P/S=1 high and LE=0 or P/S=0 low and LE=1, the default power-up signal attenuation is set to the value present on the five control bits on the five parallel data inputs (C0.5 to C8). This allows any one of the 32 attenuation settings to be specified as the power-up state.

During power up with P/S=0 high and LE=0, the control bits are automatically set to one of two possible values presented through the PUP interface. These two values are selected by the power-up control bit, PUP2, as shown in Table 6. Pins 1 and 7 are open and may be connected to any bias.

Resistor on Pin 3

A 10 kΩ resistor on the input to pin 3 (Figure 16) will eliminate package resonance between the RF input pin and the digital input. Specified attenuation error versus frequency performance is dependent upon this condition.

Figure 15. Evaluation Board Layout

Peregrine Specification 101/0112

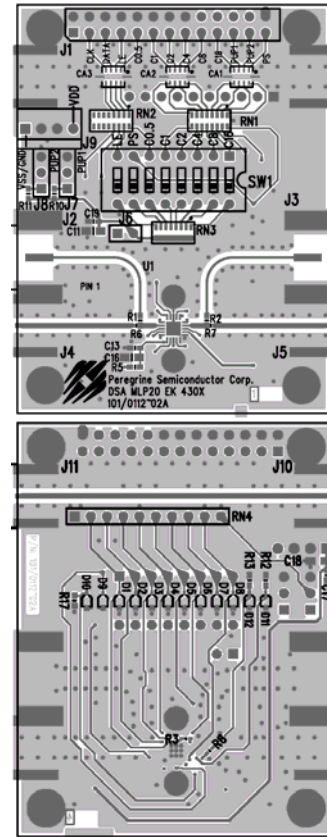
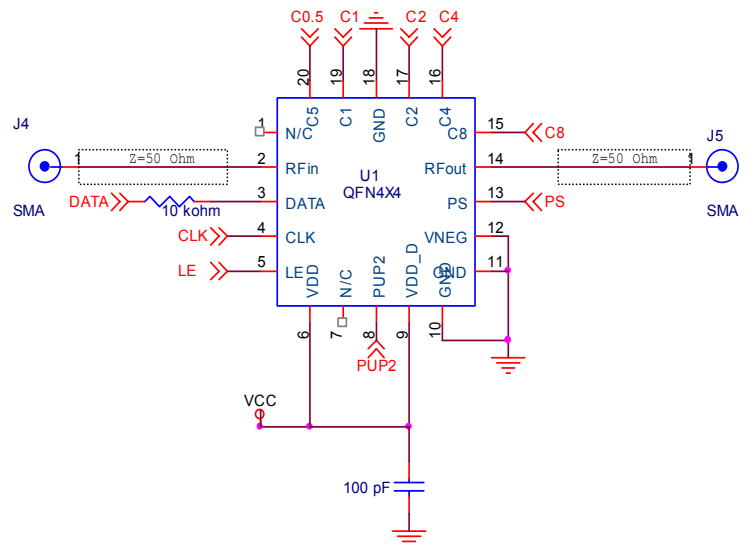


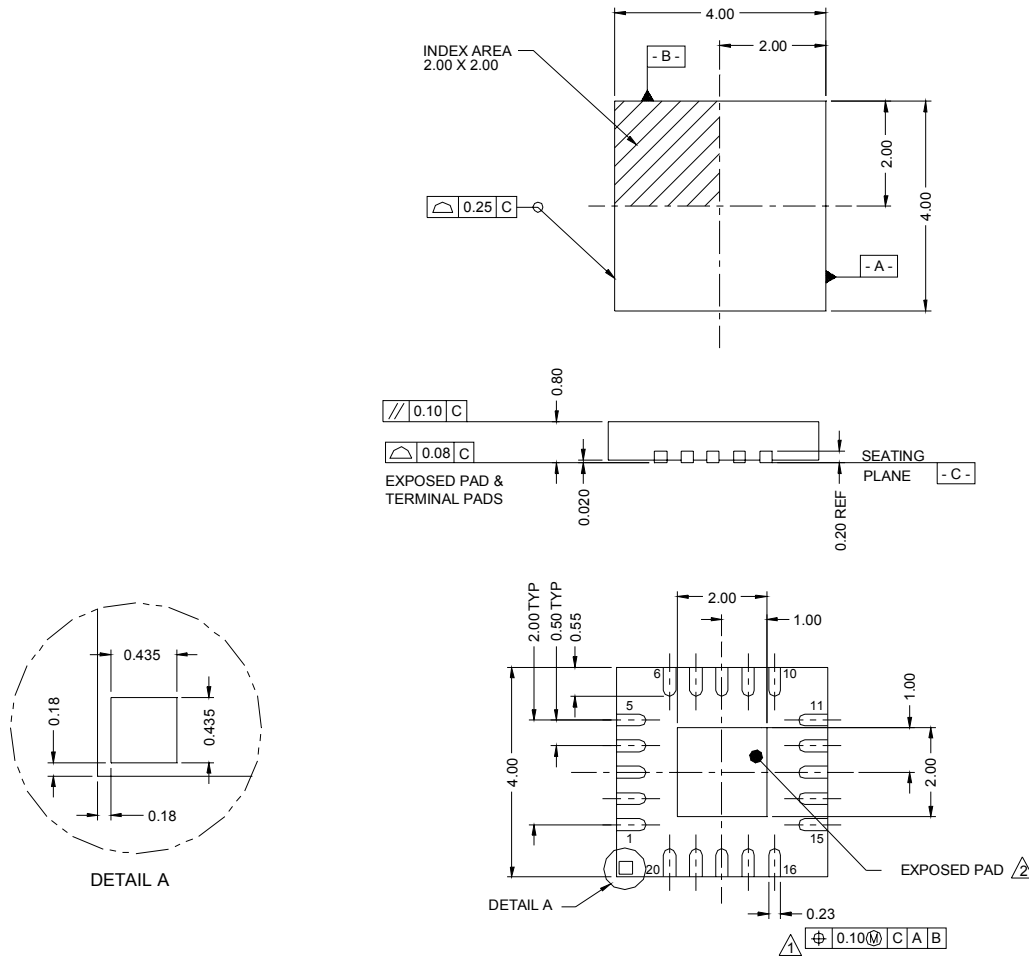
Figure 16. Evaluation Board Schematic

Peregrine Specification 102/0144



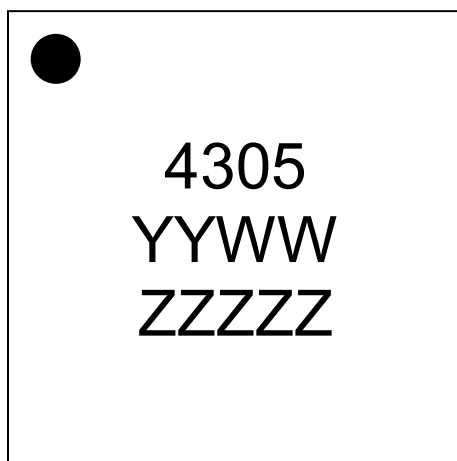
Note: Resistor on pin 3 is required and should be placed as close to the part as possible to avoid package resonance and meet error specifications over frequency.

Figure 19. Package Drawing



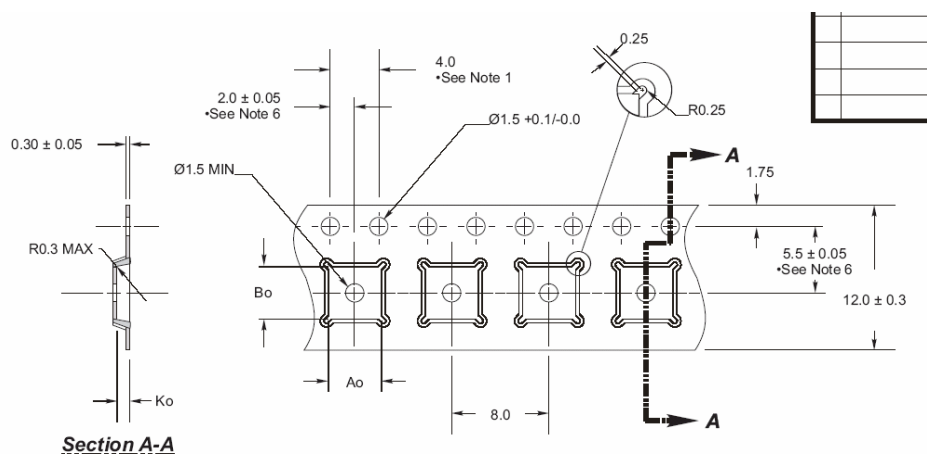
1. Dimension applies to metallized terminal and is measured between 0.25 and 0.30 from terminal tip.
2. Coplanarity applies to the exposed heat sink slug as well as the terminals.
3. Dimensions are in millimeters.

Figure 20. Marking Specifications



YYWW = Date Code
ZZZZZ = Last five digits of PSC Lot Number

Figure 21. Tape and Reel Drawing



Ao = 4.35 mm
Bo = 4.35 mm
Ko = 1.1 mm

- Notes:
1. 10 sprocket hole pitch cumulative tolerance ± 0.2 .
 2. Camber not to exceed 1mm in 100mm.
 3. Material: PS + C.
 4. Ao and Bo measured as indicated.
 5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
 6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Table 10. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4305-01	4305	PE4305-20MLP 4x4mm-75A	20-lead 4x4mm QFN	75 units / Tube
4305-02	4305	PE4305-20MLP 4x4mm-3000C	20-lead 4x4mm QFN	3000 units / T&R
4305-00	PE4305-EK	PE4305-20MLP 4x4mm-EK	Evaluation Kit	1 / Box
4305-51	4305	PE4305G-20MLP 4x4mm-75A	Green 20-lead 4x4mm QFN	75 units / Tube
4305-52	4305	PE4305G-20MLP 4x4mm-3000C	Green 20-lead 4x4mm QFN	3000 units / T&R

Sales Offices

The Americas

Peregrine Semiconductor Corporation

9450 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe

Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-4741-9173
Fax : +33-1-4741-9173

Space and Defense Products

Americas:

Tel: 858-731-9453

Europe, Asia Pacific:

180 Rue Jean de Guiramand
13852 Aix-En-Provence Cedex 3, France
Tel: +33-4-4239-3361
Fax: +33-4-4239-7227

North Asia Pacific

Peregrine Semiconductor K.K.

Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

Peregrine Semiconductor, Korea

#B-2402, Kolon Tripolis, #210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-480 S. Korea
Tel: +82-31-728-4300
Fax: +82-31-728-4305

South Asia Pacific

Peregrine Semiconductor, China

Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

For a list of representatives in your area, please refer to our Web site at: www.psemi.com

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS and HaRP are trademarks of Peregrine Semiconductor Corp.

SUNSTAR 商斯达实业集团是集研发、生产、工程、销售、代理经销、技术咨询、信息服务等为一体的高科技企业，是专业高科技电子产品生产厂家，是具有 10 多年历史的专业电子元器件供应商，是中国最早和最大的仓储式连锁规模经营大型综合电子零部件代理分销商之一，是一家专业代理和分销世界各大品牌 IC 芯片和电子元器件的连锁经营综合性国际公司，专业经营进口、国产名厂名牌电子元件，型号、种类齐全。在香港、北京、深圳、上海、西安、成都等全国主要电子市场设有直属分公司和产品展示展销窗口门市部专卖店及代理分销商，已在全国范围内建成强大统一的供货和代理分销网络。我们专业代理经销、开发生产电子元器件、集成电路、传感器、微波光电元器件、工控机/DOC/DOM 电子盘、专用电路、单片机开发、MCU/DSP/ARM/FPGA 软件硬件、二极管、三极管、模块等，是您可靠的一站式现货配套供应商、方案提供商、部件功能模块开发配套商。商斯达实业公司拥有庞大的资料库，有数位毕业于著名高校——有中国电子工业摇篮之称的西安电子科技大学（西军电）并长期从事国防尖端科技研究的高级工程师为您精挑细选、量身订做各种高科技电子元器件，并解决各种技术问题。

微波光电部专业代理经销高频、微波、光纤、光电元器件、组件、部件、模块、整机；电磁兼容元器件、材料、设备；微波 CAD、EDA 软件、开发测试仿真工具；微波、光纤仪器仪表。欢迎国外高科技微波、光纤厂商将优秀产品介绍到中国、共同开拓市场。长期大量现货专业批发高频、微波、卫星、光纤、电视、CATV 器件：晶振、VCO、连接器、PIN 开关、变容二极管、开关二极管、低噪晶体管、功率电阻及电容、放大器、功率管、MMIC、混频器、耦合器、功分器、振荡器、合成器、衰减器、滤波器、隔离器、环行器、移相器、调制解调器；光电子器件和组件：红外发射管、红外接收管、光电开关、光敏管、发光二极管和发光二极管组件、半导体激光二极管和激光器组件、光电探测器和光接收组件、光发射接收模块、光纤激光器和光放大器、光调制器、光开关、DWDM 用光发射和接收器件、用户接入系统光收发器件与模块、光纤连接器、光纤跳线/尾纤、光衰减器、光纤适配器、光隔离器、光耦合器、光环行器、光复用器/转换器；无线收发芯片和模组、蓝牙芯片和模组。

更多产品请看本公司产品专用销售网站：

商斯达微波光电产品网：[HTTP://www.rfoe.net/](http://www.rfoe.net/)

商斯达中国传感器科技信息网：<http://www.sensor-ic.com/>

商斯达工控安防网：<http://www.pc-ps.net/>

商斯达电子元器件网：<http://www.sunstare.com/>

商斯达消费电子产品网：<http://www.icasic.com/>

商斯达实业科技产品网：<http://www.sunstars.cn/> 射频微波光电元器件销售热线：

地址：深圳市福田区福华路福庆街鸿图大厦 1602 室

电话：0755-83396822 83397033 83398585 82884100

传真：0755-83376182 (0) 13823648918 MSN: SUNS8888@hotmail.com

邮编：518033 E-mail:szss20@163.com QQ: 195847376

深圳赛格展销部：深圳华强北路赛格电子市场 2583 号 电话：0755-83665529 25059422

技术支持：0755-83394033 13501568376

欢迎索取免费详细资料、设计指南和光盘；产品凡多，未能尽录，欢迎来电查询。

北京分公司：北京海淀区知春路 132 号中发电子大厦 3097 号

TEL: 010-81159046 82615020 13501189838 FAX: 010-62543996

上海分公司：上海市北京东路 668 号上海赛格电子市场 D125 号

TEL: 021-28311762 56703037 13701955389 FAX: 021-56703037

西安分公司：西安高新开发区 20 所(中国电子科技集团导航技术研究所)

西安劳动南路 88 号电子商城二楼 D23 号

TEL: 029-81022619 13072977981 FAX:029-88789382