

QUARTZ CRYSTAL OSCILLATOR
■ GENERAL DESCRIPTION

The NJU6329 series is a C-MOS quartz crystal oscillator which consists of an oscillation amplifier, 3-stage divider and 3-state output buffer.

The oscillation frequency is as wide as up to 50MHz and the symmetry of 45-55% is realized over full oscillation frequency range.

The oscillation amplifier incorporates feed-back resistance and oscillation capacitors(C_g , C_d), therefore, it requires no external component except quartz crystal.

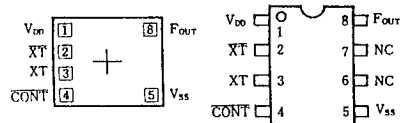
The 3-stage divider generates f_o , $f_o/2$, $f_o/4$ and $f_o/8$ and only one frequency selected by internal circuits is output.

The 3-state output buffer is TTL compatible and capable of 10 TTL driving.

The difference between NJU6329 and NJU6322 series is pin configuration only.

■ PACKAGE OUTLINE

NJU6329XC

NJU6329XE
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■ PIN CONFIGURATION/PAD LOCATION

■ FEATURES

- Operating Voltage -- 3.0~6.0V
- Maximum Oscillation Frequency -- 50MHz
- Low Operating Current
- High Fan-out -- TTL 10
- 3-state Output Buffer
- Selected Frequency OutPut (mask option)
Only one frequency of f_o , $f_o/2$, $f_o/4$ and $f_o/8$ output
- Oscillation Capacitor C_g and C_d on-chip
- Oscillation and/or Output Stand-by Function
- Package Outline -- CHIP/EMP8
- C-MOS Technology

■ COORDINATES

 Unit: μm

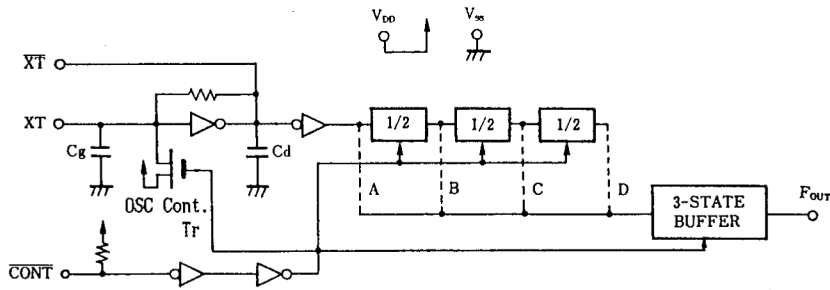
No.	PAD	X	Y
1	V_{DD}	-450	257
2	\overline{XT}	-450	84
3	XT	-450	-83
4	\overline{CONT}	-450	-249
5	V_{SS}	475	-249
8	F_{OUT}	475	257

Chip Size : 1.24 X 0.8mm
 Chip Center : $X=0\mu\text{m}, Y=0\mu\text{m}$
 Chip Thickness : $400\mu\text{m} \pm 30\mu\text{m}$
 (Note) No. 6 and 7 terminals are only for package type information. There are no PAD on the chip.

■ LINE-UP TABLE

Type No.	Output Freq.	C_g	C_d	Osc.Stop Function
NJU6329A	f_o	23pF	23pF	No
NJU6329B	$f_o/2$	23pF	23pF	No
NJU6329C	$f_o/4$	23pF	23pF	No
NJU6329D	$f_o/8$	23pF	23pF	No

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N						
1	V_{DD}	+ 5V						
2	\overline{XT}	Quartz Crystal Connecting Terminals						
3	XT							
4	\overline{CONT}	3-State Output Control and Divider Reset						
		<table border="1"> <thead> <tr> <th>CONT</th> <th>F_{OUT}</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Output either one frequency from f_0, $f_0/2$, $f_0/4$, and $f_0/8$</td> </tr> <tr> <td>L</td> <td>Output High Impedance and Divider Reset</td> </tr> </tbody> </table>	CONT	F_{OUT}	H	Output either one frequency from f_0 , $f_0/2$, $f_0/4$, and $f_0/8$	L	Output High Impedance and Divider Reset
		CONT	F_{OUT}					
H	Output either one frequency from f_0 , $f_0/2$, $f_0/4$, and $f_0/8$							
L	Output High Impedance and Divider Reset							
5	V_{SS}	GND						
8	F_{OUT}	Output either one frequency from f_0 , $f_0/2$, $f_0/4$, and $f_0/8$ (Note)						

(Note) Reference the Line-Up Table

■ ABSOLUTE MAXIMUM RATINGS

 ($T_a=25^\circ\text{C}$)

P A R A M E T E R	SYMBOL	R A T I N G S	UNIT
Supply Voltage	V_{DD}	-0.5 ~ +7.0	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_O	-0.5 ~ $V_{DD}+0.5$	V
Input Current	I_{IN}	± 10	mA
Output Current	I_O	± 25	mA
Power Dissipation	P_D	200 (EMP)	mW
Operating Temperature Range	T_{OPR}	-40 ~ + 85	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 ~ +125	$^\circ\text{C}$

 (Note) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the circuit.

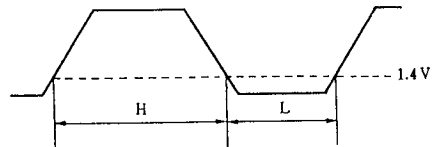
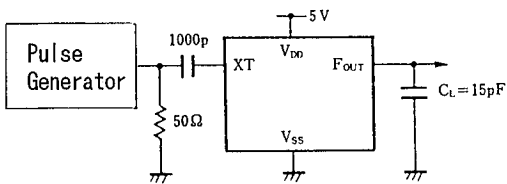
■ ELECTRICAL CHARACTERISTICS

 ($T_a=25^{\circ}\text{C}$, $V_{DD}=5\text{V}$)

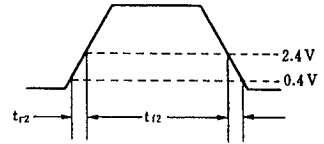
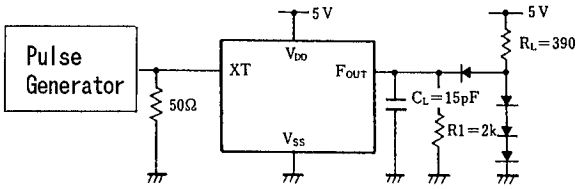
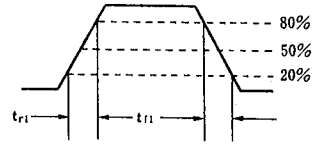
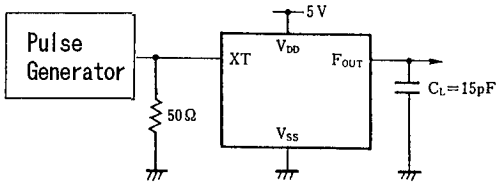
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}		3		6	V
Operating Current	I_{DD}	$f_{OSC}=16\text{MHz}$, No Load			15	mA
Stand-by Current	I_{st}	$\overline{\text{CONT}}, \text{XT}=\overline{V_{SS}}$, No Load (Note)			1	μA
Input Voltage	V_{IH}		3.5		5.0	V
	V_{IL}		0		1.5	
Output Current	I_{OH}	$V_{DD}=5\text{V}$, $V_{OH}=4.5\text{V}$	4			mA
	I_{OL}	$V_{DD}=5\text{V}$, $V_{OL}=0.5\text{V}$	16			
Input Current	I_{IN}	$\overline{\text{CONT}}$ Terminal, $\overline{\text{CONT}}=\overline{V_{SS}}$			400	μA
3-St Off-leakage Current	I_{OZ}	$\overline{\text{CONT}}=\overline{V_{SS}}$, $F_{OUT}=\overline{V_{SS}}$ or $\overline{V_{DD}}$			± 0.1	μA
Internal Capacitor	C_g, C_d	$f_{osc}=16\text{MHz}$		23		pF
Max. Oscillation Freq.	f_{MAX}		50			MHz
Output Signal Symmetry	SYM	$C_L=15\text{pF}$ at 1.4V	45	50	55	%
Output Signal Rise Time	t_{r1}	$C_L=15\text{pF}$, 20~80%			8	ns
	t_{r2}	$C_L=15\text{pF}$, $R_L=390\Omega$, 0.4~2.4V			6	
Output Signal Fall Time	t_{f1}	$C_L=15\text{pF}$, 80~20%			6	ns
	t_{f1}	$C_L=15\text{pF}$, $R_L=390\Omega$, 2.4~0.4V			4	

 Note) Excluding input current on $\overline{\text{CONT}}$ terminal.

■ MEASUREMENT CIRCUITS

 (1) Output Signal Symmetry ($C_L=15\text{pF}$)


(2) Output Signal Rise/Fall Time ($C_L=15\text{pF}$)



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NJU6329 Series

MEMO

[CAUTION]

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