PRELIMINARY

VFD CONTROLLER DRIVER

■ GENERAL DESCRIPTION

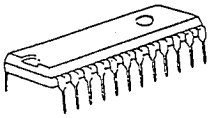
The **NJU3422** is a VFD (Vacuum Fluorescent Display) Controller Driver.

It contains display data RAM, address counter, command register, high voltage drivers, and serial interface circuit.

The display data and the command data can be transmitted with the serial interface circuit and VFD driving voltage can operate up to 45V.

The NJU3422 is useful for car audio, VCR and other VFD application items.

■ PACKAGE OUTLINE

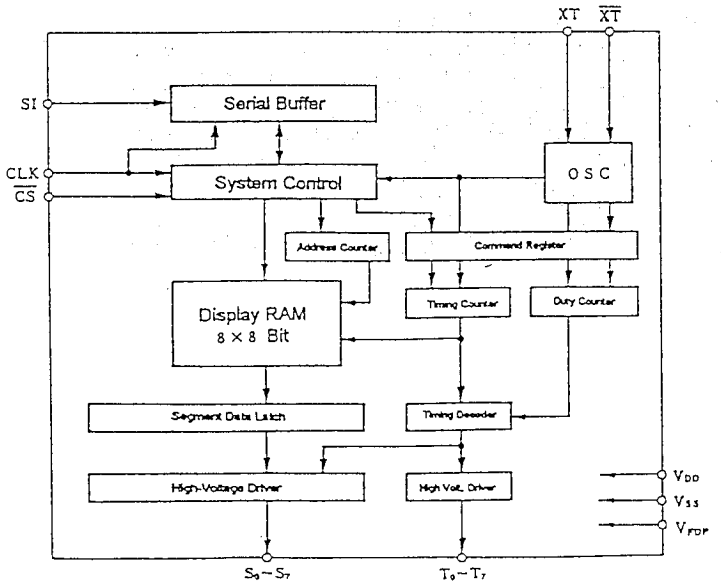


NJU3422L

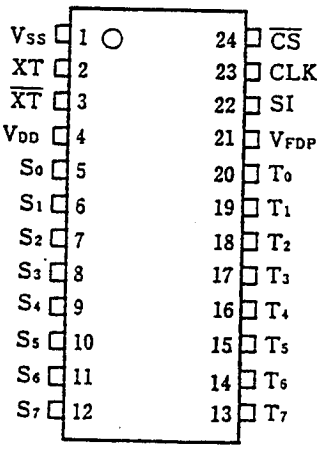
■ FEATURES

- VFD Driving Voltage $|V_{DD}-V_{FDP}| \leqq 45V$
- Display Mode 8 Segments Display × 8 Digits
- Serial Interface
- Display ON/OFF Function
- Display Data RAM 8 × 8 Bits
- Oscillation Circuit on-chip Ceramic Resonator or External R
- Power On Initialization
- Operating Voltage 5V±10%
- Package Outline SDIP 24
- C-MOS Technology

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



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■ TERMINAL DESCRIPTION

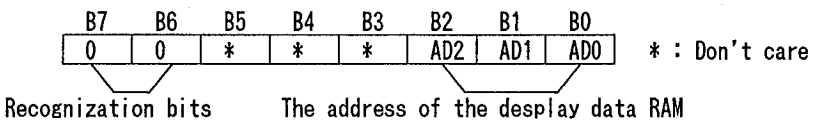
NO.	SYMBOL	FUNCTION
4 1 21	V_{DD} V_{SS} V_{FDP}	POWER SOURCE GND VFD Driving Voltage
2,3	XT, $\overline{XT}$	Oscillation Terminals. For external clock operation, The clock should be input on XT terminal.
5~12 13~20	S_0~S_7 T_7~T_0	Segment Output Terminals(Pull-Down Resistance) Timing Output Terminals(Pull-Down Resistance)
22	SI	Serial Data (Address, display, Command) input Terminal.
23	CLK	Shift Clock Input Terminal.
24	$\overline{CS}$	Chip Select Input Terminal. "L":Activated

■ FUNCTION DESCRIPTION

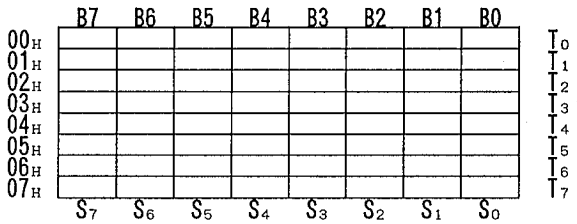
(1) Address Counter

The address counter addresses the display data RAM which data are sent by the serial data transmission.When the first word of the serial data is recognized as the address of the display data RAM (The upper two bits of a byte must be "00" .) , the lower 3bits are set up into the address counter as the address of the display data RAM. The data of the display data RAM which are input sequentially are set into the specified address and the address counter increments.
Though the address counter consists of the 3-bit counter,the effective range is from "00_H" to "07_H". The address of "07_H" is incremented to "00_H".

The Address Data



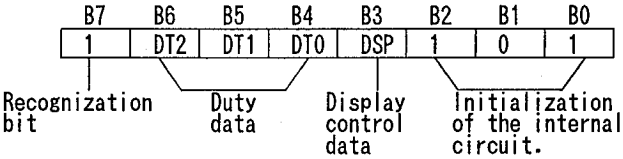
The mapping of the display data RAM



(2) COMMAND REGISTER

The Command Register is the register for setting the status of Display Duty, and Display ON/OFF.
When the first word of serial transmmitted data is recognized as the command data (The upper one bit of a byte must be "1".), the lower 7 bits are set into the command register.
The internal circuit has been initialized until the CS signal is set to "H" level when "101" is written into the lower 3 bits of the command register (When the NJU3422 is powered on, the status of the display is Display OFF by the power-on initialization.)

The command data



(2-1) Duty set

DT2	DT1	DT0	Timing signal Duty
0	0	0	2/16
0	0	1	4/16
0	1	0	6/16
0	1	1	8/16
1	0	0	10/16
1	0	1	12/16
1	1	0	14/16
1	1	1	15/16

(2-2) Display contorol set

DSP	Display
0	OFF
1	ON

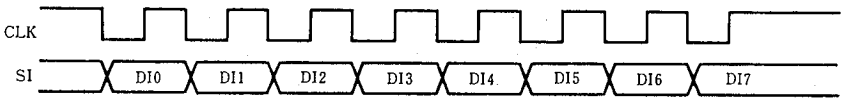
(5) SERIAL DATA TRANSMISSION

The data transmission with the external can be executed by the serial interface circuit only. This interface circuit requires the external shift clock input and can execute the input action synchronously as shown below.

The serial data are grouped at a word which equalles to a byte (8 bits) for this device. The serial interface circuit is activated when the CS terminal is set to "L" level. While the CS is "L", the words of the serial data can be transmitted using the shift clock (the CLK terminal) and the serial data input (the SI terminal) synchronously.

The first transmitted word must be the address or the command data. When the first word is the address data, the following words should be the display data. When the first word is the command data, the following words, if transmitted, are ineffective.

■ CLK and SI TIMING CHART



Serial baffer shift timing

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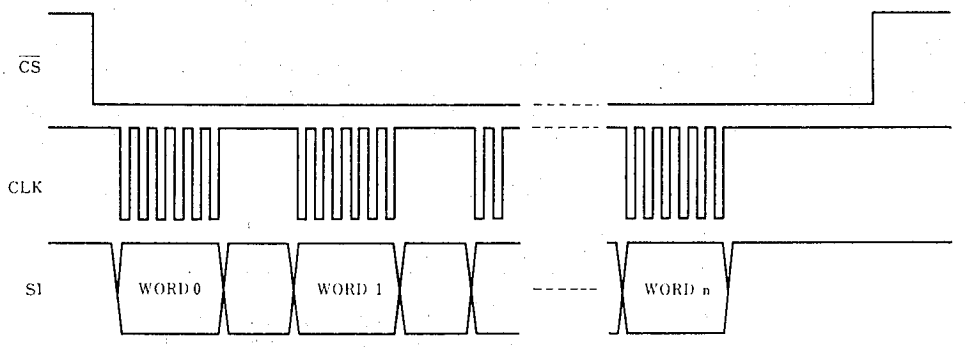
■ SERIAL TRANSMISSION FORMAT



· SERIAL INPUT DATA

WORD 0

The address data

B7	B6	B5	B4	B3	B2	B1	B0
0	0	*	*	*	AD2	AD1	AD0

* : Don't care

The command data

B7	B6	B5	B4	B3	B2	B1	B0
1	DT2	DT1	DT0	DSP	*	*	*

* : When (B2, B1, B0) = (1, 0, 1), the internal circuit is initialized.

WORD 1~n

Display data are required when WORD 0 = address data
Any data are become ineffective when WORD 0 = not address data

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃, V_{SS}=0V)

PARAMETER	SYMBOL	RATINGS	CONDITIONS	UNIT
Operating Voltage	V_{DD}	-0.3 ~ +7.0		V
Input Voltage	V_{IN}	-0.3 ~ V_{DD}+0.3		V
Output Voltage	V_{OUT}	-0.3 ~ V_{DD}+0.3		V
VFD Driving Voltage	V_{FDP}	V_{DD}-40~V_{DD}+0.3		V
"H" level Output Current	I_{ODH1}	-15	For a terminal, S_0~S_7 Terminals only	mA
	I_{ODH2}	-35	For a terminal, T_0~T_7 Terminals only	
"H" level Total Output Current	ΣI_{ODH}	-100	Sum of the Display Terminals	mA
"L" level Total Output Current	ΣI_{OL}	100	Sum of the Output Terminals	mA
Power Dissipation	P_D	SDIP:700		mW
Operating Temperature Range	Topr	-30 ~ +80		℃
Storage Temperature Range	Tstg	-55 ~ +125		℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V_{SS}=0V)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}	V_{DD} Terminal	4.5		5.5	V
"H" Level Input Voltage	V_{IH}	XT, $\overline{CS}$, SI, CLK Terminals	0.8V_{DD}			V
"L" Level Input Voltage	V_{IL}	XT, $\overline{CS}$, SI, CLK Terminals			0.2V_{DD}	V
Input Off Leak Current	I_{IZ}	$\overline{CS}$, CLK, SI Terminals V_{DD}=5.5V, V_{IN}=0 or 5.5V			±1	uA
Display Output Current	I_{OH}	S_0~S_7 Terminals V_{DD}=4.5V, V_{OH}=V_{DD}-2.5V	-7			mA
		T_0~T_7 Terminals V_{DD}=4.5V, V_{OH}=V_{DD}-2.5V	-15			
Pull-Down resistance	R_{DST}	S_0~S_7, T_0~T_7 Term. V_{DD}=5.0V V_{OUT}=V_{DD}, V_{FDP}=V_{DD}-40V	70		200	
Logic Operating Current	I_{DD1A}	V_{SS} Terminal, V_{DD}=5.0V, 4MHz Ceramic resonator, C1=C2=27pF Output Open, All Segment or Timing Output is OFF		1	2	mA
	I_{DD1B}	V_{SS} Terminal, V_{DD}=5.0V, CR Oscillation(R=5.1kΩ) Output Open, All Segment or Timing Output is OFF		2	4	mA
Display Operating Current	I_{DD2}	V_{FDP} Terminal V_{DD}=5.0V V_{FDP}=V_{DD}-40V All Segment or Timing Output is ON		3	6	mA

■ AC Characteristics

(Ta=25℃, V_{DD}=5V±10%, V_{SS}=0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Oscillation Frequency External Clock Input	f_{XT} f_{CL}	Fig.1	1	4	5	MHz
CR Oscillation Frequency	f_{CR}	Fig.1	3	5.5	8	MHz
External Clock Shift Clock Pulse Width	PW_H/PW_L	Fig.1, Fig.2	90			ns
External Clock Rise/Fall Time	t_{CLH}/t_{CLL}	Fig.1, Fig.2			20	ns
Serial Input Setup Time	t_{SIS}	Fig.2	60			ns
Serial Input Hold Time	t_{SIH}		10			ns
Shift Clock Frequency	f_{CLK}	Fig.3			f_{XT}/3, f_{CL}/3, f_{CR}/3	MHz
Shift Clock Interval Time	t_{CLK1}		10			us
Minimum Blanking Time	t_{BKA}	Fig.4, f_{XT}=4MHz	20		30	us
	t_{BKB}	Fig.4, CR Osillation	10		40	
Power Rise Time	t_R	Fig.5	0.05		50	ms

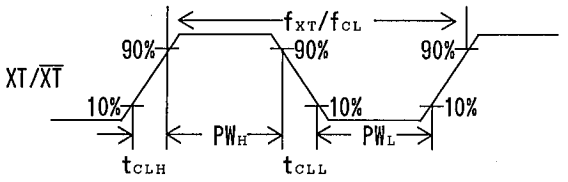


Fig.1

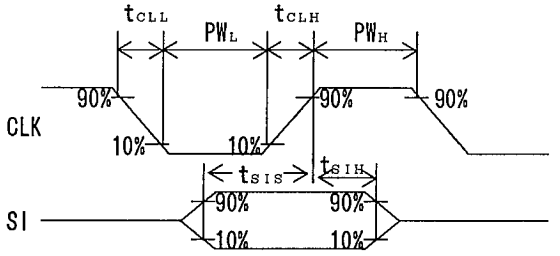


Fig.2

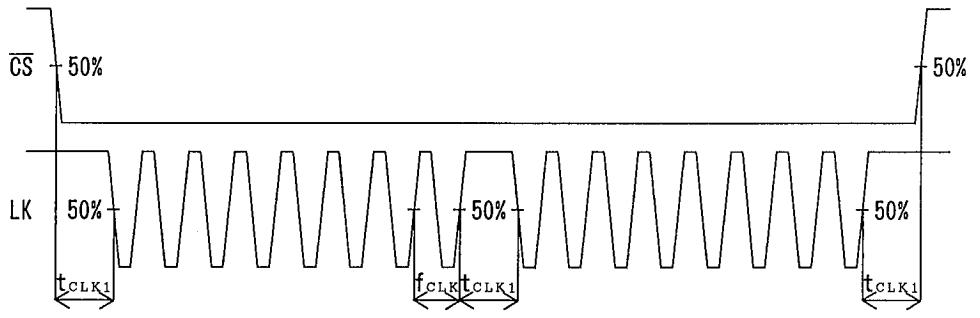


Fig.3

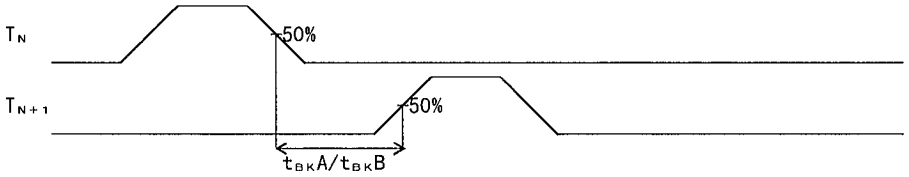


FIG. 4

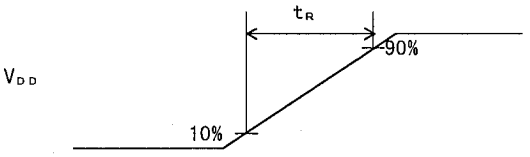
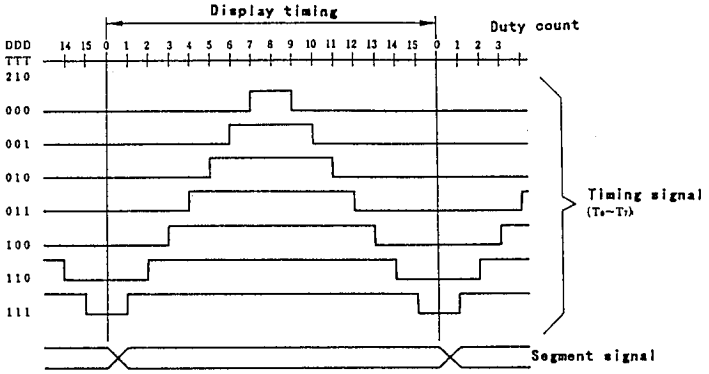
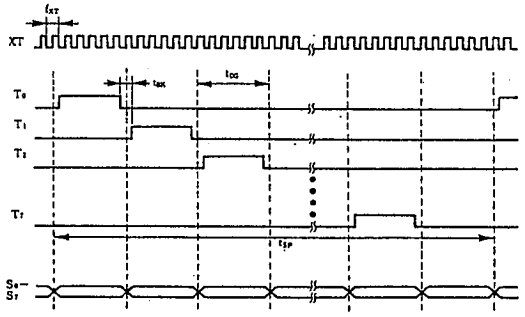


FIG. 5

■ TIMING SIGNAL / DUTY CHANGE WAVEFORM



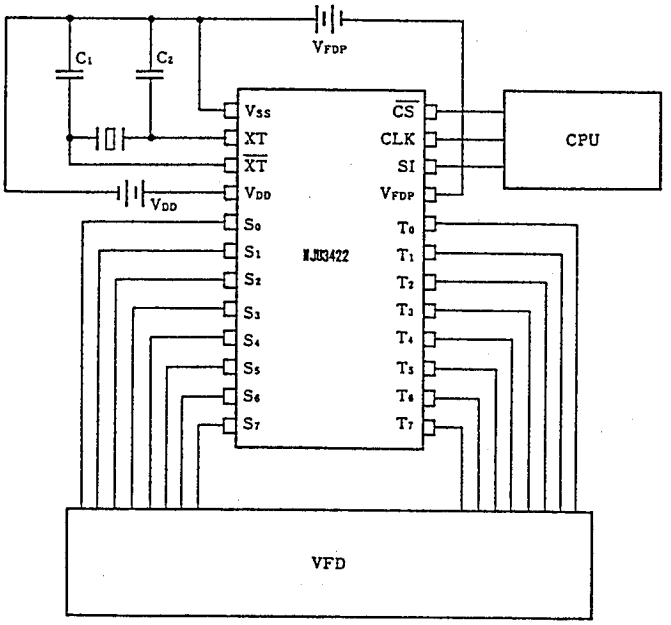
■ DISPLAY TIMING CHART



Oscillation frequency	:	f_{XT}
Minimum blanking time (Duty 15/16)	:	$t_{BK} = (1/f_{XT}) \times 96$
1character display time	:	$t_{DG} = t_{BK} \times 16$
1cycle display time	:	$t_{SP} = t_{DG} \times 8$character

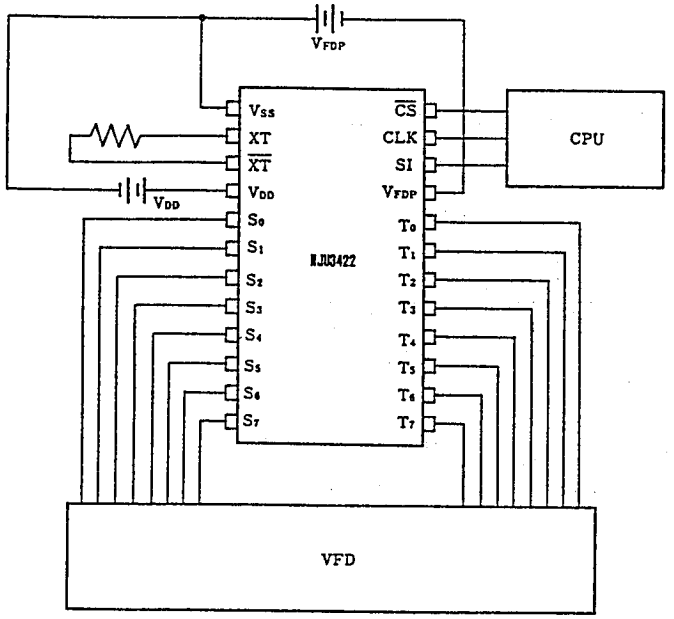
■ APPLICATION CIRCUIT

(1) Ceramic Resonator Oscillation



NOTE) The capacitance of C1 and C2 are determinded by the experiment.

(2) CR Oscillation



MEMO

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