Preliminary

# Multi-Function Digital Audio Decoder

## ■ General Description

The NJU26501 is a multi-function digital audio signal decoder.
The NJU26501 processes the stereo matrix-encoded or compressed signal into spacious sound of up to 7.1(max) channels by Dolby Digital, Dolby Digital EX or DTS with Bass Management System. Also non matrix-encoded audio signal can be processed into effective spacious sound by Dolby ProLogic II.
The decoded multi-channel signal can be downmixed into 2-channel virtual surround output by the Dolby Virtual technology.
The applications of the NJU26501 are suitable for multi-channel products such as DVD Player, AV AMP, Home Theater and Car Audio, or any kinds of multi-channel audio products.

■Package

TQFP- 52

## ■ FEATURES

- Dolby Digital / Dolby Digital EX (7.1ch)
- DTS (5.1ch)
- Dolby Pro Logic II
- Virtual Dolby Digital
- Bass Management

## ■ Digital Signal Processor Specification

- 24bit Fixed-point Digital Signal Processing
- Maximum Clock Frequency : 24.576MHz(Standard), built-in PLL Circuit
- Digital Audio Interface : 2 Input ports / 4 Output ports
- Microcomputer Interface : $I^2C$ Bus (Standard-mode/100Kbps, Fast-mode/400kbps)
  : 4-Wire Serial Bus (4-Wire: Clock, Enable, Input data, Output data)
- Power Supply : DSP Core : 1.8V
  : I/O interface: 3.3V(+5.0V tolerant)
- Package : TQFP 52pins

* Note1: "Dolby," "Pro Logic II," "Dolby Digital," "Dolby Digital EX," and the double-D symbol are trademarks of Dolby Laboratories. The NJU26501 may only be supplied to licensees of or companies authorized by Dolby Laboratories. Please refer all licensing inquiries to Dolby Laboratories.

* Note2: "DTS" is a registered trademark of DTS, Inc.

* Note3: Purchase of **$I^2C$** components of New Japan Radio Co. ,Ltd or one of sublicensed Associated Companies conveys a license under the Philips **$I^2C$** Patent Rights to use these components in an **$I^2C$** system, provided that the system conforms to the **$I^2C$** Standard specification as defined by Philips.

## ■ DSP Block Diagram

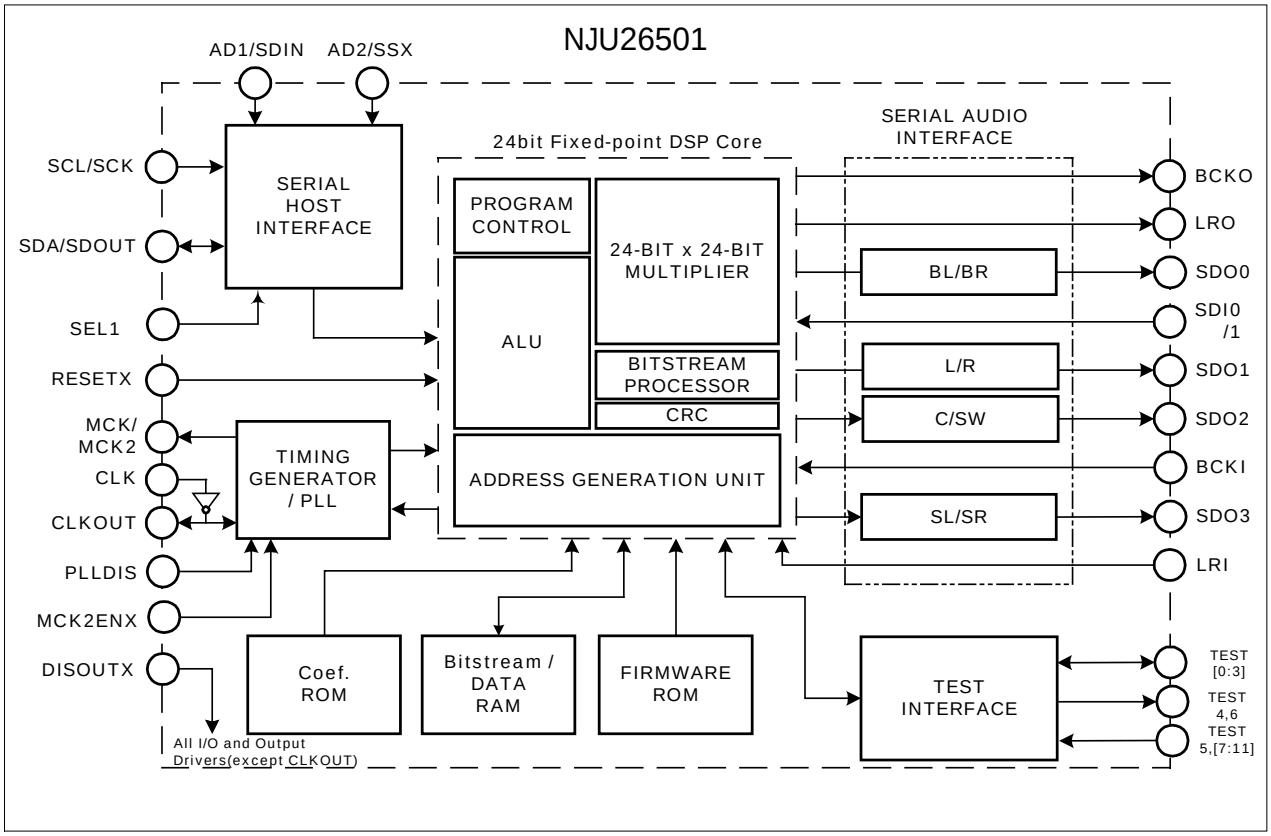



**Fig.1-1 NJU26501 Block Diagram**

## ■ Multi-function Digital Audio Decoder

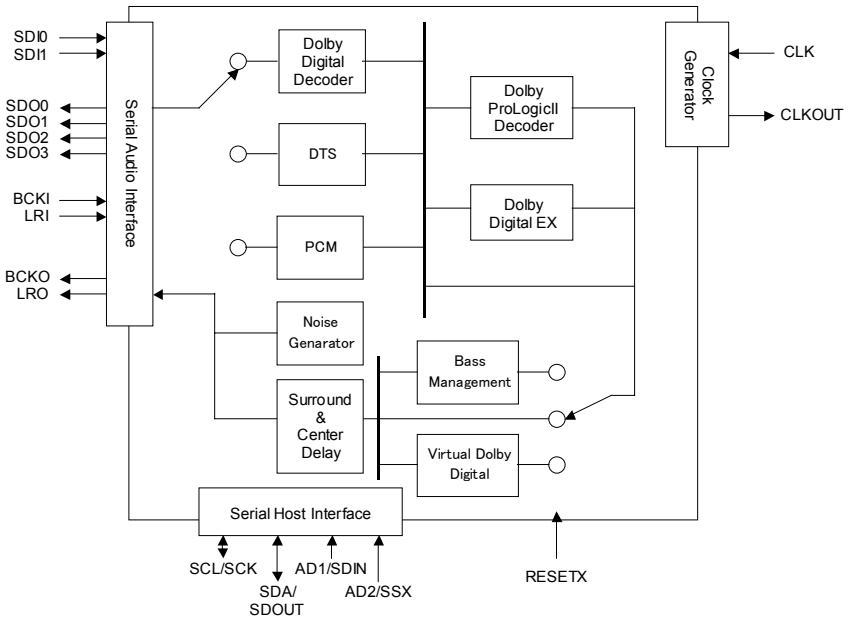



**Fig.1-2 NJU26501 Function Diagram**

## ■ Pin Configuration

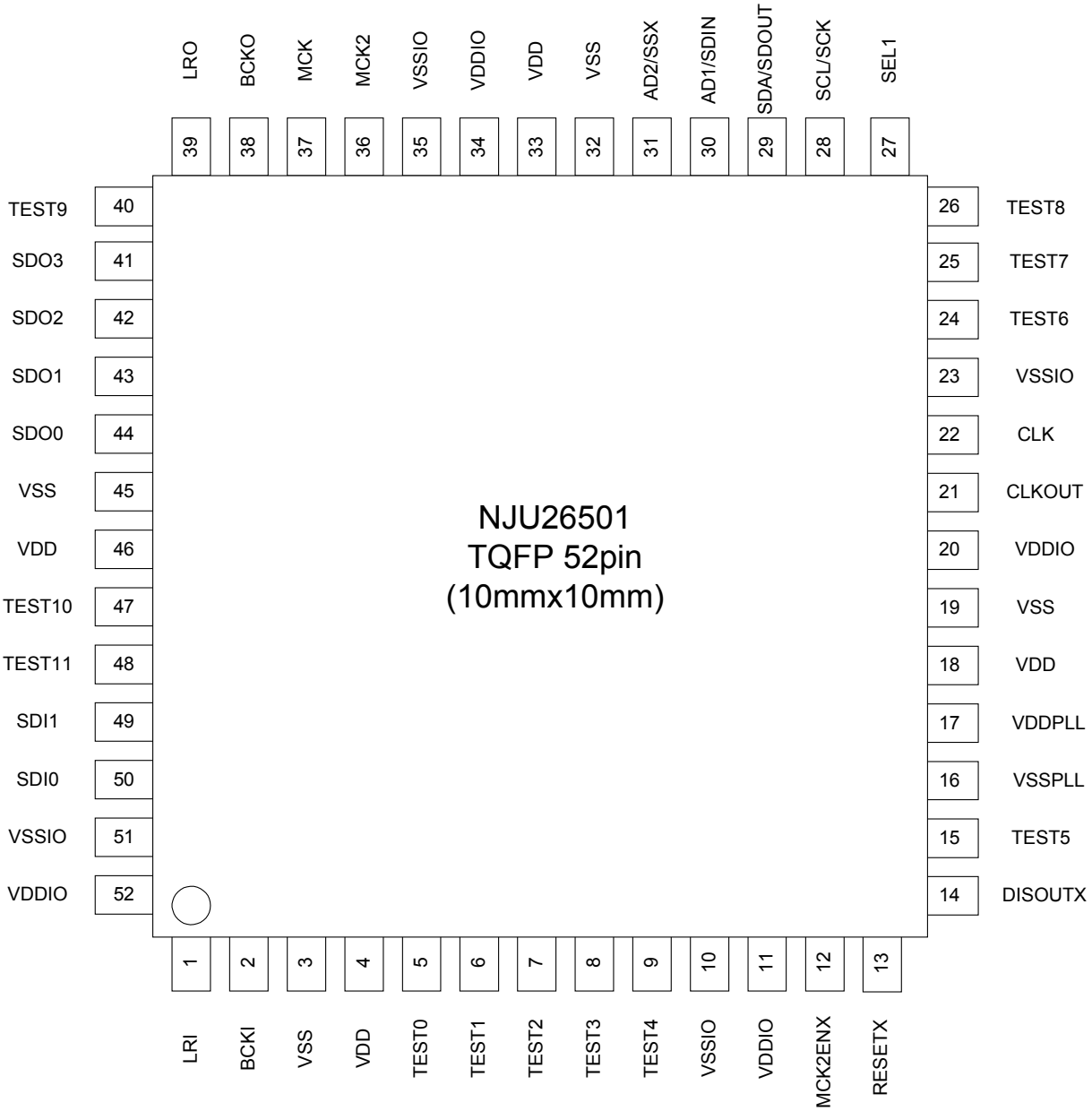



**Fig.1-3 Pin Configuration**

## ■ Pin Description

### Table1-1 Pin Description

| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 1 | LRI | I | LR Clock Input |
| 2 | BCKI | I | Bit Clock Input |
| 3 | VSS | G | DSP Core Power Supply GND |
| 4 | VDD | P | DSP Core Power Supply +1.8V |
| 5 | TEST0 | I/O | for test (connect with VSSIO through 3.3-ohm resistance.) |
| 6 | TEST1 | I/O | for test (connect with VDDIO or VSSIO through 3.3-ohm resistance.) |
| 7 | TEST2 | I/O | for test (connect with VDDIO or VSSIO through 3.3-ohm resistance.) |
| 8 | TEST3 | I/O | for test (connect with VDDIO or VSSIO through 3.3-ohm resistance.) |
| 9 | TEST4 | O | for test (Open) |
| 10 | VSSIO | G | I/O Power Supply GND |
| 11 | VDDIO | P | I/O Power Supply +3.3V |
| 12 | MCK2ENX | Ipd | MCK2 Enable ('0' : MCK2 enable / '1' : MCK2 turns Hi-Z ) |
| 13 | RESETX | I | Reset (RESX='0' : DSP Reset) |
| 14 | DISOUTX | Ipu | Disable Output ('0':All outputs (except CLKOUT) turn Hi-Z) |
| 15 | TEST5 | Ipd | for test (connect to VSSIO) |
| 16 | VSSPLL | G | PLL Power Supply GND |
| 17 | VDDPLL | P | PLL Power Supply +1.8V |
| 18 | VDD | P | DSP Core Power Supply +1.8V |
| 19 | VSS | G | DSP Core Power Supply GND |
| 20 | VDDIO | P | I/O Power Supply +3.3V |
| 21 | CLKOUT | I/O | OSC Clock Output |
| 22 | CLK | I | OSC Clock Input (24.576MHz) |
| 23 | VSSIO | G | I/O Power Supply GND |
| 24 | TEST6 | O | for test (Open) |
| 25 | TEST7 | Ipd | for test (connect to VSSIO) |
| 26 | TEST8 | Ipd | for test (connect to VSSIO) |
| 27 | SEL1 | Ipu | Select Host Interface ('1' : 4-wire serial mode / '0' : $I^2C$ mode) |
| 28 | SCL/SCK | I | $I^2C$ SCL ($I^2C$ mode) / Serial clock (4-wire serial mode) |
| 29 | SDA/SDOUT | I/O | $I^2C$ SDA ($I^2C$ mode) / Serial Out (4-wire serial mode) |
| 30 | AD1/SDIN | I | $I^2C$ Address ($I^2C$ mode) / Serial In (4-wire serial mode) |
| 31 | AD2/SSX | I | $I^2C$ Address ($I^2C$ mode) / Serial enable (4-wire serial mode) |
| 32 | VSS | G | DSP Core Power Supply GND |
| 33 | VDD | P | DSP Core Power Supply +1.8V |
| 34 | VDDIO | P | I/O Power Supply +3.3V |
| 35 | VSSIO | G | I/O Power Supply GND |
| 36 | MCK2 | O | A/D,D/A Clock Output (Buffered output of CLK input) |
| 37 | MCK | O | A/D,D/A Clock Output (2-Divided output of CLK input) |
| 38 | BCKO | O | Bit Clock Output |
| 39 | LRO | O | LR Clock Output |
| 40 | TEST9 | Ipu | for test (connect to VDDIO) |
| 41 | SDO3 | O | Audio Data Output ch.3 (Surround channel (LS/RS) output) |
| 42 | SDO2 | O | Audio Data Output ch.2 (Center/Sub Woofer channel (C/SW) output) |
| 43 | SDO1 | O | Audio Data Output ch.1 (Front channel (L/R) output) |
| 44 | SDO0 | O | Audio Data Output ch.0 (Back Surround channel (BL/BR) output) |
| 45 | VSS | G | DSP Core Power Supply GND |
| 46 | VDD | P | DSP Core Power Supply +1.8V |
| 47 | TEST10 | I | for test (connect to VSSIO) |
| 48 | TEST11 | I | for test (connect to VSSIO) |
| 49 | SDI1 | I | Audio Data Input ch.1 |
| 50 | SDI0 | I | Audio Data Input ch.0 |
| 51 | VSSIO | G | I/O Power Supply GND |
| 52 | VDDIO | P | I/O Power Supply +3.3V |

Note I:In, Ipd:Input Pull-down, Ipu:Input Pull-Up, O:Out, I/O:Bidir, P:+Power, G:GND

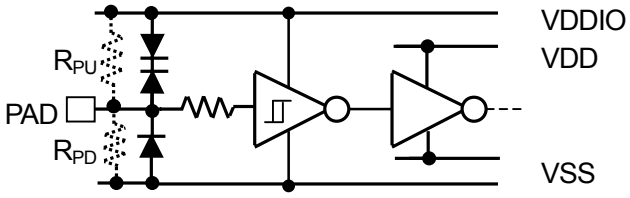
## ■ Absolute Maximum Ratings

**Table1-2 Absolute Maximum Ratings**

| Parameter | | Symbol | Rating | Units |
|---|---|---|---|---|
| Supply Voltage | Logic | $V_{DD}$ | -0.3 - 2.1 | V |
| | PLL | $V_{DDPLL}$ | -0.3 - 2.1 | |
| | I/O | $V_{DDIO}$ | VDD - 3.8 | |
| Pin Voltage | In, I/O | $V_x$ | -0.3 - 5.5 | V |
| | Out | $V_{x(OUT)}$ | -0.3 - $V_{DDIO}$ +0.3 | |
| | CLK | $V_{x(Xi)}$ | -0.3 - $V_{DDIO}$ +0.3 | |
| | CLK OUT | $V_{x(Xo)}$ | -0.3 - $V_{DD}$ +0.3 | |
| Power Dissipation | | $P_D$ | 0.3 | W |
| Storage Temperature | | $T_{STR}$ | -40～+125 | ℃ |

* $V_x$ : Pin No. 1,2,5,6,7,8,12,13,14,15,25,26,27,28,29,30,31,40,47,48,49,50
* $V_{x(OUT)}$ : Pin No. 9,24,36,37,38,39,41,42,43,44
* $V_{x(Xi)}$ : Pin No. 22
* $V_{x(Xo)}$ : Pin No. 21

## ■ Terminal equivalent circuit diagram

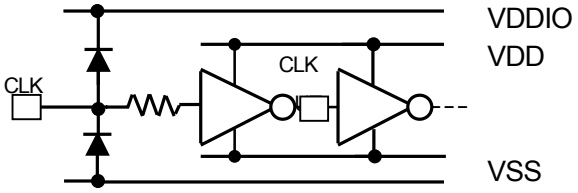



Input, I/O (Input part)

(No.1,2,5,6,7,8,13,28,29,30,31,47,48,49,50 pin)

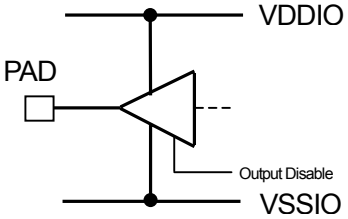
(With $R_{PU}$: No. 14, 27, 40 pin)

(With $R_{PD}$: No. 12,15,25,26 pin)




CLK/CLKOUT

(No.21, 22 pin)




Output, I/O (Output part)

(No. 5,6,7,8,9,29,36,37,38,39,41,42,43,44 pin)

**Fig.1-4 NJU26501 Terminal equivalent circuit diagram**

## ■ Electric Characteristics

**Table1-3 Electric Characteristics**

**($V_{DD}$=$V_{DDPLL}$=1.8V, $V_{DDIO}$=$V_{DDO}$=3.3V, $f_{OSC}$=24.576MHz, Ta=25°C)**

| Parameter | | Symbol | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| Operating Voltage | Logic | $V_{DD}$ | $V_{DD}$ pins | 1.7 | 1.8 | 1.9 | V |
| | PLL | $V_{DDPLL}$ | $V_{DDPLL}$ pins | 1.7 | 1.8 | 1.9 | |
| | I/O | $V_{DDIO}$ | $V_{DDIO}$ pins | 3.0 | 3.3 | 3.6 | |
| Operating Current | | $I_{DD}$ | $V_{DD}$=$V_{DDPLL}$=1.8V | - | 40 | - | mA |
| | | $I_{DDPLL}$ | $V_{DD}$=$V_{DDPLL}$=1.8V | - | 4.0 | - | |
| | | $I_{DDIO}$ | $V_{DDIO}$ =3.3V | - | 3.0 | - | |
| Operating Temperature | | $T_{OPR}$ | | -40 | 25 | 85 | ℃ |
| High Level Input Voltage | | $V_{IH}$ | $V_{DDIO}$=3.0 - 3.6V | 2.0 | - | 5.25 | V |
| (for OSC Input pad) | | $V_{IH(OSC)}$ | $V_{DDIO}$=3.0 - 3.6V<br>$V_{DD}$=1.7 - 1.95V | $V_{DD}$ * 0.7 | - | $V_{DDIO}$ + 0.3 | |
| Low Level Input Voltage | | $V_{IL}$ | $V_{DDIO}$=3.0 - 3.6V | -0.3 | - | 0.5 | V |
| (for OSC Input pad) | | $V_{IL(OSC)}$ | $V_{DDO}$=3.0 - 3.6V<br>$V_{DD}$=1.7 - 1.95V | -0.3 | - | $V_{DD}$ * 0.3 | |
| Input Current | | $I_{IN}$ | $V_{IN}$ = $V_{DDIO}$ – 5.25V | - | - | 10 | μA |
| | | | $V_{IN}$ = $V_{SSIO}$ | -10 | - | - | |
| | | | $V_{IN}$ = $V_{SSIO}$ - $V_{DDIO}$ | −150 | - | 10 | |
| (for Pull-Down pads) | | $I_{IN(PD)}$ | $V_{IN}$ = $V_{DDIO}$ – 5.25V | 100 | - | 400 | |
| | | | $V_{IN}$ = $V_{SSIO}$ | -10 | - | - | |
| | | | $V_{IN}$ = $V_{SSIO}$ - $V_{DDIO}$ | −100 | - | 400 | |
| (for Pull-Up pads) | | $I_{IN(PU)}$ | $V_{IN}$ = $V_{DDIO}$ – 5.25V | - | - | 10 | |
| | | | $V_{IN}$ = $V_{SSIO}$ | −200 | - | −50 | |
| | | | $V_{IN}$ = $V_{SSIO}$ - $V_{DDIO}$ | −300 | - | 10 | |
| (for OSC Input pad) | | $I_{IN(OSC)}$ | $V_{IN}$ = $V_{SSIO}$ - $V_{DDIO}$ | −10 | - | 10 | |
| Leakage Current (at output high impedance) | | $I_{OZ(IO)}$ | $V_{IN}$= $V_{DDIO}$ – 5.25V<br>DISOUTX=$V_{IL}$ | - | - | 10 | μA |
| (for I/O Pad) | | | $V_{IN}$= $V_{SSIO}$<br>DISOUTX=$V_{IL}$ | -10 | - | - | |
| | | | $V_{IN}$= $V_{SSIO}$ – $V_{DDIO}$<br>DISOUTX=$V_{IL}$ | -150 | - | 10 | |
| (for Output Pad) | | $I_{OZ(OUT)}$ | $V_{IN}$= $V_{SSIO}$ – $V_{DDIO}$<br>DISOUTX=$V_{IL}$ | -30 | - | 10 | |
| High Level Output Voltage | | $V_{OH}$ | $I_{OH}$= -2mA<br>$V_{DDIO}$=3.0V | 2.7 | - | - | V |
| | | | $I_{OH}$= -300uA<br>$V_{DDIO}$=3.0 – 3.6V | $V_{DDIO}$ * 0.9 | - | - | |
| (for OSC Output Pad) | | $V_{OH(OSC)}$ | $I_{OH}$=-100uA<br>$V_{DDIO}$=3.0V, $V_{DD}$=1.7V | 1.5 | - | - | |
| Low Level Output Voltage | | $V_{OL}$ | $I_{OL}$=2mA, $V_{DDIO}$=3.0V | - | - | 0.4 | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | $I_{OL}$=300uA<br>$V_{DDIO}$=3.0 – 3.6V | - | - | $V_{DDIO}$ * 0.1 | |
| (for OSC Output Pad) | $V_{OL(OSC)}$ | $I_{OL}$=100uA<br>$V_{DDIO}$=3.0V, $V_{DD}$=1.7V | - | - | 0.2 | |
| Input Capacitance | $C_{IN}$ | | - | 6 | - | pF |
| Input Transition Time | $t_r$ / $t_f$ | except for No.28, 29, 30, 31pin * | - | - | 100 | ns |
| Clock Frequency | $f_{OSC}$ | No.22pin(CLK) | 24 | 24.576 | 25 | MHz |
| Clock Duty Cycle | $r_{EC}$ | No.22pin(CLK) | 45 | 50 | 55 | % |

* The tr / tf of these terminals are specified separately.

* All input / input-and-output terminals serve as the Schmidt trigger inputs except for No.22pin(Xi).

* To fix a terminal level, the fixed level should be lower than $\mathbf{V_{DDIO}}$.

* Do not carry out the pull-up of the output terminals on the voltage more than $\mathbf{V_{DDIO}}$.

# 1. Power Supply, Clock and Reset

## 1.1 Power Supply

The NJU26501 has three power supplies $V_{DD}/V_{SS}$, $V_{DDPLL}/V_{SSPLL}$ and $V_{DDIO}/V_{SSIO}$. $V_{DD}/V_{SS}$ is used as an internal core power supply, $V_{DDPLL}/V_{SSPLL}$ is used as an internal PLL power supply and $V_{DDIO}/V_{SSIO}$ is used as I/O terminal power supply.

**NOTICE:**
**The power supply is turned on or turned off in order of the follow.**

**The power supply is turned on: $V_{DD}$ -> $V_{DDPLL}$ -> $V_{DDIO}$**
**The power supply is turned off: $V_{SS}$ -> $V_{SSPLL}$ -> $V_{SSIO}$**

There is a procedure to turn on the NJU26501.
A power supply should surely start $V_{DDIO}$ first. Then, please start $V_{DD}$ and, finally supply $V_{DDPLL}$.
If the procedure to turn on is not kept right, there is possibility that excessive current makes fatal damage to the NJU26501 and the external circuit parts.
Moreover, turn off of a power supply by the reverse sequence of turning on a power supply.

To setup good power supply condition, the decoupling capacitors should be implemented at the all power supply terminals.

Although there is no time parameter about the injection of a power supply, potential should not be crossed during an injection between power supplies

The $V_{DDPLL}/V_{SSPLL}$ supplies the power for internal PLL circuit. The $V_{DDPLL}/V_{SSPLL}$ is sensitive to power-line noise. The $V_{DDPLL}/V_{SSPLL}$ line should be separate from internal core power supply $V_{DD}$ or provide noise filters to prevent from power supply noise. Without these countermeasures, there is possibility of PLL oscillation-stop and so on.

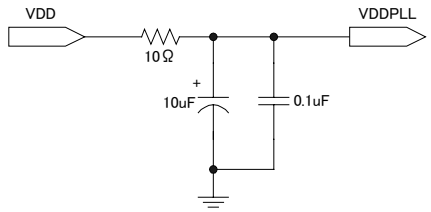



**Fig. 1-5 The example of a simple power supply filter**

### 1.2 Clock

The NJU26501 CLK pin requires the system clock that should be related to the sample frequency fs. The CLK/CLKOUT pins can generate the system clock by connecting the crystal oscillator or the ceramic resonator. Refer to the application circuit diagram about the circuit parameters.

When the external oscillator is connected to CLK/CLKOUT pins, check the voltage level of the pins. Because the maximum input voltage level of CLK pin is deferent from the other input or bi-directional pins. The maximum voltage-level of CLK pin equals to $V_{DD}$.

Note: Contact with a manufacture maker about use of a crystal oscillator/ceramic vibrator.

When a crystal oscillator or a ceramic vibrator is used, it connects only required parts of an oscillator.
Do not take out a signal from CLK/CLKOUT.
It becomes the cause of an unusual oscillation and oscillation stop.

When an external clock is used, do not connect other parts to CLKOUT.

When the clock inputted into a CLK terminal is required to be used further externally, fix MCK2ENX terminal to a Low level, and use the signal outputted from MCK terminal.

When a crystal oscillator is used, choose a crystal oscillator of a basic wave.

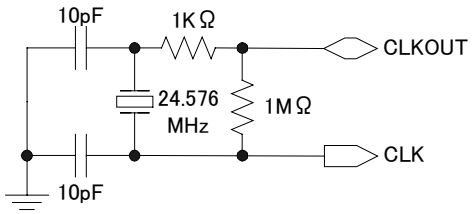



**Fig.1-6 The example of the oscillator circuit.**

### 1.3 Reset

To initialize the NJU26501, RESETX pin should be set low level during some period. After some period of Low level, RESETX pin should be High level. This procedure starts the initialization of the NJU26501.
After the power supply and the oscillation of the NJU26501 becomes stable, RESETX pin should be kept Low-level at least $t_{RESETX}$ period.
To finalize the initialization procedure takes 1 m sec. After 1 m sec, the NJU26501 can accept a command from Host controller. The detail status of the initialized NJU26501 is referred to the each command that describes the initial status.

To select $I^2C$ bus or 4-Wire serial bus, some level should be supplied to SEL1 pin. When SEL1="L", $I^2C$ bus is selected. When SEL1="H", 4-Wire serial bus is selected. The level of SEL1 is checked by the NJU26501 in 1 m sec after RESETX pin level goes to "H".

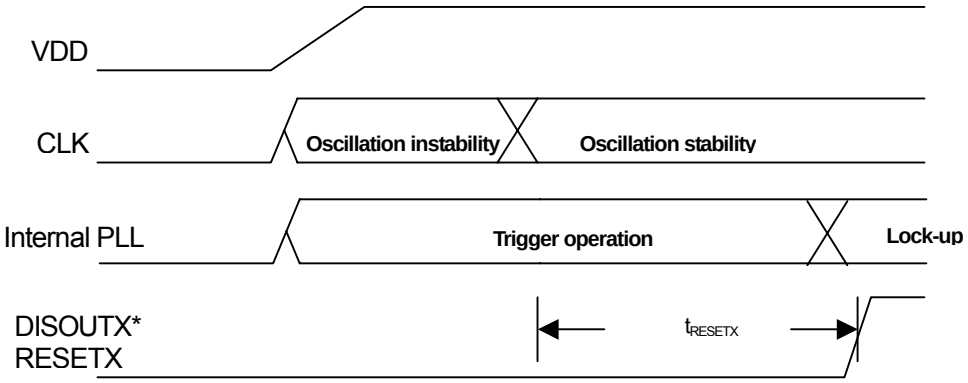



**Fig. 1-7 Reset Timing**

**Table 1-4 Reset Time**

| Symbol | Time |
|---|---|
| $t_{RESETX}$ | >= 300us |

Note: It is better to connect a RESETX terminal and a DISOUTX terminal so that it avoids to compete bi-direction terminals in instability state after a power supply injection. If DISOUTX terminal is fixed "L" level, output driver of output terminal except CLKOUT terminal and bi-direction terminal becomes invalid.

A clock should continue supplying during operation. The NJU26501 has the PLL circuit. When supply of a clock is stopped, the NJU26501 is impossible for PLL to send a normal clock to an inside.

If supply of a clock is stopped or the NJU26501 is reset again, it requires locking PLL again. Putting a normal clock into CLK terminal, the period RESETX terminal of $t_{RESETX}$ is kept "L" level. Next, the NJU26501 is reset. Then redo from initial setting.

**2 System Clock**

Audio data samples must be transferred in synchronism between all components of the digital audio system. That is, for each audio sample originated by an audio source there must be one and only one audio sample processed by the NJU26501 and delivered to the D/A converters. To accomplish this, one device in the system is selected to generate the audio sample rate; the other devices are designated to follow this sample rate. The device that generates the audio sample rate is called the MASTER device; all devices following this sample rate are called SLAVE(s)

Although the NJU26501 is usually used as a slave device, it can also be used as MASTER device. The clock frequency supplied to the NJU26501 is 24.576MHz. When the NJU26501 is in MASTER mode, the NJU26501 can generate a required system clock to 48MHz of sampling frequency.

**NOTICE**

**The clock frequency of 24.576MHz(48KHz x 512) should be supplied to the NJU26501. The NJU26501 employs PLL circuit and divider circuit for Master mode inside. These circuits are designed for 24.576MHz clock frequency. If the clock frequency does not meet the clock frequency specification, this causes possibility of the next troubles. For example, PLL is out of lock. The NJU26501 cannot process the decoding correctly.**

## 2.1 Audio Clock

Three types of clock signals are included in the serial audio interface. Two of the clock signals LR (LRI and LRO) and BCK (BCKI and BCKO) establish data transfer on the serial data lines. The third clock, MCK and MCK2 , is not associated with serial data transfer but is required by delta-sigma A/D and D/A converters. In the NJU26501, it has two kinds of output terminals of MCK and MCK2 so that it may be properly used by apprications.

The frequency of the LR clock is, by definition, equal to the digital audio sample rate, Fs. BCK and MCK operate at multiples of the LR clock rate. Therefore the signals LR, BCK and MCK/MCK2 must be locked, that is, they must be generated or derived from a single frequency reference.

When RESETX is “L”, the NJU26501 dose not generate MCK clock. In “H”, the clock signal divided CLK in half is generated to MCK.

In case of MCKENX=”L”, buffered CLK is generated to MCK2. In case of MCKENX=“H”, CLK does not generate MCK2 by changing a terminal into a high impedance state.

**Table2-1 Sampling Frequency and BCK, MCK, CLK**

| Mode | Clock Signal | Multiple Frequency | 32Khz | 44.1kHz | 48kHz |
|---|---|---|---|---|---|
| Slave | LR | 1Fs | 32kHz | 44.1kHz | 48kHz |
| | BCK(32Fs) | 32Fs | 1.024MHz | 1.4112MHz | 1.536MHz |
| | BCK(64Fs) | 64Fs | 2.048MHz | 2.822MHz | 3.072MHz |
| Master | LR | 1Fs @Fs=48KHz | 48kHz | | |
| | BCK(32Fs) | 32Fs @Fs=48KHz | 1.536MHz | | |
| | BCK(64Fs) | 64Fs @Fs=48KHz | 3.072MHz | | |
| | MCK(256Fs) from DSP | 256Fs @Fs=48KHz | 12.288MHz | | |
| | MCK2(512Fs) from DSP* | 512Fs @Fs=48KHz | 24.576MHz | | |
| | CLK | 512Fs @Fs=48KHz | 24.576MHz | | |

* Set MCK2ENX=Low

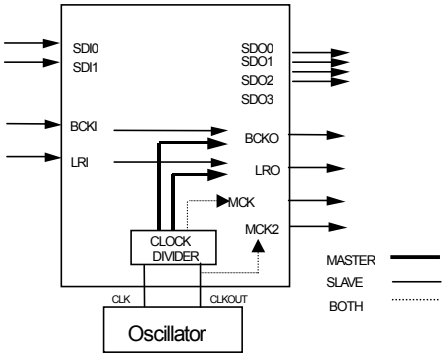



**Fig. 2-1 MASTER / SLAVE Mode**

## 3. Audio Interface

The serial audio interface carries audio data to and from the NJU26501. Industry standard serial data formats of $I^2S$, MSB-first left-justified or MSB-first right-justified are supported. These serial audio formats define a pair of digital audio signals (stereo audio) on each data line. Two clock lines, BCK (bit clock) and LR (left/right word clock) establish timing for serial data transfers. Serial audio data which synchronized with two kinds of clocks spreads on a system by SDI/SDO.

The NJU26501 serial audio interface includes 2 data input lines: SDI0/SDI1 and 4 data output lines: SDO0 to SDO3 as shown in the figure below. The input serial data is selected by the firmaware command.

**Table 3-1 Serial Audio Output Pin Description**

| Symbol | Pin No. | Description |
|---|---|---|
| SDO0 | 44 | Back Surround (BL/BR) Output |
| SDO1 | 43 | Front (L/R) Output(*) |
| SDO2 | 42 | Center/Sub Woofer (C/SW) Output |
| SDO3 | 41 | Surround (LS/RS) Output |

(*) In Virtual Dolby Surround mode, only front Lch/Rch outputs are active. The other channels are muted.

The NJU26501 has a pair of bit clock lines (BCKI and BCKO) and a pair of left/right clock lines (LRI and LRO). The clock inputs BCKI and LRI are used to accept timing signals from an external device when the NJU26501 operates in SLAVE mode.

The clock outputs BCKO and LRO are provided for delta-sigma A/D and D/A converters when the NJU26501 operates in MASTER mode. In SLAVE mode, the output of BCKO and LRO are the buffered output of BCKI and LRI, In SLAVE mode, the NJU26501 does not generate MCK clock and fixes MCK to “L”.

The MCK always generates half of the system clock supplied to the NJU26501 expect RESET sequence. In MCK2ENX=”L”, the MCK2 is always buffered output of system clock supplied to the NJU26501. In MCK2ENX=”H”, the MCK2 is high impedance output. In MASTER mode, the MCK/MCK2 and BCKO/LRO synchronize.

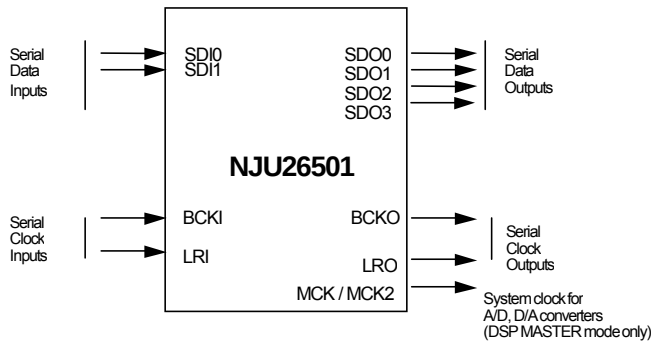



**Fig. 3-1 Serial Audio Interface**

### 3.1 Audio Data Format

The NJU26501 can exchange data using any of three industry-standard digital audio data formats: $I^2S$, MSB-first Left-justified, or MSB-first Right-justified.

The three serial formats differ primarily in the placement of the audio data word relative to the LR clock. Left-justified format places the most-significant data bit (MSB) as the first bit after an LR transition. $I^2S$ format places the most-significant data bit (MSB) as the second bit after an LR transition (one bit delay relative to left-justified format). Right-justified format places the least-significant data bit (LSB) as the last bit before an LR transition. All formats transmit the stereo sample left channel first. Note that polarity of LR is opposite in $I^2S$ format (LR:LOW = Left channel data) compared to Left-Justified or Right-Justified formats.

Clock LR (LRI, LRO) marks data word boundaries and clock BCK (BCKI, BCKO) clocks the transfer of serial data bits. One period of LR defines a complete stereo audio sample and thus the rate of LR equals the audio sample rate (Fs).

The number of BCK clock must follow the serial data format. If the BCK clock is not enough , the right sound are not produced. The serial data format should be the same as A/Ds ,D/As or Codecs which are used.

The NJU26501 supports serial data format which includes 32(32fs) or 64(64fs) BCK clocks. This serial data format is applied to both MASTER and SLAVE mode.

### 3.2 Serial Audio Data Transmitting Diagram

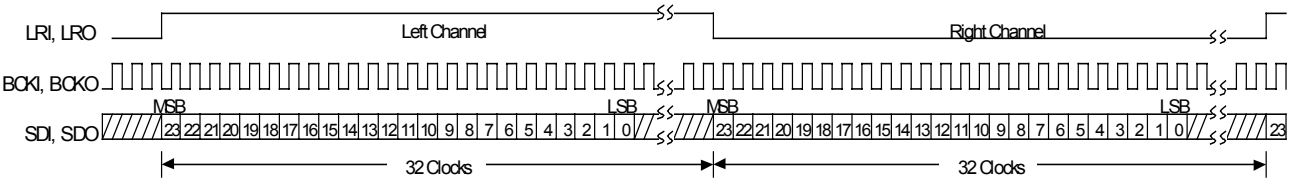



**Fig. 3-2 Left-Justified Data Format 64Fs, 24bit Data**

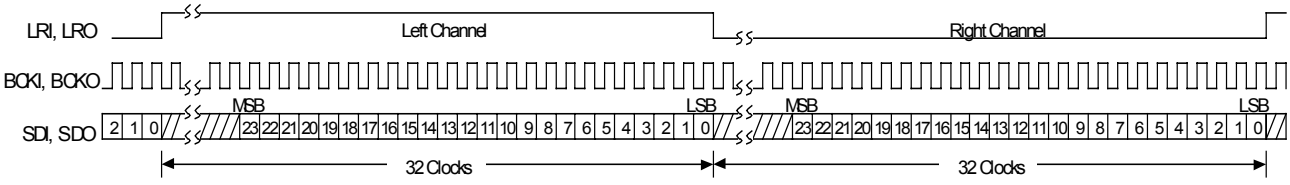



**Fig. 3-3 Right-Justified Data Format 64Fs, 24bit Data**

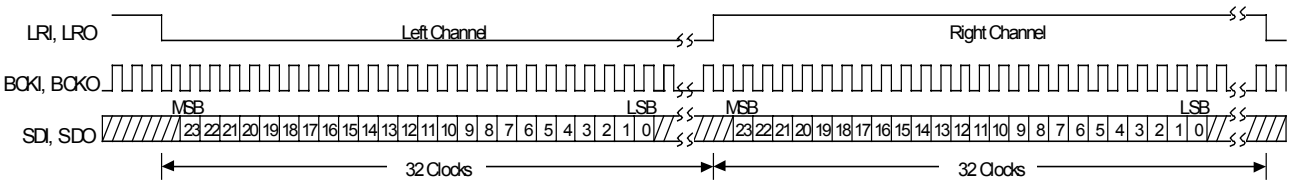



**Fig. 3-4 $I^2S$ Data Format 64Fs, 24bit Data**

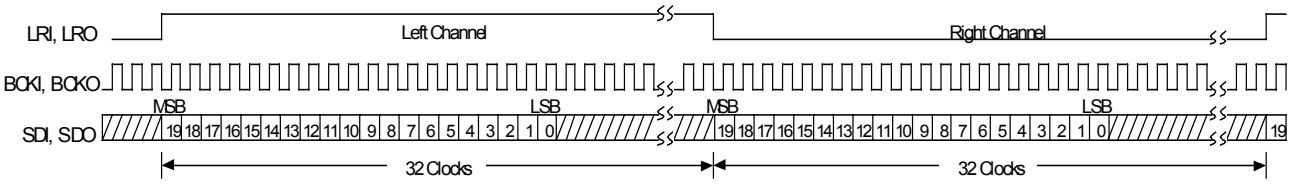



**Fig. 3-5 Left-Justified Data Format 64Fs, 20bit Data**

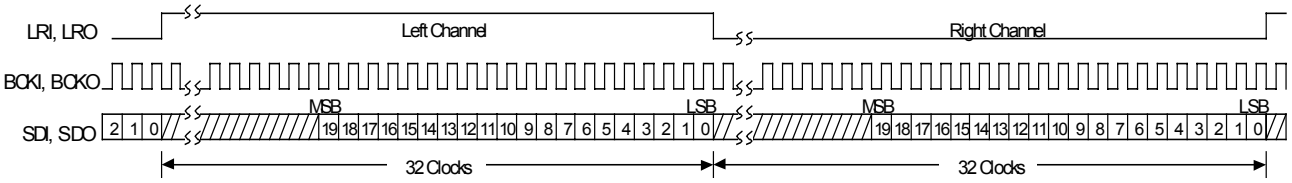



**Fig. 3-6 Right-Justified Data Format 64Fs, 20bit Data**

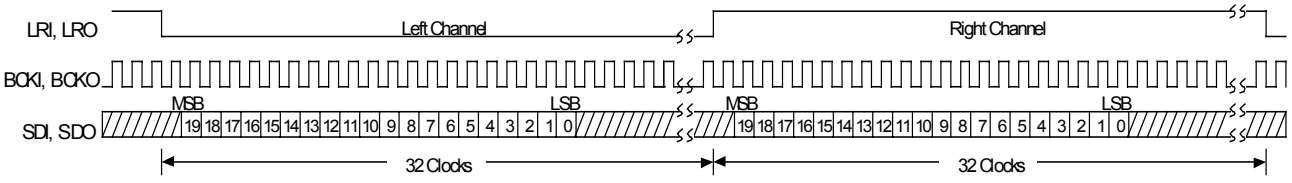



**Fig. 3-7 $I^2S$ Data Format 64Fs, 20bit Data**

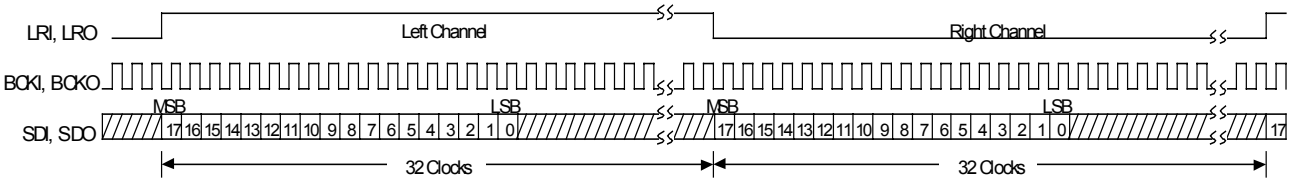



**Fig. 3-8 Left-Justified Data Format 64Fs, 18bit Data**

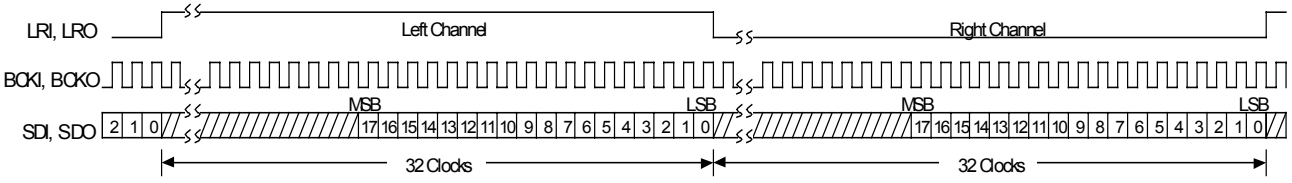



**Fig. 3-9 Right-Justified Data Format 64Fs, 18bit Data**

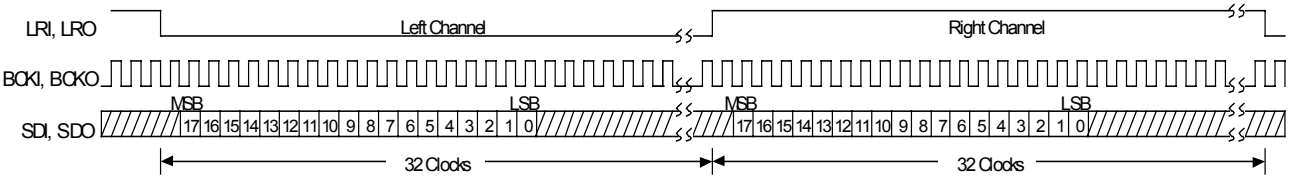



**Fig. 3-10 $I^2S$ Data Format 64Fs, 18bit Data**

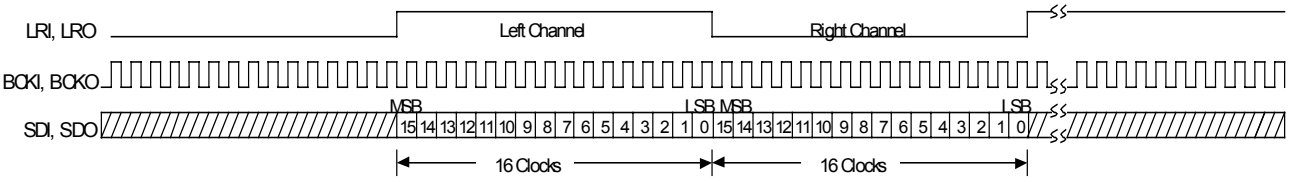



**Fig. 3-11 Left-Justified Data Format 32Fs, 16bit Data**

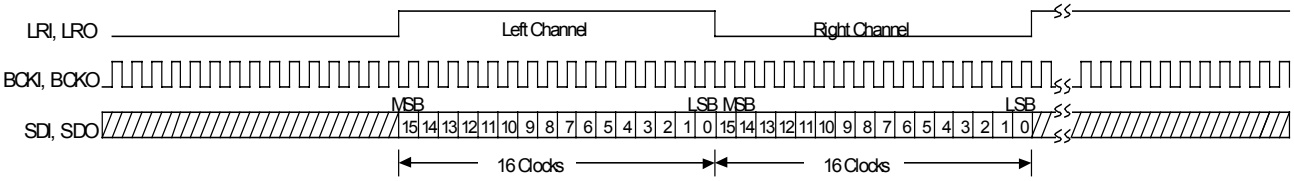



**Fig. 3-12 Right-Justified Data Format 32Fs, 16bit Data**

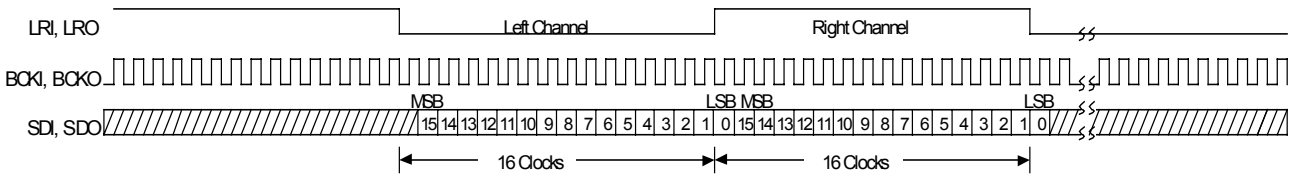



**Fig. 3-13 $I^2S$ Data Format 32Fs, 16bit Data**

### 3.3 Serial Audio Timing

**Table 3-2 Serial Audio Input Timing Parameters**

**($V_{DD}$=$V_{DDPLL}$=1.8V, $V_{DDIO}$=$V_{DDO}$=3.3V, $f_{OSC}$=24.576MHz, Ta=25°C)**

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| BCKI Frequency | | | - | - | 4.0 | MHz |
| BCKI Period | | | | | | |
| L Pulse Width | $t_{SIL}$ | | 85 | | | |
| H Pulse Width | $t_{SIH}$ | | 85 | - | - | ns |
| BDKI to LRI Time | $t_{SLI}$ | | 40 | - | - | ns |
| LRI to BCKI Time | $t_{LSI}$ | | 40 | - | - | ns |
| Data Setup Time | $t_{DS}$ | | 40 | - | - | ns |
| Data Hold Time | $t_{DH}$ | | 40 | - | - | ns |

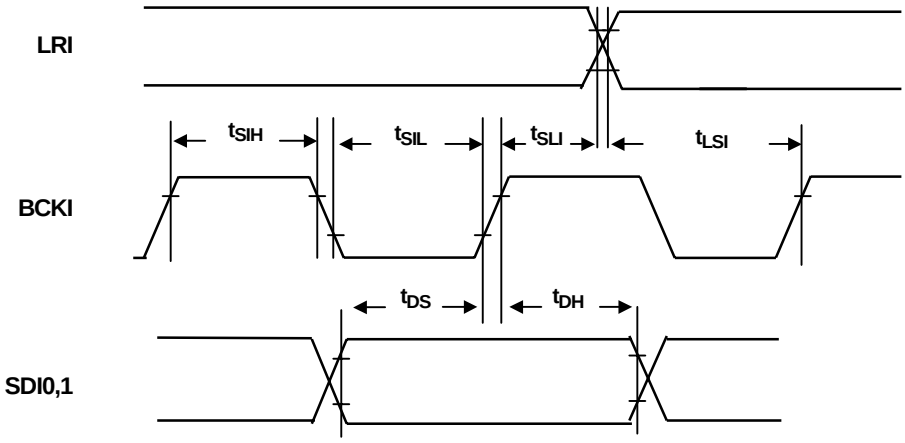



**Fig. 3-14 Serial Audio Input Timing**

**Table 3-3 Serial Audio Output Timing Parameters**

**($V_{DD}$=$V_{DDPLL}$=1.8V, $V_{DDIO}$=$V_{DDO}$=3.3V, $f_{OSC}$=24.576MHz, Ta=25°C)**

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| BCKO to LRO Time | $t_{SLO}$ | $C_L$:LRO, BCKO, SDO=25pF | 20 | - | - | ns |
| LRO to BCKO Time | $t_{LSO}$ | | 20 | - | - | ns |
| Data Output Delay | $t_{DOD}$ | | - | - | 20 | ns |

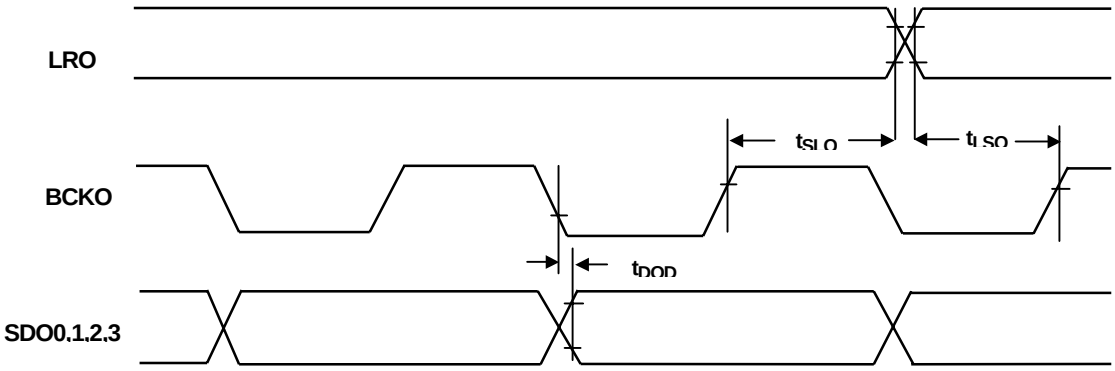



**Fig. 3-15 Serial Audio Output Timing**

**Table 3-4 Serial Audio Clock Parameters (SLAVE mode)**

**($V_{DD}$=$V_{DDPLL}$=1.8V, $V_{DDIO}$=$V_{DDO}$=3.3V, $f_{OSC}$=24.576MHz, Ta=25°C)**

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| LRI to LRO Delay | $t_{PDL}$ | $C_L$:LRO, BCKO, SDO=25pF DSP Slave mode | - | - | 20 | ns |
| BCKI to BCKO Delay | $t_{PDB}$ | | - | - | 20 | ns |

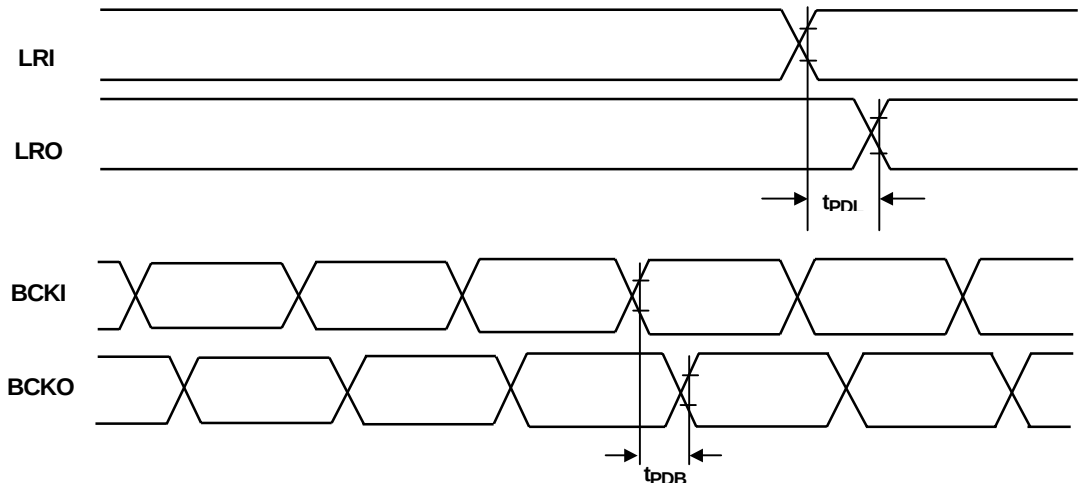



**Fig. 3-16 Serial Audio Clock Timing (SLAVE mode)**

**Table 3-5 Serial Audio Clock Parameters (MASTER mode)**

**($V_{DD}$=$V_{DDPLL}$=1.8V, $V_{DDIO}$=$V_{DDO}$=3.3V, $f_{OSC}$=24.576MHz, Ta=25°C)**

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| CLK to MCK2 Delay | $t_{PDM2}$ | $C_L$:LRO, BCKO, MCK, MCK2=25pF DSP Master mode MCK2ENX="L" CLK:$r_{EC}$=50% | - | - | 20 | ns |
| MCK2 to MCK, BCKO, LRO Delay | $t_{PDM}$ | | -20 | - | 20 | ns |
| Output Clock Duty Cycle | $r_{EM}$ | | 45 | 50 | 55 | % |

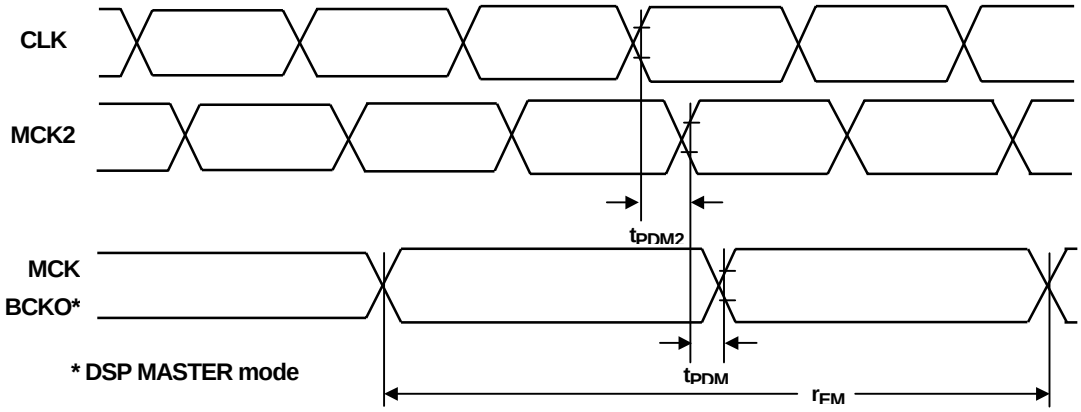



**Fig. 3-17 Serial Audio Clock Timing (MASTER mode)**

## 4. Host Interface

The NJU26501 can be controlled via Serial Host Interface (SHI) using either of two serial bus format : 4-Wire serial bus or $I^2C$ bus. Data transfers are in 8 bit packets (1 byte) when using either format. The SHI operates only in a SLAVE fashion. A host controller connected to the interface always drives the clock (SCL / SCK) line and initiates data transfers, regardless of the chosen communication protocol.

The SEL1 pin controls the serial bus mode. When the SEL1 is low during the NJU26501 initialization, 4-Wire serial bus is available. When the SEL1 is high during the NJU26501 initialization, $I^2C$ bus is available.

**Table 4-1 Serial Host Interface Pin Description**

| Symbol (Serial/$I^2C$) | Pin No. | 4-Wire Serial bus Format | $I^2C$ bus Format |
|---|---|---|---|
| SCK/SCL | 28 | Serial Clock | Serial Clock |
| SDOUT/SDA | 29 | Serial Data Output | Serial Data |
| SDIN/AD1 | 30 | Serial Data Input | $I^2C$ bus address Bit1 |
| SSX/AD2 | 31 | SLAVE Select | $I^2C$ bus address Bit2 |

Note : When 4-Wire Serial bus is selected, SDA /SDOUT pin is CMOS output. When $I^2C$ is selected, this pin is a bi-directional open drain. This pin, which is assigned for $I^2C$, requires a pull-up resister.

### 4.1 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL1="H" during the Reset Sequence initialization. SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin.

Data transfers are MSB first and are enabled by setting SSX = "L". Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte(MSB) which is latched on the falling transitions of SSX. SDOUT is always CMOS output. SDOUT does not require a pull-up resistor.

**Table 4-2 4-Wire Serial Interface Timing Parameters**

**($V_{DD}$=$V_{DDPLL}$=1.8V, $V_{DDIO}$=$V_{DDO}$=3.3V, $f_{OSC}$=24.576MHz, Ta=25°C)**

| Parameter | Symbol | Timelines | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input Data Rising Time | $t_{MSDr}$ | a-b | - | - | 100 | ns |
| Input Data Falling Time | $t_{MSDf}$ | a-b | - | - | 100 | ns |
| Serial Clock Rising Time | $t_{MSCr}$ | d-e | - | - | 100 | ns |
| Serial Clock Falling Time | $t_{MSCf}$ | f-g | - | - | 100 | ns |
| Serial Strobe Rising Time | $t_{MSSr}$ | p-q | - | - | 100 | ns |
| Serial Strobe Falling Time | $t_{MSSf}$ | m-n | - | - | 100 | ns |
| Serial Clock H Duration | $t_{MSCa}$ | e-f | 0.5 | - | - | μs |
| Serial Clock L Duration | $t_{MSCn}$ | g-h | 0.5 | - | - | μs |
| Serial Clock Period | $t_{MSCc}$ | e-i | 1.0 | - | - | μs |
| Serial Strobe Setup Time | $t_{MSSs}$ | n-e | 0.5 | - | - | μs |
| Serial Strobe Hold Time | $t_{MSSh}$ | j-q | 0.5 | - | - | μs |
| Serial Strobe L Duration | $t_{MSSa}$ | n-p | - | 8.5 | - | μs |
| Serial Strobe H Duration | $t_{MSSn}$ | q-r | - | 1.0 | - | μs |
| Input Data Setup Time | $t_{MSDis}$ | b-e | 0.1 | - | - | μs |
| Input Data Hold Time | $t_{MSDih}$ | e-c | 0.1 | - | - | μs |
| Output Data Hold Time (from SCK) | $t_{MSDoh}$ | g-k | 0 | - | 0.25 | μs |
| Output Data Hold Time (from SSX) | $t_{MSDov}$ | n-o, q-l | 0 | - | 0.25 | μs |

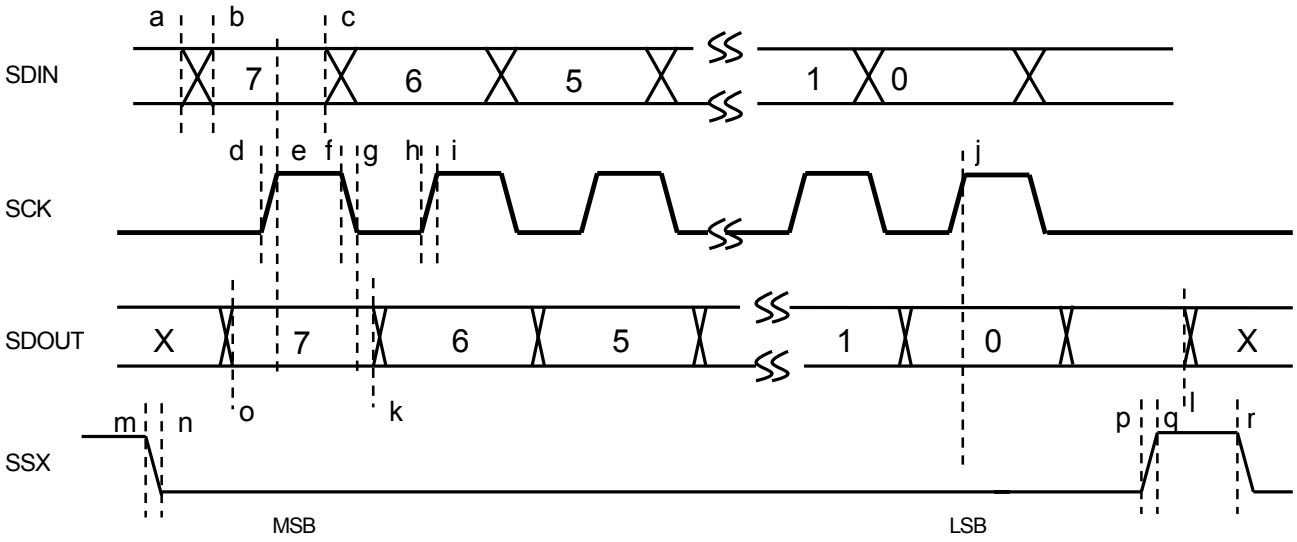



**Fig. 4-1 4-Wire Serial Interface Timing**

Note : When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSX="H".
When the data-clock is more than 8 clocks, the last 8 bit data becomes valid.
After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSX becomes "H".

### 4.2 I²C Bus

When the NJU26501 is configured for I²C bus communication in SEL1="L", the serial host interface transfers data on the SDA pin and clocks data on the SCL pin. SDA is an open drain pin requiring a pull-up resistor. Pins AD1 and AD2 are used to configure the seven-bit SLAVE address of the serial host interface. This offers additional flexibility in a system design by offering two different possible SLAVE addresses for which the NJU26501 will respond to.

An address can be arbitrarily set up with an internal setup and this AD1 terminal. In the NJU26501, AD2 pin should be connected to "H". Any I²C address could be chosen for AD1. The I²C address of AD1 is decided by connection of AD1-pin. The I²C address should be the same level of AD1-pin

.

**Table 4-3 I²C Bus SLAVE Address**

| bit7 | bit6 | bit5 | bit4 | Bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | AD2*1 | AD1*2 | R/W |

*1 AD2 pin should be connected to "H". The I²C address of AD2 should be 1.

*2 SLAVE address is 0 when AD1 is "L". SLAVE address is 1 when AD1 is "H".

The figure on the following shows the basic timing relationships for transfers. A transfer is initiated with a START condition, followed by the SLAVE address byte. The SLAVE address consists of the seven-bit SLAVE address followed by a read/write (R/W) bit. When an address with an effective serial host interface is detected, the acknowledgement bit which sets a SDA line to "L" in the ninth bit clock cycle is returned.

The R/W bit in the SLAVE address byte sets the direction of data transmission until a STOP condition terminates the transfer. R/W = 0 indicates the host will send to the NJU26501 while R/W = 1 indicates the host will receive data from the NJU26501.

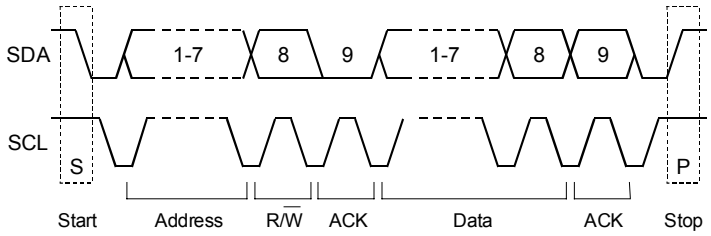



**Fig. 4-2 I²C Bus Format**

In case of the NJU26501, only single-byte transmission is available.
The serial host interface supports "Standard-Mode (100kbps)" and "Fast-Mode (400kbps)" I²C bus data transfer.
However, the NJU26501 is not completely based on I²C bus specification from the characteristic of a SDA I/O terminal and a SCL input terminal.

**Table 4-4 $I^2C$ Bus Interface Timing Parameters**

**($V_{DD}$=$V_{DDPLL}$=1.8V, $V_{DDIO}$=$V_{DDO}$=3.3V, $f_{OSC}$=24.576MHz, Ta=25°C)**

| Parameter | Symbol | Standard Mode | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| SCL Clock Frequency | $f_{SCL}$ | 0 | 400 | kHz |
| Start Condition Hold Time | $t_{HD:STA}$ | 0.6 | - | μs |
| SCL "L" Duration | $t_{LOW}$ | 1.3 | - | μs |
| SCL "H" Duration | $t_{HIGH}$ | 0.6 | - | μs |
| Start Condition Setup Time | $t_{SU:STA}$ | 0.6 | - | μs |
| Data Hole Time | $t_{HD:DAT}$ | 0.1 | 0.9 | μs |
| Data Setup Time | $t_{SU:DAT}$ | 250 | - | ns |
| Rising Time | $t_R$ | - | 1000 | ns |
| Falling Time | $t_F$ | - | 300 | ns |
| Stop Condition Setup Time | $t_{SU:STO}$ | 0.6 | - | μs |
| Bus Release Time | $t_{BUF}$ | 1.3 | - | μs |

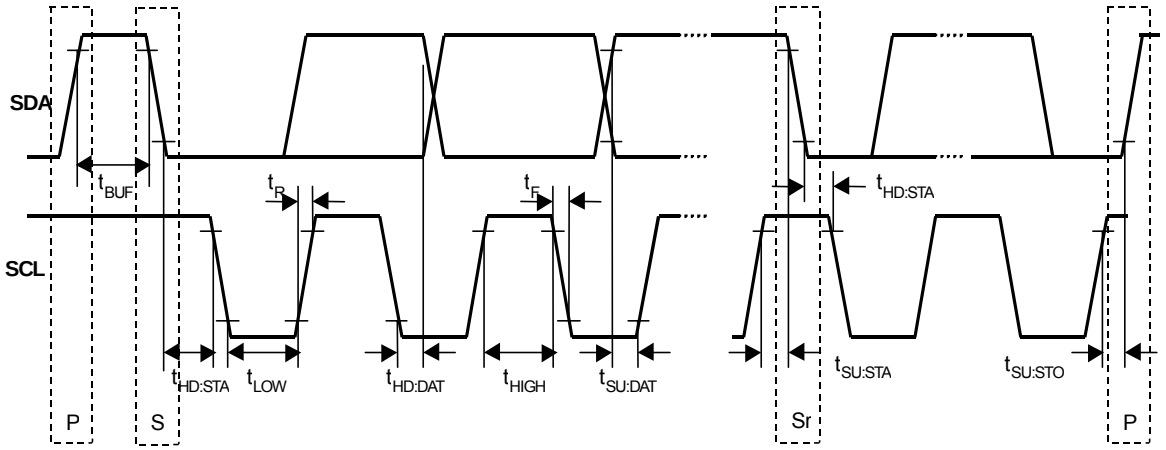



**Fig. 4-3 $I^2C$ Bus Timing**

Note : The NJU26501 has similar protocol as $I^2C$ bus specification from the characteristic of a SDA I/O terminal and a SCL input terminal. Check the bus driver of other devices intermingled into the same bus has bus drive capability.

$t_{HD:DAT}$: Keep Data Hold Time to avoid indefinite state by SCL falling edge.

This item shows the interface specification.

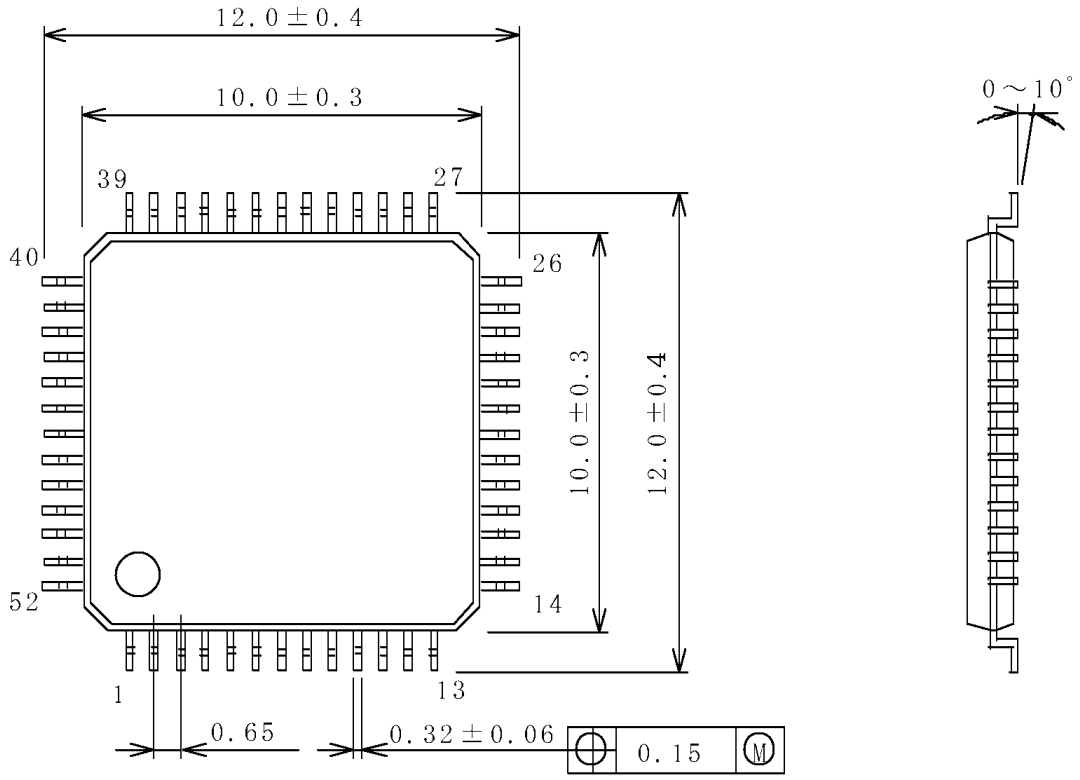
## 5. Firmware Command Table

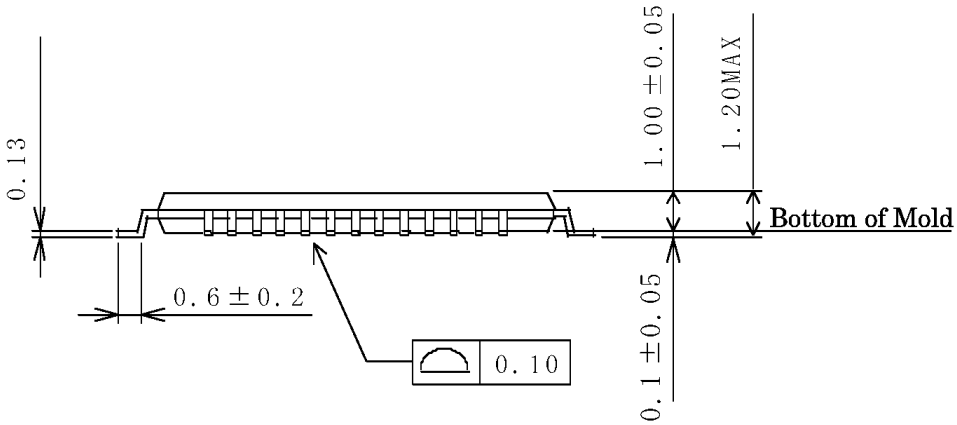
The NJU26501 allows for user configuration of the decoder with micro controller commands entered via Host interface (serial interface or $I^2C$ bus). The following table summarizes the available user commands.

**Table5-1 NJU26501 Command**

| No. | Command System | Command Description |
|---|---|---|
| 1 | Set Task Command | Select Decode Mode :<br>Dolby Digital, DTS, PCM, Noise Generator, etc. |
| 2 | AC3 Decode Command | Select Dolby Digital Decode Mode :<br>Dynamic Range Control, Compression Mode, Dual Mode. |
| 3 | PCM Scale Command | Set PCM Scale Factor. |
| 4 | Maximum Frame Repeat Command | Set repeat times of valid data in case of error. |
| 5 | Pro Logic II Command | Set Pro Logic II parameters :<br>Decode mode, Panorama mode, Sample Rate, Center Width, Dimension, etc. |
| 6 | Bass Management Command | Set Bass Management parameters :<br>Speaker Size, Speakers Cutoff Frequencies. |
| 7 | Delay Command | Set Delay parameters for Center and Surround. |
| 8 | Pink Noise Generator Command | Select Noise Generator : L, R, C, LS ,RS, BL, BR. |
| 9 | Play Command | PLAY the setup environment after “STOP” command is issued. |
| 10 | Stop Command | Stop the operation and mute outputs until PLAY is issued. |
| 11 | Mute Command | Mute function |
| 12 | Unmute Command | Unmute function |
| 13 | AC3 Status Read Command | Read Command to receive Dolby Digital Decode status information. |
| 14 | Version Number Command | Check Firmware Version Number. |
| 15 | Audio Interface Configuration Command | Set Serial Audio Interface parameters. |
| 16 | NOP Command | This command is used to check DSP status. |
| 17 | READ Command | READ Command |
| 18 | Read Task Command | Read DSP status information. |
| 19 | Input Select Command | Select Serial Input port: SDI0 or SDI1. |
| 20 | Bass Management Trimmer Command | Set Bass Management trimmer parameters : L, R, C, LS, RS, SW. |
| 21 | Karaoke Command | Set Karaoke parameters : Aware mode, Capable mode, etc. |
| 22 | Virtual Command | Select Speaker Degree: 15 or 20 degree. |
| 23 | DTS Status Read Command | Read DTS status information. |
| 24 | Bypass Mode Configuration Command | Select bypass output port: SDO0, SDO1, SDO2, SDO3. |
| 25 | Dolby Digital EX Mode Configuration Command | Set Dolby Digital EX mode configuration. |

## *Package Dimensions*




[CAUTION]
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Ver. 0.90