

DOT MATRIX LCD 64-OUT SEGMENT DRIVER

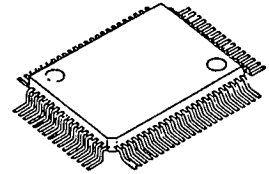
■ GENERAL DESCRIPTION

The NJU6417C is a serial input, 64-out segment driver for dot matrix LCDs, especially useful as extension driver for LCD controller drivers like NJU6408B.

It consists of 64-bit (two of 32-bit) shift register, 64-bit latch, and 64 high voltage LCD drivers.

The shift direction of each 32-bit shift register can be set independently to each other, consequently the efficient extension driver allocation according to the number of characters and easy wiring with the LCD panel can be performed.

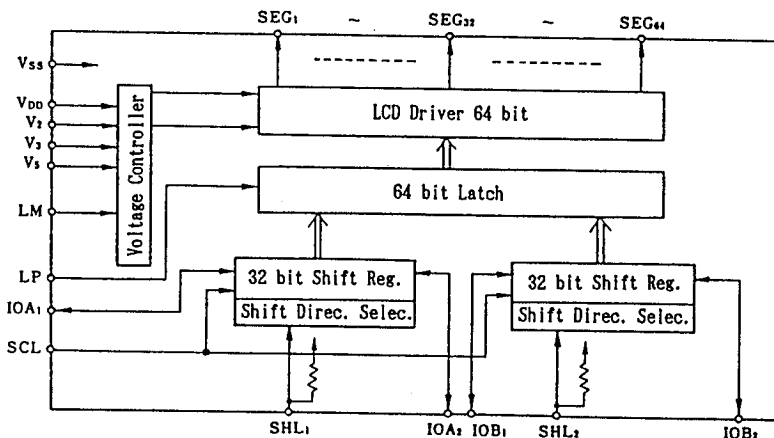
As the 64-driver have 4 level voltage inputs to drive the LCD, adjustable driving voltage according to the LCD panel can be supplied from the external power source.

■ PACKAGE OUTLINE


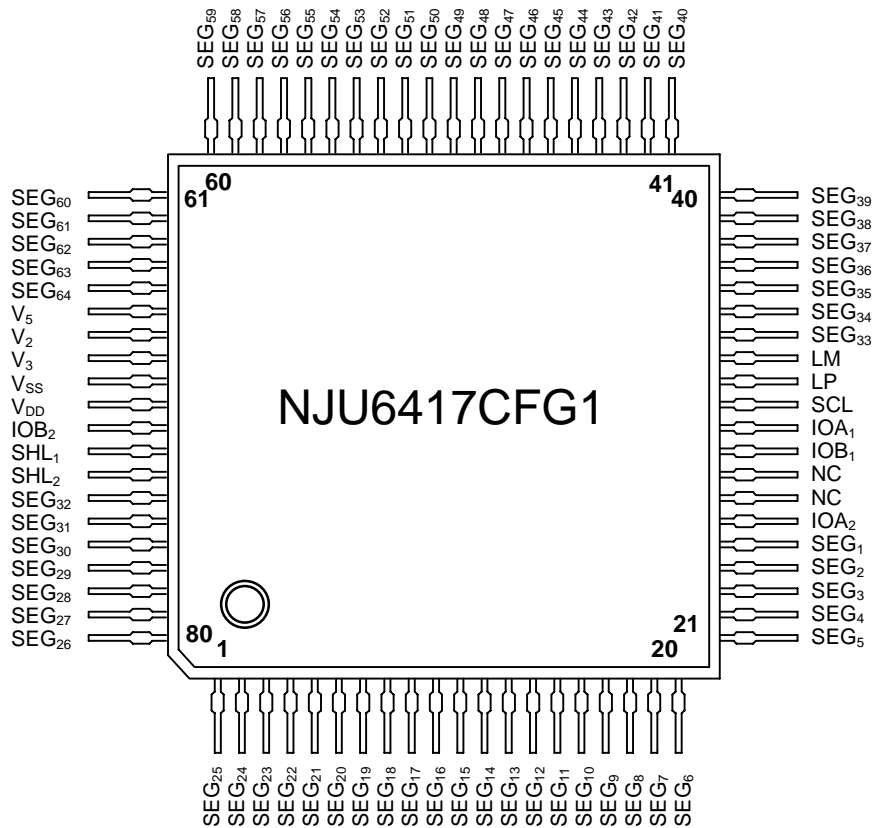
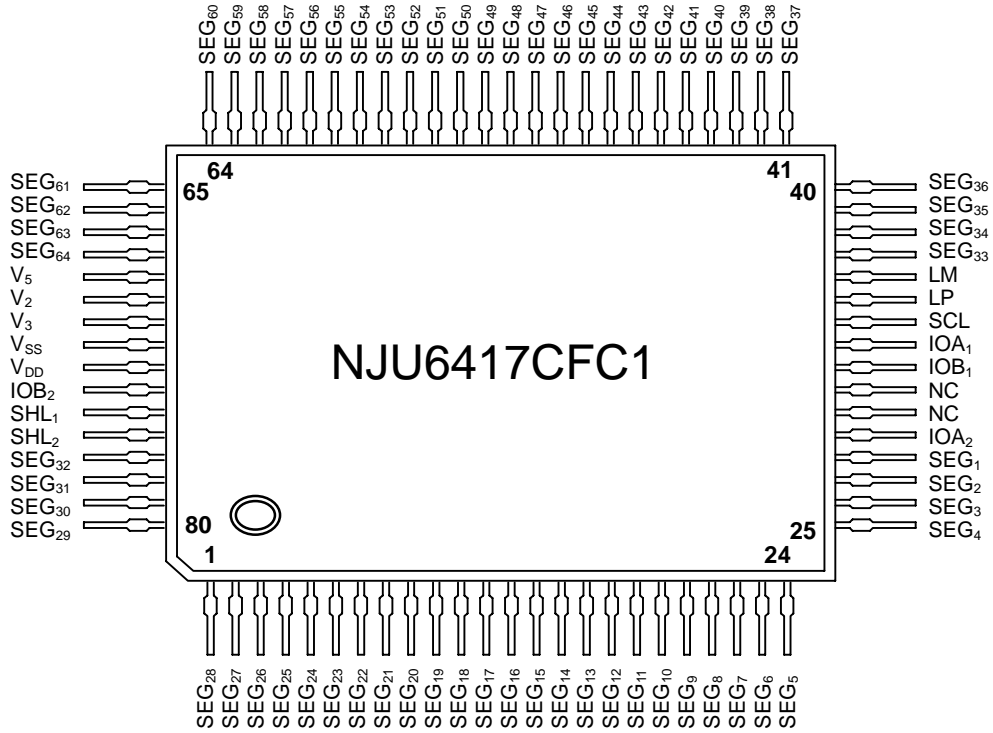
NJU6417CF

■ FEATURES

- 64 Segment Drivers
- 64-bit Shift Register
(Two of 32-bit Shift Registers)
- Shift Direction of each 32-bit
Shift Registers Selection
- Two of Shift Direction Select Terminal
- Duty Ratio 1/8 to 1/16
- Fast Data Transmission (Shift Clock 6 MHz max.)
- External Power Supply for LCD Driving Voltage
- LCD Driving Voltage --- $V_{DD} - 3V \sim V_{DD} - 13.5V$
- Operating Voltage --- $5V \pm 10\%$
- Package Outline --- QFP 80
- C-MOS Technology

■ BLOCK DIAGRAM


■ PIN CONFIGURATION



■ TERMINAL DESCRIPTION

No.		SYMBOL	FUNCTION
FC1	FG1		
1~28 37~68 77~80	1~25 34~65 74~80	SEG ₁ ~SEG ₆₄	LCD segment driving terminal. Each terminal corresponds to each bit of shift register.
29 33	26 30	IOA ₂ IOA ₁	Data input/output terminals for 1 st to 32 nd bits shift register. Display data is input (output) synchronized with clock pulse. Input or output is selected by SHL ₁ terminal.
32 74	29 71	IOB ₁ IOB ₂	Data input/output terminals for 33 rd to 64 th bits shift register. Display data is input (output) synchronized with clock pulse. Input or output is selected by SHL ₂ terminal.
34	31	SCL	Shift register clock pulse input terminal. The data is shifted in the shift register by the falling edge of the clock pulse. A data setup time and hold time are required between data input and SCL. Clock pulse rising time (T _{RS}) and falling time (T _{FS}) should be set less than 50ns respectively.
35	32	LP	Latch pulse input terminal. The data in the shift register is latched to the latch by this signal. "H" : Data writing, "L" : Data latch
36	33	LM	Alternate signal input for LCD driving.
69,70, 71	66,67, 68	V ₅ , V ₂ , V ₃	LCD driving power source terminals. V _{DD} ≥ V ₂ ≥ V ₃ ≥ V ₅ , V _{DD} ≥ V _{SS} ≥ V ₅
72 73	69 70	V _{SS} V _{DD}	Power supply terminal (connect to the controller's V _{SS} terminal) Power supply terminal (connect to the controller's V _{DD} terminal)
75	72	SHL ₁	Shift direction and input/output control terminal (Pull-up R) "H" or Open : Shift direction is from 1 st bit to 32 nd bit. "L" : Shift direction is from 32 nd bit to 1 st bit.
76	73	SHL ₂	Shift direction and input/output control terminal (Pull-up R) "H" or Open : Shift direction is from 33 rd bit to 64 th bit. "L" : Shift direction is from 64 th bit to 33 rd bit.
30,31	27,28	NC	Non connection.

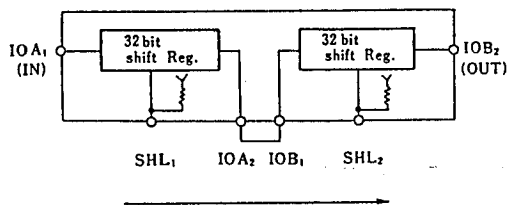
FUNCTIONAL DESCRIPTION
(1) Shift register control

The 64-bit shift register is divided into two of 32-bit shift register.

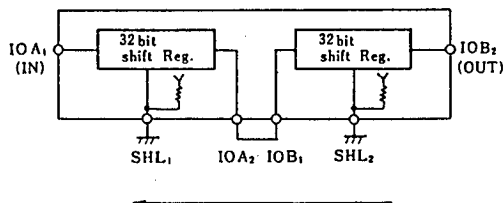
The shift direction of each 32-bit shift register can be set independently to each other shown in below.

Control Terminal	Input	Shift Direction
SHL ₁	"H" or Open	IOA ₁ → IOA ₂
	"L"	IOA ₁ ← IOA ₂
SHL ₂	"H" or Open	IOB ₁ → IOB ₂
	"L"	IOB ₁ ← IOB ₂

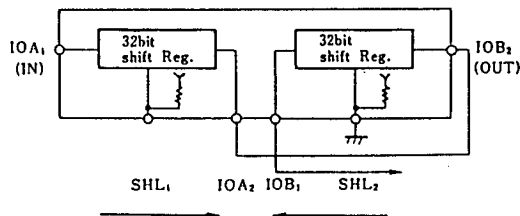
(1-1) When the terminals SHL₁ and SHL₂ are "H" or open, the data shift from SEG₁ to SEG₆₄.


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(1-2) When the terminals SHL₁ and SHL₂ are "L", the data shift from SEG₆₄ to SEG₁.



(1-3) Reversed shift direction to each other is also available.
 SEG₁ → SEG₃₂ → SEG₆₄ → SEG₃₃ example is shown in below:



(2) LCD driver output truth table.

Input Data	Selection/Non-selection	LM	Driver Output (SEG ₁ to SEG _{6,4})
"H"	Selection	H	V ₅
		L	V _{DD}
"L"	Non-selection	H	V ₃
		L	V ₂

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V _{DD}	- 0.3 ~ + 7.0	V
Supply Voltage (2) Note 1)	V _{DD} ~ V ₅	V _{DD} -13.5 ~ V _{DD} +0.3	V
Input Voltage	V _{IN}	- 0.3 ~ V _{DD} +0.3	V
Operating Temperature	Topr	- 30 ~ + 80	°C
Storage Temperature	Tstg	- 55 ~ + 150	°C

 Note 1) The relation : V_{DD} ≥ V₂ ≥ V₃ ≥ V₅ must be maintained.

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

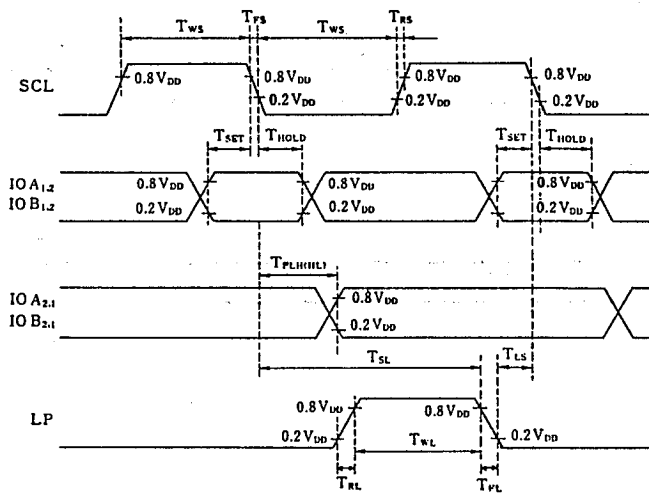
 (V_{DD}=5V±10% , Ta=-20 ~ +75°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
Input Voltage	V _{IH}	LM, LP, SHL ₁ , SHL ₂ Terminals	0.8V _{DD}		V _{DD}	V	
	V _{IL}				0.2V _{DD}		
Input Current	I _{IH1}	V _{IH} =V _{DD}	LM, LP Terminals		1	uA	
	I _{IL1}	V _{IL} =0V			- 1		
	I _{IH2}	V _{IH} =V _{DD}		SHL ₁ , SHL ₂ Terminals			1
	I _{IL2}	V _{IL} =0V			- 10		- 15
Output Voltage	V _{OH}	I _O =- 40uA	10A ₁ , 10A ₂ , 10B ₁ , 10B ₂ Terminals	4.2		V	
	V _{OL}	I _O = 400uA					0.4
Driver On-resistance	R _{ON}	I _d =0.05mA	SEG ₁ ~ SEG _{6,4} Terminals		30	kΩ	
Operating Current (Logic Part)	I _{SSO}	LM,LP=130us cycle, SCL=1.5MHz Every one bit Inverted Data. No Load.		0.85	1.2	mA	
Operating Current (LCD Driver Part)	I _{SSHO}	LM,LP=130us cycle, SCL=1.5MHz Every one bit Inverted Data. No Load.		70	100	uA	
LCD Driving Voltage	V _{LCD}	V _{DD} - V ₅	V _{DD} - 3.0		V _{DD} - 13.5	V	

• AC Characteristics

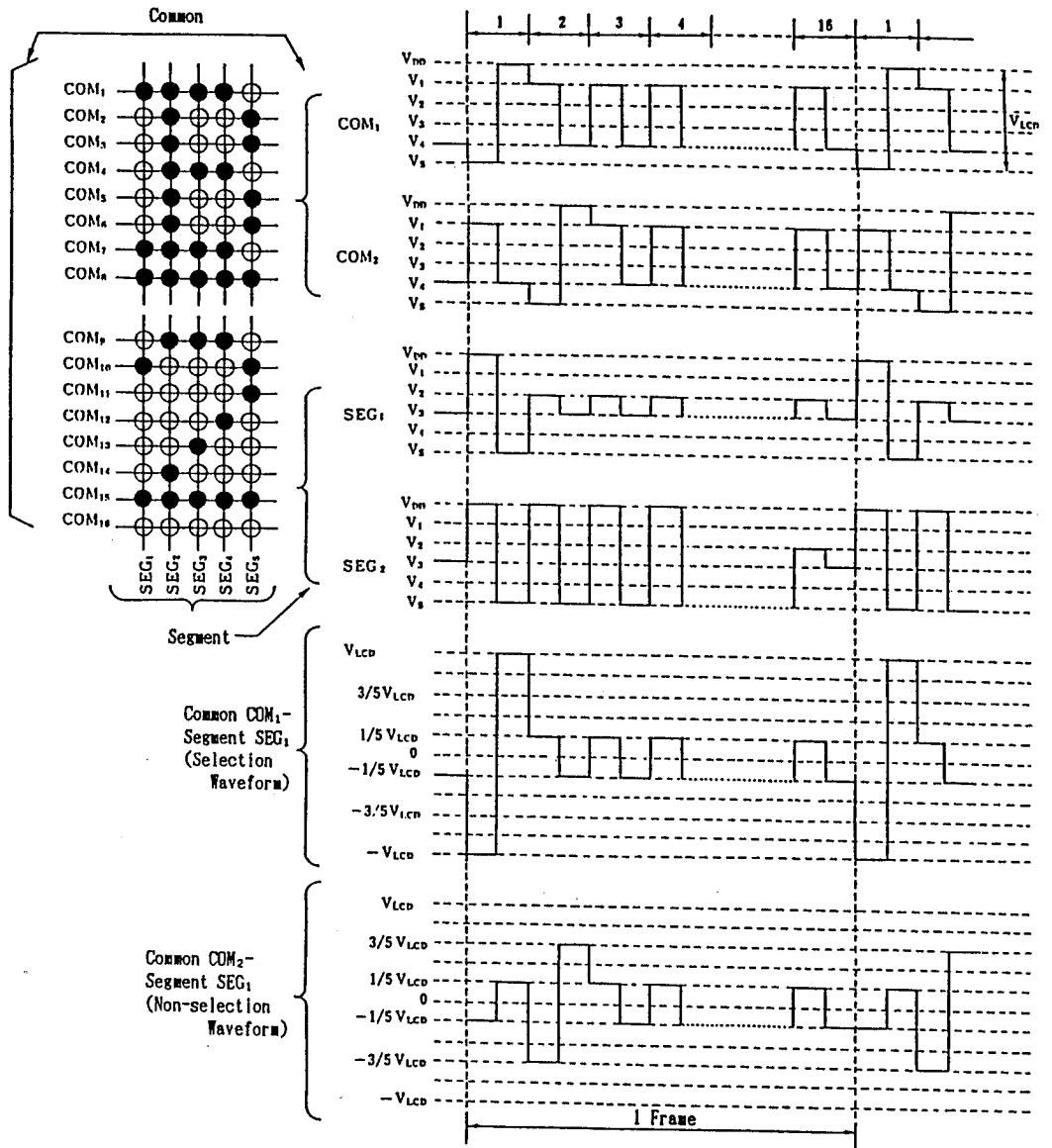
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time	$T_{PLH(HL)}$				150	ns
Maximum Operating Frequency	f_{SCL}	Duty = 50 %			6	MHz
SCL Pulse Width	T_{WS}		63			ns
LP Pulse Width	T_{WL}		110			ns
Set up Time	T_{SET}		50			ns
SCL → LP Time	T_{SL}		100			ns
LP → SCL Time	T_{LS}		0			ns
Data Hold Time	T_{HOLD}		30			ns
SCL Rise, Fall Time	T_{RS}, T_{FS}				50	ns
LP Rise, Fall Time	T_{RL}, T_{FL}				1	us

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LCD DRIVING WAVEFORM EXAMPLE

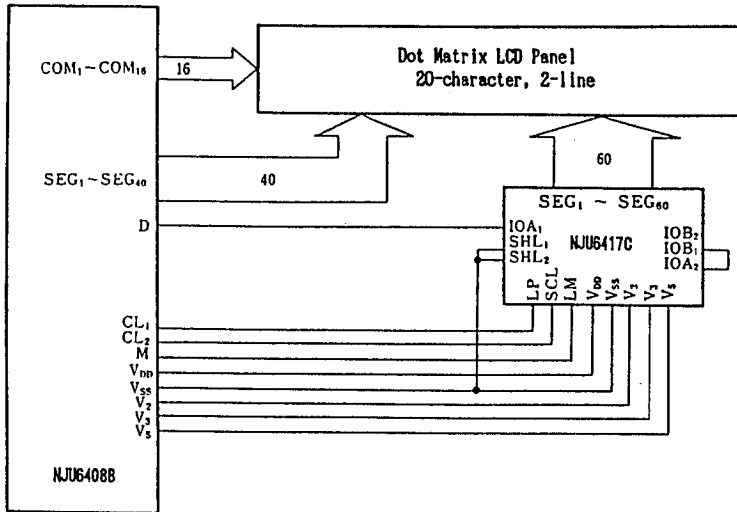
1/5 Bias, 1/16 Duty Ratio



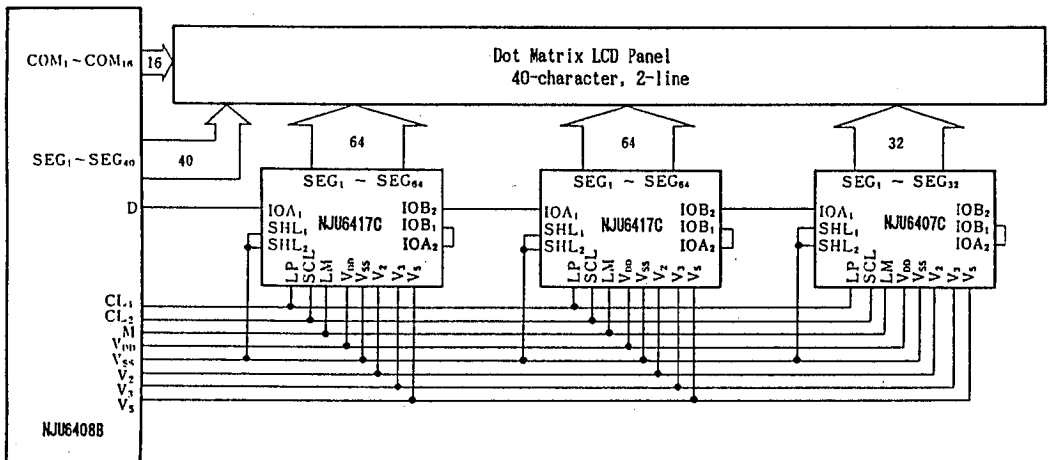
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APPLICATION CIRCUITS

(1) 20-character 2-line Display Example (Combine with NJU6408B)



(2) 40-character 2-line Display Example (NJU6408B + NJU6417C x 2 + NJU6407C)



MEMO

[CAUTION]

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