

# SP4T SWITCH GaAs MMIC

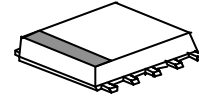
## GENERAL DESCRIPTION

NJG1519KC1 is a GaAs high power SP4T switch MMIC for antenna switch of dual mode cellular phone application such as GSM/DCS1800.

This switch is designed for an antenna switch between an antenna and one of two Tx ports or two Rx ports to control RF signals up to 2.5GHz.

The ultra small & ultra thin FLP10 package is applied.

## PACKAGE OUTLINE

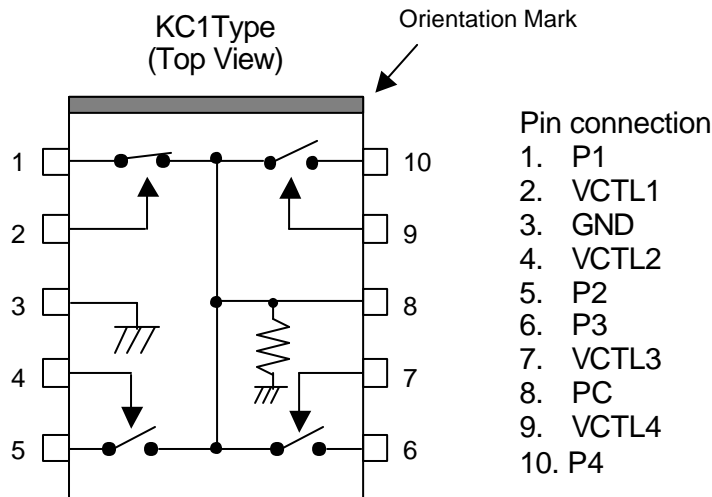


NJG1519KC1

## FEATURES

- Low voltage operation +2.5V min
- Pin at 0.2dB compression point 36dBm typ. @f=1.9GHz,  $V_{CTL}=3V$
- Low insertion loss 0.55dB typ. @f=0.9GHz,  $P_{IN}=34dBm$ ,  $V_{CTL}=3V$   
0.80dB typ. @f=1.9GHz,  $P_{IN}=32dBm$ ,  $V_{CTL}=3V$
- High isolation 24dB typ. @f=0.9GHz,  $V_{CTL}=3V$   
18dB typ. @f=1.9GHz,  $V_{CTL}=3V$
- Low control current 30uA typ. @f=0.9GHz,  $P_{IN}=34dBm$ ,  $V_{CTL}=3V$
- Ultra small & ultra thin package FLP10-C1 (Mount Size: 2.8x3.0x0.75mm)

## PIN CONFIGURATION



## TRUTH TABLE

ON Pass	VCTL1	VCTL2	VCTL3	VCTL4
PC-P1	H	L	L	L
PC-P2	L	H	L	L
PC-P3	L	L	H	L
PC-P4	L	L	L	H

NOTE: Please note that any information on this catalog will be subject to change.

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## ■ABSOLUTE MAXIMUM RATINGS

( $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	$P_{IN}$	$V_{CTL(L)}=0\text{V}$ , $V_{CTL(H)}=3\text{V}$	38	dBm
Operating Voltage	$V_{CTL}$	$V_{CTL(H)}-V_{CTL(L)}$	12	V
Power Dissipation	$P_D$		550	mW
Operating Temp.	$T_{opr}$		-40~+85	$^{\circ}\text{C}$
Storage Tempe.	$T_{stg}$		-55~+125	$^{\circ}\text{C}$

## ■ELECTRICAL CHARACTERISTICS

(General conditions:  $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ ,  $V_{CTL(L)}=0\text{V}$ ,  $V_{CTL(H)}=3\text{V}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Control Voltage (Low)	$V_{CTL(L)}$	$f=0.01\sim 2.5\text{GHz}$	-0.2	0	0.2	V
Control Voltage (High)	$V_{CTL(H)}$	$f=0.01\sim 2.5\text{GHz}$	2.5	3.0	6.5	V
Control Current	$I_{CTL}$	$f=0.9\text{GHz}$ , $P_{IN}=34\text{dBm}$	-	30	50	$\mu\text{A}$
Insertion loss 1	LOSS1	$f=0.9\text{GHz}$ , $P_{IN}=34\text{dBm}$	-	0.55	0.75	dB
Insertion loss 2	LOSS2	$f=1.9\text{GHz}$ , $P_{IN}=32\text{dBm}$	-	0.80	0.95	dB
Isolation 1	ISL1	$f=0.9\text{GHz}$ , $P_{IN}=34\text{dBm}$	22	24	-	dB
Isolation 2	ISL2	$f=1.9\text{GHz}$ , $P_{IN}=32\text{dBm}$	16	18	-	dB
Pin at 0.2dB Compression point	$P_{-0.2\text{dB}}$	$f=1.9\text{GHz}$	34	36	-	dBm
VSWR	$VSWR_i$	on-state ports, $f=1.9\text{GHz}$	-	1.4	1.6	
Switching time	$T_{SW}$	$f=0.1\sim 2.5\text{GHz}$	-	60	100	ns

## ■ TERMINAL INFORMATION

No.	SYMBOL	EXPLANATION
1	P1	RF port. This terminal is connected under the condition of 2pin- $V_{CTL(H)}$ (+2.5~+6.5V), 4, 7, 9pin- $V_{CTL(L)}$ (-0.2~+0.2V). A DC cut capacitor 56pF is required at this terminal to block DC voltage of inner circuit.
2	VCTL1	Control port1. Please connect bypass capacitor (10pF) between this terminal and GND close to this IC.
3	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
4	VCTL2	Control port2. Please connect bypass capacitor (10pF) between this terminal and GND close to this IC.
5	P2	RF port. This terminal is connected under the condition of 4pin- $V_{CTL(H)}$ (+2.5~+6.5V), 2, 7, 9pin- $V_{CTL(L)}$ (-0.2~+0.2V). A DC cut capacitor 56pF is required at this terminal to block DC voltage of inner circuit.
6	P3	RF port. This terminal is connected under the condition of 7pin- $V_{CTL(H)}$ (+2.5~+6.5V), 2, 4, 9pin- $V_{CTL(L)}$ (-0.2~+0.2V). A DC cut capacitor 56pF is required at this terminal to block DC voltage of inner circuit.
7	VCTL3	Control port3. Please connect bypass capacitor (10pF) between this terminal and GND close to this IC.
8	PC	Common RF port. This terminal is connected by the control voltage supplied to each control terminal (VCTL1~VCTL4 terminal). Please see the description of each terminal. A DC cut capacitor (56pF) is required at this terminal to block DC voltage of inner circuit. This terminal and GND are connected by high resistance (200K $\Omega$ ) to avoid unexpected signal output that is possibly generated right after burst signal switching.
9	VCTL4	Control port4. Please connect bypass capacitor (10pF) between this terminal and GND close to this IC.
10	P4	RF port. This terminal is connected under the condition of 9pin- $V_{CTL(H)}$ (+2.5~+6.5V), 2, 4, 7pin- $V_{CTL(L)}$ (-0.2~+0.2V). A DC cut capacitor 56pF is required at this terminal to block DC voltage of inner circuit.

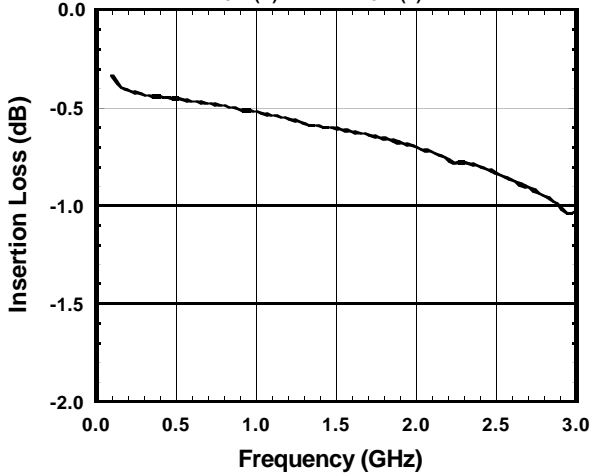
# NJG1519KC1

## ■ ELECTRICAL CHARACTERISTICS

( $f=100\text{MHz}\sim 3.0\text{GHz}$ , with application circuit, losses of external circuit are excluded)

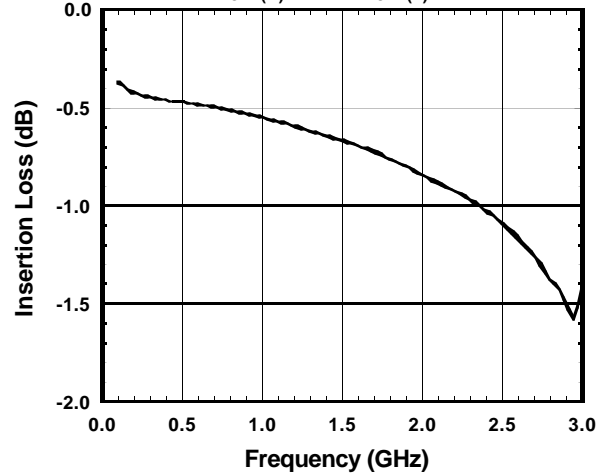
### PC-P1 Insertion Loss vs. Frequency

( $V_{\text{CTL(H)}}=3.0\text{V}$ ,  $V_{\text{CTL(L)}}=0\text{V}$ )



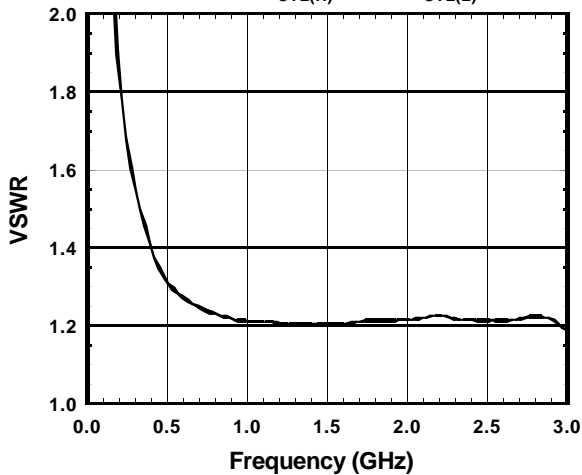
### PC-P4 Insertion Loss vs. Frequency

( $V_{\text{CTL(H)}}=3.0\text{V}$ ,  $V_{\text{CTL(L)}}=0\text{V}$ )



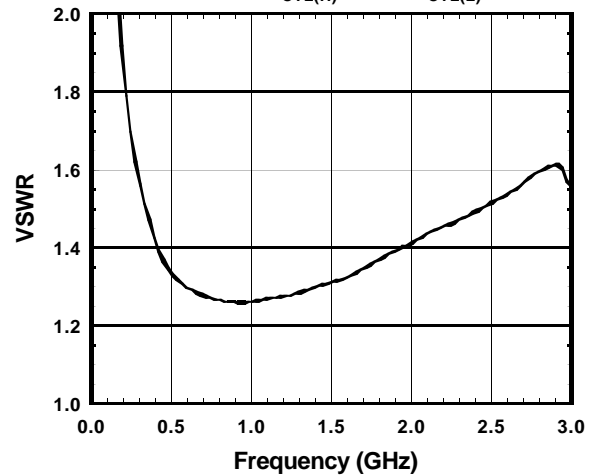
### VSWR(P1) vs. Frequency

(PC-P1 ON,  $V_{\text{CTL(H)}}=3.0\text{V}$ ,  $V_{\text{CTL(L)}}=0\text{V}$ )



### VSWR(P4) vs. Frequency

(PC-P4 ON,  $V_{\text{CTL(H)}}=3.0\text{V}$ ,  $V_{\text{CTL(L)}}=0\text{V}$ )

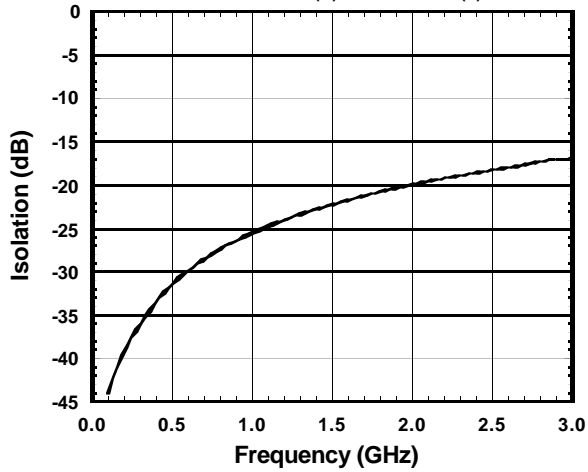


## ■ ELECTRICAL CHARACTERISTICS

(f=100MHz~3.0GHz, with application circuit, losses of external circuit are excluded)

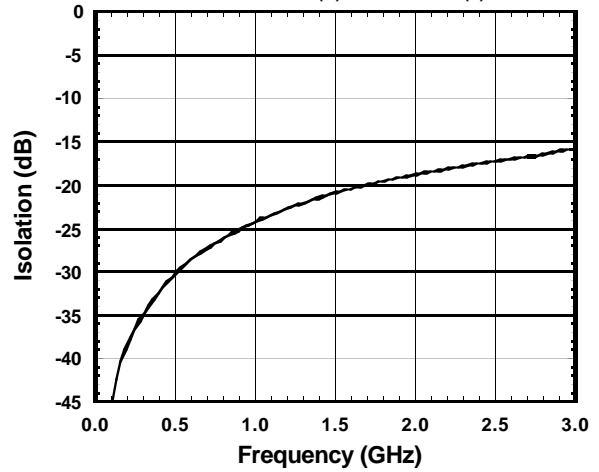
### PC-P1 Isolation vs. Frequency

(PC-P2 ON,  $V_{CTL(H)}=3.0V, V_{CTL(L)}=0V$ )



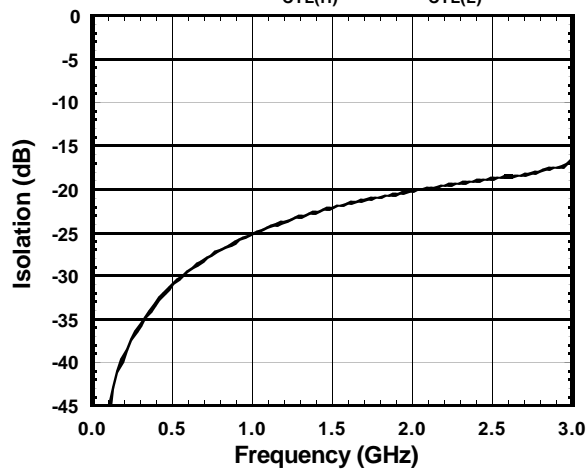
### PC-P2 Isolation vs. Frequency

(PC-P3 ON,  $V_{CTL(H)}=3.0V, V_{CTL(L)}=0V$ )



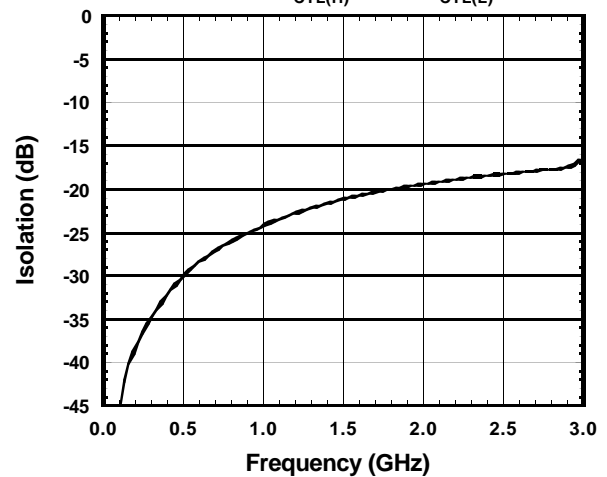
### PC-P3 Isolation vs. Frequency

(PC-P4 ON,  $V_{CTL(H)}=3.0V, V_{CTL(L)}=0V$ )



### PC-P4 Isolation vs. Frequency

(PC-P1 ON,  $V_{CTL(H)}=3.0V, V_{CTL(L)}=0V$ )

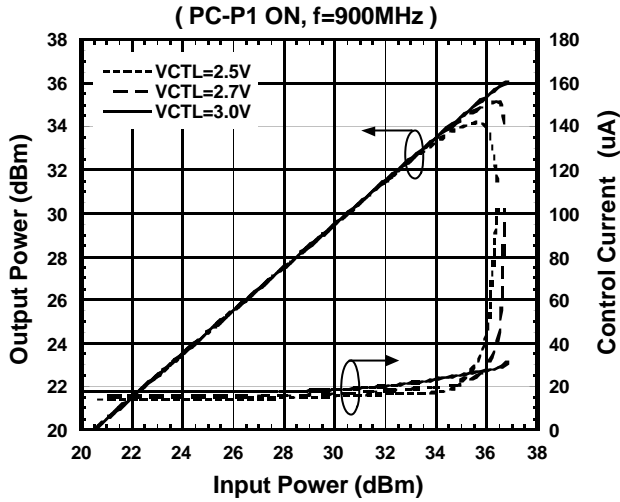


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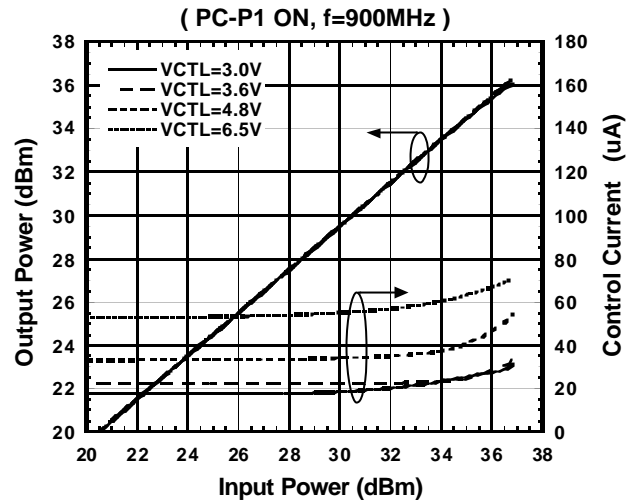
## ■ ELECTRICAL CHARACTERISTICS

(f=900MHz, with application circuit, losses of PCB, connector and DC blocking capacitor are excluded)

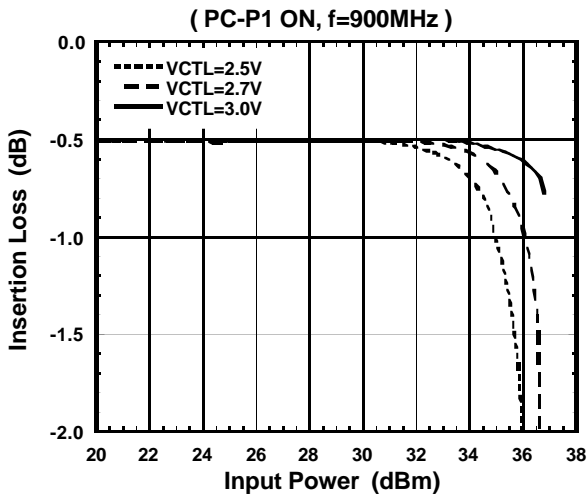
Output Power,Control Current vs. Input Power



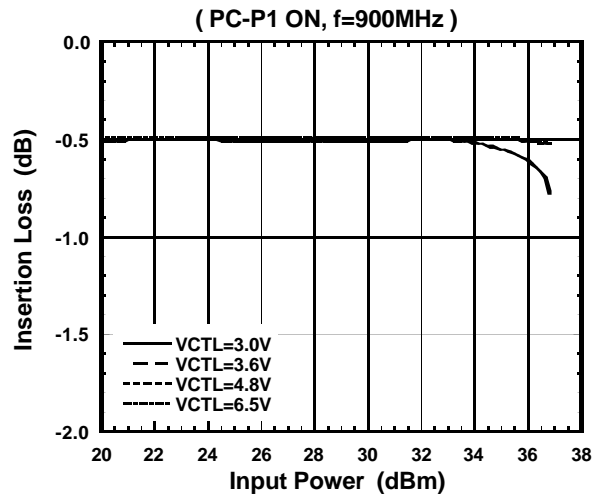
Output Power,Control Current vs. Input Power



Insertion Loss vs. Input Power



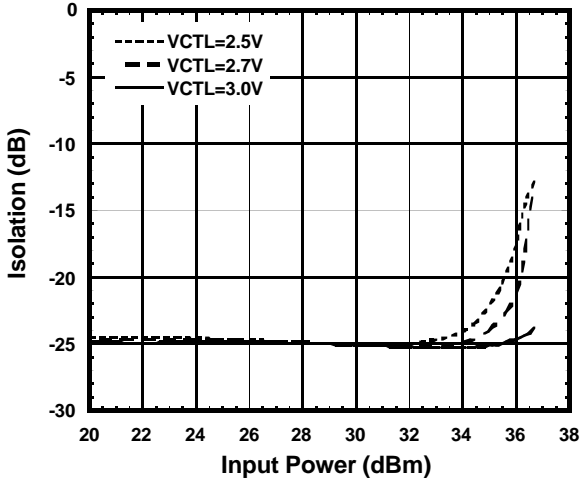
Insertion Loss vs. Input Power



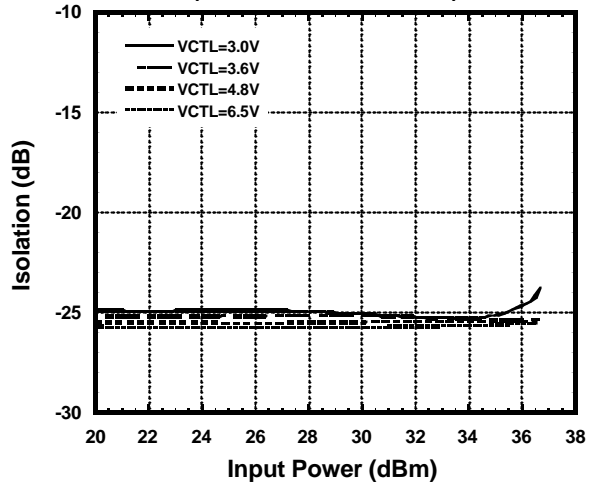
## ■ ELECTRICAL CHARACTERISTICS

(f=900MHz, with application circuit, losses of PCB, connector and DC blocking capacitor are excluded)

**PC-P1 Isolation vs. Input Power**  
(PC-P4 ON, f=900MHz)



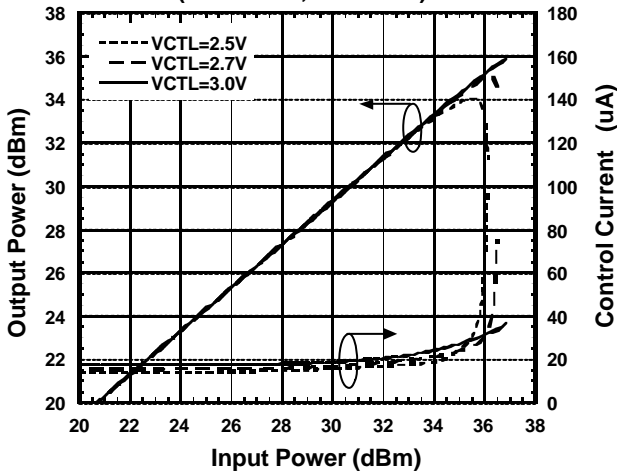
**PC-P1 Isolation vs. Input Power**  
(PC-P4 ON, f=900MHz)



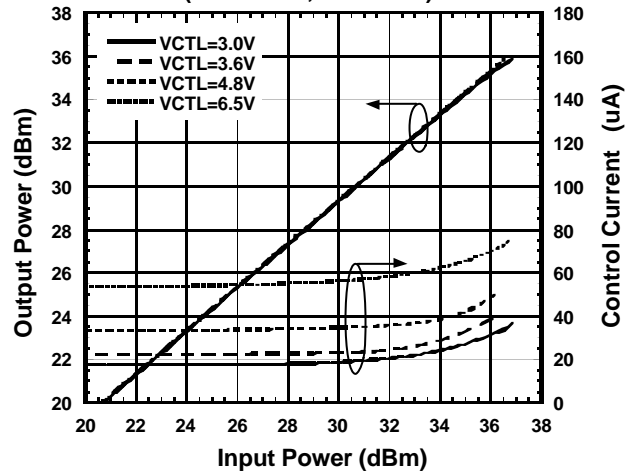
## ■ ELECTRICAL CHARACTERISTICS

(f=1.9GHz, with application circuit, losses of PCB, connector and DC blocking capacitor are excluded)

**Output Power, Control Current vs. Input Power**  
(PC-P1 ON, f=1.9GHz)



**Output Power, Control Current vs. Input Power**  
(PC-P1 ON, f=1.9GHz)



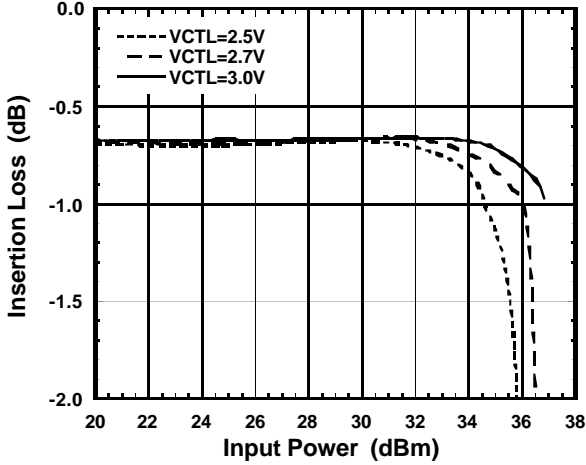
# NJG1519KC1

## ■ ELECTRICAL CHARACTERISTICS

(f=1.9GHz, with application circuit, losses of PCB, connector and DC blocking capacitor are excluded)

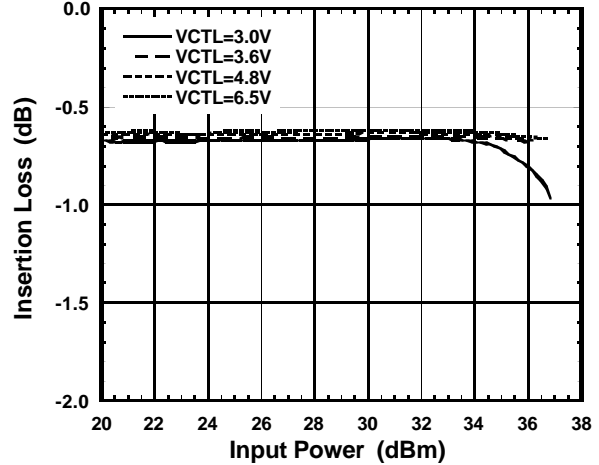
**Insertion Loss vs. Input Power**

( PC-P1 ON, f=1.9GHz )



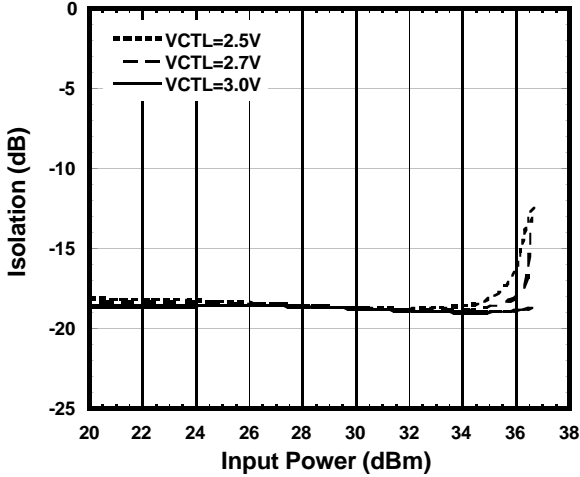
**Insertion Loss vs. Input Power**

( PC-P1 ON, f=1.9GHz )



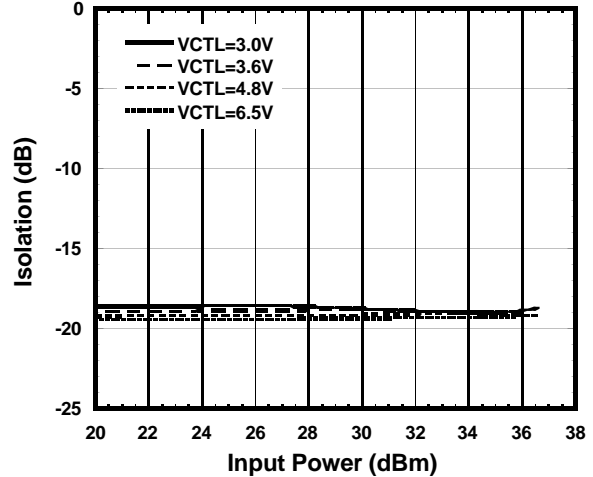
**PC-P1 Isolation vs. Input Power**

( PC-P4 ON, f=1.9GHz )



**PC-P1 Isolation vs. Input Power**

( PC-P4 ON, f=1.9GHz )

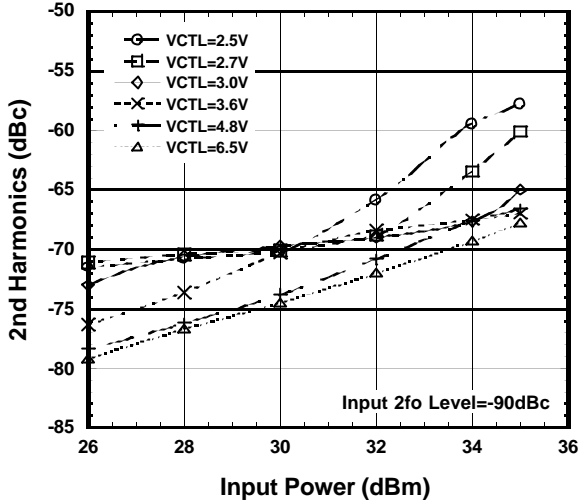




## ■ ELECTRICAL CHARACTERISTICS (with application circuit)

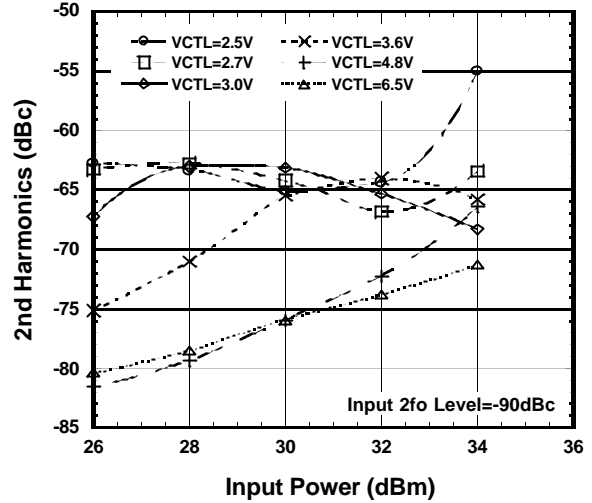
### 2nd Harmonics vs. Input Power

(PC-P1 ON,  $f=900\text{MHz}$ )



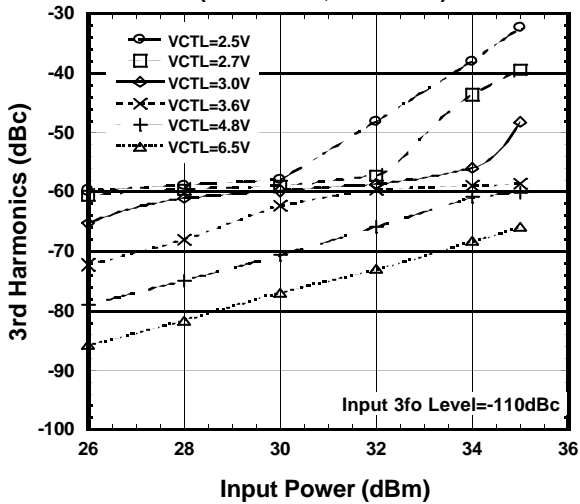
### 2nd Harmonics vs. Input Power

(PC-P1 ON,  $f=1.9\text{GHz}$ )



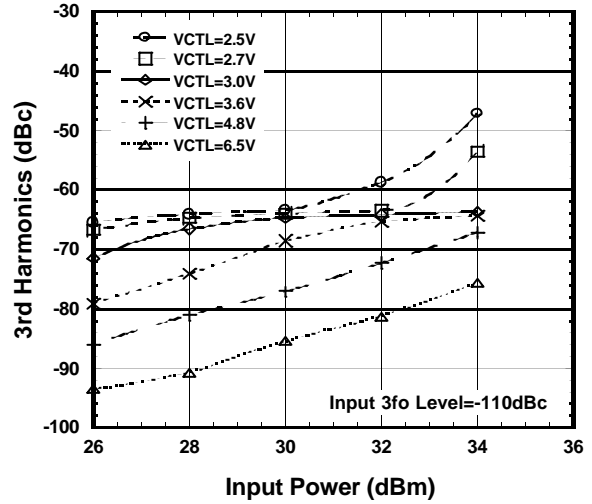
### 3rd Harmonics vs. Input Power

(PC-P1 ON,  $f=900\text{MHz}$ )



### 3rd Harmonics vs. Input Power

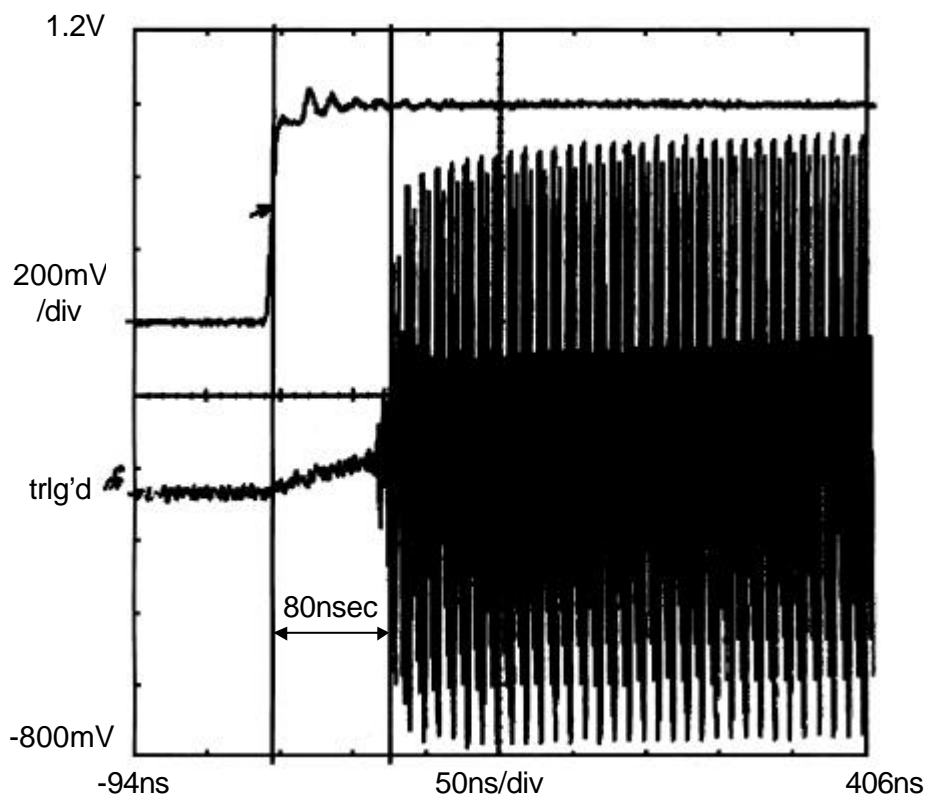
(PC-P1 ON,  $f=1.9\text{GHz}$ )



# NJG1519KC1

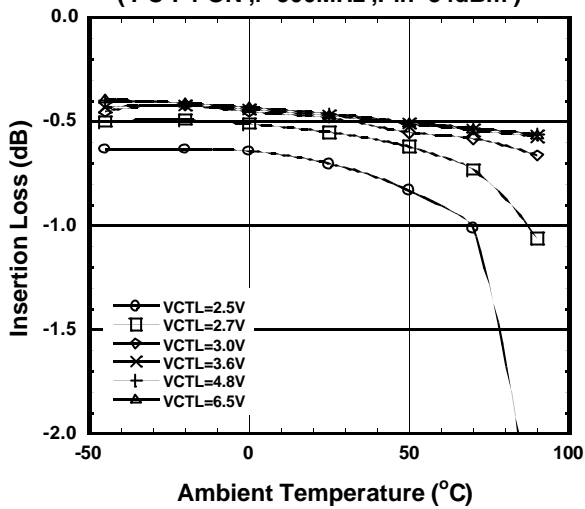
## ■ ELECTRICAL CHARACTERISTICS (with application circuit)

Switching speed  
( $V_{CTL1}=3.0V$ ,  $V_{CTL2}=0V$ )

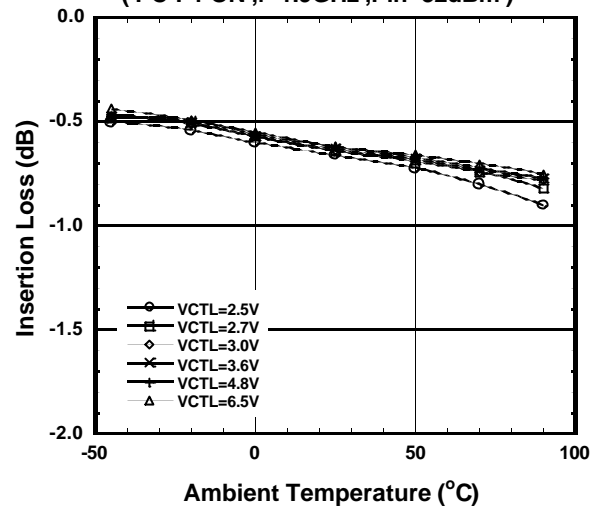


## ■ TEMPERATURE CHARACTERISTICS (with application circuit)

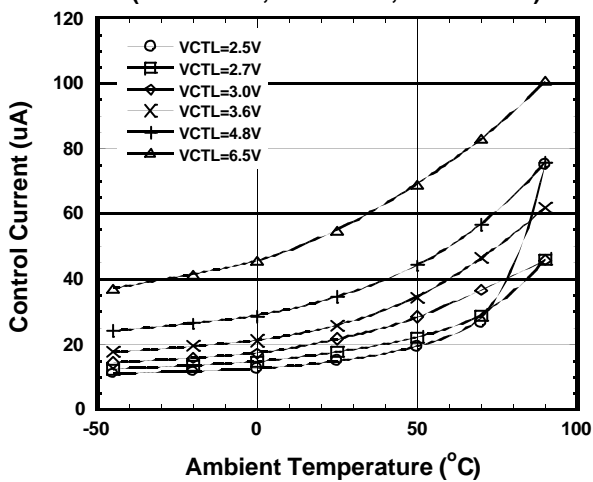
**Insertion Loss vs. Ambient Temperature**  
( PC-P1 ON , f=900MHz , Pin=34dBm )



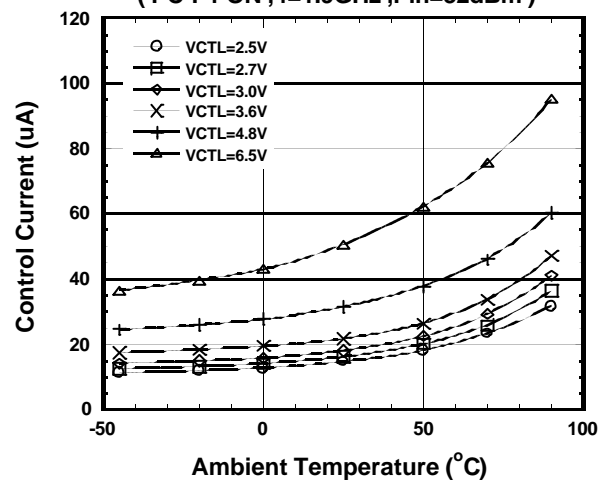
**Insertion Loss vs. Ambient Temperature**  
( PC-P1 ON , f=1.9GHz , Pin=32dBm )



**Control Current vs. Ambient Temperature**  
( PC-P1 ON , f=900MHz , Pin=34dBm )



**Control Current vs. Ambient Temperature**  
( PC-P1 ON , f=1.9GHz , Pin=32dBm )

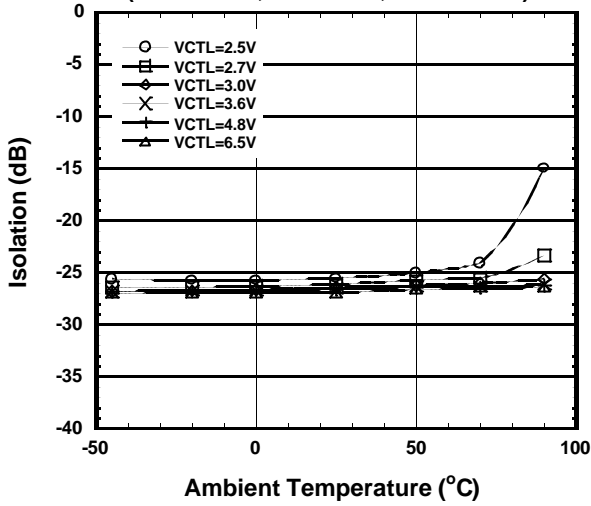


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## TEMPERATURE CHARACTERISTICS (with application circuit)

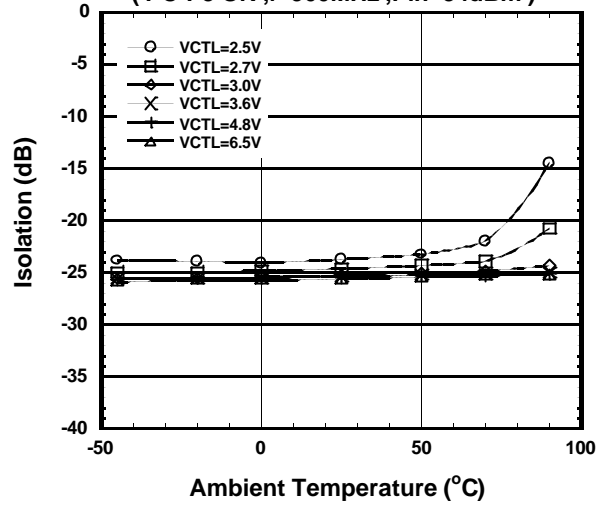
**PC-P1 Isolation vs. Ambient Temperature**

( PC-P2 ON ,f=900MHz ,Pin=34dBm )



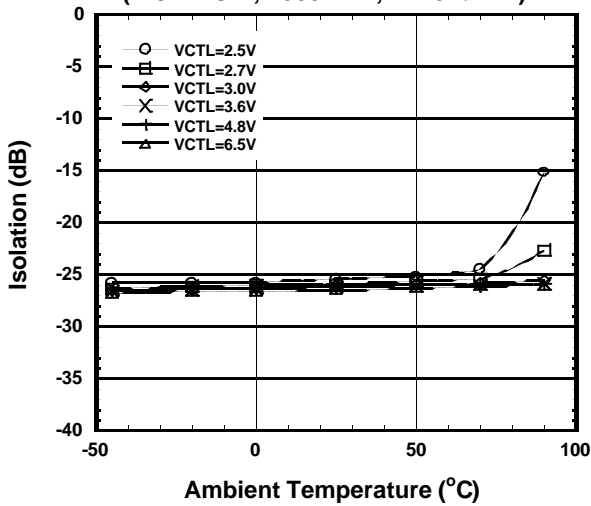
**PC-P2 Isolation vs. Ambient Temperature**

( PC-P3 ON ,f=900MHz ,Pin=34dBm )



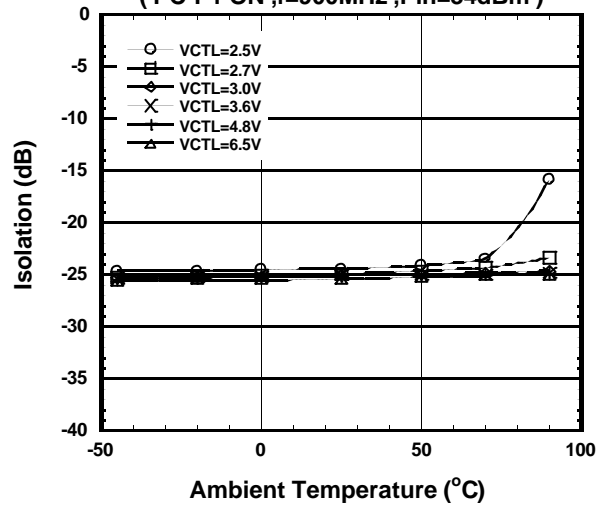
**PC-P3 Isolation vs. Ambient Temperature**

( PC-P4 ON ,f=900MHz ,Pin=34dBm )



**PC-P4 Isolation vs. Ambient Temperature**

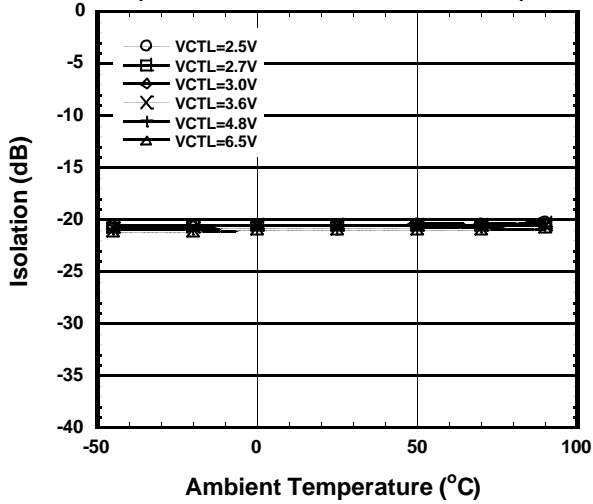
( PC-P1 ON ,f=900MHz ,Pin=34dBm )



## ■ TEMPERATURE CHARACTERISTICS (with application circuit)

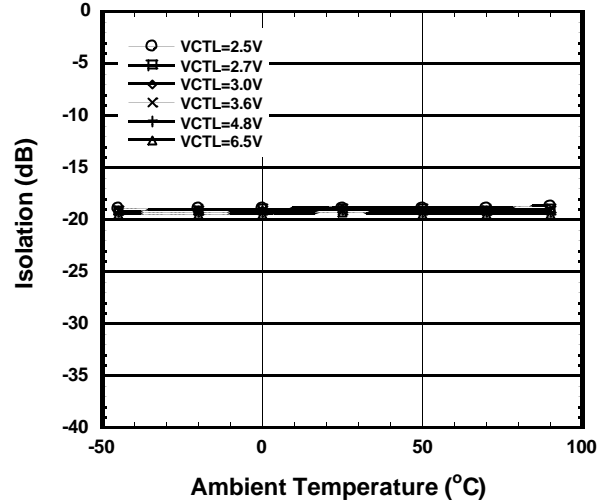
**PC-P1 Isolation vs. Ambient Temperature**

( PC-P2 ON ,f=1.9GHz ,Pin=32dBm )



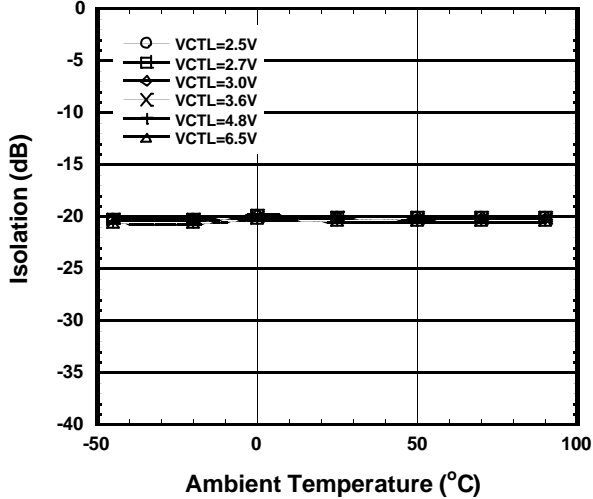
**PC-P2 Isolation vs. Ambient Temperature**

( PC-P3 ON ,f=1.9GHz ,Pin=32dBm )



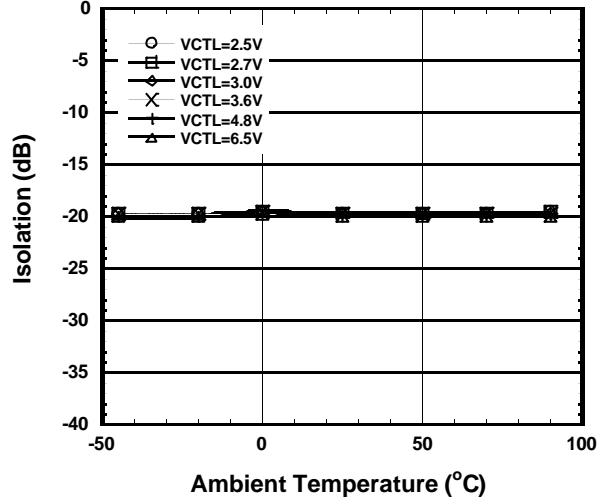
**PC-P3 Isolation vs. Ambient Temperature**

( PC-P4 ON ,f=1.9GHz ,Pin=32dBm )



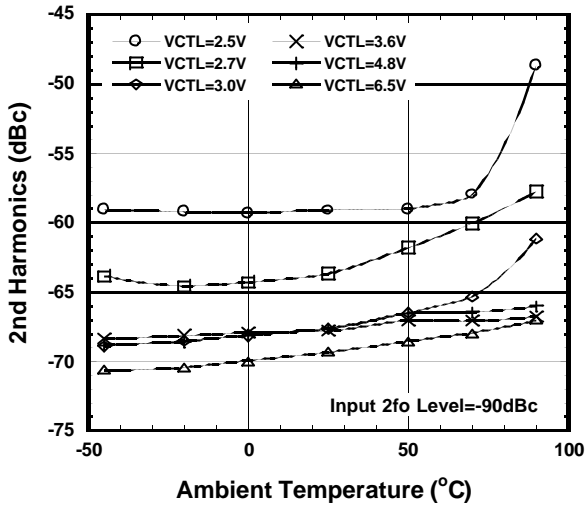
**PC-P4 Isolation vs. Ambient Temperature**

( PC-P1 ON ,f=1.9GHz ,Pin=32dBm )

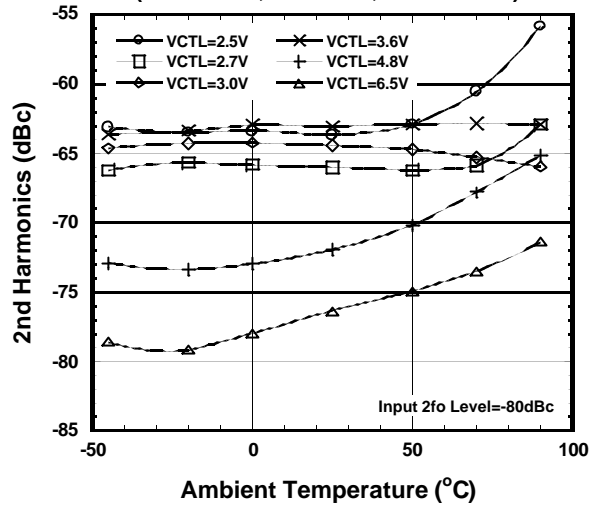


## TEMPERATURE CHARACTERISTICS (with application circuit)

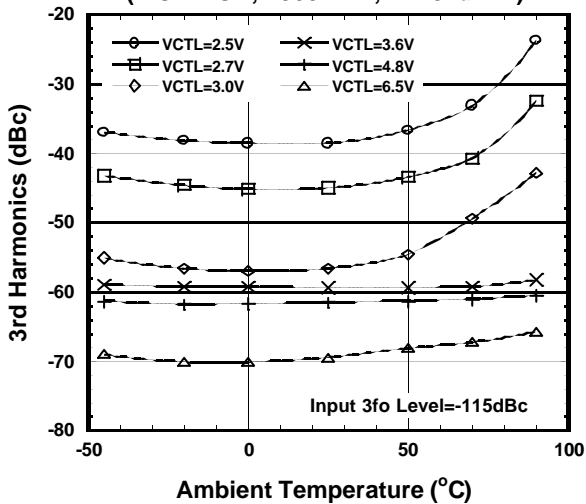
**2nd Harmonics vs. Ambient Temperature**  
( PC-P1 ON, f=900MHz, Pin=34dBm )



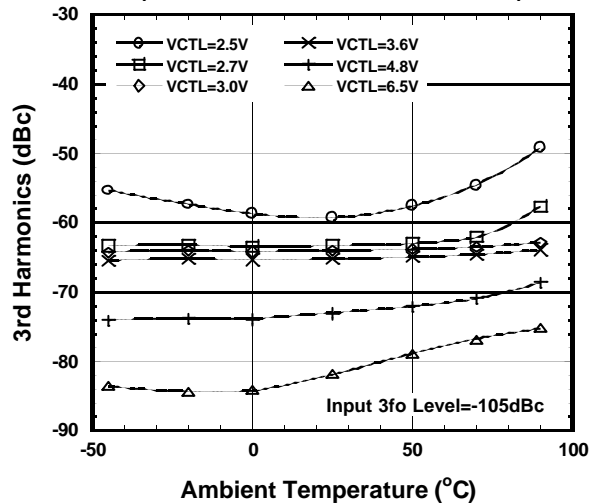
**2nd Harmonics vs. Ambient Temperature**  
( PC-P1 ON, f=1.9GHz, Pin=32dBm )



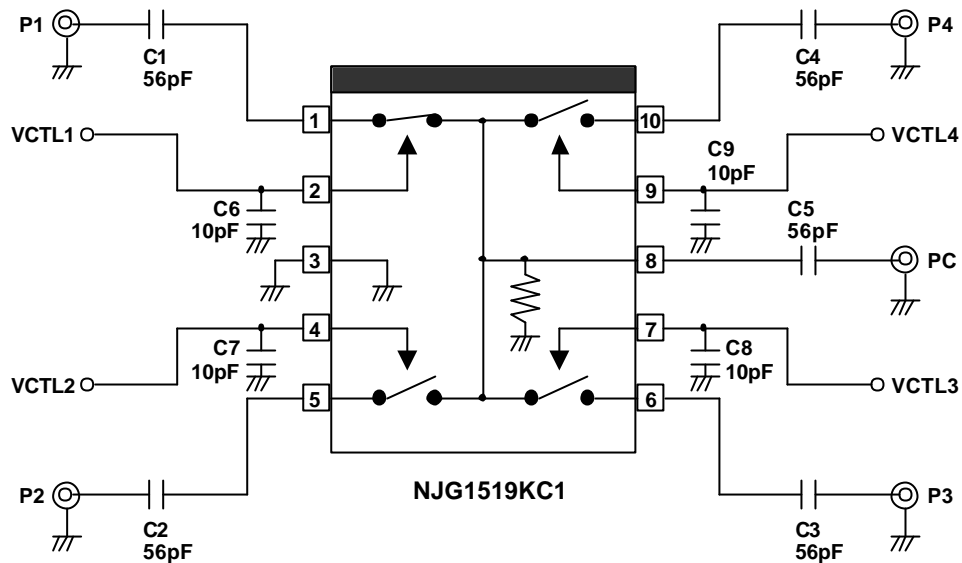
**3rd Harmonics vs. Ambient Temperature**  
( PC-P1 ON, f=900MHz, Pin=34dBm )



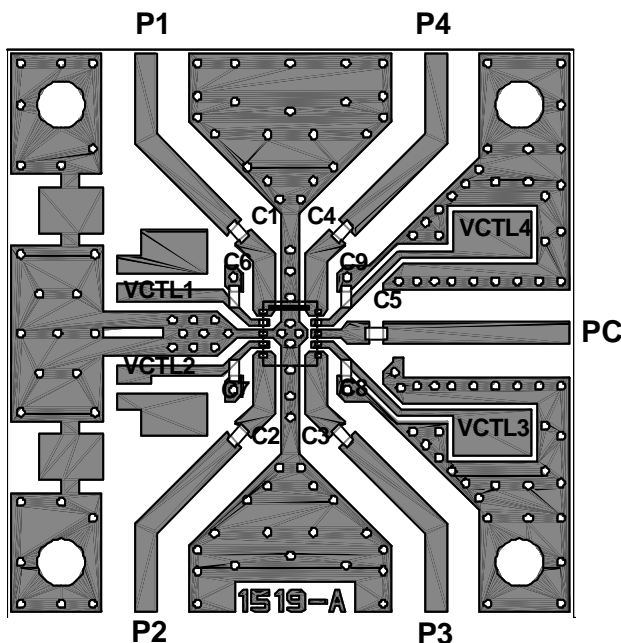
**3rd Harmonics vs. Ambient Temperature**  
( PC-P1 ON, f=1.9GHz, Pin=32dBm )



## APPLICATION CIRCUIT



## RECOMMENDED PCB DESIGN



PCB: FR-4,  $t=0.5\text{mm}$   
 Microstrip Line Width: 1mm ( $Z_0=50\Omega$ )  
 PCB Size: 26x26mm

### PARTS LIST

Parts	Value	Notes
C1~C5	56pF	MURATA (GRM36)
C6~C9	10pF	MURATA (GRM36)

### Circuit losses including losses of capacitors and connectors

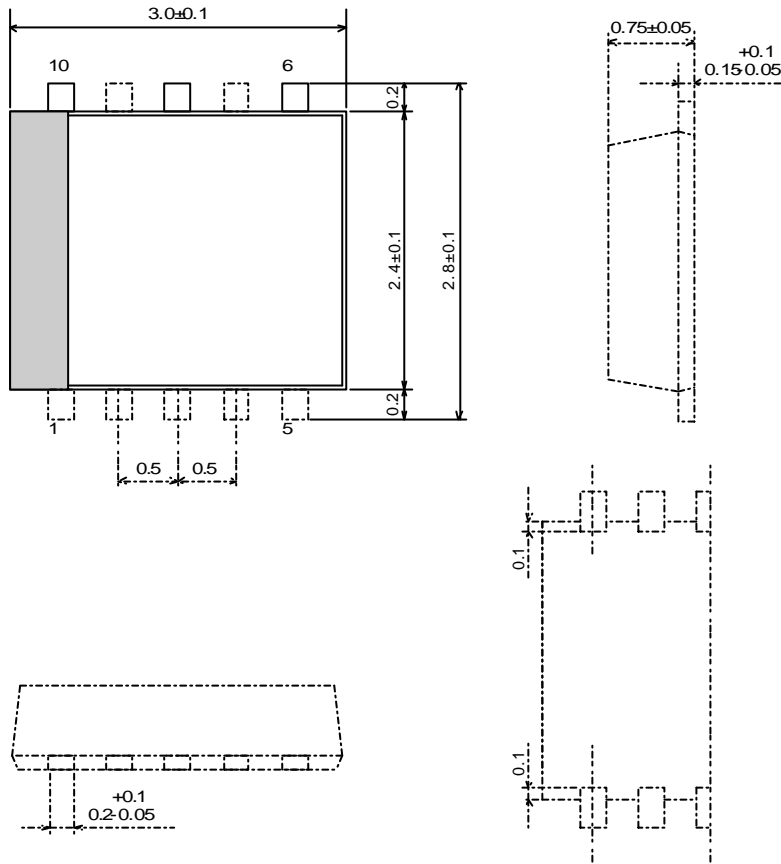
Frequency	900MHz	1.9GHz
Loss (dB)	0.20	0.36

## PRECAUTIONS

- [1] The DC blocking capacitors have to be placed at RF terminal of P1, P2 and PC.
- [2] Bypass capacitors (C4, C5) should be placed close to terminals of  $V_{CTL1}$ ,  $V_{CTL2}$  to reduce stripline influence of RF characteristics.
- [3] For good isolation, the GND terminal (2nd pin) must be placed possibly close to ground plane of substrate, and through holes for GND should be placed near by the pin connection.
- [4] To avoid degradation of isolation or high power characteristics, please layout ground pattern right under this IC.

# NJG1519KC1

## PACKAGE OUTLINE (FLP10-C1)



Lead material	: Copper
Lead surface finish	: Solder plating
Molding material	: Epoxy resin
UNIT	: mm
Weight	: 15mg

### Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

### [CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including