APPLICATION NOTE

A wide-band class-AB hybrid coupled amplifier (470 – 860 MHz) with two balanced transistors BLV57

NCO8205

Philips Semiconductors

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CONTENTS

1 SUMMARY

For application in TV transmitters in band 4/5 a wideband linear power amplifier has been designed with two balanced transistors BLV57 in a class AB DC-setting (V_{CE} = 25 V and I_{CZ} = 2 × 100 mA).
A class A amplifier designed around the BLV57 has been described in reports NCO8101 and NCO8201.
The results of the class AB input and output circuit calculations are about similar to the results of the class A application. Therefore the p.c.-board design of the class A-amplifier can be used.
The applied circuit board is a double copper clad PFTE fibre-glass print with an ε_r = 2.74 and a thickness of 1/32 inch.
The heatsink has a forced air cooling.
The main results are given in Table 1.

Table 1

DC-setting	I_{CZ} = 4 × 100 mA, V_{CE} = 25 V
Gain at P_{out} = 5 W	≥6 dB
P_{out} at 1 dB gain compression	≥42.5 W
Efficiency at 1 dB gain compression	≥45%

2 INTRODUCTION

The BLV57 is a balanced transistor in an 8 lead envelope (SOT161) for class A operation in TV-transposers for band 4/5.
A class A amplifier, designed around two transistors BLV57, has been described in report NCO8101 and the construction of this amplifier in report NCO8201.
Because there is also a typical class AB specification a wide-band power amplifier has been designed around two transistors BLV57 in class AB.
The quiescent current I_{CZ} = 100 mA per chip and the V_{CE} = 25 V.

3 DESIGN OF THE AMPLIFIER

3.1 General remarks

The schematic line-up of the complete amplifier is given in Fig.1.

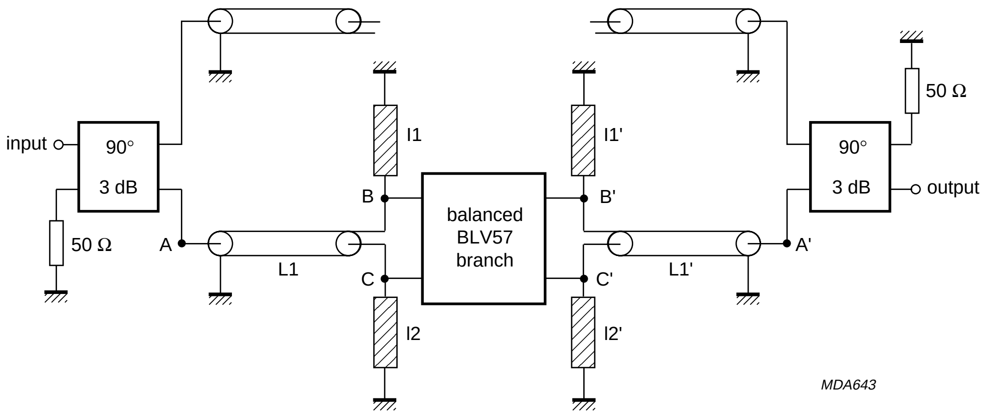


Fig.1 Schematic line-up.

The amplifier consists of two branches, both with a BLV57 transistor, which are coupled by means of a wide-band 3 dB – 90° coaxial hybrid coupler at the input and output.
Each BLV57 has 2 input circuits and 2 output circuits (one for each chip) connected to a coax balun (L_1 and L'_1) which connects the 25 Ω balanced ports B and C to the unbalanced 50 Ω port A.
The phase-shift between B and C is 180°.
The p.c.-board design, the material and the construction of the amplifier is equal to the class A amplifier described in the reports NCO8101 and NCO8201.

3.2 Bias circuit

Each transistor has its own bias unit to obtain a stable DC-setting for class AB operation (see Fig.2). This bias unit enables a stable adjustment of the collector currents of the BLV57 by means of potentiometer R_2.
To follow the temperature variation of the BLV57 the transistor T_1 has been situated on the heatsink near to the HF-transistor for a good thermal contact (see Fig.5).

3.3 Some properties of the BLV57

The optimum DC-setting of the BLV57 for class AB operation is V_{CE} = 25 V and a quiescent current of I_{CZ} = 100 mA for each transistor chip. The typical gain, input and load impedance of a half BLV57 (one chip) are given in Table 2.
These figures have been calculated with the aid of a large signal equivalent circuit (P_O = 17.5 W).

Table 2

FREQUENCY (MHz)	GAIN (dB)	INPUT IMPEDANCE (Ω)	OUTPUT IMPEDANCE (Ω)
400	11.95	1.21 + j1.71	10.52 + j4.04
500	10.29	1.24 + j2.53	9.06 + j4.02
600	9.01	1.28 + j3.32	7.70 + j3.63
700	7.99	1.36 + j4.11	6.50 + j2.98
800	7.17	1.49 + j4.93	5.49 + j2.13
900	6.48	1.68 + j5.81	4.67 + j1.17

3.4 Input and output circuit

The calculation of the input and output circuit is the same as described in NCO8101 *“input and output network”*.
The results are about similar to the results of the class A application, making it possible to apply the same p.c.-board design.
The tuning of the output circuit is also as described in report NCO8101. The dummy now consists of a 30 Ω resistance in parallel with an 8.2 pF capacitance.
In Fig.3 the return losses at the output of one branch are given after tuning the output circuit with the help of this dummy.
To achieve a sufficiently flat gain the capacitance of C_3 and C_4 and also the position of C_3 (see Fig.4 and Table 4) can be optimized in a sweep set-up with a constant output power of 5 W. The position of C_4 and C_5 is close to the ceramic cap of the BLV57.

3.5 Hybrid coupled amplifier

As mentioned in Chapter 4 of NCO8101 the two branches are coupled by means of 3 dB – 90° hybrid couplers. Figure 5 gives the p.c.-board of the complete amplifier and the lay-out.

4 MEASURED PERFORMANCE

4.1 Gain and return losses

Figures 6 and 7 show the gain and input return losses as a function of the frequency at a constant output power P_O = 5 W. The gain varies from 6 to 6.9 dB. The input return losses are at least 12 dB.
Figures 10 and 11 show the gain versus output power at the frequencies 500 and 800 MHz. The increase of gain at low power level can be reduced at the cost of the average gain level by decreasing the quiescent current.

4.2 Output power

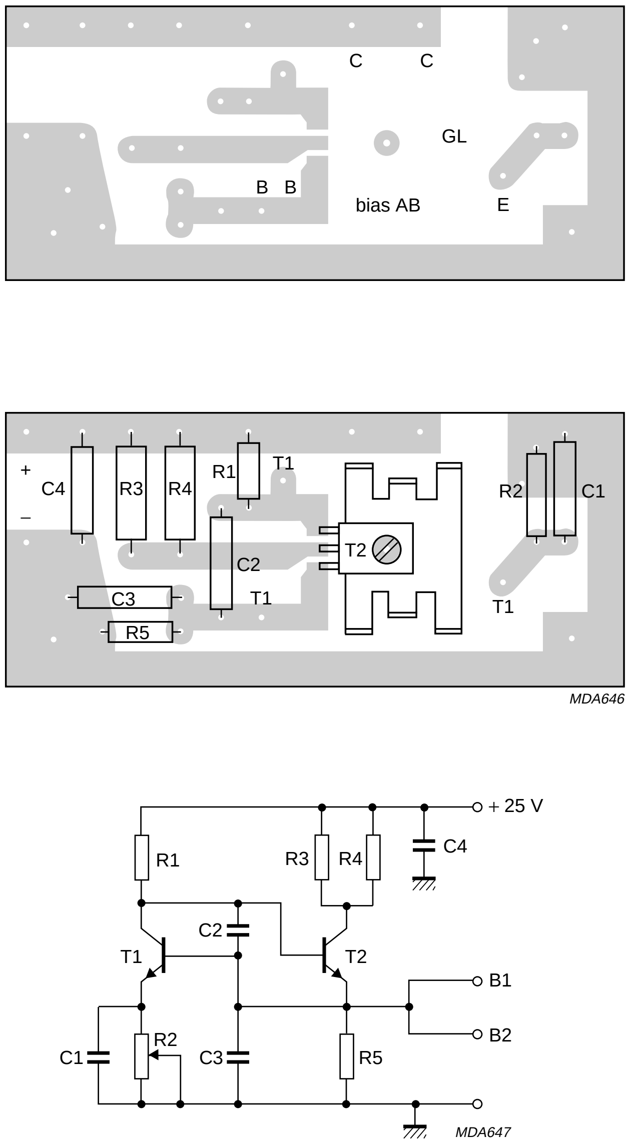
Figures 8 and 9 show the output power and efficiency as a function of the frequency at 1 dB gain compression. The output power is at least 42.5 W and above 530 MHz between 50 and 60 W. The average efficiency at 1 dB gain compression is 50%.

5 CONCLUSION

This report shows that it is possible to operate the class A transistor BLV57 with a class AB DC-setting in a hybrid coupled wideband amplifier (470 to 860 MHz) with good performances.
The main properties of the amplifier are given in Table 3.

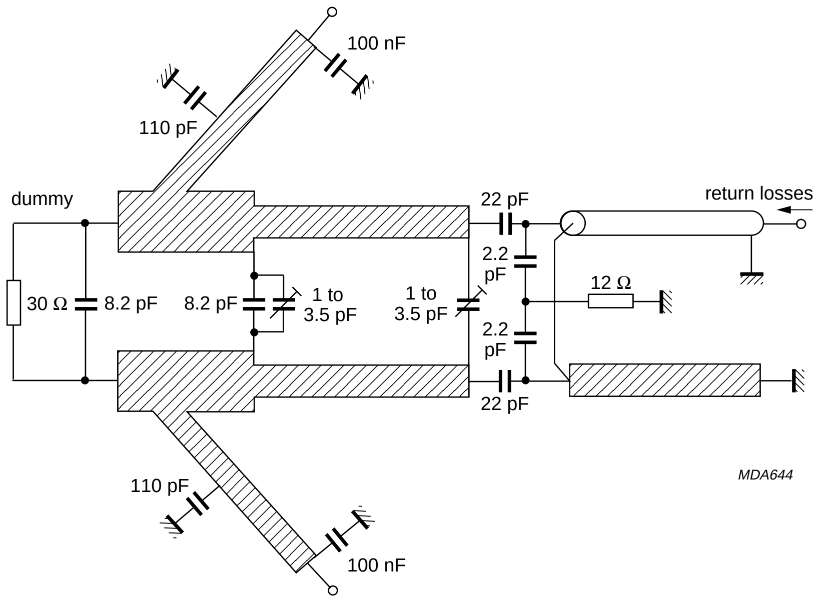
Table 3

BLV57 BAND 4/5 AMPLIFIER	
DC-setting	I_{CZ} = 4 × 100 mA, V_{CE} = 25 V
Gain at P_{out} = 5 W	≥6 dB
P_{out} at 1 dB gain compression	≥42.5 W
Efficiency at 1 dB gain compression	≥45%



$C_1 = C_2 = C_3 = C_4$ = 150 nF, metallised film capacitor, cat. no. 2222 352 45154.
R_1 = 1500 Ω, CR 25 type, cat. no. 2322 211 13152.
R_2 = 10 Ω, cermet potentiometer, cat. no. 2122 350 00056.
$R_3 = R_4$ 120 Ω, CR 52 type, cat. no. 2322 213 13121.
R_5 = 150 Ω, CR 25 type, cat. no. 2322 211 13151.
$T_1 = T_2$ BD 139.

Fig.2 Bias circuit and lay-out.



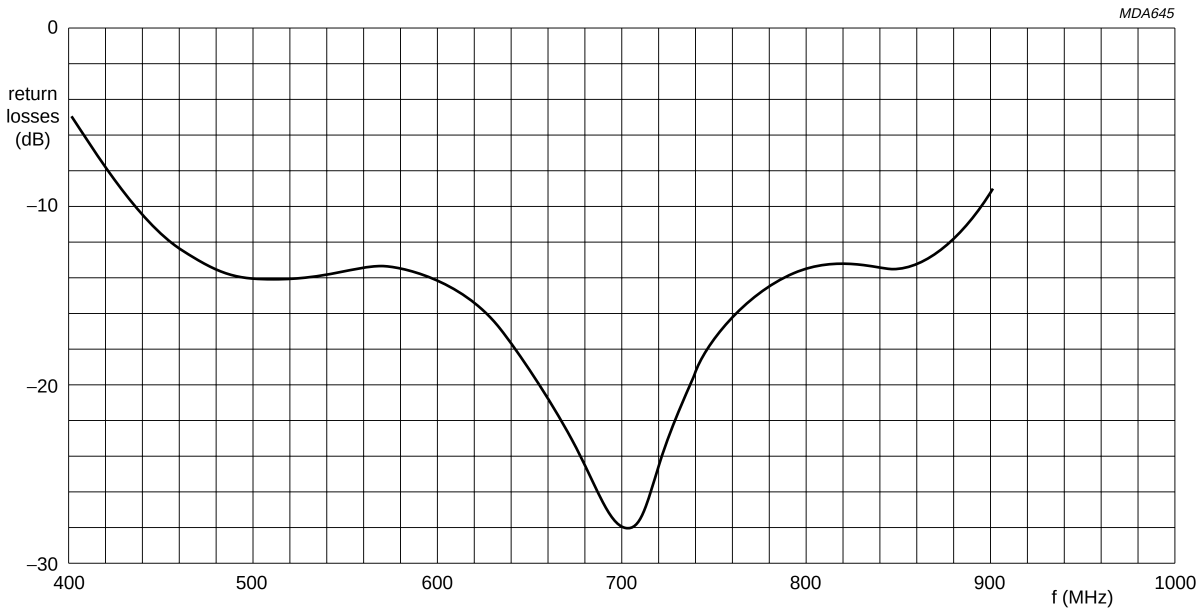


Fig.3 Tuning of the output circuit.

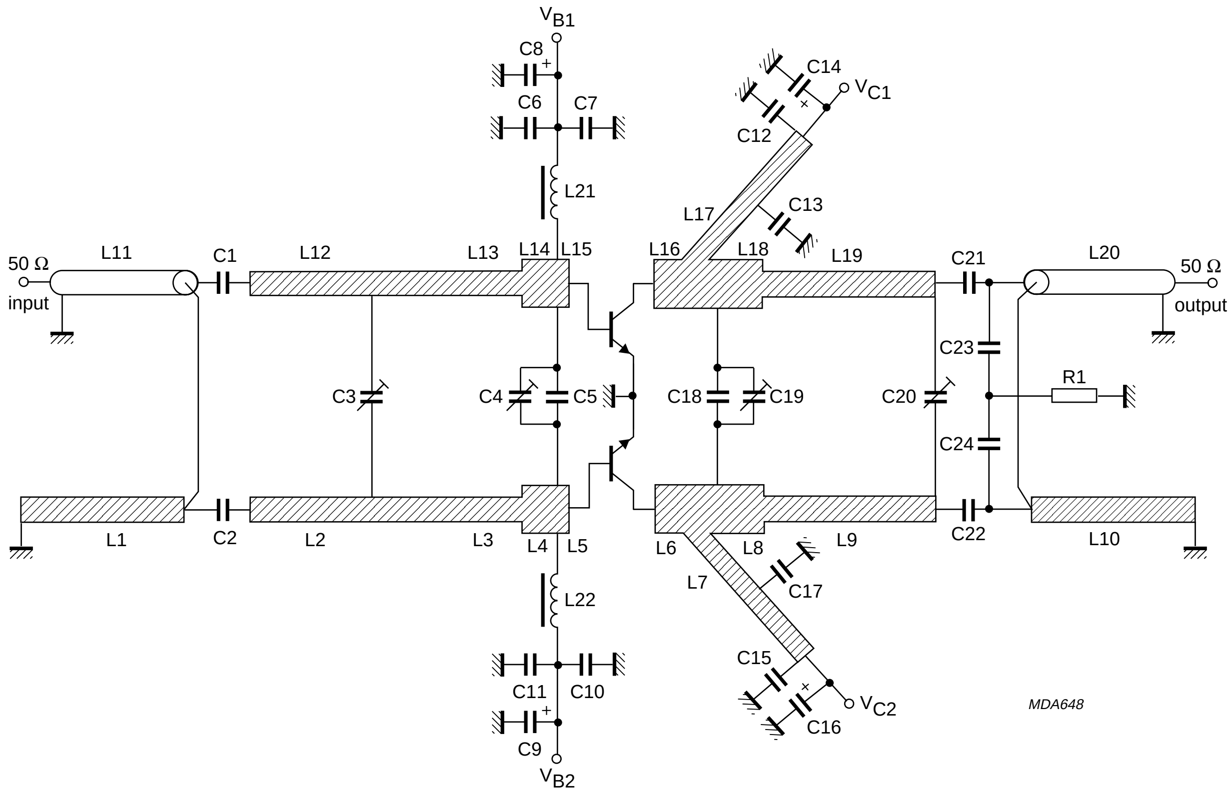


Fig.4 Circuit of one BLV57 branch.

Table 4 List of components BLV57 class AB (one branch)

$C_1 = C_2$ = 12 pF	chip capacitor, Philips NPO, cat.no. 2222 851 13129
$C_3 = C_4 = C_{19} = C_{20}$ = 1 – 3.5 pF	film dielectric trimmer, Philips cat.no. 2222809 05001
$C_5 = C_{18}$ = 8.2 pF	chip capacitor, ATC, 8R2J
$C_6 = C_{11} = C_{12} = C_{15}$ = 100 nF	chip capacitor, Philips NPO, cat.no. 2222855 48104
$C_7 = C_{10}$ = 100 pF	chip capacitor, Philips NPO, cat.no. 2222852 13101
$C_8 = C_9 = C_{14} = C_{16}$ = 6.8 μF, (40 V)	electrolytic capacitor, Philips, cat.no. 2222 030 87688
$C_{13} = C_{17}$ = 110 pF	chip capacitor, ATC, 111J
$C_{21} = C_{22}$ = 22 pF	chip capacitor, Philips NPO, cat.no. 2222 851 13229
$C_{23} = C_{24}$ = 2.2 pF	chip capacitor, Johanson, no. 500 R, 15 N, 2R2BA
L_1 = stripline	(Z_C = 50 Ω), 49 × 2 mm
$L_2 = L_{12}$ = stripline	(Z_C = 57 Ω), 14.5 × 1.5 mm
$L_3 = L_4$ = stripline	(Z_C = 57 Ω), 12.8 × 1.5 mm
$L_4 = L_{14}$ = stripline	(Z_C = 36 Ω), 2 × 3 mm
$L_5 = L_{15}$ = stripline	(Z_C = 36 Ω), 1 × 3 mm
$L_6 = L_{16}$ = stripline	(Z_C = 36 Ω), 3 × 3 mm
$L_7 = L_{17}$ = stripline	(Z_C = 48 Ω), 17.7 × 2 mm
$L_8 = L_{18}$ = stripline	(Z_C = 36 Ω), 8.8 × 3 mm
$L_9 = L_{19}$ = stripline	(Z_C = 57 Ω), 15.2 × 1.5 mm
L_{10} = stripline	(Z_C = 50 Ω), 46 × 2 mm
L_{11} = 49 mm semi-rigid coax, 2.2 mm ∅, Z_C = 50 Ω, PTFE dielectric, soldered on 2 mm stripline	
L_{20} = 46 mm semi-rigid coax, 2.2 mm ∅, Z_C = 50 Ω, PTFE dielectric, soldered on 2 mm stripline	
$L_{21} = L_{22}$ = 0.1 μH	microchoke, cat.no. 2322 057 01071
R = 12 Ω	CR 25 type cat.no. 2322 211 13129

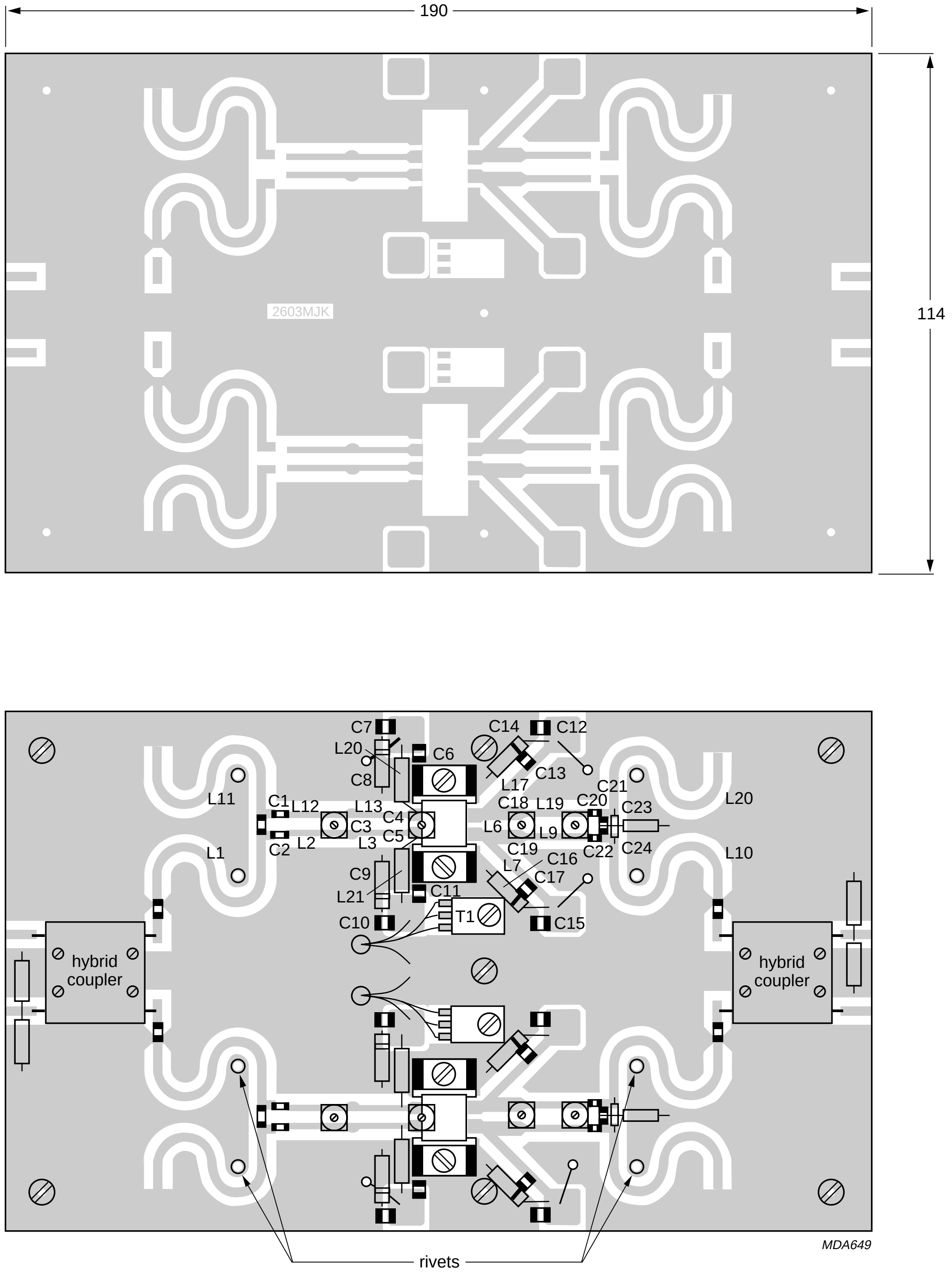


Fig.5 Lay-out and PC-board of the BLV57 amplifier.

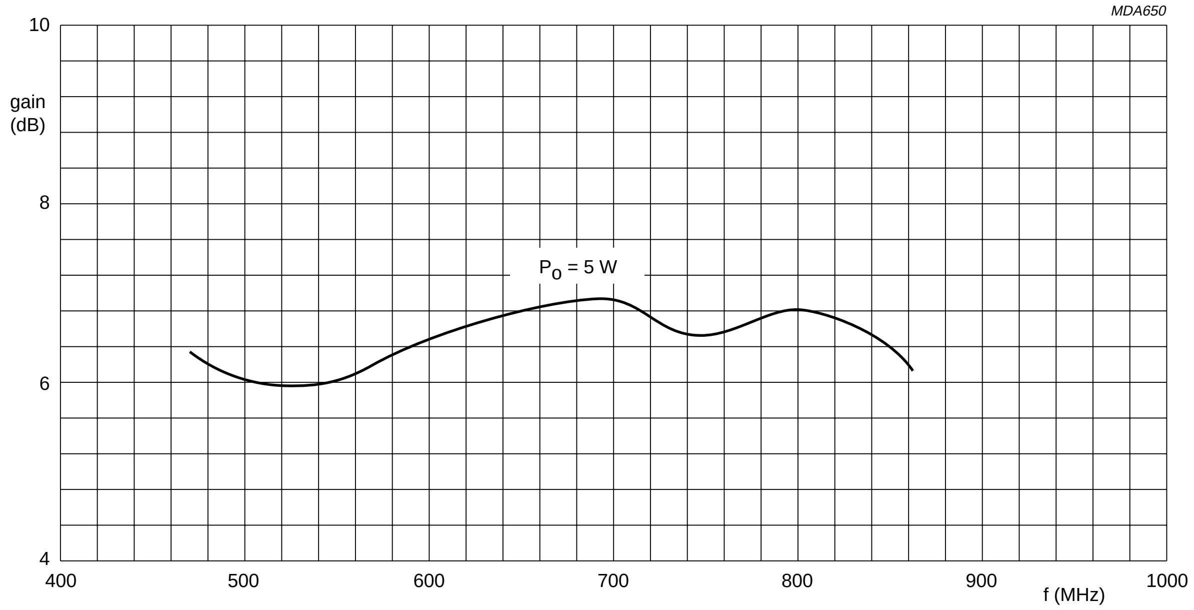


Fig.6 Gain versus frequency.

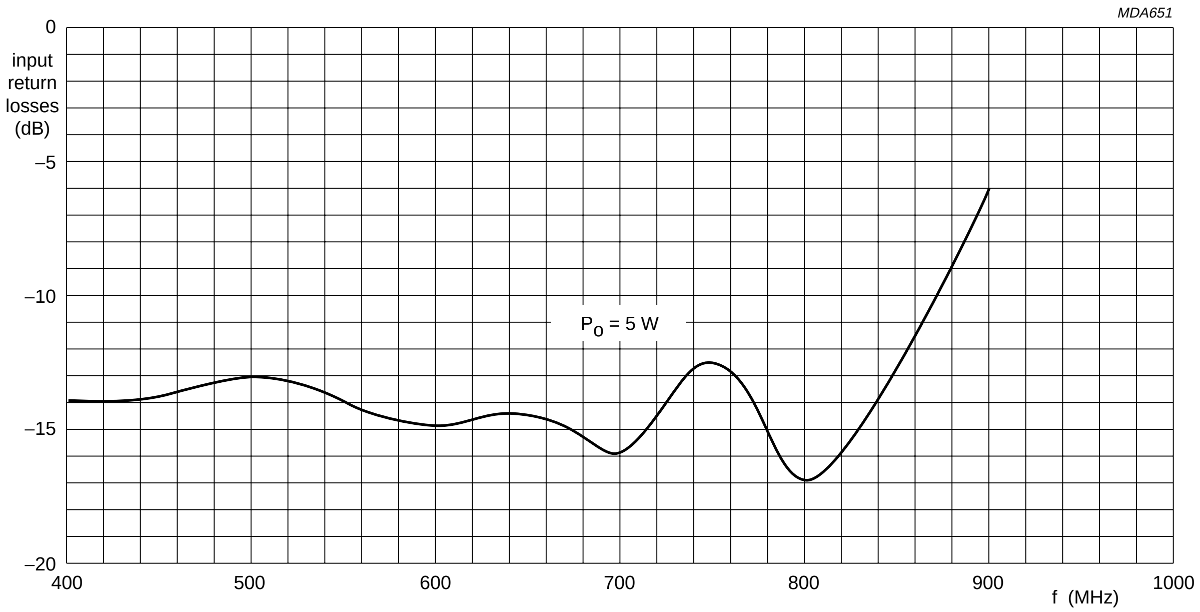


Fig.7 Return losses versus frequency.

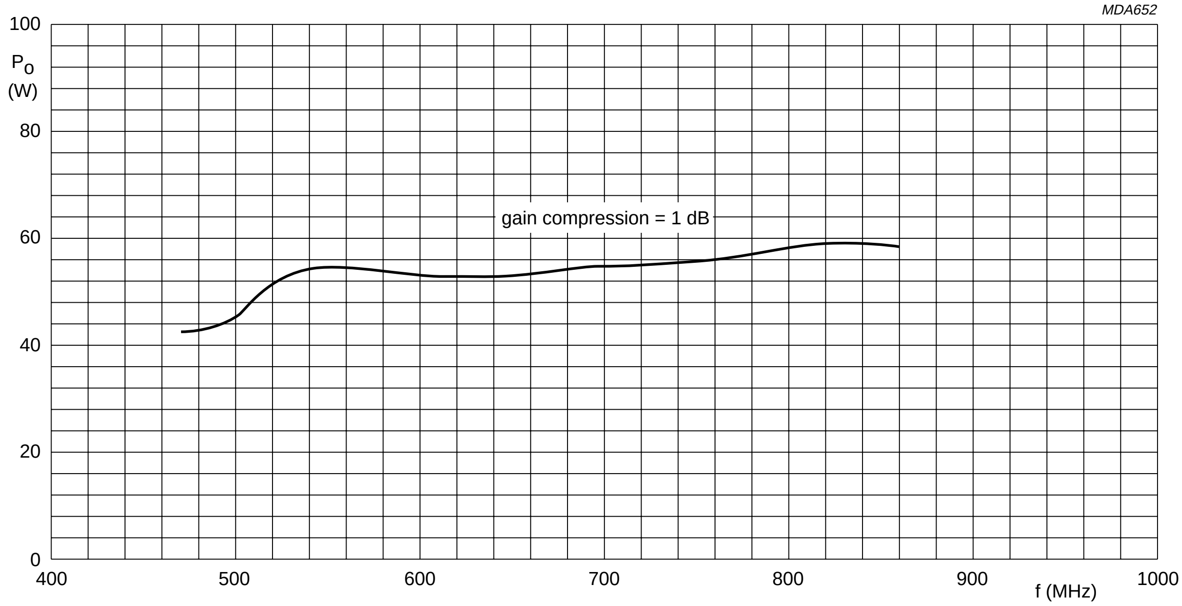


Fig.8 Output power versus frequency.

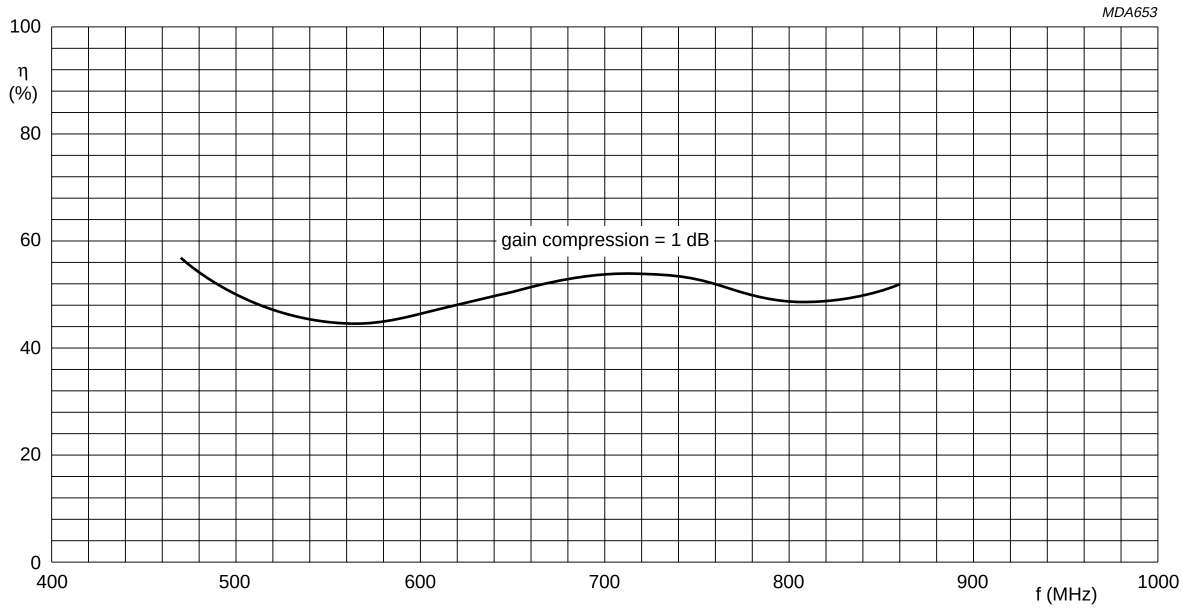


Fig.9 Efficiency versus frequency.

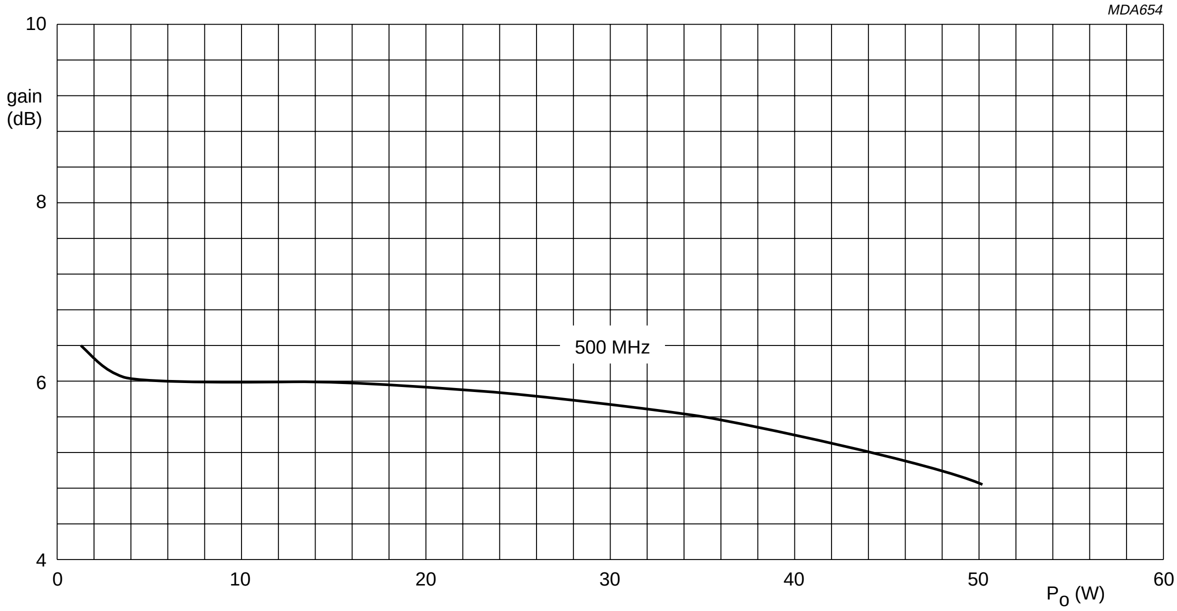


Fig.10 Gain versus output power.

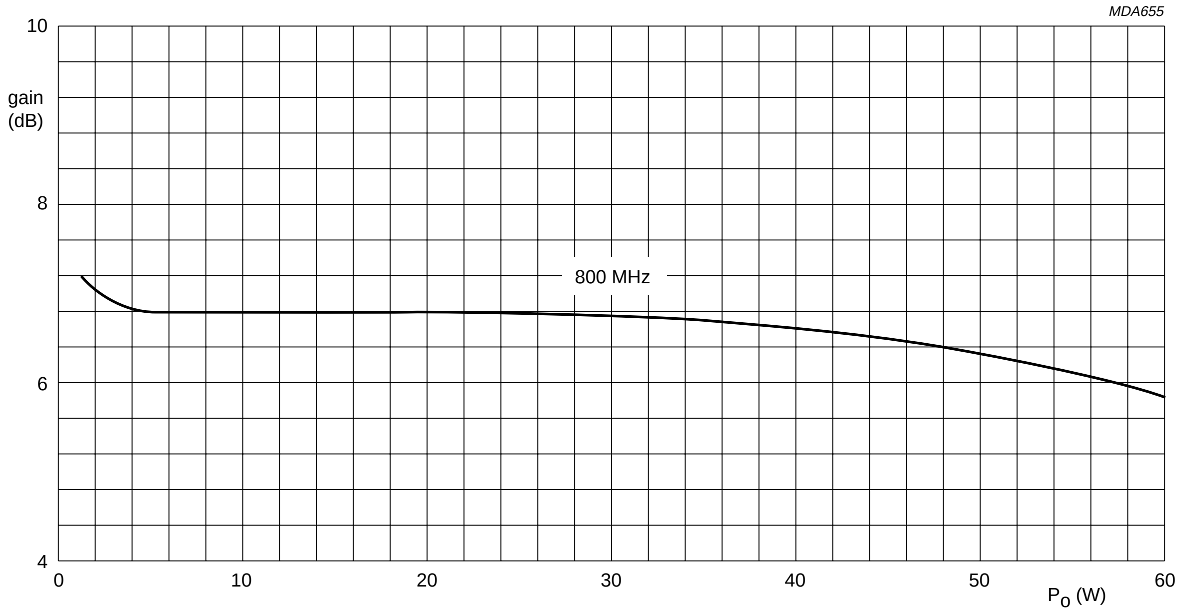


Fig.11 Gain versus output power.

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Printed in The Netherlands

Date of release: 1998 Mar 23

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