4 RF AND MICROWAVE TRANSISTOR PACKAGES

The packages of electronic devices are, in general, designed to:

- Protect the electronics from mechanical damage
- Ensure adequate heat transfer to the ambient, and
- Provide robust, solderable electrical terminations.

For RF and microwave transistors however, the package itself forms an important part of the total electronic circuit, and this places additional requirements upon its electrical characteristics.

These requirements together with the available technologies have influenced RF transistor package design over the years. As a result, there are a variety of packages on the market today. The design and characteristics of the main package types are outlined in the following sections. Information on specific packages is given in data handbooks SC18: Discrete Semiconductor Packages, and SC19a: RF & Microwave Power Transistors, RF Power Modules and Circulators/Isolators.

4.1 Basics of RF and microwave transistor packages

In general, two (the base/gate and emitter/source) of the three electrical contacts of a transistor die are on the top of the die, and are connected to the external package terminations by bonding wires. The underside of the die is the third contact (the collector/drain) and connection is usually made to this contact by bonding the die to an electrical conductor which also serves as a heatsink.

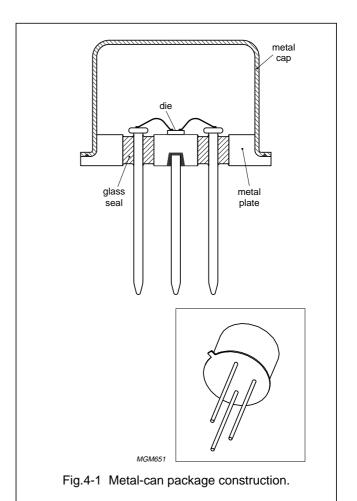
4.2 Metal-can packages

Included here for historical completeness, metal-can packages used to house bipolar transistors are rapidly being replaced by newer, superior alternatives.

In a metal-can package (e.g. TO-39 (SOT5)), the transistor die is attached to a small, thin metal plate (usually round). All the external electrical terminations are wire leads. The collector lead is connected to the plate; the emitter and base leads are fed through the plate and isolated from it by a glass seal.

The package is sealed with a metal cap welded onto the plate. This design combined with stringent well-controlled manufacture provide a hermetic package.

The power that a metal-can package can handle however is very limited, because heat is mainly removed from the die by radiation. And, while mounting the package directly onto a heatsink in a circuit lowers the packages thermal



resistance, it means the collector is connected to the heatsink, whereas most applications require a common-emitter or common-base configuration. The solution to this drawback was found with the introduction of ceramic packages.

4.3 Ceramic packages with a copper stud or flange

In a ceramic package, the transistor die is soldered on a metallized ceramic heat-spreader located on top of a stud or flange used to mount the transistor and to conduct heat away from the die. The function of the somewhat inappropriately named heat-spreader is to electrically isolate the bottom of the die from the stud or flange, allowing the transistor package to be mounted directly to a heatsink.

The electrical terminations are formed by brazing several, usually flat, leads to the heat-spreader, with wire bonding from the leads to the two contacts on top of the die. Beryllia (BeO) used to be the most-commonly used heat-spreader

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material since it combines good thermal conductivity (250 W/mK) with good electrical isolation. A disadvantage of BeO is that it is toxic. So, in line with Philips' policy to eliminate toxic and environmentally harmful substances from its products, packages with aluminiumnitride (AIN) heat-spreaders have been developed - the slightly lower thermal conductivity of AIN being compensated for by using thinner ceramic.

The first ceramic packages incorporated a copper stud or flange brazed to the bottom of the heat-spreader. Since there is considerable mismatch between the thermal coefficients of expansion (TCE) of copper and beryllia, the contact area must be limited to prevent the heat-spreader from cracking. Larger (higher power) packages (e.g. SOT121 and SOT171) were therefore designed using a copper pedestal to which the heat-spreader was attached (brazed) with the die on top. The pedestal allows a larger heat-spreader (and hence die) to be used whilst maintaining the metal-to-ceramic contact area well below the practical limit. Even with this design, however, the size of the heat-spreader is limited as only the region directly above the pedestal has a low thermal resistance, and thus conducts heat effectively. Those areas of a transistor die and heat-spreader extending beyond the top of the pedestal have a higher thermal resistance. Nevertheless, since such packages can be mounted directly onto a heatsink in the application, the power handling, though still restricted, is much better than that of the standard design.

This type of package (with or without pedestal) is sealed by epoxy-glueing a ceramic cap to the top of the package. Though forming a high-quality reliable seal, epoxy resin does not provide a hermetic barrier. To ensure that the package is completely sealed and that there are no pinholes in the epoxy, the packages are tested for gross leaks. Note that all epoxy glues start to degrade at temperatures close to 300 °C and, for long-term stability, standard ceramic packages should not be exposed to temperatures above about 150 °C. Short exposure to higher temperatures is allowed (e.g. during reflow soldering). In addition, during fluxing and cleaning, minimize exposure to liquids, for example by dipping.

Though not strictly hermetic, all of Philips' standard ceramic packages contain glass-passivated transistor dies. Effectively isolating the die from its surroundings, glass passivation contributes to extremely high levels of transistor reliability.

4.4 Ceramic packages with special flange materials

As indicated above, the size of ceramic packages with copper flanges is limited by the different TCEs of copper

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and ceramic. This limitation was overcome by replacing the copper by a material with a much lower TCE. Nowadays, two materials are commonly used which combine a much lower TCE with a still acceptable thermal conductance:

- A tungsten-copper alloy (e.g. SOT262), and
- A copper-molybdenum-copper sandwich (e.g. SOT468).

These materials allow the contact area between flange and ceramic to be much larger while the ceramic can be even thinner without increased risk of cracking. Since these materials are at present very expensive, packages with a copper flange remain in widespread use. For improved RF grounding at high frequencies, flanged packages with through-plated holes in the ceramic have been developed.

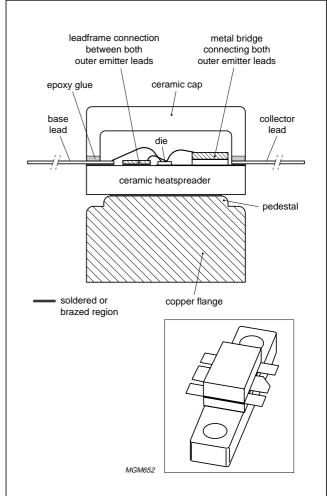


Fig.4-2 Construction of a typical ceramic package with flange.

4.5 Hermetic ceramic packages

A hermetic transistor package provides the highest levels of reliability in extremely harsh environments as required in aerospace and military applications for example.

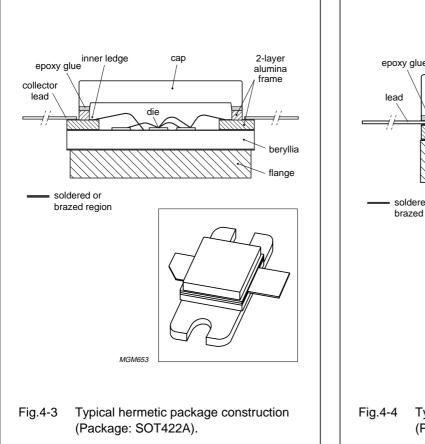
Ceramic packages can be made hermetic, however a special design is required. The leads are no longer brazed directly onto the heat-spreader as in a standard ceramic package but are brazed onto a two-layer alumina frame (i.e. consisting of two frames sintered together). The bottom frame is larger than the top one, thus forming inner and outer ledges (electrically connected by metallization on the bottom frame) The external leads are brazed to the outer ledge, while the inner ledge is used to make a connection to the transistor die by wire-bonding. The top side of the second frame is flat and completely metallized to enable a metal or ceramic cap to be soldered to it.

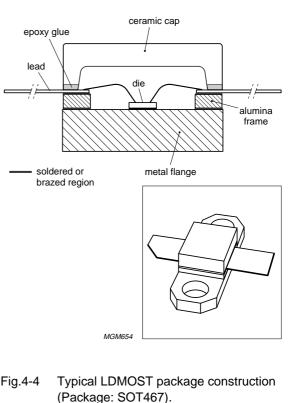
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4.6 LDMOST packages

Whereas the abovementioned packages are suitable for bipolar and VDMOS transistors, packages for the LDMOS transistors are somewhat different. This is because the bottom of an LDMOST die is the source, not the drain (collector) as in a standard MOS (bipolar) transistor. This is a major advantage as it is no longer necessary to electrically isolate the die from the heatsink in the application - the die is mounted directly on the flange. The flange material therefore must have a good thermal conductivity and a TCE close to that of silicon. Two materials in current use are a tungsten-copper alloy flange, and the copper-molybdenum-copper sandwich mentioned earlier. In order to electrically isolate the drain and gate leads from the flange, an alumina frame is brazed onto the flange, with the leads brazed on top of this frame. The package is completed by a ceramic cap sealed with epoxy.

Offering superb electrical and thermal performance, and ease of heatsinking, Philips' LDMOS packages are an attractive solution in an increasing number of applications.





4.7 Flangeless and SMD packages

In order to reduce the board space required by transistors, packages without a flange have been introduced (e.g. SOT333). Eliminating the flange however also eliminates the mounting holes, so other mounting methods have to be used. These include clamping or even reflow soldering. Eliminating the flange is in general only possible with packages for bipolar devices in which the dies are mounted on a ceramic heat-spreader. However, for Philips' SOT391B package, eliminating the flange alone was not an option as this package has through-plated holes in the heat-spreader. Without a flange, the package could not be sealed adequately. The solution is to braze a thin copper plate to the back of the package. This has two advantages. First, the holes are sealed, and second, the lead height of the package can be optimized to suit standard printed board materials.

With LDMOST packages, the entire flange cannot be eliminated as the dies are mounted on top of the flange. The board space required can be reduced however by reducing the length of the flange, most effectively by shortening it to the size of the alumina frame. Packages with such modified flanges are often referred to as 'earless'. Clamping or reflow soldering are again the recommended mounting methods.

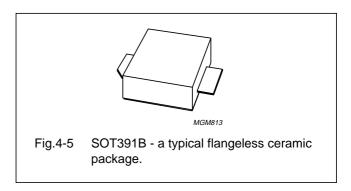
Besides flangeless and earless packages, Philips has introduced a leaded surface-mount package (SOT409). This package, which is based upon the plastic SO8 package, has a copper backpad, a ceramic (alumina or AIN) heat-spreader, a copper leadframe extending beyond the heat-spreader and a ceramic cap. The backpad enables the package to be soldered onto a PCB. To ensure reliable solder joints and low thermal resistance, the specification stipulates that the leads are J-shaped such that backpads and leads are coplanar to within 0.1 mm, and that the leads never extend beyond the backpad plane.

An even more effective way of reducing the required board area is to use leadless packages. Besides saving board space, these are highly cost-effective as they can be mounted in a standard automated SMD reflow soldering process. This kind of package consists of a ceramic (AIN) heat-spreader and a ceramic cap. Leads are replaced by plated contacts on the package sides. To increase the soldering area for the electrical connections (and to obtain more reliable solder joints), the plating is extended onto the back of the package.

Reflow soldering footprints are available for all SMD packages for optimum soldering results. For optimum heat flow between package and heatsink (through a printed

RF and microwave transistor packages

circuit board), it is recommended to incorporate vias in the board. The optimum size and location of these vias for each package are available.



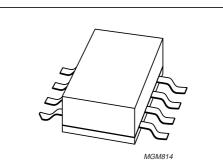
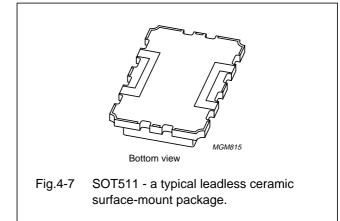


Fig.4-6 SOT409B - a ceramic surface-mount transistor package derived from the SO8 package.



4.8 Coefficients of linear thermal expansion of packages

The data of Tables 4-1 and 4-2 (together with manufacturers' board and heatsink data) can be used to obtain good thermal matching in practical amplifiers.

Table 4-1 Overview of materials used in packages

PACKAGE		FLANGE		LEADFRAME				BACKPAD	CERAMIC INSULATOR	
	COPPER	TUNGSTEN -COPPER	Cu-Mo-Cu	ALLOY 42 (Fe58/Ni42)	NICKEL	KOVAR (Fe54/Ni29)	COPPER	COPPER	BeO	AIN
SOT119		_	_	\checkmark	-	_	_	_	\checkmark	_
SOT121		-	_	\checkmark	-	_	_	_	\checkmark	1
SOT123		_	_	\checkmark	-	_	_	_	\checkmark	1
SOT161		_	_		_	_	_	_	\checkmark	-
SOT171	\checkmark	_	_	\checkmark	_	_	_	_		_
SOT262	_		_	\checkmark	_	_	_	_		_
SOT268	_		_		-	_	_	_		_
SOT273		_	_	\checkmark	-	_	_	_	\checkmark	_
SOT279	\checkmark	_	_	\checkmark	-	_	_	_		_
SOT289	_		_		-	\checkmark	_	_		_
SOT324	_		_	\checkmark	-	_	_	_		_
SOT333	\checkmark	_	_	\checkmark	_	_	_	_		_
SOT390	_		_	\checkmark	_	_	_	_		_
SOT391	_	√	_		_	_	_	_		-
SOT391B	_	_	_	\checkmark	_	_	_	\checkmark		_
SOT409	_	_	_	_	_	_	\checkmark	\checkmark	_	
SOT422	\checkmark	_	_	_	ν	_	_	_		_
SOT423	\checkmark	_	_	_		_	_	_		_
SOT437	_		_	\checkmark		_	_	_		_
SOT439	\checkmark	_	_	_		_	_	_		_
SOT440	\checkmark	_	_	_	_	\checkmark	_	_		_
SOT443	_	√	_	_	_		_			
SOT445		_	_	_	_		_	_		_
SOT448	_	√	_	_		_	_	_		_
SOT460	_	√	_		_	_	_		\checkmark	_
SOT467	_	√	_		_	_	_	_	_	_
SOT468	_	_			_	_	_		_	
SOT502	_		_		_	_	_	_	_	_
SOT511	_	_	_	_	_	_	_	_	_	

Source: Suppliers' data sheets

Philips Semiconductors

RF transmitting transistor and power amplifier fundamentals

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Table 4-2 Coefficients of linear thermal expansion, α , (in ppm/K) of package materials between 25 and 150 °C;										
COPP	ER TUNG	STEN PER	Cu-Mo-Cu	ALLOY 42 (Fe58/Ni42)	NICKEL	KOVAR (Fe54/Ni29/Co17)	BERYLLIA	ALUMINIUM NITRIDE		

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Source: Suppliers' data sheets

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4.9 Mounting recommendations

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When mounting transistors, observing the following recommendations will ensure good thermal and good electrical contact between transistor package and heatsink - a requisite for trouble-free, reliable operation.

9.5-6.0

4.9.1 Heatsink preparation

- For transistors dissipating up to 80 W, heatsink thickness should be:
 - At least 3 mm for copper heatsinks (>99.9% ETP-Cu)
 - At least 5 mm for aluminium heatsinks (99% Al)

These thicknesses should be increased proportionally for transistors dissipating more power.

- Minimum depth of tapped holes in heatsinks: 6 mm
- Ensure holes in heatsinks are free of burrs
- Ensure that the mounting area is at a level such that there is a small positive clearance between the transistor leads and the printed circuit board. This prevents any upward bending of the leads which can damage the ceramic heat-spreader and/or the encapsulation.
- Flatness of the mounting area: better than 0.02 mm
- Mounting area roughness: <0.5 μm
- Mounting area should be free of oxidation.
- 4.9.2 Printed circuit board preparation
- Tin and wash the printed circuit board.

4.9.3 Transistor preparation

- Transistor leads are gold plated. To avoid brittle solder joints (due to too much gold in the joint), pre-tin the leads, for example, by dipping their full length into a solder bath at a temperature of about 230 °C. Minimize the use of flux.

- Apply a thin, evenly-distributed layer of heatsink compound to the flange
- Recommended heatsink compounds are:
 - 'WPS II' (silicone free) Austerlitz-Electronics
 - '340' from Dow Corning.

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- When using a thermal pad, take special care with respect to the size as well as the positioning of the pad. If the pad does not cover the entire flange, the package can be stressed so much that the ceramic heat-spreader cracks. Ensure that mounting screws do not contact the thermal pad (prevents the pad wrinkling if the screws are turned).

4.9.4 Mounting sequence

- Position the device with the washers in place
- Use 4-40 UNC-2A cheese-head screws with a flat washer to spread the joint pressure
- Tighten the screws until finger tight (0.05 Nm)
- _ Further tighten the screws until the specified torque is reached (do not lubricate); for torgues, refer to the package outlines section of each data handbook
- To lock mounting screws, allow about 30 minutes for them to bed-down after the specified torque has been applied, re-tighten to the specified torque and apply locking paint
- Solder the transistor leads onto the printed circuit board.

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