HB28B1700IA2SR
HB28B1000IA2SR
HB28B512IA2SR

Wide Temperature Range Version
IDE Card

REJ03C0043-0200Z
(Previous ADE-203-1381A (Z) Rev.1.0)
Rev. 2.00
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Description

HB28B1700IA2SR, HB28B1000IA2SR, HB28B512IA2SR are IDE cards. These cards comply with ATA-5 specification standard, and are suitable for the usage of data storage memory medium for PC or any other electric equipment. These cards are equipped with Renesas 512 Mega bit Flash memory. By using these cards it is possible to operate good performance for a system which has ATA interface.

Features

- Conform to ANSI AT Attachment-5 (ATA-5) specification standard
- 5 V power supplies are used
- Card density is 1.7 Giga bytes maximum
  - This card is equipped with Renesas 512 Mega bit Flash memory
- Data write is 300,000 cycle/block
- Temperature range: −25 to +85°C
- Data reliability is less than 1 error in 10^{14} bits read
- High reliability based on internal ECC (Error Correcting Code) function
- High reliability based on CRC (Cyclic Redundancy Code) on Ultra DMA mode transfer

Card Line Up*[1]

Type No.	Card density	Capacity*[4]	Total sectors/ card*[3]	Sectors/ track*[2]	Number of head	Number of cylinder
HB28B1700IA2SR	1.7 GB	1,794,465,792 byte	3,504,816	63	16	3,477
HB28B1000IA2SR	1.0 GB	1,025,482,752 byte	2,002,896	63	16	1,987
HB28B512IA2SR	512 MB	512,483,328 byte	1,000,944	63	16	993

Notes: 1. These data are written in ID.
2. Total tracks = number of head × number of cylinder.
3. Total sectors/card = sectors/track × number of head × number of cylinder.
4. It is the logical address capacity including the area which is used for file system.

Card Pin Assignment

Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	GND	24	—	47	—
2	D3	25	—	48	—
3	D4	26	—	49	—
4	D5	27	A2	50	—
5	D6	28	A1	51	VCC
6	D7	29	A0	52	—
7	-CS0	30	D0	53	—
8	—	31	D1	54	—
9	—	32	D2	55	—
10	—	33	-IOIS16	56	-CSEL
11	—	34	GND	57	—*1
12	—	35	GND	58	-RESET
13	—	36	—*1	59	IORDY
14	—	37	D11	60	DMARQ
15	—	38	D12	61	-DMACK
16	INTRQ	39	D13	62	-DASP
17	V_{CC}	40	D14	63	-PDIAG
18	—	41	D15	64	D8
19	—	42	-CS1	65	D9
20	—	43	—*1	66	D10
21	—	44	-DIOR	67	—*1
22	—	45	-DIOW	68	GND
23	—	46	—		

Note: 1. Host system should not connect these pin.

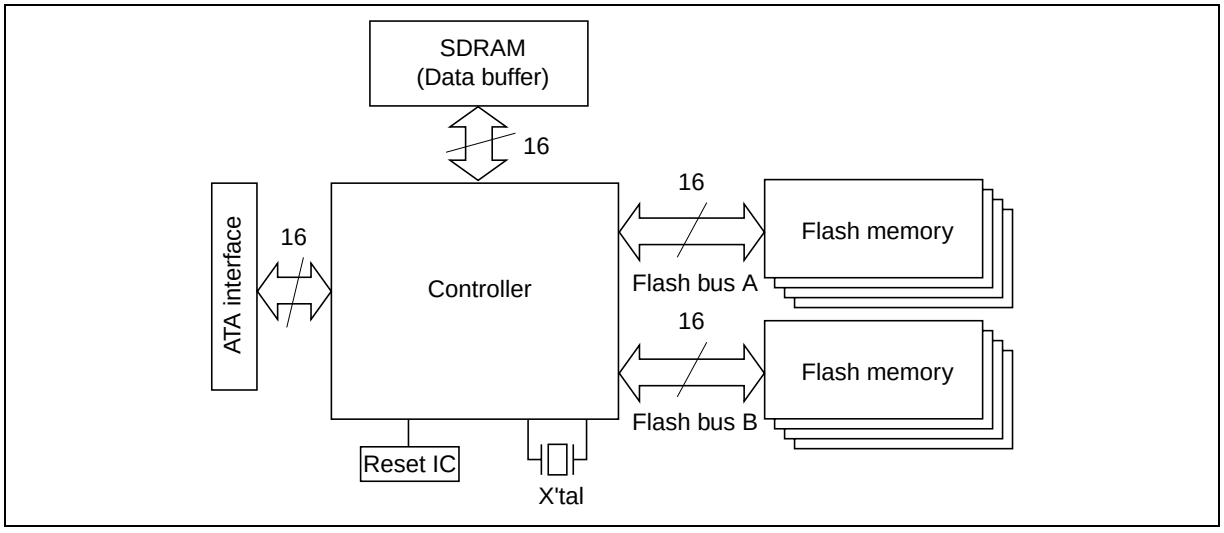
Card Pin Explanation

Host Interface Pin Explanation

Signal name	Direction	Pin No.	Description
-RESET	I	58	This signal is active low host reset pin. Once the host asserts -RESET, the host must keep -RESET asserting for at least 25 µs.
A2 to A0	I	27, 28, 29	Address bus of Host I/F is A2 to A0. A2 is MSB and A0 is LSB.
D15 to D0	I/O	41, 40, 39 38, 37, 66 65, 64, 6 5, 4, 3 2, 32, 31 30	Data bus of Host I/F is D15 to D0. D0 is the LSB of the even byte of the word. D8 is the LSB of the odd byte of the word.
-CS0 -CS1	I	7, 42	-CS1 is used for selecting the Alternate Status register and the Device Control register. -CS0 is used for the other task file registers.
-DIOW	I	45	-DIOW is used for control of write data in I/O task file area.
STOP (Ultra DMA mode)			This signal must be negated prior to initiation of an Ultra DMA burst. And this signal must be negated before data is transferred in an Ultra DMA burst. Assertion during an Ultra DMA burst flowing indicates the termination of the Ultra DMA burst.
-DIOR	I	44	-DIOR is used for control of read data in I/O task file area.
-HDMARDY (Ultra DMA data-in)			-HDMARDY is a data flow control signal. The host shall assert this signal to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate this signal to indicate that the host pauses an Ultra DMA data-in burst.
HSTROBE (Ultra DMA data-out)			HSTROBE is a data strobe signal. Both the rising and falling edges of HSTROBE latch the data of D15 to D0 into this card. Stopping generating HSTROBE edges indicates that the host pauses an Ultra DMA data-out burst.
-DMACK	I	61	This signal is used for response to asserting DMARQ to initiate DMA transfers.
-IOIS16	O	33	This output signal is asserted low when the 16-bit wide data register is addressed and the card is prepared to send or receive a 16-bit wide data.
INTRQ	O	16	This signal is the active high Interrupt Request to the host.
DMARQ	O	60	This signal is asserted high when the card is ready to DMA data transfers.
-PDIAG	I/O	63	-PDIAG is the Pass Diagnostic signal in Master/Slave handshake protocol.

Signal name	Direction	Pin No.	Description
IORDY	O	59	IORDY is used at PIO modes 3 and above. IORDY is negated to extend the host transfer cycle of any host register access (Read or Write) when the card is not ready to respond to a data transfer request.
DSTROBE (Ultra DMA data-in)			DSTROBE is a data strobe signal. The host latches the data of D15 to D0 at both the rising and falling edge of DSTROBE. Stopping generating DSTROBE edges indicates that the card pauses an Ultra DMA data-in burst.
-DDMARDY (Ultra DMA data-out)			-DDMARDY is a data flow control signal. The card asserts this signal to indicate that the card is ready to receive Ultra DMA data-out bursts. The card negates this signal to indicate that the card pauses an Ultra DMA data-out burst.
-DASP	I/O	62	-DASP is the Device Active/Slave Present signal in the Master/Slave handshake protocol.
-CSEL	I	56	This signal is used to configure this card as a Master or a Slave. When this pin is grounded, this card is configured as a Master. When the pin is open, this card is configured as a Slave.

Card Block Diagram



Card Function Explanation

Register Construction

- Task File region
  - Data register
  - Error register
  - Feature register
  - Sector Count register
  - Sector Number register
  - Cylinder Low register
  - Cylinder High register
  - Device Head register
  - Status register
  - Alternate Status register
  - Command register
  - Device Control register

Host Access Specifications

Read I/O Function

Mode	-CS1	-CS0	A2 to A0	-DIOR	-DIOW	D15 to D8	D7 to D0
Invalid mode	L	L	×	×	×	High-Z	High-Z
Standby mode	H	H	×	×	×	High-Z	High-Z
Data register access	H	L	0	L	H	odd byte	even byte
Alternate status access	L	H	6H	L	H	×	status out
Other task file access	H	L	1-7H	L	H	×	data out

Note: ×: L or H

Write I/O Function

Mode	-CS1	-CS0	A2 to A0	-DIOR	-DIOW	D15 to D8	D7 to D0
Invalid mode	L	L	×	×	×	don't care	don't care
Standby mode	H	H	×	×	×	don't care	don't care
Data register access	H	L	0	H	L	odd byte	even byte
Device Control register access	L	H	6H	H	L	don't care	control in
Other task file access	H	L	1-7H	H	L	don't care	data in

Note: ×: L or H

Task File Register Specification

These registers are used for reading and writing the storage data in this card. The decoded addresses are shown as follows.

I/O map

-CS1	-CS0	A2	A1	A0	-DIOR	-DIOW
0	1	0	0	0	Data register	Data register
0	1	0	0	1	Error register	Feature register
0	1	0	1	0	Sector Count register	Sector Count register
0	1	0	1	1	Sector Number register	Sector Number register
0	1	1	0	0	Cylinder Low register	Cylinder Low register
0	1	1	0	1	Cylinder High register	Cylinder High register
0	1	1	1	0	Device Head register	Device Head register
0	1	1	1	1	Status register	Command register
1	0	1	1	0	Alt. Status register	Device Control register

1. Data register: This register is a 16-bit register that has read/write ability, and it is used for transferring 1 sector data between the card and the host.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D15 to D0															

2. Error register: This register is a read only register, and it is used for analyzing the error content at the card accessing. This register is valid when the BSY bit in Status register and Alternate Status register are set to "0" (Ready).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ICRC	UNC	0	IDNF	0	ABRT	0	0

bit	Name	Function
7	ICRC (Interface CRC error)	This bit is set to one when an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA data transfer.
6	UNC (Data ECC error)	This bit is set when Uncorrectable error is occurred at reading the card.
4	IDNF (ID Not Found)	The requested sector cannot be found.
2	ABRT (ABoRTed command)	This bit is set if the command has been aborted because of the card status condition. (Not ready, Write fault, Invalid command, etc.)

3. Feature register: This register is write only register, and provides information regarding features of the card which the host wishes to utilize.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature byte							

4. Sector Count register: This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value of this register is zero, a count of 256 sectors is specified. This register's initial value is "01H".

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector count byte							

5. Sector Number register: This register contains the starting sector number which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector number byte							

6. Cylinder Low register: This register contains the low 8-bit of the starting cylinder address which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder low byte							

7. Cylinder High register: This register contains the high 8-bit of the starting cylinder address which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder high byte							

8. Device Head register: This register is used for selecting the Device number and Head number for the following command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	LBA	1	DEV	Head number			

bit	Name	Function
7	1	This bit is set to "1".
6	LBA	LBA is a flag to select either Cylinder / Head / Sector (CHS) or Logical Block Address (LBA) mode. When LBA=0, CHS mode is selected. When LBA=1, LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows: LBA07-LBA00: Sector Number register. LBA15-LBA08: Cylinder Low register. LBA23-LBA16: Cylinder High register. LBA27-LBA24: Head number in Device Head register.
5	1	This bit is set to "1".
4	DEV (DEVice select)	This bit is used for selecting the Master (Device 0) and Slave (Device 1) in Master/Slave organization.
3 to 0	Head number	This bit is used for selecting the Head number for the following command. Bit 3 is MSB.

9. Status register: This register is read only register, and it indicates the card status of command and reset execution. Other bits are invalid when BSY bit is "1". When this register is read, H_INTRQ is negated.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

bit	Name	Function
7	BSY (BuSY)	This bit is set when the card internal operation is executing. When this bit is set to "1", other bits in this register are invalid.
6	DRDY (Device ReaDY)	If this bit and DSC bit are set to "1", the card is capable of receiving the read or write or seek requests.
5	DWF (Device Write Fault)	This bit is set if this card indicates the write fault status.
4	DSC (Device Seek Complete)	This bit is set when the card seek complete.
3	DRQ (Data ReQuest)	This bit is set when the information can be transferred between the host and Data register. This bit is cleared when the card receives the other command.
2	CORR (CORRected data)	This bit is set when a correctable data error has been occurred and the data has been corrected.
1	IDX (InDeX)	This bit is always set to "0".
0	ERR (ERRor)	This bit is set when the previous command has ended in some type of error. The error information is set in Error register. This bit is cleared by the next command.

10. Alternate Status register: This register is the same as Status register physically, so the bit assignment refers to previous item of Status register. But this register is different from Status register that INTRQ is not negated when data read.

11. Command register: This register is write only register, and it is used for writing the command at executing the card operation. The command code is written in the command register, after the parameter is written in the Task File registers during the card is Ready state.

12. Device Control register: This register is write only register, and it is used for controlling the card interrupt request and issuing an ATA soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
×	×	×	×	×	SRST	nIEN	0

bit	Name	Function
7 to 3	×	don't care
2	SRST (Software ReSeT)	This bit is set to "1" in order to force the card to perform Task File Reset operation. Once the host sets SRST bit to "1", SRST bit must be kept to "1" for at least 5 μs. The card remains in Reset until this bit is reset to "0". While BSY bit is set to "1" in Status register as a result of executing either the power-on or hardware reset protocol, the host must not set SRST bit to "1" in Device Control register.
1	nIEN (Interrupt ENable)	This bit is used for enabling INTRQ. When this bit is set to "0", INTRQ is enabled. When this bit is set to "1", INTRQ is disabled.
0	0	This bit is set to "0".

ATA Command specifications

This table summarizes the ATA Command set with the paragraphs. Following shows the support commands and command codes which are written in command registers.

ATA Command Set

No.	Command set	Code	FR	SC	SN	CY	DR	HD	LBA
1	CHECK POWER MODE	98h,E5h	N	N	N	N	Y	N	N
2	EXECUTE DEVICE DIAGNOSTIC	90h	N	N	N	N	N	N	N
3	FLUSH CACHE	E7h	N	N	N	N	Y	N	N
4	FORMAT TRACK	50h	N	Y	Y	Y	Y	Y	Y
5	IDENTIFY DEVICE	ECh	N	N	N	N	Y	N	N
6	IDLE	97h,E3h	N	Y	N	N	Y	N	N
7	IDLE IMMEDIATE	95h,E1h	N	N	N	N	Y	N	N
8	INITIALIZE DEVICE PARAMETERS	91h	N	Y	N	N	Y	Y	N
9	NOP	00h	N	N	N	N	Y	N	N
10	READ BUFFER	E4h	N	N	N	N	Y	N	N
11	READ DMA	C8h,C9h	N	Y	Y	Y	Y	Y	Y
12	READ LONG	22h,23h	N	Y	Y	Y	Y	Y	Y
13	READ MULTIPLE	C4h	N	Y	Y	Y	Y	Y	Y
14	READ NATIVE MAX ADDRESS	F8h	N	N	N	N	Y	N	Y
15	READ SECTOR(S)	20h,21h	N	Y	Y	Y	Y	Y	Y
16	READ VERIFY SECTOR(S)	40h,41h	N	Y	Y	Y	Y	Y	Y
17	RECALIBRATE	1Xh	N	N	N	N	Y	N	Y
18	SEEK	7Xh	N	N	Y	Y	Y	Y	Y
19	SET FEATURES SET TRANSFER MODE	EFh	03h	Y	N	N	Y	N	N

No.	Command set	Code	FR	SC	SN	CY	DR	HD	LBA
20	SET FEATURES SET 4BYTES APPENDED	EFh	BBh	N	N	N	Y	N	N
21	SET MAX ADDRESS	F9h	N	Y	Y	Y	Y	Y	Y
22	SET MAX SET PASSWORD	F9h	01h	N	N	N	Y	N	N
23	SET MAX LOCK	F9h	02h	N	N	N	Y	N	N
24	SET MAX UNLOCK	F9h	03h	N	N	N	Y	N	N
25	SET MAX FREEZE LOCK	F9h	04h	N	N	N	Y	N	N
26	SET MULTIPLE MODE	C6h	N	Y	N	N	Y	N	N
27	SLEEP	99h,E6h	N	N	N	N	Y	N	N
28	SMART ENABLE/DISABLE AUTO SAVE	B0h	D2h	Y	N	Y	Y	N	N
29	SMART ENABLE OPERATION	B0h	D8h	N	N	Y	Y	N	N
30	SMART DISABLE OPERATION	B0h	D9h	N	N	Y	Y	N	N
31	SMART RETURN STATUS	B0h	DAh	N	N	Y	Y	N	N
32	STANDBY	96h,E2h	N	Y	N	N	Y	N	N
33	STANDBY IMMEDIATE	94h,E0h	N	N	N	N	Y	N	N
34	WRITE BUFFER	E8h	N	N	N	N	Y	N	N
35	WRITE DMA	CAh,CBh	N	Y	Y	Y	Y	Y	Y
36	WRITE LONG	32h,33h	N	Y	Y	Y	Y	Y	Y
37	WRITE MULTIPLE	C5h	N	Y	Y	Y	Y	Y	Y
38	WRITE SAME	E9h	Y	Y	Y	Y	Y	Y	Y
39	WRITE SECTOR(S)	30h,31h	N	Y	Y	Y	Y	Y	Y
40	WRITE VERIFY	3Ch	N	Y	Y	Y	Y	Y	Y

Note: FR: Feature register
SC: Sector Count register
SN: Sector Number register
CY: Cylinder Low/High register
DR: Device bit of Device/Head register
HD: Head No.(3 to 0) of Device/Head register
NH: No. of Heads
LBA: Logical Block Address
Y: Set up
N: Not set up

1. CHECK POWER MODE (code: 98h or E5h): This command checks the power mode.

2. EXECUTE DEVICE DIAGNOSTIC (code: 90h): This command performs the internal diagnostic tests implemented by the card.

3. FLUSH CACHE (code: E7h): This command is used by the host request the card to flush the write cache.

4. FORMAT TRACK (code: 50h): This command writes the desired head and cylinder of the selected drive. But selected sector data is not exchange. This controller excepts a sector buffer of data from the host to follow the command with same protocol as the WRITE SECTOR(S) command.

5. IDENTIFY DEVICE (code: ECh): The IDENTIFY DEVICE command enables the host to receive parameter information from the card.

IDENTIFY DEVICE Information

Word	bit	Description	Default value	F / V
0		General configuration bit-significant information		
	15	0 = ATA device	0040h	F
	14-8	Retired		
	7	1 = removable media device		
	6	1 = not removable controller and/or device		
	5-3	Retired		
	2	1 = Response incomplete		V
	1	Retired		F
	0	Reserved		
1		Default number of logical cylinders	xxxxh	V
2		Specific configuration	0000h	V
3		Default number of logical heads	xxxxh	F
4-5		Retired	0000h	F
6		Default number of logical sectors per logical track	xxxxh	F
7-8		Reserved for assignment by CompactFlash™ Association	0000h	V
9		Retired	0000h	F
10-19		Serial Number	xxxxh	F
20-21		Retired	0000h	F
22		Number of vendor specific bytes available on READ/WRITE LONG commands	0004h	F
23-26		Firmware revision (8 ASCII characters)	xxxxh	F
27-46		Model Number (40 ASCII characters)	xxxxh	F
47		READ/WRITE MULTIPLE support		
	15-8	80h	8010h	X
	7-0	Maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands		F
48		Reserved	0000h	R

Word	bit	Description	Default value	F / V
49		Capabilities		
	15-14	Reserved	2F00h	R
	13	1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device		F
	12	Reserved		R
	11	1 = device supports IORDY operation		F
	10	1 = device supports the disabling IORDY		
	9	1		R
	8	1		
	7-0	Retired		X
50		Capabilities		
	15	0	4000h	F
	14	1		
	13-1	Reserved		
	0	Shall be set to one to indicate a device specific Standby timer value minimum		
51		PIO data transfer mode number		
	15-8	00h = PIO mode-0 is supported	0200h	F
		01h = PIO mode-1 is supported		
		02h = PIO mode-2 is supported		
	7-0	Obsolete		X
52		Obsolete	0000h	R
53		Field validity		
	15-3	Reserved	0007h	R
	2	1 = Word88 is valid		F
	1	1 = Words 64 through 70 are valid		
	0	1 = Words 54 through 58 are valid		V
54		Number of current logical cylinders	xxxxh	V
55		Number of current logical heads	xxxxh	V
56		Number of current logical sectors per track	xxxxh	V
57-58		Current capacity in sectors	xxxxh	V
59		Multiple sector setting		
	15-9	Reserved	0110h	R
	8	1 = Multiple sector setting is valid		V
	7-0	xxh = Current setting for number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE command		

Word	bit	Description	Default value	F / V
60-61		Total number of user addressable sectors (LBA mode only)	xxxxh	F
62		obsolete	0000h	F
63		Multiword DMA transfer		
	15-11	Reserved	0007h	R
	10	1 = Multiword DMA mode-2 is selected		V
	9	1 = Multiword DMA mode-1 is selected		
	8	1 = Multiword DMA mode-0 is selected		
	7-3	Reserved		R
	2	1 = Multiword DMA mode-2 and below are supported		F
	1	1 = Multiword DMA mode-1 and below are supported		
	0	1 = Multiword DMA mode-0 is supported		
64		Advanced PIO transfer modes supported		
	15-2	Reserved	0003h	R
	1	1 = PIO mode-4 is supported		F
	0	1 = PIO mode-3 is supported		
65		Minimum Multiword DMA transfer cycle time per word	0078h	F
66		Manufacturer's recommended Multiword DMA transfer cycle time	0078h	F
67		Minimum PIO transfer cycle time without flow control	0078h	F
68		Minimum PIO transfer cycle time with IORDY flow control	0078h	F
69-79		Reserved	0000h	R
80		Major version number	0030h	F
81		Reserved	0000h	F

Word	bit	Description	Default value	F / V
82		Command sets supported		
	15	Obsolete	7409h	F
	14	1 = NOP command supported		
	13	1 = READ BUFFER command supported		
	12	1 = WRITE BUFFER command supported		
	11	Obsolete		
	10	1 = Host Protect Area feature set supported		
	9-5	Reserved		
	4	0		
	3	1 = Power Management feature set supported		
	2-1	Reserved		
	0	1 = SMART feature set supported		
83		Command sets supported		
	15	0	4100h	F
	14	1		
	13-9	Reserved		
	8	1 = SET MAX security extension supported		
	7-0	Reserved		
84	15	0	4000h	F
	14	1		
	13-0	Reserved		

Word	bit	Description	Default value	F / V
85		Command set/feature enabled		
	15	Obsolete	7408h	V
	14	1 = NOP command enabled		
	13	1 = READ BUFFER command enabled		
	12	1 = WRITE BUFFER command enabled		
	11	Obsolete		
	10	1 = Host Protect Area feature set enabled		
	9-5	Reserved		
	4	0		
	3	1 = Power Management feature set enabled		
	2-1	Reserved		
	0	1 = SMART feature set enabled		
86		Command set/feature enabled		
	15-9	Reserved	0000h	V
	8	1 = SET MAX security extension enabled by SET MAX SET PASSWORD		
	7-0	Reserved		
87		Command set/feature default		
	15	0	4000h	V
	14	1		
	13-0	Reserved		
88		Ultra DMA mode		
	15-13	Reserved	101Fh	R
	12	1 = Ultra DMA mode-4 is selected		V
	11	1 = Ultra DMA mode-3 is selected		
	10	1 = Ultra DMA mode-2 is selected		
	9	1 = Ultra DMA mode-1 is selected		
	8	1 = Ultra DMA mode-0 is selected		
	7-5	Reserved		R
	4	1= Ultra DMA mode-4 and below are supported		F
	3	1= Ultra DMA mode-3 and below are supported		
	2	1= Ultra DMA mode-2 and below are supported		
	1	1= Ultra DMA mode-1 and below are supported		
	0	1= Ultra DMA mode-0 is supported		

Word	bit	Description	Default value	F / V
89-92		Reserved	0000h	R
93		Hardware Reset result		
	15	0	xxxxh	V
	14	1		
	13	1 = device detected CBLID_N above V_{IH} 0 = device detected CBLID_N below V_{IL}		
	12	Reserved		
	11	0 = Device 1 did not assert H_PDIAG_N 1 = Device 1 asserted H_PDIAG_N		
	10-9	These bit indicate how Device1 determined the device number 00 = Reserved 01 = a jumper was used 10 = H_CSEL_N signal was used 11 = some other method was used or the method is unknown		
	8	1		
	7	Reserved		
	6	0 = Device 0 does not respond when Device 1 is selected 1 = Device 0 responds when Device 1 is selected		
	5	0 = Device 0 did not detect the assertion of H_DASP_N 1 = Device 0 detected the assertion of H_DASP_N		
	4	0 = Device 0 did not detect the assertion of H_PDIAG_N 1 = Device 0 detected the assertion of H_PDIAG_N		
	3	0 = Device 0 failed diagnostics 1 = Device 0 passed diagnostics		
	2-1	These bit indicate how Device 0 determined the device number. 00= Reserved 01 = a jumper was used 10 = H_CSEL_N signal was used 11 = some other method was used or the method was unknown		
	0	1		
94-128		Reserved	0000h	R

Word	bit	Description	Default value	F / V
129-159		Vendor Specific	0000h	X
160-254		Reserved	0000h	R
255		Integrity word	xxA5h	
	15-8	Checksum		V
	7-0	Signature		F

Note: 1. F: the content of the word is fixed and does not change.
V: the content of the word is variable and may change depending on the state of the device or the commands executed by the device.
X: the content of the word is Vendor Specific
R: the content of the word is reserved and set to zero

6. IDLE (code: 97h or E3h): This command allows the host to place the card in the Idle mode and also set the Standby timer. H_INTRQ_P may be asserted even through the card may not have fully transitioned to Idle mode. If the Sector Count register is non-zero then the Standby timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer. If the Sector Count register is zero then the Standby timer is disabled.

Automatic Standby timer periods

Sector Count register contents		Corresponding timeout period
0	(00h)	Timeout disabled
1-240	(01h-F0h)	(Value × 5)s
241-251	(F1h-FBh)	((Value – 240) × 30) min
252	(FCh)	21 min
253	(FDh)	Period between 8 and 12 hrs
254	(FEh)	Reserved
255	(FFh)	21 min 15s

Note: 1. Times are approximate.

7. IDLE IMMEDIATE (code: 95h or E1h): This command causes the card to set BSY, enter the Idle mode, clear BSY and generate an interrupt.

8. INITIALIZE DEVICE PARAMETERS (code: 91h): This command enables the host to set the number of sectors per track and the number of heads per cylinder.

9. NOP (code: 00h): If this command is issued, the card respond with command aborted.

10. READ BUFFER(code: E4h): This command enables the host to read the current contents of the card's sector buffer.

11. READ DMA (code: C8h or C9h): This command reads from 1 to 256 sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

12. READ LONG (code: 22h or 23h): This command is provided for compatibility purposes and nearly performs one sector READ SECTOR(S) command except that it transfers the data and 4 bytes appended to the sector. These appended 4 bytes are all 0 data.

13. READ MULTIPLE (code: C4h): This command performs similarly to the READ SECTOR(S) command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

14. READ NATIVE MAX ADDRESS (code: F8h): This command returns the native maximum address.

15. READ SECTOR(S) (code: 20h or 21h): This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

16. READ VERIFY SECTOR(S) (code: 40h or 41h): This command is identical to the READ SECTOR(S) command, except that DRQ is never set and no data is transferred to the host .

17. RECALIBRATE (code: 1Xh): This command return value is select address mode by the host request.

Return address mode status

Request Addressing	Sector Number Reg.
CHS	0x01h
LBA	0x00h

18. SEEK (code: 7Xh): This command perform a range check.

19. SET FEATURES SET TRANSFER MODE (code: EFh): This command is a host can choose the transfer mechanism by Set Transfer Mode.

20. SET FEATURES SET 4BYTES APPENDED (code: EFh): This command allows the host to set the 4 byte data appended to the data transfer on READ LONG and WRITE LONG commands.

21. SET MAX ADDRESS (code: F9h): This command allows the host to redefine the maximum address of the user-accessible address space.

22. SET MAX SET PASSWORD (code: F9h): This command requests a transfer of a single sector of data from the host. Password data table defines the content of this sector of information. The password is retained by the card until the next power cycle. When the card accepts this command the card is in Set Max Unlocked state.

SET MAX SET PASSWORD content

Word	Content
0	Reserved
1-16	Password (32 bytes)
17-255	Reserved

23. SET MAX LOCK (code: F9h): This command sets the card into Set Max Locked state. After this command is completed any other SET MAX commands except SET MAX UNLOCK and SET MAX FREEZE LOCK are rejected. The card remains in this state until a power cycle or the acceptance of a SET MAX UNLOCK or SET MAX FREEZE LOCK command.

24. SET MAX UNLOCK (code: F9h): This command requests a transfer of a single sector of data from the host. Password data Table defines the content of this sector of information. The password supplied in the sector of data transferred shall be compared with the stored SET MAX password. If the password compare fails, then the card returns command aborted and decrements the unlock counter. On the acceptance of the SET MAX LOCK command, this counter is set to a value of five and shall be decremented for each password mismatch when SET MAX UNLOCK is issued and the card is locked. When this counter reaches zero, then the SET MAX UNLOCK command shall return command aborted until a power-cycle. If the password compare matches, then the card shall make a transition to the Set Max Unlocked state and all SET MAX commands shall be accepted.

SET MAX SET PASSWORD content

Word	Content
0	Reserved
1-16	Password (32 bytes)
17-255	Reserved

25. SET MAX FREEZE LOCK (code: F9h): The SET MAX FREEZE LOCK command sets the card to Set Max Frozen state. After command completion any subsequent SET MAX commands are rejected. Commands disabled by Set Max Freeze Lock

- SET MAX ADDRESS
- SET MAX SET PASSWORD
- SET MAX LOCK
- SET MAX UNLOCK

26. SET MULTIPLE MODE (code: C6h): This command enables the card to perform READ/WRITE MULTIPLE operations and establishes the block count for these commands.

27. SLEEP (code: 99h or E6h): This command causes the card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

28. SMART ENABLE/DISABLE AUTO SAVE (code: B0h): This command enables and disables the optional attribute auto save feature of the card.

29. SMART ENABLE OPERATIONS (code: B0h): This command enables access to all SMART capabilities within the card.

30. SMART DISABLE OPERATIONS (code: B0h): This command disables all SMART capabilities within the card.

31. SMART RETURN STATUS (code: B0h): This command causes the card return the reliability status of the card to the host.

32. STANDBY (code: 96h or E2h): This command causes the card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

33. STANDBY IMMEDIATE (code: 94h or E0h): This command causes the card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

34. WRITE BUFFER (code: E8h): This command enables the host to overwrite contents of the card's sector buffer with any data pattern desired.

35. WRITE DMA (code: CAh or CBh): This command writes from 1 to 256 sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

36. WRITE MULTIPLE (code: C5h): This command is similar to the WRITE SECTOR(S) command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by SET MULTIPLE MODE command.

37. WRITE LONG (code: 32h or 33h): This command is provided for compatibility purposes and nearly performs one sector WRITE SECTOR(S) command except that it transfers the data and 4 bytes appended to the sector. These appended 4 bytes are not written on the flash memories.

38. WRITE SAME (code: E9h): This command nearly performs one sector WRITE SECTOR(S) command except that only one sector of data transferred. The Sector Count register value means one sector data write counts. (ex: value is 5 to nearly fifth one sector write execute.)

39. WRITE SECTOR(S) (code: 30h or 31h): This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

40. WRITE VERIFY (code: 3Ch): This command is similar to the WRITE SECTOR(S) command, except that each sector is verified before the command is completed.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
All input/output voltages	Vin, Vout	–0.3 to V_{CC} + 0.3	V	1
V_{CC} voltage	V_{CC}	–0.3 to +6.7	V	
Operating temperature range	Topr	–25 to +85	°C	
Storage temperature range	Tstg	–25 to +85	°C	

Notes: 1. Vin, Vout min = –2.0 V for pulse width ≤ 20 ns.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating temperature	Ta	0	25	70	°C
V_{CC} voltage	V_{CC}	4.5	5.0	5.5	V

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	—	25	pF	Vin = 0 V	1
Output capacitance	Cout	—	—	25	pF	Vout = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

DC Characteristics-1 (Ta = –25 to +85°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Output leakage current	I_{LO}	—	—	1	µA	Vout = high impedance	1
Pull-up current	$-I_{PE}$	40	100	240	µA	Vin = GND	
Output voltage	V_{OL}	—	—	0.5	V	I_{OL} = 4 mA	2
	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA	2
Input voltage	V_{IL}	—	—	0.8	V		
	V_{IH}	2.2	—	—	V		

Note: 1. Except pulled up input pin.
2. Output voltage is measured at static status.

DC Characteristics-2 (Ta = –25 to +85°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Sleep current	I_{SL}	—	5	10	mA	CMOS level (Host control signal = V_{CC} – 0.2)	
Standby current	I_{SB}	—	10	20	mA	CMOS level (Host control signal = V_{CC} – 0.2)	
Idle current	I_{ID}	—	100	150	mA	CMOS level (Host control signal = V_{CC} – 0.2)	
Sector read current	I_{CCR} (DC)	—	170	220	mA	CMOS level (Host control signal = V_{CC} – 0.2)	1
	I_{CCR} (Peak)	—	200	300	mA	CMOS level (Host control signal = V_{CC} – 0.2)	1
Sector write current	I_{CCW} (DC)	—	550	900	mA	CMOS level (Host control signal = V_{CC} – 0.2)	2
	I_{CCW} (Peak)	—	800	1300	mA	CMOS level (Host control signal = V_{CC} – 0.2)	2

Notes 1. Measured during sector read transfer.
2. Measured during sector write transfer.

AC Characteristics (Ta = –25 to +85°C, V_{CC} = 5 V ± 10%)

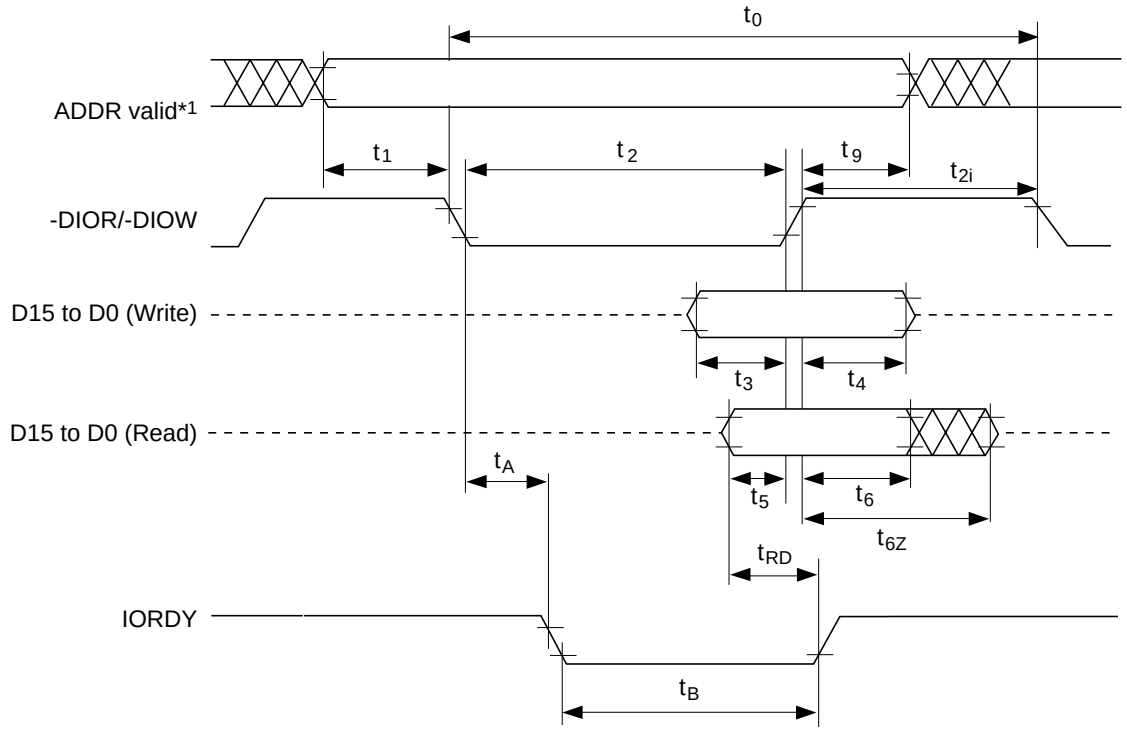
Register Access AC Characteristics

Parameter		Symbol	Mode0	Mode1	Mode2	Mode3	Mode4	Unit
Cycle time	(min)	t_0	600	383	330	180	120	ns
Address valid to -DIOR/-DIOW setup	(min)	t_1	70	50	30	30	25	ns
-DIOR/-DIOW pulse width 8bit	(min)	t_2	290	290	290	80	70	ns
-DIOR/-DIOW recovery time	(min)	t_{2i}	—	—	—	70	25	ns
-DIOW data setup	(min)	t_3	60	45	30	30	20	ns
-DIOW data hold	(min)	t_4	30	20	15	10	10	ns
-DIOR data setup	(min)	t_5	50	35	20	20	20	ns
-DIOR data hold	(min)	t_6	5	5	5	5	5	ns
-DIOR data tristate	(max)	t_{6Z}	30	30	30	30	30	ns
-DIOR/-DIOW to address valid hold	(min)	t_9	20	15	10	10	10	ns
Read data valid to IORDY active (If IORDY initially low after t_A)	(min)	t_{RD}	0	0	0	0	0	ns
IORDY setup time	(min)	t_A	35	35	35	35	35	ns
IORDY pulse width	(max)	t_B	1250	1250	1250	1250	1250	ns

PIO Mode Access AC Characteristics

Parameter		Symbol	Mode0	Mode1	Mode2	Mode3	Mode4	Unit
Cycle time	(min)	t_0	600	383	240	180	120	ns
Address valid to -DIOR/-DIOW setup	(min)	t_1	70	50	30	30	25	ns
-DIOR/-DIOW pulse width 16bit	(min)	t_2	165	125	100	80	70	ns
-DIOR/-DIOW recovery time	(min)	t_{2i}	—	—	—	70	25	ns
-DIOW data setup	(min)	t_3	60	45	30	30	20	ns
-DIOW data hold	(min)	t_4	30	20	15	10	10	ns
-DIOR data setup	(min)	t_5	50	35	20	20	20	ns
-DIOR data hold	(min)	t_6	5	5	5	5	5	ns
-DIOR data tristate	(max)	t_{6Z}	30	30	30	30	30	ns
-DIOR/-DIOW to address valid hold	(min)	t_9	20	15	10	10	10	ns
Read data valid to IORDY active (If IORDY initially low after t_A)	(min)	t_{RD}	0	0	0	0	0	ns
IORDY setup time	(min)	t_A	35	35	35	35	35	ns
IORDY pulse width	(max)	t_B	1250	1250	1250	1250	1250	ns

Register Access/PIO Mode Access Timing

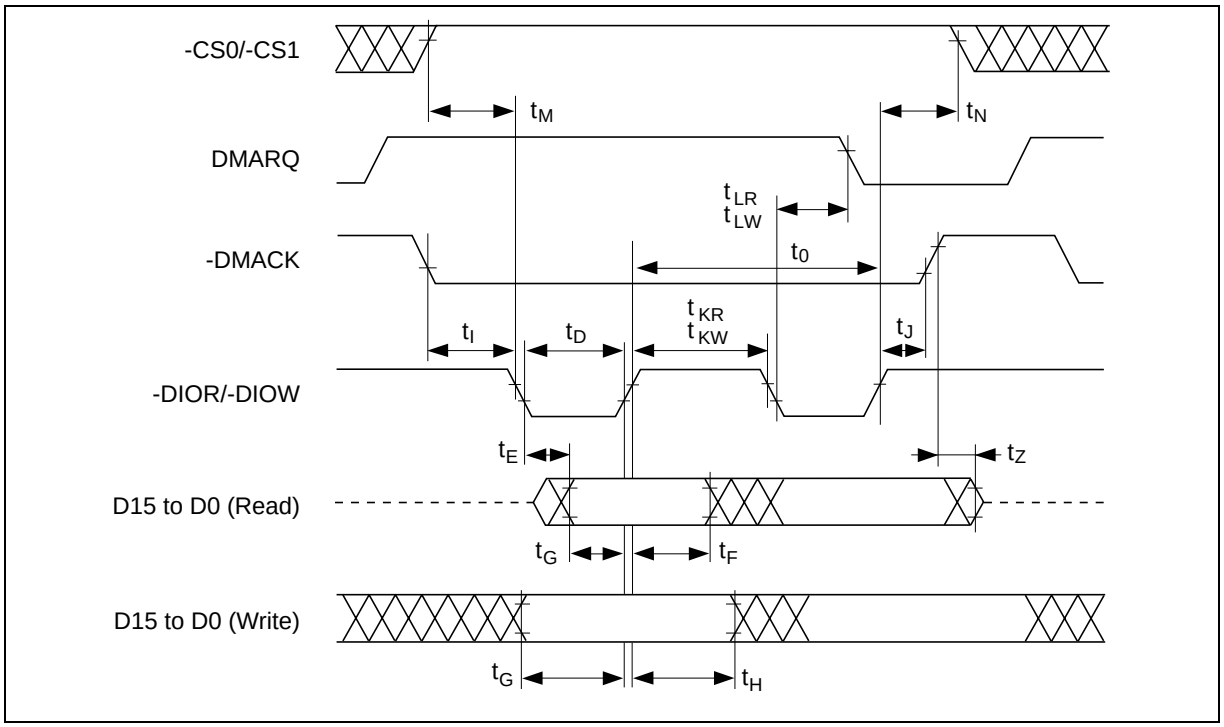


Note: 1. ADDR valid consists of signals -CS0, -CS1 and A2 to A0.

Multiword DMA Mode Access AC Characteristics

Parameter		Symbol	Mode0	Mode1	Mode2	Unit
Cycle time	(min)	t_0	480	150	120	ns
-DIOR/-DIOW asserted pulse width	(min)	t_D	215	80	70	ns
-DIOR data access	(max)	t_E	150	60	50	ns
-DIOR data hold	(min)	t_F	5	5	5	ns
-DIOR/-DIOW data setup	(min)	t_G	100	30	20	ns
-DIOW data hold	(min)	t_H	20	15	10	ns
-DMACK to -DIOR/-DIOW setup	(min)	t_I	0	0	0	ns
-DIOR/-DIOW to -DMACK hold	(min)	t_J	20	5	5	ns
-DIOR negated pulse width	(min)	t_{KR}	50	50	25	ns
-DIOW negated pulse width	(min)	t_{KW}	215	50	25	ns
-DIOR to DMARQ delay	(max)	t_{LR}	120	40	35	ns
-DIOW to DMARQ delay	(max)	t_{LW}	40	40	35	ns
-CS0/-CS1 valid to -DIOR/-DIOW	(min)	t_M	50	30	25	ns
-CS0/-CS1 hold	(min)	t_N	15	10	10	ns
-DMACK to read data released	(max)	t_Z	20	25	25	ns

Multiword DMA Mode Access Timing



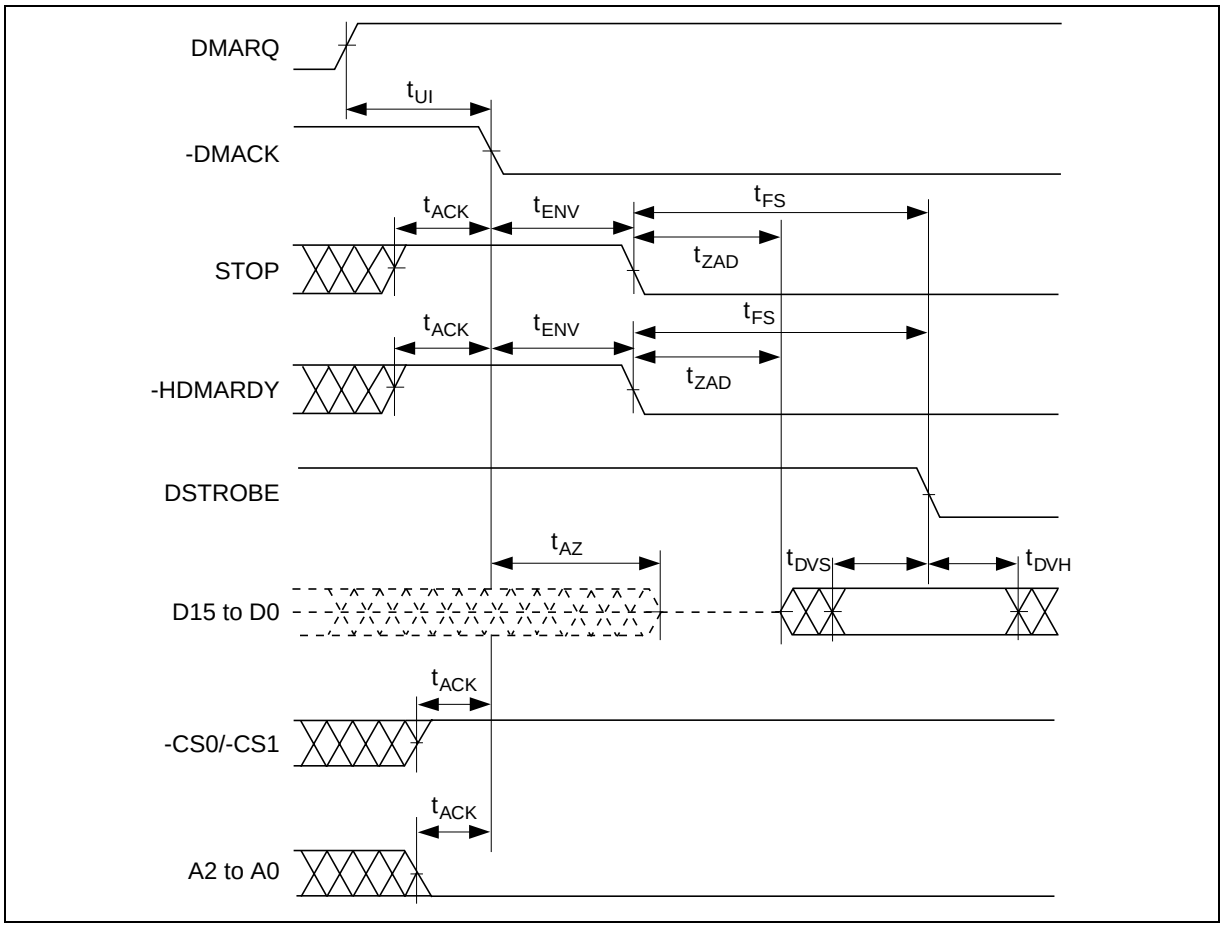
Ultra DMA Mode Access AC Characteristics

		Mode0		Mode1		Mode2		Mode3		Mode4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle time allowing for asymmetry and clock variations	t_{CYC}	112	—	73	—	54	—	39	—	25	—	ns
Two cycle time allowing for clock variations	t_{2CYC}	230	—	154	—	115	—	86	—	57	—	ns
Data setup time at recipient	t_{DS}	15	—	10	—	7	—	7	—	5	—	ns
Data hold time at recipient	t_{DH}	5	—	5	—	5	—	5	—	5	—	ns
Data valid setup at sender	t_{DVS}	70	—	48	—	30	—	20	—	6	—	ns
Data valid hold at sender	t_{DVH}	6	—	6	—	6	—	6	—	6	—	ns
First STROBE time*[2]	t_{FS}	0	230	0	200	0	170	0	130	0	120	ns
Limited interlock time*[3]	t_{LI}	0	150	0	150	0	150	0	100	0	100	ns
Interlock time with minimum	t_{MLI}	20	—	20	—	20	—	20	—	20	—	ns
Unlimited interlock time	t_{UI}	0	—	0	—	0	—	0	—	0	—	ns
Maximum time allowed for output drivers to release	t_{AZ}	—	10	—	10	—	10	—	10	—	10	ns
Minimum delay time required for output	t_{ZAH}	20	—	20	—	20	—	20	—	20	—	ns
Drivers to assert or negate	t_{ZAD}	0	—	0	—	0	—	0	—	0	—	ns
Envelope time	t_{ENV}	20	70	20	70	20	70	20	55	20	55	ns
STROBE–to–DMARDY time	t_{SR}	—	50	—	30	—	20	—	NA*[1]	—	NA*[1]	ns
Ready-to-final STROBE time	t_{RFS}	—	75	—	70	—	60	—	60	—	60	ns
Minimum time to assert STOP or negate DMARQ	t_{RP}	160	—	125	—	100	—	100	—	100	—	ns
Setup and hold times for DMACK	t_{ACK}	20	—	20	—	20	—	20	—	20	—	ns
Time from STROBE edge to negation of DMARQ or assertion of STOP	t_{SS}	50	—	50	—	50	—	50	—	50	—	ns

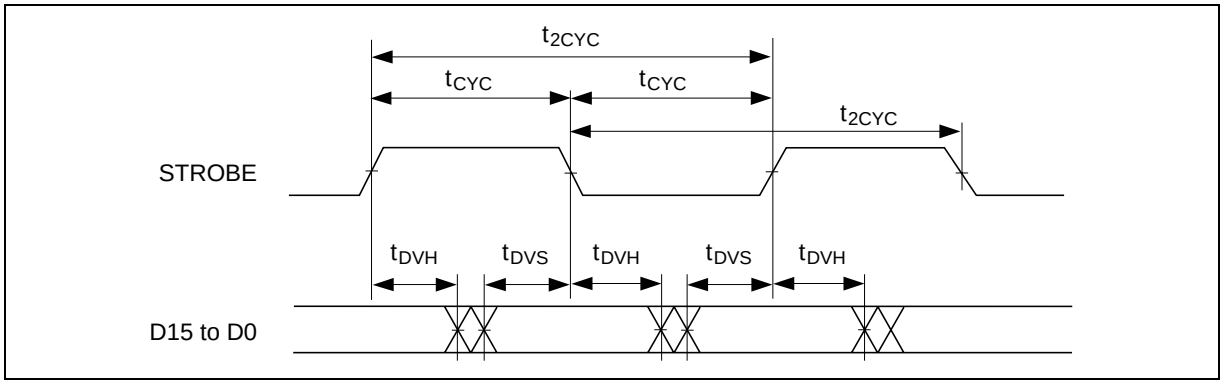
Note: 1. NA = Not Available

2. When Ultra DMA data-in burst termination is occurred before command completion and then the host resumes Ultra DMA data-in burst, the Fast STROBE time may be longer than t_{FS}.
3. When Ultra DMA data-out burst termination is occurred before command completion and then the host resumes Ultra DMA data-out burst, the STOP–to–DMARDY time may be longer than t_{LI}.
4. All timing measurement switching points (low to high and high to low) is taken at 1.5 V.

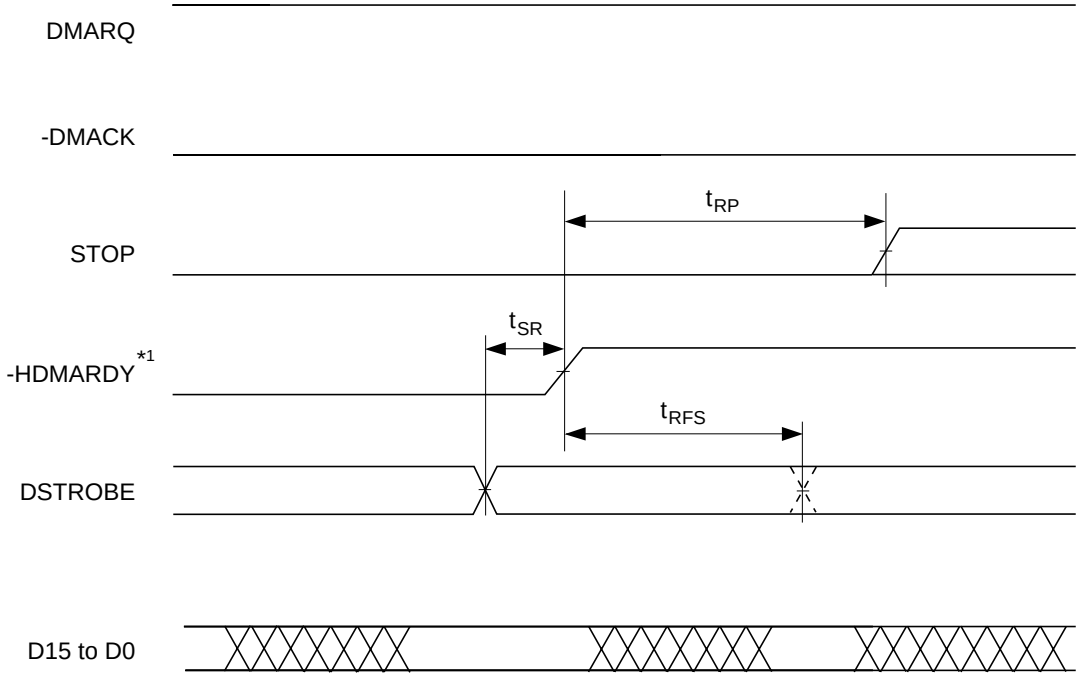
Timing of Initializing an Ultra DMA data-in Burst



Timing of Sustained Ultra DMA data-in Burst

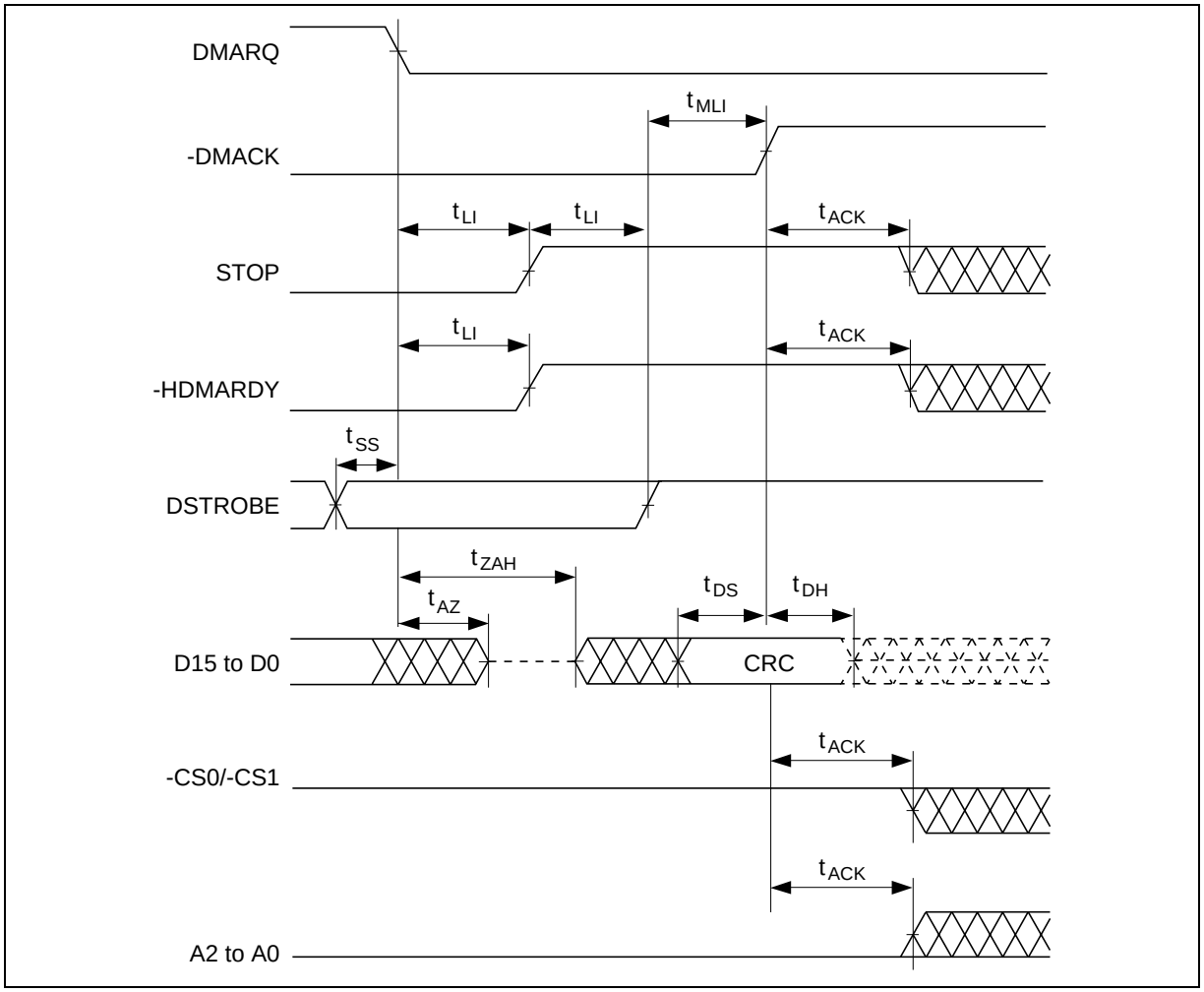


Timing of Host pausing an Ultra DMA data-in Burst

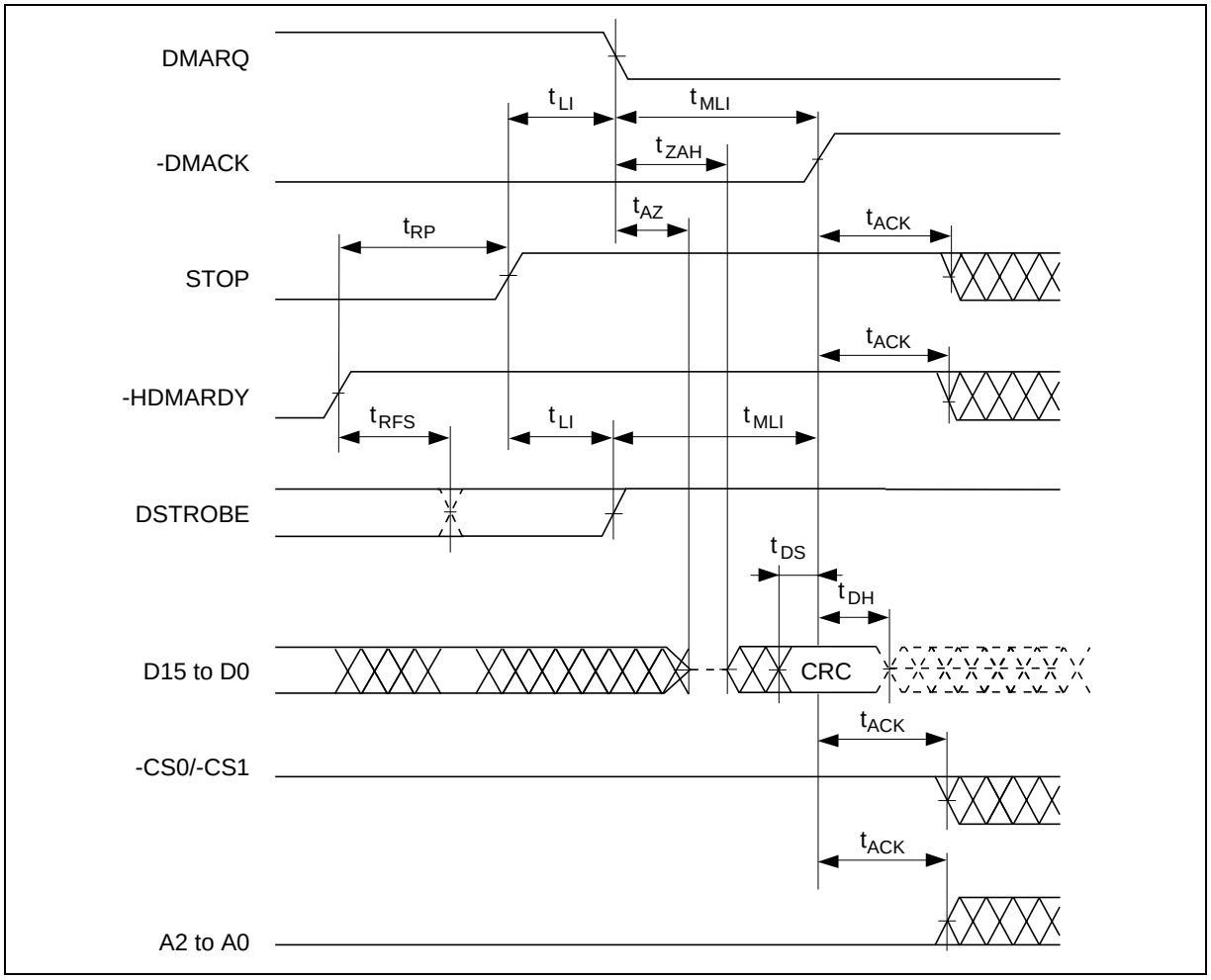


Note: 1. If the t_{SR} timing is not satisfied, the host may receive zero, one, or two more data words from the card.

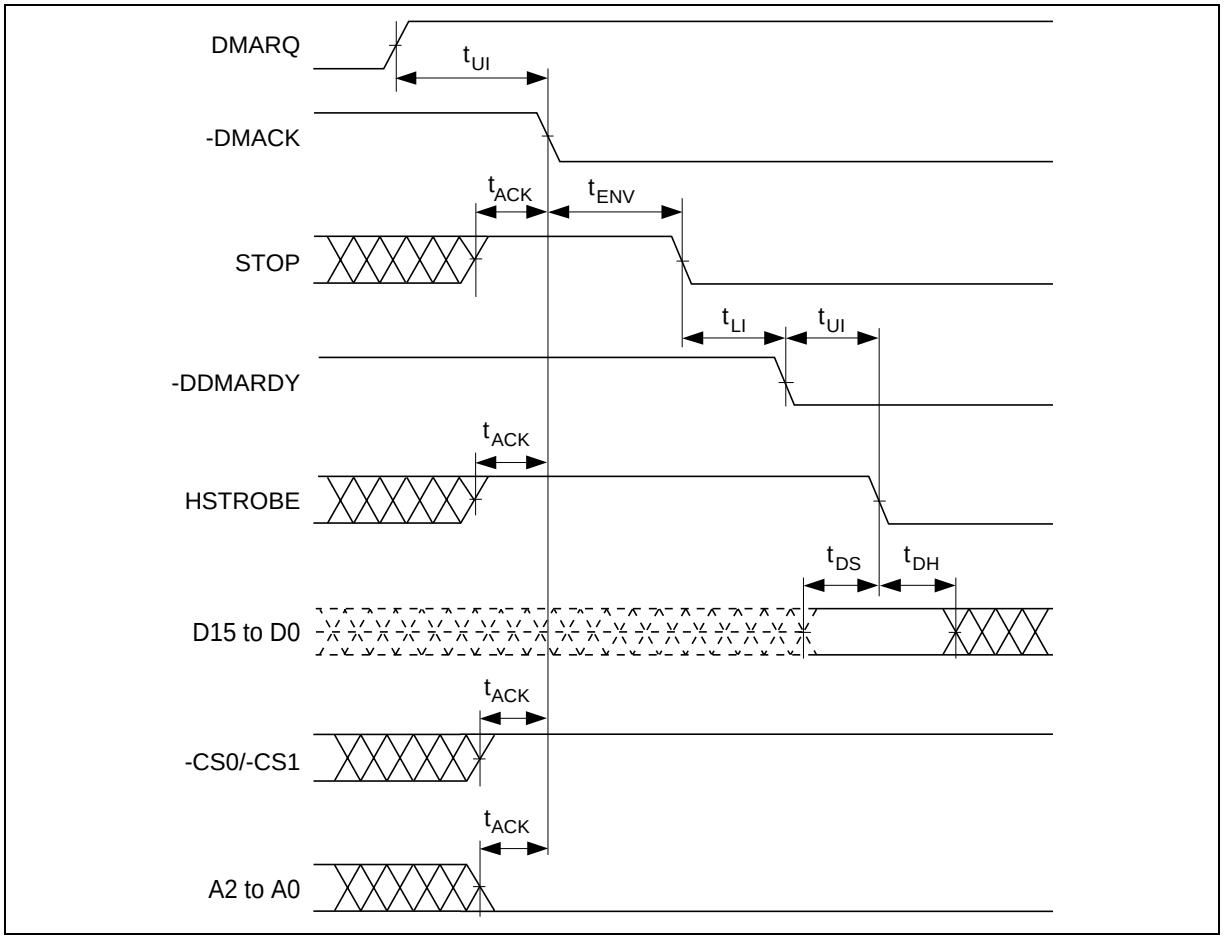
Timing of Card Terminating Ultra DMA data-in Burst



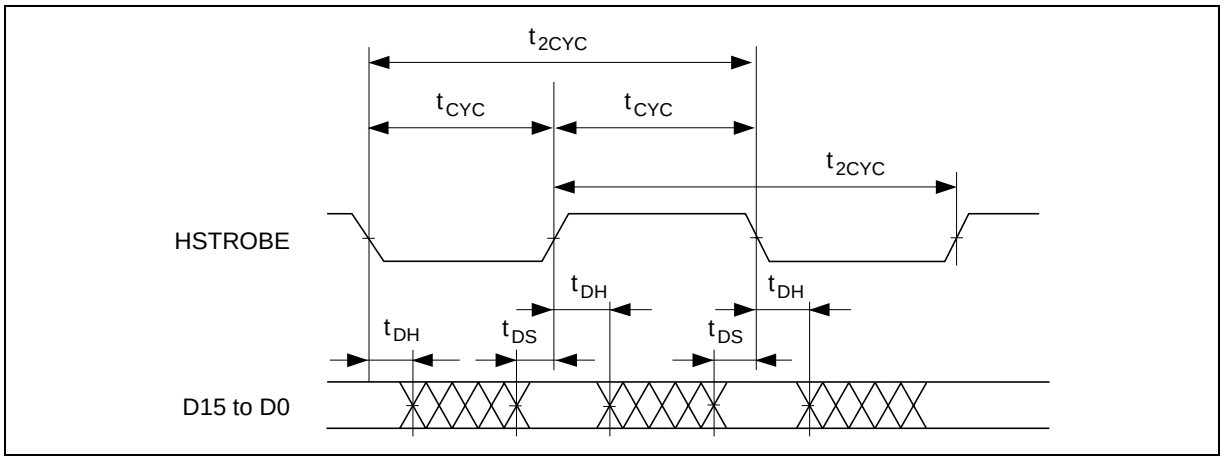
Timing of Host terminating an Ultra DMA data-in Burst



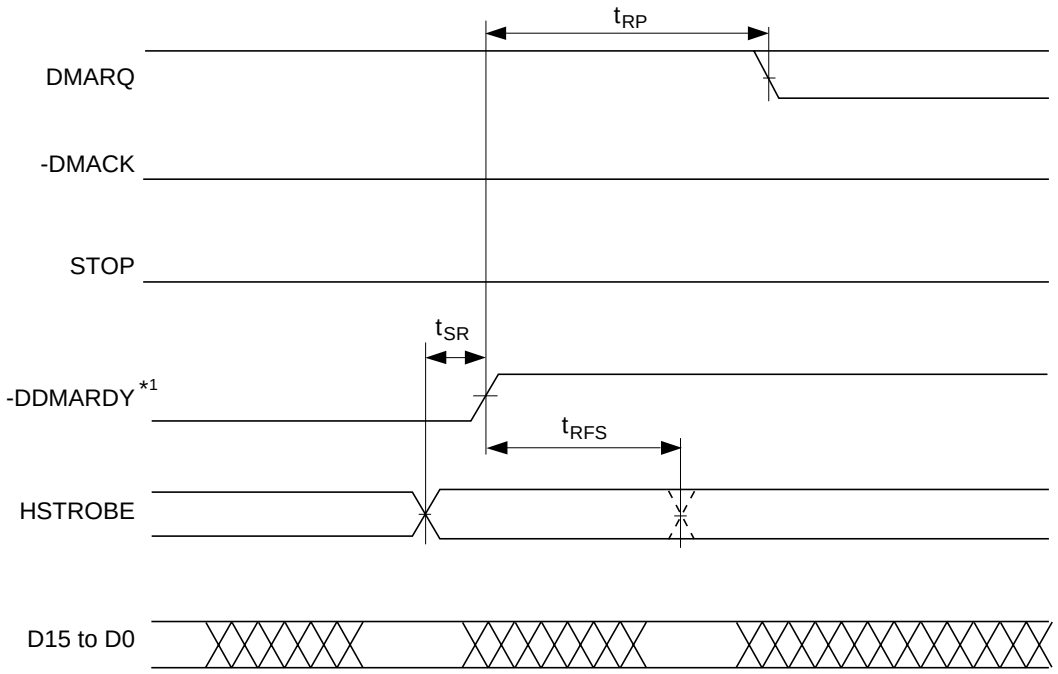
Timing of Initializing an Ultra DMA data-out Burst



Timing of Sustained Ultra DMA data-out Burst

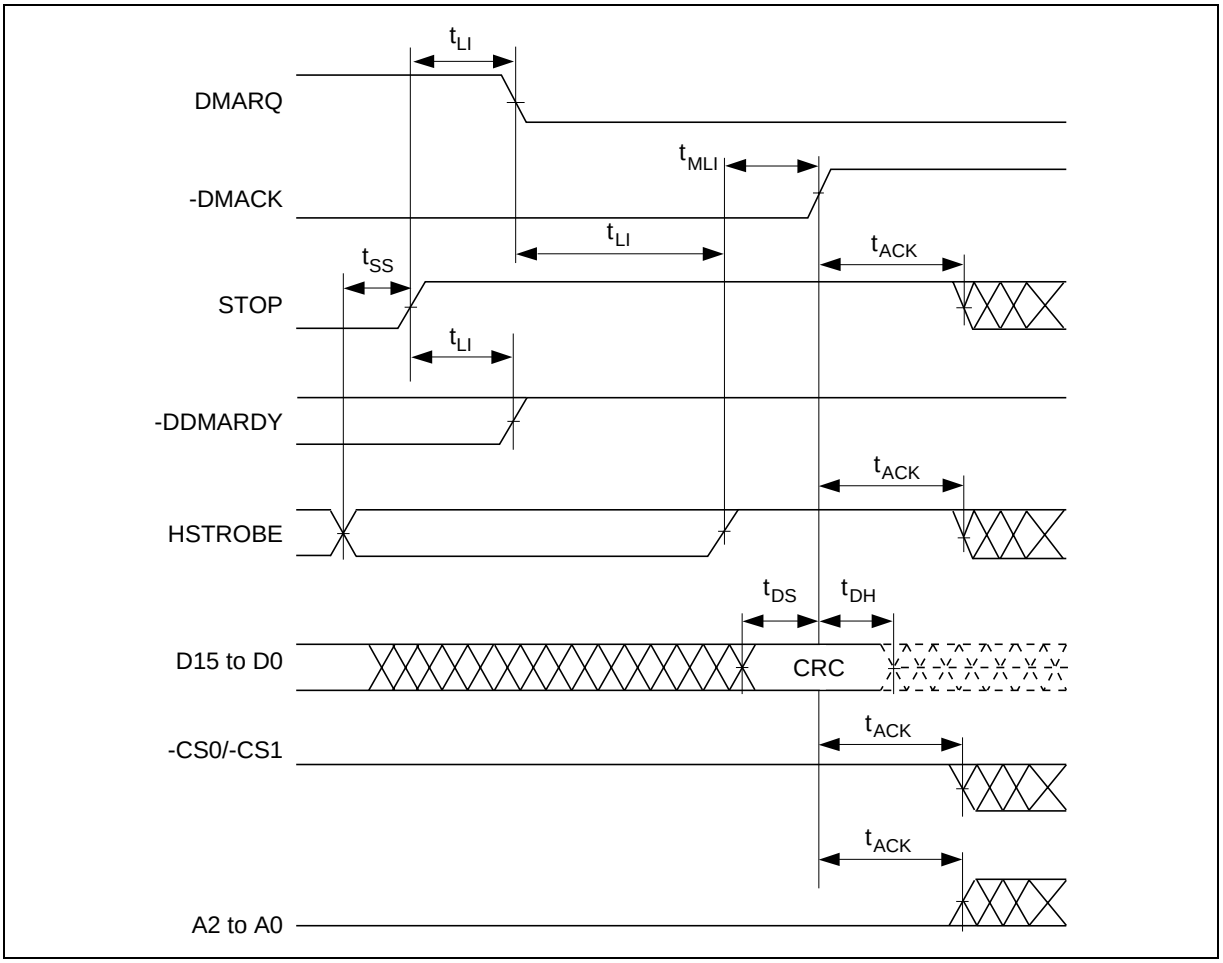


Timing of Card pausing an Ultra DMA data-out Burst

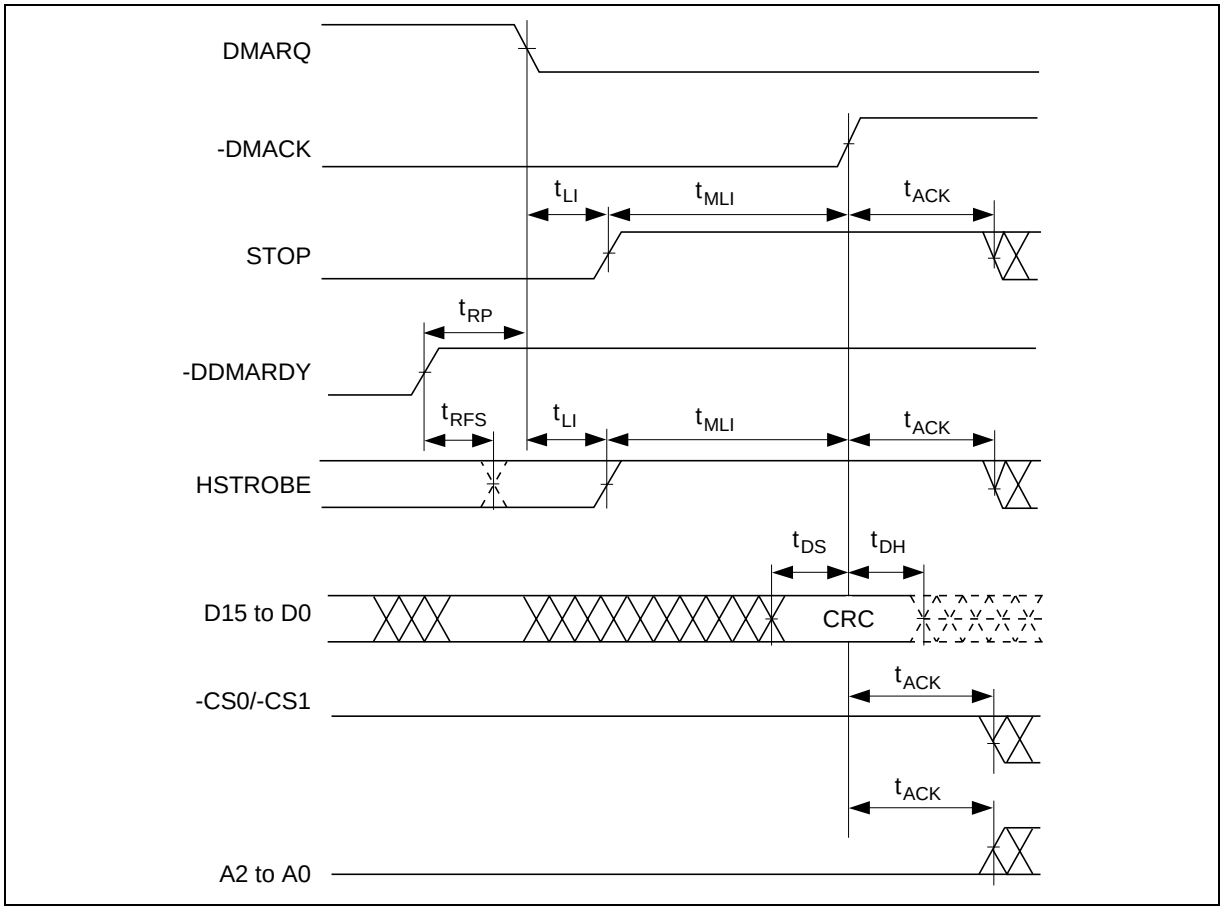


Note: 1. If the t_{SR} timing is not satisfied, the card may receive zero, one, or two more data words from the host.

Timing of Host terminating an Ultra DMA data-out Burst



Timing of Card Terminating Ultra DMA data-out Burst



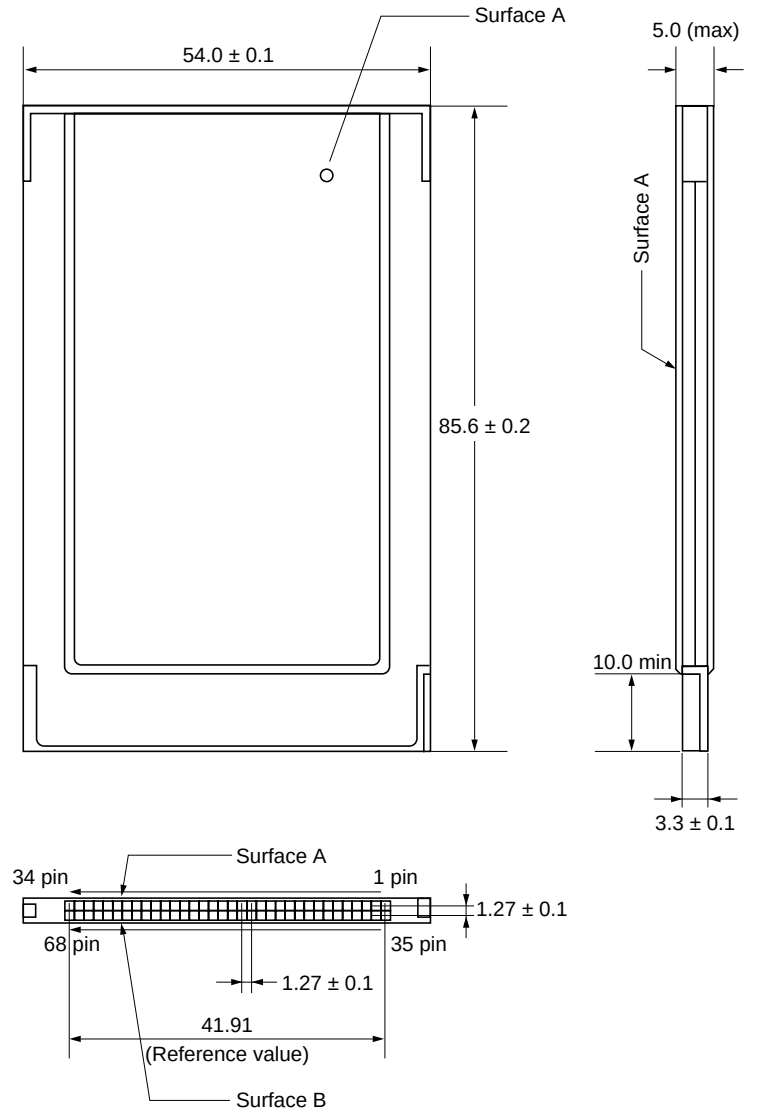
Attention for Card Use

- In the reset or power off, all register informations are cleared.
- After the card hard reset, soft reset, or power on reset, the host cannot access the card during BSY bit in Status register is set.
- The card shall not have a pull-up resistor on D7. The host shall have a 10 kΩ pull-down resistor and not a pull-up resistor on D7 to allow a host to recognize the absence of a card at power-up so that a host shall detect BSY as being cleaned when attempting to read the status register of a card that is not present.
- Power off should not be done during internal operation. When power off occurred during internal operation, there is the possibility that data are lost.
- All card status are cleared automatically when V_{CC} voltage turns below about 2.5V.
- Notice that the card insertion/removal should not be executed while host is kept power supply.
- Before the card insertion V_{CC} can not be supplied to the card.
- We recommend that a circuit to detect the level of power supply voltage be added to the host.
- When a read error occurs, rewriting of the sector is recommended. This may avoid the error.

Physical Outline

As of January, 2003

Unit: mm



Caution for Handling Cards

- Confirm the direction of insertion before inserting the card.
- Be careful not to damage the connector.
- To avoid damaging the card, never insert it in the wrong direction.
- Do not bend the card; do not drop the card or expose the card to mechanical shock of any other kind.
- Never modify or disassemble the card.
- Do not expose the card to static electricity or electrical noise.
- Make regular backups of the data in the card.
- Do not insert the card in PC card slot. It is possible to have a bad influence on the host and the card, so do not insert it.

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RENESAS

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Colophon 0.0