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April 1, 2003

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HM66AEB36102/HM66AEB18202
HM66AEB9402

36-Mbit DDR II SRAM
2-word Burst

ADE-203-1365 (Z)

Preliminary
Rev. 0.0
Dec. 18, 2002

Description

The HM66AEB36102 is a 1,048,576-word by 36-bit, the HM66AEB18202 is a 2,097,152-word by 18-bit, and the HM66AEB9402 is a 4,194,304-word by 9-bit synchronous double data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell. It integrates unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (K and $\overline{K}$) and are latched on the positive edge of K and $\overline{K}$. These products are suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration. These products are packaged in 165-pin plastic FBGA package.

Features

- 1.8 V ± 0.1 V power supply for core (V_{DD})
- 1.4 V to V_{DD} power supply for I/O (V_{DDQ})
- DLL circuitry for wide output data valid window and future frequency scaling
- Pipelined double data rate operation
- Common data input/output bus
- Two-tick burst for low DDR transaction size
- Two input clocks (K and $\overline{K}$) for precise DDR timing at clock rising edges only
- Two output clocks (C and $\overline{C}$) for precise flight time and clock skew matching-clock and data delivered together to receiving device
- Internally self-timed write control
- Clock-stop capability with µs restart
- User programmable impedance output
- Fast clock cycle time: 3.0 ns (333 MHz)/3.3 ns (300 MHz)/4.0 ns (250 MHz)/ 5.0 ns (200 MHz)/6.0 ns (167 MHz)
- Simple control logic for easy depth expansion
- JTAG boundary scan

Ordering Information

Type No.	Organization	Cycle time	Clock frequency	Package
HM66AEB36102BP-30	1-M word	3.0 ns	333 MHz	Plastic FBGA 165-pin
HM66AEB36102BP-33	× 36-bit	3.3 ns	300 MHz	(BP-165A)
HM66AEB36102BP-40		4.0 ns	250 MHz	
HM66AEB36102BP-50		5.0 ns	200 MHz	
HM66AEB36102BP-60		6.0 ns	167 MHz	
HM66AEB18202BP-30	2-M word	3.0 ns	333 MHz	
HM66AEB18202BP-33	× 18-bit	3.3 ns	300 MHz	
HM66AEB18202BP-40		4.0 ns	250 MHz	
HM66AEB18202BP-50		5.0 ns	200 MHz	
HM66AEB18202BP-60		6.0 ns	167 MHz	
HM66AEB9402BP-30	4-M word	3.0 ns	333 MHz	
HM66AEB9402BP-33	× 9-bit	3.3 ns	300 MHz	
HM66AEB9402BP-40		4.0 ns	250 MHz	
HM66AEB9402BP-50		5.0 ns	200 MHz	
HM66AEB9402BP-60		6.0 ns	167 MHz	

Pin Arrangement (HM66AEB36102) 165PIN-BGA

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	V_{SS}	SA	R/$\overline{W}$	$\overline{BW2}$	$\overline{K}$	$\overline{BW1}$	$\overline{LD}$	SA	NC	CQ
B	NC	DQ27	DQ18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	NC	NC	DQ8
C	NC	NC	DQ28	V_{SS}	SA	SA0	SA	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	SA	SA	C	SA	SA	NC	DQ9	DQ0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

(Top view)

Pin Arrangement (HM66AEB18202) 165PIN-BGA

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	V_{SS}	SA	R/$\overline{W}$	$\overline{BW1}$	$\overline{K}$	NC	$\overline{LD}$	SA	SA	CQ
B	NC	DQ9	NC	SA	NC	K	$\overline{BW0}$	SA	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	SA	SA0	SA	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	SA	SA	C	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

(Top view)

Pin Arrangement (HM66AEB9402) 165PIN-BGA

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	V_{SS}	SA	R/$\overline{W}$	NC	$\overline{K}$	NC	$\overline{LD}$	SA	SA	CQ
B	NC	NC	NC	SA	NC	K	$\overline{BW}$	SA	NC	NC	DQ3
C	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	NC	DQ5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ1	NC
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	DQ6	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
N	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ7	SA	SA	C	SA	SA	NC	NC	DQ8
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

(Top view)

Note: Note that 6C is not SA0. The ×9 product does not permit random start address on the least significant address bit. SA0 = 0 at the start of each address.

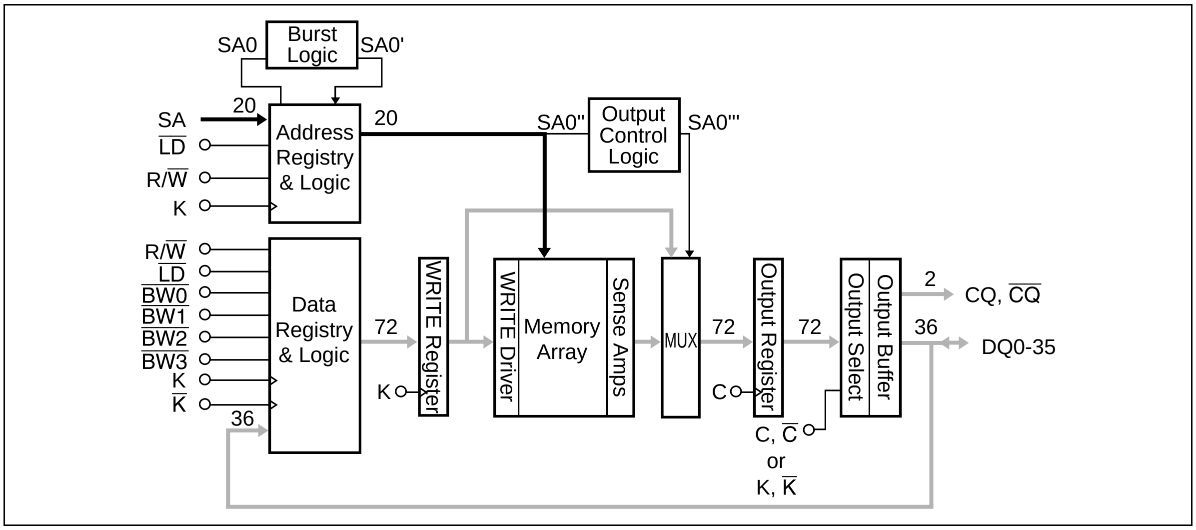
Pin Descriptions

Name	I/O type	Descriptions
SA0 SAn	Input	Synchronous address inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. Ball 2A is reserved for the next higher-order address input on future devices. All transactions operate on a burst-of-two words (one clock period of bus activity). SA0 is used as the lowest address bit for burst READ and burst WRITE operations permitting a random burst start address on ×18 and ×36 devices. These inputs are ignored when device is deselected.
$\overline{LD}$	Input	Synchronous load: This input is brought low when a bus cycle sequence is to be defined. This definition includes address and READ / WRITE direction. All transactions operate on a burst-of-two data (one clock period of bus activity).
R/$\overline{W}$	Input	Synchronous read / write input: When $\overline{LD}$ is low, this input designates the access type (READ when R/$\overline{W}$ is high, WRITE when R/$\overline{W}$ is low) for the loaded address. R/$\overline{W}$ must meet the setup and hold times around the rising edge of K.
$\overline{BW}$ $\overline{BWn}$	Input	Synchronous byte writes: When low, these inputs cause their respective byte to be registered and written during WRITE cycles. These signals must meet setup and hold times around the rising edges of K and $\overline{K}$ for each of the two rising edges comprising the WRITE cycle. See Byte Write Truth Table for signal to data relationship.
K, $\overline{K}$	Input	Input clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of $\overline{K}$. $\overline{K}$ is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges.
C, $\overline{C}$	Input	Output clock: This clock pair provides a user-controlled means of tuning device output data. The rising edge of C is used as the output timing reference for second output data. The rising edge of $\overline{C}$ is used as the output reference for first output data. Ideally, $\overline{C}$ is 180 degrees out of phase with C. C and $\overline{C}$ may be tied high to force the use of K and $\overline{K}$ as the output reference clocks instead of having to provide C and $\overline{C}$ clocks. If tied high, C and $\overline{C}$ must remain high and not to be toggled during device operation.
$\overline{DOFF}$	Input	DLL disable: When low, this input causes the DLL to be bypassed for stable, low-frequency operation.
ZQ	Input	Output impedance matching input: This input is used to tune the device outputs to the system data bus impedance. DQ and CQ output impedance are set to 0.2 × RQ, where RQ is a resistor from this ball to ground. Alternately, this ball can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This ball cannot be connected directly to V_{SS} or left unconnected.
TMS TDI	Input	IEEE1149.1 test inputs: 1.8 V I/O levels. These balls may be left not connected if the JTAG function is not used in the circuit.
TCK	Input	IEEE1149.1 clock input: 1.8 V I/O levels. This ball must be tied to V_{SS} if the JTAG function is not used in the circuit.

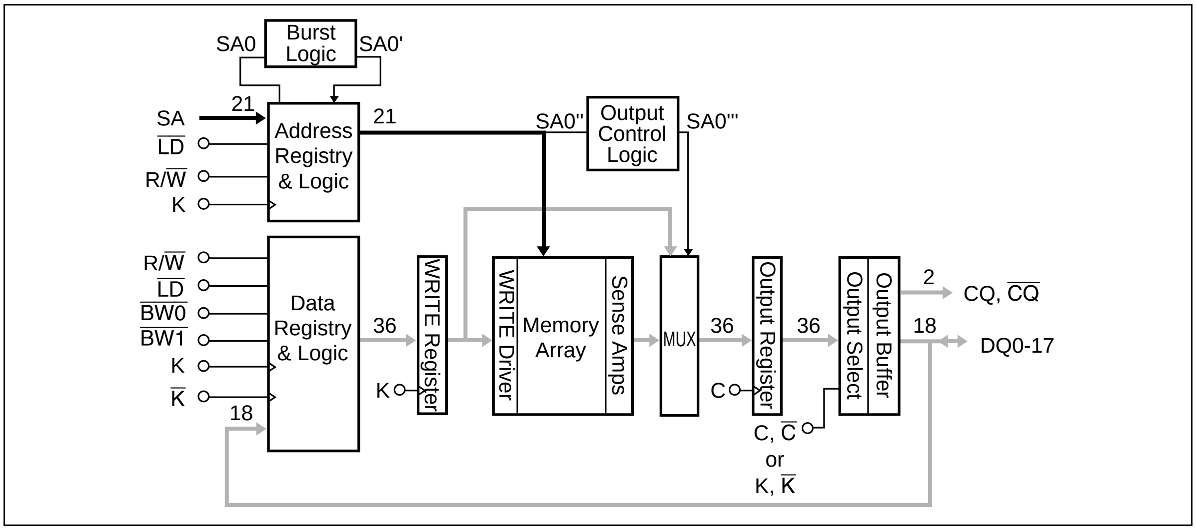
Name	I/O type	Descriptions
DQ0 to DQn	Input/ output	Synchronous data I/Os: Input data must meet setup and hold times around the rising edges of K and $\overline{K}$. Output data is synchronized to the respective C and $\overline{C}$ data clocks, or to the respective K and $\overline{K}$ if C and $\overline{C}$ are tied to high. The ×9 device uses DQ0 to DQ8. Remaining signals are NC. The ×18 device uses DQ0 to DQ17. Remaining signals are NC. The ×36 device uses DQ0 to DQ35. NC signals are read in the JTAG scan chain as the logic level applied to the ball site.
CQ, $\overline{CQ}$	Output	Synchronous echo clock outputs: The edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when DQ tri-states.
TDO	Output	IEEE 1149.1 test output: 1.8 V I/O level.
V_{DD}	Supply	Power supply: 1.8 V nominal. See DC Characteristics and Operating Conditions for range.
V_{DDQ}	Supply	Power supply: Isolated output buffer supply. Nominally 1.5 V. 1.8 V is also permissible. See DC Characteristics and Operating Conditions for range.
V_{SS}	Supply	Power supply: Ground
V_{REF}	—	HSTL input reference voltage: Nominally $V_{DDQ}/2$. Provides a reference voltage for the input buffers.
NC	—	No connect: These signals are internally connected and appear in the JTAG scan chain as the logic level applied to the ball sites. These signals may be connected to ground to improve package heat dissipation.

Note: 1. All power supply and ground balls must be connected for proper operation of the device.

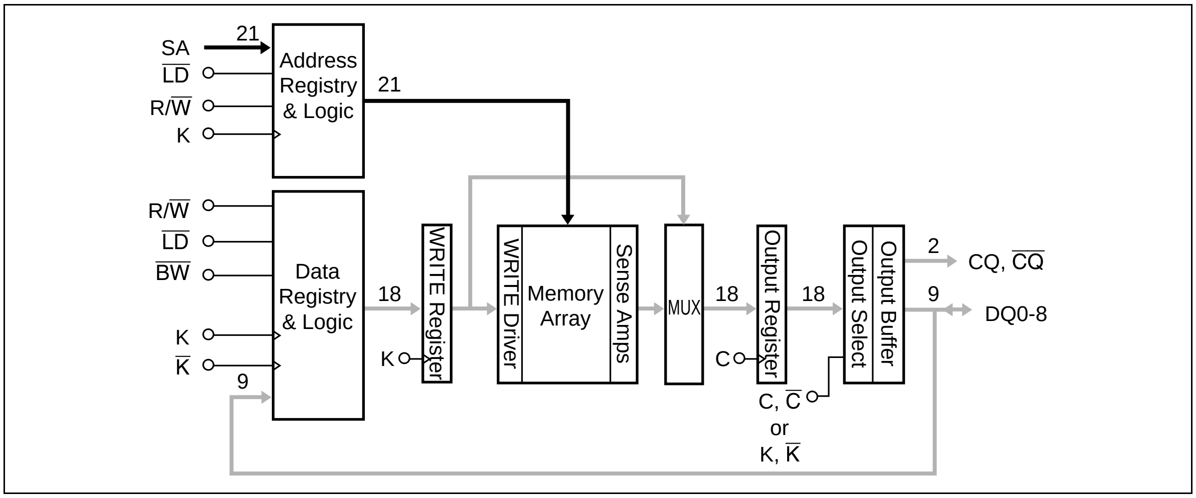
Block Diagram (HM66AEB36102)



Block Diagram (HM66AEB18202)



Block Diagram (HM66AEB9402)



Burst Sequence

Linear Burst Sequence Table

(HM66AEB36102/18202)

	SA0	SA0
External address	0	1
1st internal burst address	1	0

Truth Table

Operation	K	$\overline{LD}$	R/$\overline{W}$	DQ		
WRITE cycle	L→H	L	L	Data in		
Load address, input write data on consecutive K and $\overline{K}$ rising edges				Input data	D_A(A1)	D_A(A2)
				Input clock	K(t+1)↑	$\overline{K}$(t+1)↑
READ cycle	L→H	L	H	Data out		
Load address, read data on consecutive C and $\overline{C}$ rising edges				Output data	Q_A(A1)	Q_A(A2)
				Output clock	$\overline{C}$(t+1)↑	C(t+2)↑
NOP (No operation)	L→H	H	×	High-Z		
STANDBY (Clock stopped)	Stopped	×	×	Previous state		

Notes:
1. H: high level, L: low level, ×: don't care, ↑: rising edge.
2. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered at C and $\overline{C}$ rising edges, except if C and $\overline{C}$ are high, then data outputs are delivered at K and $\overline{K}$ rising edges.
3. All control inputs in the truth table must meet setup/hold times around the rising edges (low to high) of K and are registered at the rising edge of K.
4. This device contains circuitry that will ensure the outputs will be in high-Z during power-up.
5. Refer to state diagram and timing diagrams for clarification.
6. It is recommended that (K) = /($\overline{K}$) = (C) = /($\overline{C}$) when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
7. A1 refers to the address input during a WRITE or READ cycle. A2 refers to the next internal burst address in accordance with the linear burst sequence.

Byte Write Truth Table

(HM66AEB36102)

Operation	K	$\overline{K}$	$\overline{BW0}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$
Write D0 to D35	L→H	—	0	0	0	0
	—	L→H	0	0	0	0
Write D0 to D8	L→H	—	0	1	1	1
	—	L→H	0	1	1	1
Write D9 to D17	L→H	—	1	0	1	1
	—	L→H	1	0	1	1
Write D18 to D26	L→H	—	1	1	0	1
	—	L→H	1	1	0	1
Write D27 to D35	L→H	—	1	1	1	0
	—	L→H	1	1	1	0
Write nothing	L→H	—	1	1	1	1
	—	L→H	1	1	1	1

Notes: 1. H: high level, L: low level, →: rising edge.
2. Assumes a WRITE cycle was initiated. $\overline{BW0}$ to $\overline{BW3}$ can be altered for any portion of the burst WRITE operation provided that the setup and hold requirements are satisfied.

(HM66AEB18202)

Operation	K	$\overline{K}$	$\overline{BW0}$	$\overline{BW1}$
Write D0 to D17	L→H	—	0	0
	—	L→H	0	0
Write D0 to D8	L→H	—	0	1
	—	L→H	0	1
Write D9 to D17	L→H	—	1	0
	—	L→H	1	0
Write nothing	L→H	—	1	1
	—	L→H	1	1

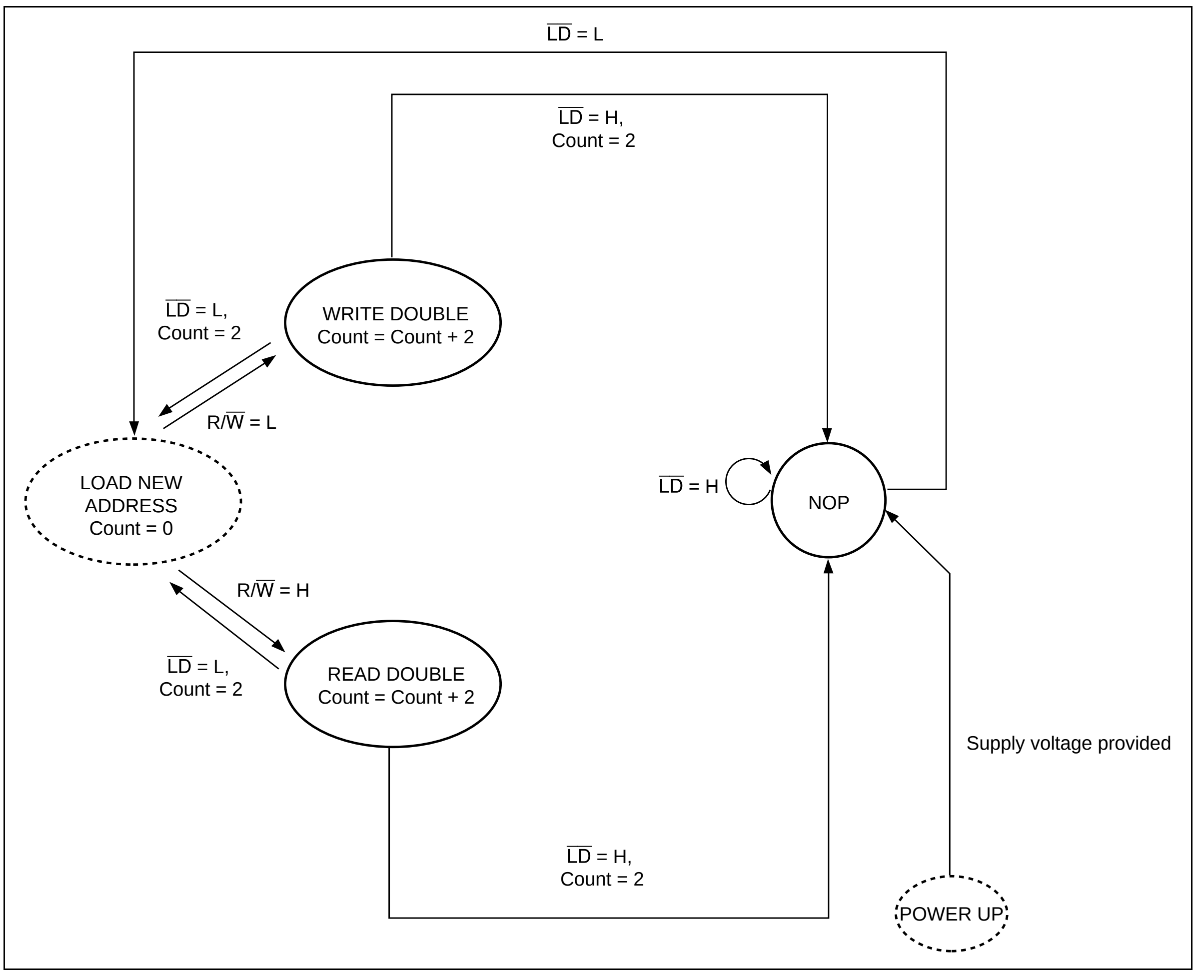
Notes: 1. H: high level, L: low level, →: rising edge.
2. Assumes a WRITE cycle was initiated. $\overline{BW0}$ and $\overline{BW1}$ can be altered for any portion of the burst WRITE operation provided that the setup and hold requirements are satisfied.

(HM66AEB9402)

Operation	K	$\overline{K}$	$\overline{BW}$
Write D0 to D8	L→H	—	0
	—	L→H	0
Write nothing	L→H	—	1
	—	L→H	1

Notes: 1. H: high level, L: low level, →: rising edge.
2. Assumes a WRITE cycle was initiated. $\overline{BW}$ can be altered for any portion of the burst WRITE operation provided that the setup and hold requirements are satisfied.

Bus Cycle State Diagram



Notes: 1. SA0 is internally advanced in accordance with the burst order table. Bus cycle is terminated after burst count = 2.
2. State machine control timing sequence is controlled by K.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Input voltage on any ball	V_{IN}	–0.5 to V_{DD} + 0.5 (2.9 V max.)	V	1, 4
Input/output voltage	$V_{I/O}$	–0.5 to V_{DDQ} + 0.5 (2.9 V max.)	V	1, 4
Core supply voltage	V_{DD}	–0.5 to 2.9	V	1, 4
Output supply voltage	V_{DDQ}	–0.5 to V_{DD}	V	1, 4
Junction temperature	Tj	+125 (max)	°C	
Storage temperature	T_{STG}	–55 to +125	°C	

Notes: 1. All voltage is referenced to V_{SS}.

2. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted the Operation Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
3. These CMOS memory circuits have been designed to meet the DC and AC specifications shown in the tables after thermal equilibrium has been established.
4. The following supply voltage application sequence is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF} then V_{IN}. Remember, according to the Absolute Maximum Ratings table, V_{DDQ} is not to exceed 2.9V, whatever the instantaneous value of V_{DDQ}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power supply voltage -- core	V_{DD}	1.7	1.8	1.9	V	
Power supply voltage -- I/O	V_{DDQ}	1.4	1.5	V_{DD}	V	
Input reference voltage -- I/O	V_{REF}	0.68	0.75	0.95	V	1
Input high voltage	$V_{IH (DC)}$	V_{REF} + 0.1	—	V_{DDQ} + 0.3	V	2, 3
Input low voltage	$V_{IL (DC)}$	–0.3	—	V_{REF} – 0.1	V	2, 3

Notes: 1. Peak to peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.

2. V_{REF} = 0.75 V (typ).
3. Overshoot: $V_{IH (AC)} \le V_{DD}$ + 0.7 V for $t \le t_{KHKH}/2$
Undershoot: $V_{IL (AC)} \ge$ –0.5 V for $t \le t_{KHKH}/2$
Power-up: $V_{IH} \le V_{DDQ}$ + 0.3 V and $V_{DD} \le$ 1.7 V and $V_{DDQ} \le$ 1.4 V for $t \le$ 200 ms
During normal operation, V_{DDQ} must not exceed V_{DD}.
Control input signals may not have pulse widths less than t_{KHKL} (min) or operate at cycle rates less than t_{KHKH} (min).

DC Characteristics (Ta = 0 to +70°C, V_{DD} = 1.8 V ± 0.1 V)

Parameter		Symbol	Typ	HM66AEB36102/HM66AEB18202 HM66AEB9402 -30 Max	-33	-40	-50	-60	Unit	Notes
Operating supply current (READ / WRITE)	(×9 / ×18)	I_{DD}	TBD	525	475	400	330	280	mA	
	(×36)	I_{DD}	TBD	710	640	545	445	380	mA	
Standby supply current (NOP)	(×9 / ×18)	I_{SB1}	TBD	255	235	200	170	150	mA	
	(×36)	I_{SB1}	TBD	265	240	210	180	160	mA	

Notes
1. All inputs (except ZQ, V_{REF}) are held at either V_{IH} or V_{IL}.
2. I_{OUT} = 0 mA. V_{DD} = V_{DD} max, t_{KHKH} = t_{KHKH} min.
3. Typical values are measured at V_{DD} = 1.8 V, V_{DDQ} = 1.5 V, Ta = +25°C, and t_{KHKH} = 6 ns.
4. Operating supply currents are measured at 100% bus utilization.
5. NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.

Parameter	Symbol	Min	Max	Unit	Test conditions	Notes
Input leakage current	I_{LI}	–2	2	µA		8
Output leakage current	I_{LO}	–2	2	µA		9
Output high voltage	V_{OH} (Low)	V_{DDQ} – 0.2	V_{DDQ}	V	$\|I_{OH}\| \leq 0.1$ mA	3, 4
	V_{OH}	V_{DDQ}/2 – 0.08	V_{DDQ}/2 + 0.08	V	Notes1	3, 4
Output low voltage	V_{OL} (Low)	V_{SS}	0.2	V	$I_{OL} \leq 0.1$ mA	3, 4
	V_{OL}	V_{DDQ}/2 – 0.08	V_{DDQ}/2 + 0.08	V	Notes2	3, 4
Output “High” current	I_{OH}	(V_{DDQ}/2)/(RQ/5 + 10%)	(V_{DDQ}/2)/(RQ/5 – 10%)	mA		5, 7
Output “Low” current	I_{OL}	(V_{DDQ}/2)/(RQ/5 – 10%)	(V_{DDQ}/2)/(RQ/5 + 10%)	mA		6, 7

Notes: 1. Outputs are impedance-controlled. $|I_{OH}| = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
2. Outputs are impedance-controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
3. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
4. HSTL outputs meet JEDEC HSTL Class I and Class II standards.
5. Measured at $V_{OH} = V_{DDQ}/2$
6. Measured at $V_{OL} = V_{DDQ}/2$
7. Output buffer impedance can be programmed by terminating the ZQ ball to V_{SS} through a precision resistor (RQ). The value of RQ is five times the output impedance desired. The allowable range of RQ to guarantee impedance matching with a tolerance of 10% is 250 Ω typical. The total external capacitance of ZQ ball must be less than 7.5 pF.
8. $0 \le V_{IN} \le V_{DDQ}$ for all input balls (except V_{REF}, ZQ, TCK, TMS, TDI ball)
9. $0 \le V_{OUT} \le V_{DDQ}$ (except TDO ball), output disabled.
10. V_{DDQ} = 1.5 V ± 0.1 V

Capacitance (Ta = +25°C, f = 1.0 MHz, V_{DD} = 1.8 V)

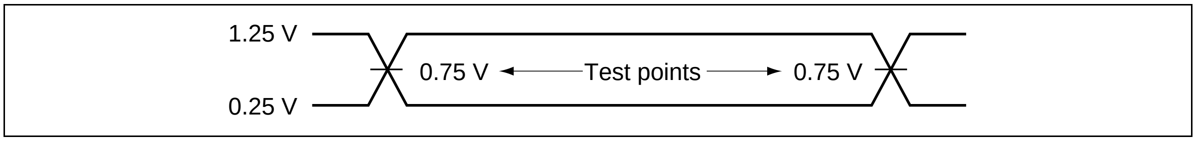
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	C_{IN}	—	4	5	pF	V_{IN} = 0 V
Clock input capacitance	C_{CLK}	—	5	6	pF	V_{CLK} = 0 V
Input/output capacitance (DQ)	$C_{I/O}$	—	6	7	pF	$V_{I/O}$ = 0 V

Notes: 1. These parameters are sampled and not 100% tested.
2. Parameters tested with RQ = 250 Ω and V_{DDQ} = 1.5 V.

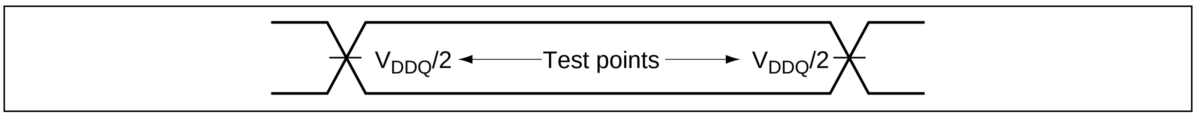
AC Characteristics (Ta = 0 to +70°C, V_{DD} = 1.8 V ± 0.1 V)

Test Conditions

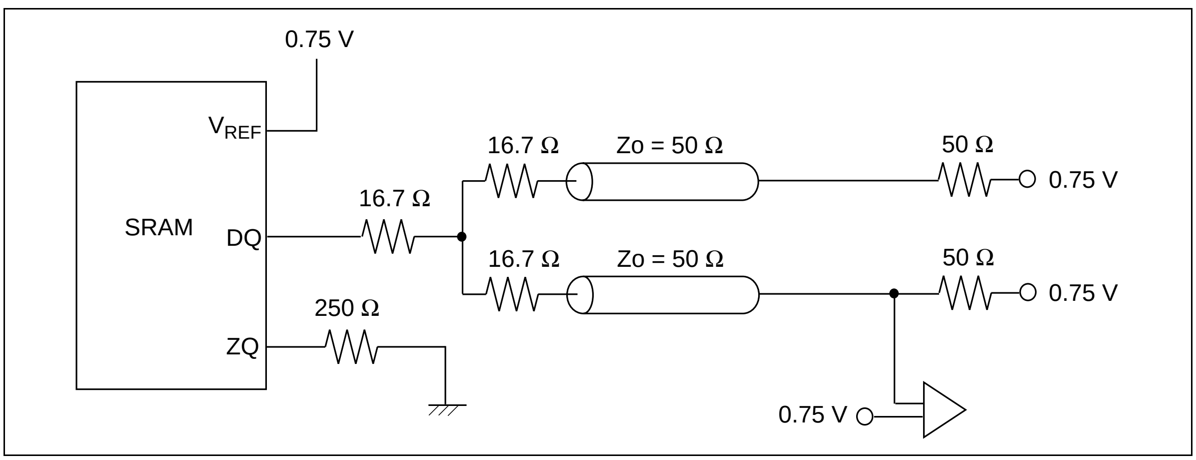
Input waveform (Rise/fall time ≤ 0.3 ns)



Output waveform



Output load condition



Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	$V_{IH (AC)}$	V_{REF} + 0.2	—	—	V	1, 2, 3
Input low voltage	$V_{IL (AC)}$	—	—	V_{REF} – 0.2	V	1, 2, 3

Notes: 1. All voltages referenced to V_{SS} (GND).

2. Overshoot: $V_{IH (AC)} \leq V_{DD}$ + 0.7 V for $t \leq t_{KHKH}/2$
Undershoot: $V_{IL (AC)} \geq$ –0.5 V for $t \leq t_{KHKH}/2$
Power-up: $V_{IH} \leq V_{DDQ}$ + 0.3 V and $V_{DD} \leq$ 1.7 V and $V_{DDQ} \leq$ 1.4 V for $t \leq$ 200 ms
During normal operation, V_{DDQ} must not exceed V_{DD}. Control input signals may not have pulse widths less than t_{KHKL} (min) or operate at cycle rates less than t_{KHKH} (min).

3. To maintain a valid level, the transitioning edge of the input must:
   a. Sustain a constant slew rate from the current AC level through the target AC level, $V_{IL (AC)}$ or $V_{IH (AC)}$.
   b. Reach at least the target AC level.
   c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL (DC)}$ or $V_{IH (DC)}$.

		HM66AEB36102/HM66AEB18202 HM66AEB9402											
		-30		-33		-40		-50		-60			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Average clock cycle time (K, $\overline{K}$, C, $\overline{C}$)	t_{KHKH}	3.00	3.47	3.30	4.20	4.00	5.25	5.00	6.30	6.00	7.88	ns	
Clock phase jitter (K, $\overline{K}$, C, $\overline{C}$)	t_{KC} var	—	0.20	—	0.20	—	0.20	—	0.20	—	0.20	ns	3
Clock high time (K, $\overline{K}$, C, $\overline{C}$)	t_{KHKL}	1.20	—	1.32	—	1.60	—	2.00	—	2.40	—	ns	
Clock low time (K, $\overline{K}$, C, $\overline{C}$)	t_{KLKH}	1.20	—	1.32	—	1.60	—	2.00	—	2.40	—	ns	
Clock to $\overline{\text{clock}}$ (K to $\overline{K}$, C to $\overline{C}$)	$t_{KH/KH}$	1.35	—	1.49	—	1.80	—	2.20	—	2.70	—	ns	
$\overline{\text{Clock}}$ to clock ($\overline{K}$ to K, $\overline{C}$ to C)	$t_{/KHKH}$	1.35	—	1.49	—	1.80	—	2.20	—	2.70	—	ns	
Clock to data clock (K to C, $\overline{K}$ to $\overline{C}$)	t_{KHCH}	0	1.30	0	1.45	0	1.80	0	2.30	0	2.80	ns	
DLL lock time (K, C)	t_{KC} lock	1,024	—	1,024	—	1,024	—	1,024	—	1,024	—	Cycle	2
K static to DLL reset	t_{KC} reset	30	—	30	—	30	—	30	—	30	—	ns	
C, $\overline{C}$ high to output valid	t_{CHQV}	—	0.45	—	0.45	—	0.45	—	0.45	—	0.50	ns	
C, $\overline{C}$ high to output hold	t_{CHQX}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	–0.50	—	ns	
C, $\overline{C}$ high to echo clock valid	t_{CHCQV}	—	0.45	—	0.45	—	0.45	—	0.45	—	0.50	ns	
C, $\overline{C}$ high to echo clock hold	t_{CHCQX}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	–0.50	—	ns	
CQ, $\overline{CQ}$ high to output valid	t_{CQHQV}	—	0.25	—	0.27	—	0.30	—	0.35	—	0.40	ns	4
CQ, $\overline{CQ}$ high to output hold	t_{CQHQX}	–0.25	—	–0.27	—	–0.30	—	–0.35	—	–0.40	—	ns	4
C high to output high-Z	t_{CHQZ}	—	0.45	—	0.45	—	0.45	—	0.45	—	0.50	ns	5
C high to output low-Z	t_{CHQX1}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	–0.50	—	ns	5

		HM66AEB36102/HM66AEB18202 HM66AEB9402											
		-30		-33		-40		-50		-60			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Address valid to K rising edge	t_{AVKH}	0.40	—	0.40	—	0.50	—	0.60	—	0.70	—	ns	1
Control inputs valid to K rising edge	t_{IVKH}	0.40	—	0.40	—	0.50	—	0.60	—	0.70	—	ns	1
Data-in valid to K, $\overline{K}$ rising edge	t_{DVKH}	0.28	—	0.30	—	0.35	—	0.40	—	0.50	—	ns	1
K rising edge to address hold	t_{KHAX}	0.40	—	0.40	—	0.50	—	0.60	—	0.70	—	ns	1
K rising edge to control inputs hold	t_{KHIX}	0.40	—	0.40	—	0.50	—	0.60	—	0.70	—	ns	1
K, $\overline{K}$ rising edge to data-in hold	t_{KHDX}	0.28	—	0.30	—	0.35	—	0.40	—	0.50	—	ns	1

Notes: 1. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.

2. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.
It is recommended that the device is kept inactive during these cycles.

3. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.

4. Echo clock is very tightly controlled to data valid / data hold. By design, there is a ±0.1 ns variation from echo clock to data. The datasheet parameters reflect tester guardbands and test setup variations.

5. Transitions are measured ±100 mV from steady-state voltage.

6. At any given voltage and temperature t_{CHQZ} is less than t_{CHQX1} and t_{CHQZ} less than t_{CHQV}.

Remarks: 1. This parameter is sampled.

2. Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.

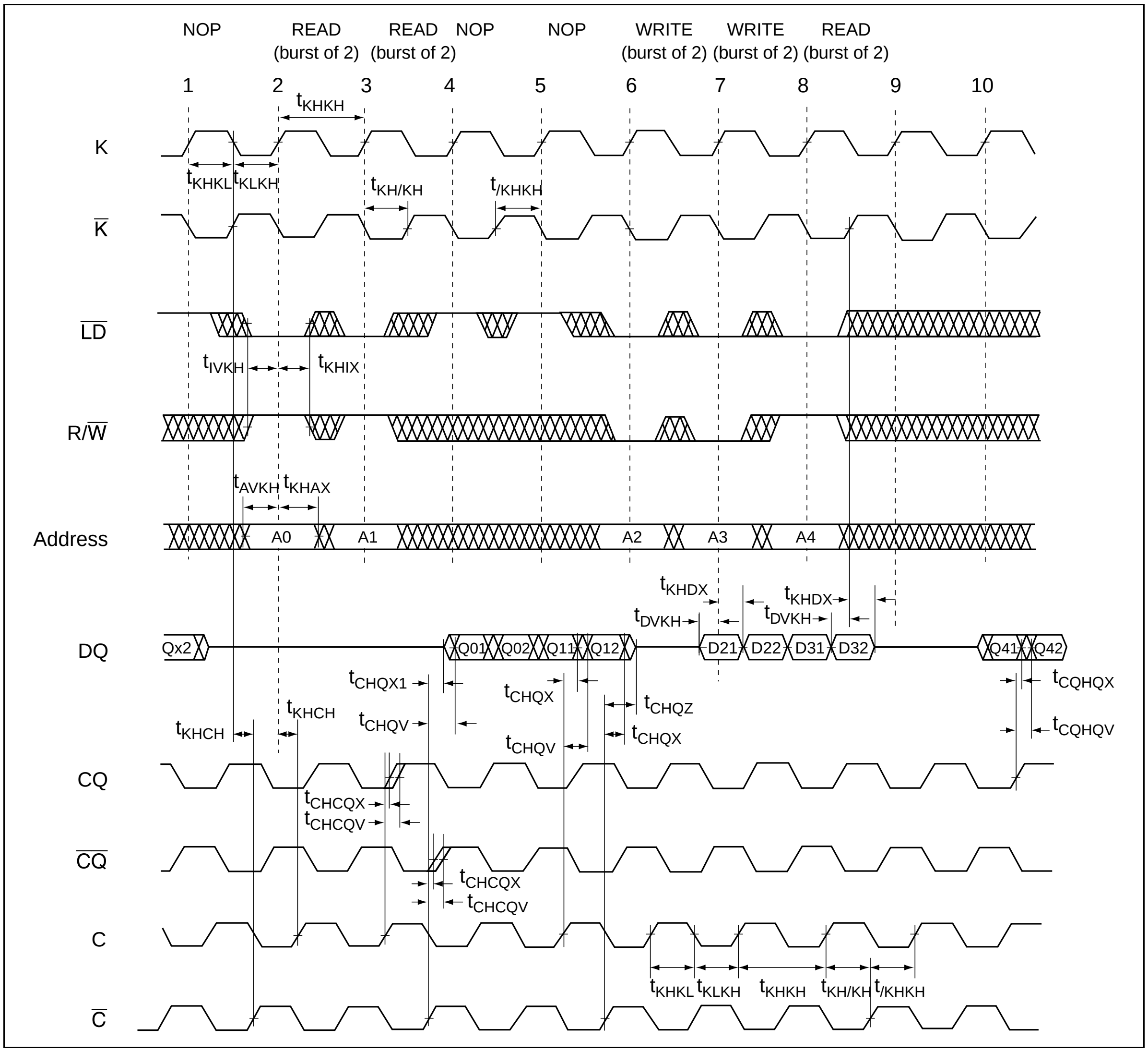
3. Control input signals may not be operated with pulse widths less than t_{KHKL} (min).

4. If C, $\overline{C}$ are tied high, K, $\overline{K}$ become the references for C, $\overline{C}$ timing parameters.

5. V_{DDQ} is +1.5 V DC.

Timing Waveforms

Read and Write Timing



Notes: 1. Q01 refers to output from address A0. Q02 refers to output from the next internal burst address following A0, etc.

2. Outputs are disable (high-Z) one clock cycle after a NOP.

3. In this example, if address A4 = A3, then data Q41 = D31, Q42 = D32. Write data is forwarded immediately as read results.

4. The second NOP cycle is not necessary for correct device operation; however, at high clock frequencies it may be required to prevent bus contention.

JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs.
TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1k resistor.
TDO should be left unconnected.

Test Access Port (TAP) Pins

Symbol I/O	Pin assignments	Description
TCK	2R	Test clock input. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	10R	Test mode select. This is the command input for the TAP controller state machine.
TDI	11R	Test data input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	1R	Test data output. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note: The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held high for five rising edges of TCK. The TAP controller state is also reset on SRAM POWER-UP.

TAP DC Operating Characteristics (Ta = 0 to +70°C, V_{DD} = 1.8 V ± 0.1 V)

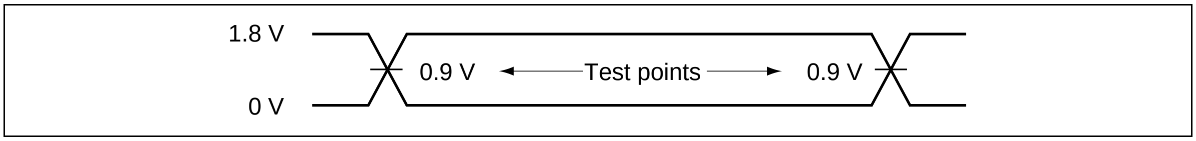
Parameter	Symbol	Min	Max	Unit	Conditions
Input high voltage	V_{IH}	1.3	V_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	+0.5	V	
Input leakage current	I_{LI}	–5.0	+5.0	µA	0 V ≤ V_{IN} ≤ V_{DD}
Output leakage current	I_{LO}	–5.0	+5.0	µA	0 V ≤ V_{IN} ≤ V_{DD}, output disabled
Output low voltage	V_{OL1}	—	0.2	V	I_{OLC} = 100 µA
	V_{OL2}	—	0.4	V	I_{OLT} = 2 mA
Output high voltage	V_{OH1}	1.6	—	V	$\|I_{OHC}\|$ = 100 µA
	V_{OH2}	1.4	—	V	$\|I_{OHT}\|$ = 2 mA

Notes: 1. All voltages referenced to V_{SS} (GND).
2. Power-up: V_{IH} ≤ V_{DDQ} + 0.3 V and V_{DD} ≤ +1.7 V and V_{DDQ} ≤ +1.4 V for t ≤ 200 ms
3. In “EXTEST” mode and “SAMPLE” mode, V_{DDQ} is nominally 1.5 V.

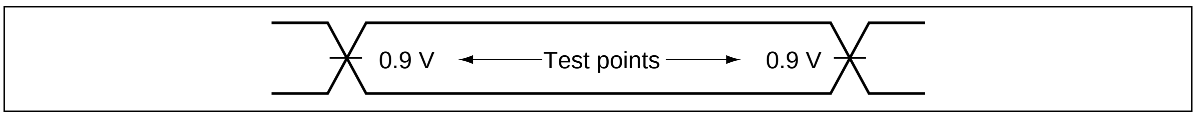
TAP AC Test Condition

- Temperature — 0°C ≤ Ta ≤ +70°C
- Input timing measurement reference levels — 0.9 V
- Input pulse levels — 0 V to 1.8 V
- Input rise/fall time — ≤ 1.0 ns
- Output timing measurement reference levels — 0.9 V
- Test load termination supply voltage (V_{TT}) — 0.9 V
- Output load — See figures

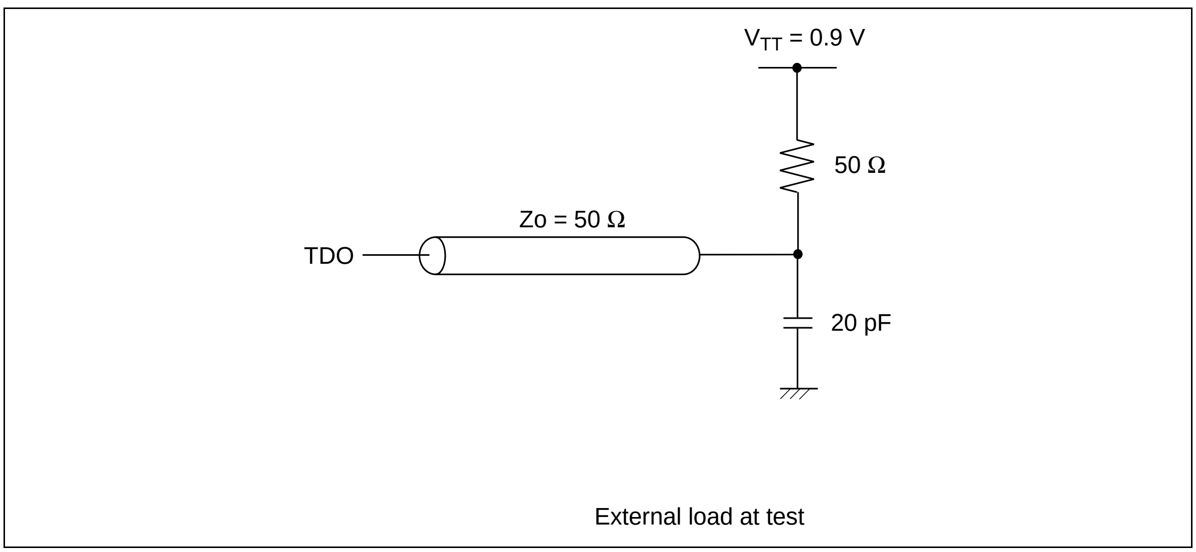
Input waveform



Output waveform



Output load

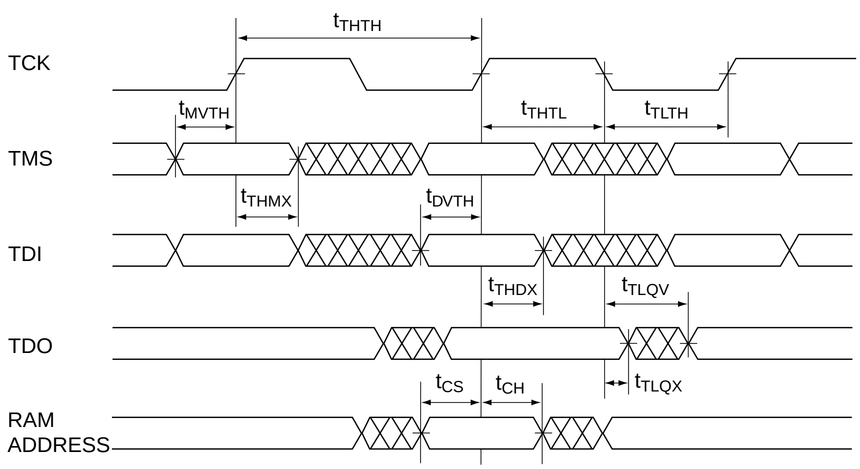


TAP AC Operating Characteristics (Ta = 0 to +70°C, V_{DD} = 1.8 V ± 0.1 V)

Parameter	Symbol	Min	Max	Unit	Note
Test clock cycle time	t_{THTH}	100	—	ns	
Test clock high pulse width	t_{THTL}	40	—	ns	
Test clock low pulse width	t_{TLTH}	40	—	ns	
Test mode select setup	t_{MVTH}	10	—	ns	
Test mode select hold	t_{THMX}	10	—	ns	
Capture setup	t_{CS}	10	—	ns	1
Capture hold	t_{CH}	10	—	ns	1
TDI valid to TCK high	t_{DVTH}	10	—	ns	
TCK high to TDI invalid	t_{THDX}	10	—	ns	
TCK low to TDO unknown	t_{TLQX}	0	—	ns	
TCK low to TDO valid	t_{TLQV}	—	20	ns	

Note: 1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

TAP Controller Timing Diagram



Test Access Port Registers

Register name	Length	Symbol
Instruction register	3 bits	IR [2:0]
Bypass register	1 bit	BP
ID register	32 bits	ID [31:0]
Boundary scan register	109 bits	BS [109:1]

TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Description	Notes
0	0	0	EXTEST	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary scan register cells at output balls are used to apply test vectors, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the Update-IR state of EXTEST, the output drive is turned on and the PRELOAD data is driven onto the output balls.	1, 2
0	0	1	IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO balls in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.	
0	1	0	SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z, except CQ, $\overline{CQ}$ ball) and the boundary register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.	
0	1	1	RESERVED	These instructions are not implemented but are reserved for future use. Do not use these instructions.	
1	0	0	SAMPLE (-PRELOAD)	When the SAMPLE instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to SAMPLE metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO balls.	
1	0	1	RESERVED		
1	1	0	RESERVED		
1	1	1	BYPASS	The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.	

Notes: 1. Data in output register is not guaranteed if EXTEST instruction is loaded.

2. After performing EXTEST, power-up conditions are required in order to return part to normal operation.

ID Register

Part	Revision number (31:29)	Type number (28:12)	Vendor JEDEC code (11:1)	Start bit (0)
HM66AEB36102	000	00010011010000000	00000000111	1
HM66AEB18202	000	00010010010000000	00000000111	1
HM66AEB9402	000	00010000010000000	00000000111	1

Boundary Scan Order

Bit #	Ball ID	Signal names ×9	×18	×36
1	6R	$\overline{C}$	$\overline{C}$	$\overline{C}$
2	6P	C	C	C
3	6N	SA	SA	SA
4	7P	SA	SA	SA
5	7N	SA	SA	SA
6	7R	SA	SA	SA
7	8R	SA	SA	SA
8	8P	SA	SA	SA
9	9R	SA	SA	SA
10	11P	DQ8	DQ0	DQ0
11	10P	NC	NC	DQ9
12	10N	NC	NC	NC
13	9P	NC	NC	NC
14	10M	NC	DQ1	DQ11
15	11N	NC	NC	DQ10
16	9M	NC	NC	NC
17	9N	NC	NC	NC
18	11L	DQ0	DQ2	DQ2
19	11M	NC	NC	DQ1
20	9L	NC	NC	NC
21	10L	NC	NC	NC
22	11K	NC	DQ3	DQ3
23	10K	NC	NC	DQ12
24	9J	NC	NC	NC
25	9K	NC	NC	NC
26	10J	DQ1	DQ4	DQ13
27	11J	NC	NC	DQ4
28	11H	ZQ	ZQ	ZQ
29	10G	NC	NC	NC
30	9G	NC	NC	NC
31	11F	NC	DQ5	DQ5
32	11G	NC	NC	DQ14
33	9F	NC	NC	NC
34	10F	NC	NC	NC
35	11E	DQ2	DQ6	DQ6

Bit #	Ball ID	Signal names ×9	×18	×36
36	10E	NC	NC	DQ15
37	10D	NC	NC	NC
38	9E	NC	NC	NC
39	10C	NC	DQ7	DQ17
40	11D	NC	NC	DQ16
41	9C	NC	NC	NC
42	9D	NC	NC	NC
43	11B	DQ3	DQ8	DQ8
44	11C	NC	NC	DQ7
45	9B	NC	NC	NC
46	10B	NC	NC	NC
47	11A	CQ	CQ	CQ
48	10A	SA	SA	NC
49	9A	SA	SA	SA
50	8B	SA	SA	SA
51	7C	SA	SA	SA
52	6C	SA	SA0	SA0
53	8A	$\overline{LD}$	$\overline{LD}$	$\overline{LD}$
54	7A	NC	NC	$\overline{BW1}$
55	7B	$\overline{BW}$	$\overline{BW0}$	$\overline{BW0}$
56	6B	K	K	K
57	6A	$\overline{K}$	$\overline{K}$	$\overline{K}$
58	5B	NC	NC	$\overline{BW3}$
59	5A	NC	$\overline{BW1}$	$\overline{BW2}$
60	4A	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$
61	5C	SA	SA	SA
62	4B	SA	SA	SA
63	3A	SA	SA	SA
64	2A	V_{SS}	V_{SS}	V_{SS}
65	1A	$\overline{CQ}$	$\overline{CQ}$	$\overline{CQ}$
66	2B	NC	DQ9	DQ27
67	3B	NC	NC	DQ18
68	1C	NC	NC	NC
69	1B	NC	NC	NC
70	3D	NC	DQ10	DQ19

Bit #	Ball ID	Signal names ×9	×18	×36
71	3C	NC	NC	DQ28
72	1D	NC	NC	NC
73	2C	NC	NC	NC
74	3E	DQ4	DQ11	DQ20
75	2D	NC	NC	DQ29
76	2E	NC	NC	NC
77	1E	NC	NC	NC
78	2F	NC	DQ12	DQ30
79	3F	NC	NC	DQ21
80	1G	NC	NC	NC
81	1F	NC	NC	NC
82	3G	DQ5	DQ13	DQ22
83	2G	NC	NC	DQ31
84	1H	$\overline{\text{DOFF}}$	$\overline{\text{DOFF}}$	$\overline{\text{DOFF}}$
85	1J	NC	NC	NC
86	2J	NC	NC	NC
87	3K	NC	DQ14	DQ23
88	3J	NC	NC	DQ32
89	2K	NC	NC	NC
90	1K	NC	NC	NC

Bit #	Ball ID	Signal names ×9	×18	×36
91	2L	DQ6	DQ15	DQ33
92	3L	NC	NC	DQ24
93	1M	NC	NC	NC
94	1L	NC	NC	NC
95	3N	NC	DQ16	DQ25
96	3M	NC	NC	DQ34
97	1N	NC	NC	NC
98	2M	NC	NC	NC
99	3P	DQ7	DQ17	DQ26
100	2N	NC	NC	DQ35
101	2P	NC	NC	NC
102	1P	NC	NC	NC
103	3R	SA	SA	SA
104	4R	SA	SA	SA
105	4P	SA	SA	SA
106	5P	SA	SA	SA
107	5N	SA	SA	SA
108	5R	SA	SA	SA
109	—	INTER-NAL	INTER-NAL	INTER-NAL

Note: In boundary scan mode,

1. Clock balls (K / $\overline{\text{K}}$, C / $\overline{\text{C}}$) are referenced to each other and must be at opposite logic levels for reliable operation.
2. CQ and $\overline{\text{CQ}}$ data are synchronized to the respective C and $\overline{\text{C}}$.
3. If C and $\overline{\text{C}}$ tied high, CQ is generated with respect to K and $\overline{\text{CQ}}$ is generated with respect to $\overline{\text{K}}$.

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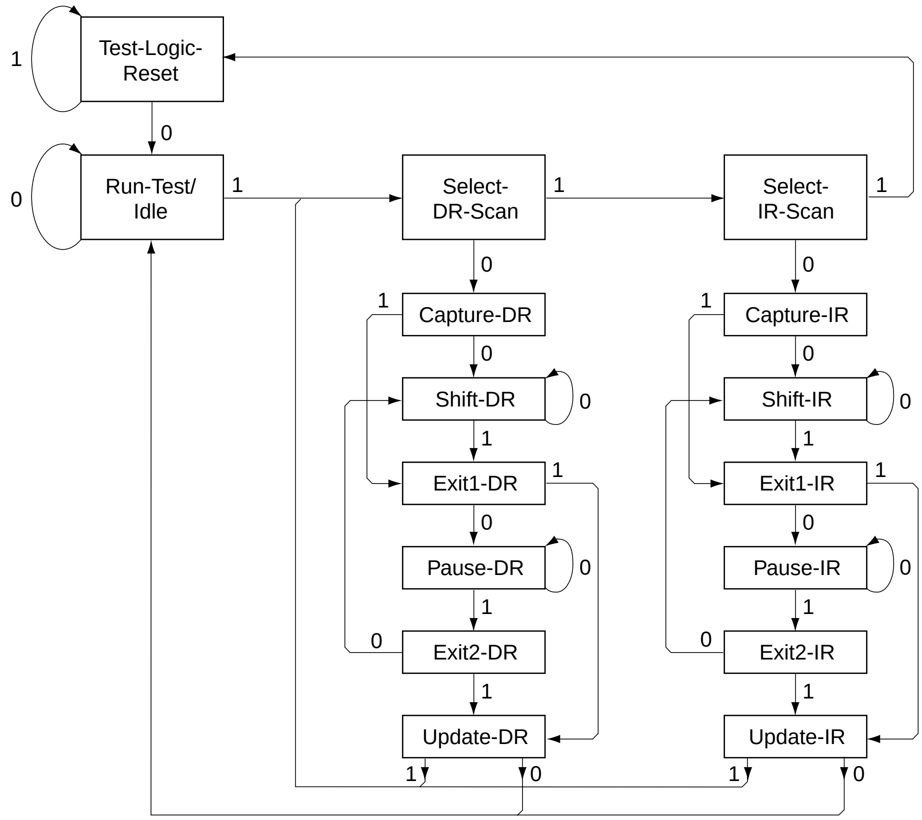
TAP Controller State Diagram

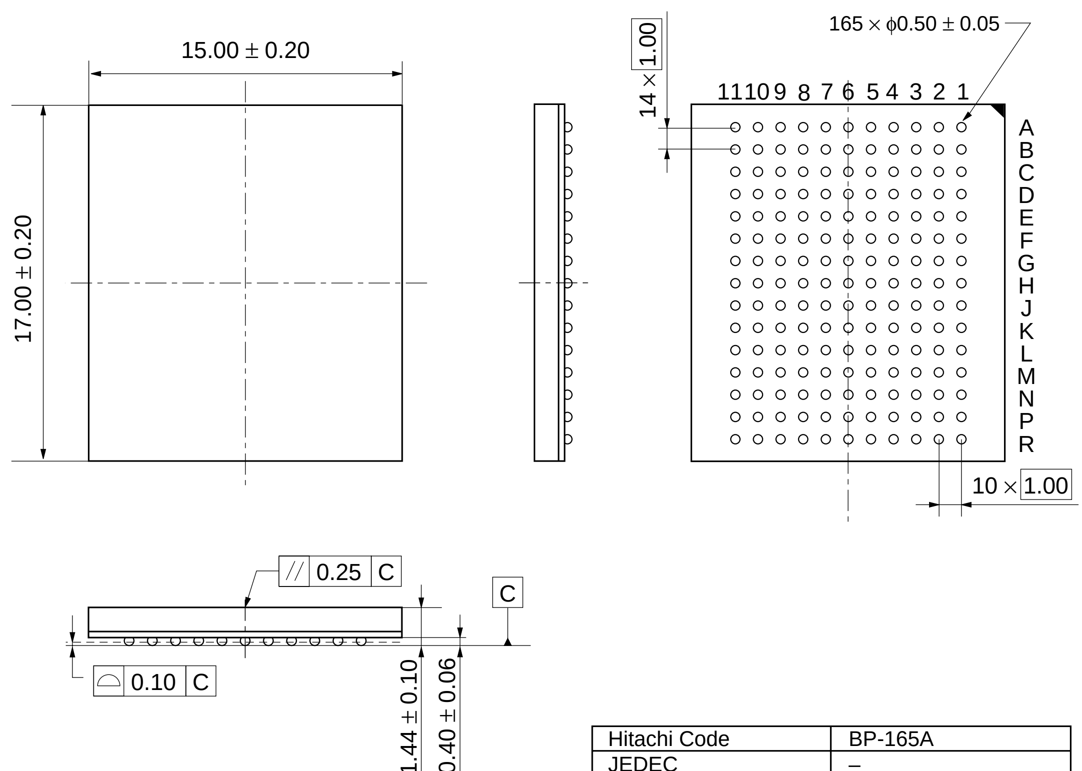


Notes: The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.
No matter what the original state of the controller, it will enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK.

Package Dimensions

HM66AEB36102/18202/9402BP (BP-165A)

Unit: mm



Hitachi Code	BP-165A
JEDEC	–
JEITA	–
Mass (reference value)	–

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