To all our customers

# Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

# M5M5Y5636TG – 25,22,20

**18874368-BIT(524288-WORD BY 36-BIT) NETWORK SRAM**

## DESCRIPTION

The M5M5Y5636TG is a family of 18M bit synchronous SRAMs organized as 524288-words by 36-bit. It is designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Mitsubishi's SRAMs are fabricated with high performance, low power CMOS technology, providing greater reliability. M5M5Y5636TG operates on a single 1.8V power supply and are 1.8V CMOS compatible.

## FEATURES

- **Fully registered inputs and outputs for pipelined operation**
- **Fast clock speed: 250, 225, and 200 MHz**
- **Fast access time: 2.1, 2.8, 3.2 ns**
- **Single 1.8V +150/-100mV power supply $V_{DD}$**
- **Separate $V_{DDQ}$ for 1.8V I/O**
- **Individual byte write (BWa# - BWd#) controls may be tied LOW**
- **Single Read/Write control pin (W#)**
- **Echo Clock outputs track data output drivers**
- **ZQ mode pin for user-selectable output drive strength**
- **2 User programmable chip enable inputs for easy depth expansion**
- **Linear or Interleaved Burst Modes**
- **JTAG boundary scan support**

## APPLICATION

High-end networking products that require high bandwidth, such as switches and routers.

## FUNCTION

Synchronous circuitry allows for precise cycle control triggered by a positive edge clock transition.

Synchronous signals include : all Addresses, all Data Inputs, all Chip Enables (E1#, E2, E3), Address Advance/Load (ADV), Byte Write Enables (BWa#, BWb#, BWc#, BWd#), Echo Clock outputs (CQ1, CQ1#, CQ2, CQ2#) and Read/Write (W#). Write operations are controlled by the eight Byte Write Enables (BWa# - BWd#) and Read/Write(W#) inputs. All writes are conducted with on-chip synchronous self-timed write circuitry.

The Echo Clocks are delayed copies of the RAM clock, CLK. Echo Clocks are designed to track changes in output driver delays due to variance in die temperature and supply voltage.

The ZQ pin supplied with selectable impedance drivers, allows selection between nominal drive strength (ZQ LOW) for multi-drop bus application and low drive strength (ZQ floating or HIGH) point-to-point applications.

The sense of two User-Programmable Chip Enable inputs (E2, E3), whether they function as active LOW or active HIGH inputs, is determined by the state of the programming inputs, EP2 and EP3.

The Linear Burst order (LBO#) is DC operated pin. LBO# pin will allow the choice of either an interleaved burst, or a linear burst.

All read, write and deselect cycles are initiated by the ADV Low input. Subsequent burst address can be internally generated as controlled by the ADV HIGH input.

## PACKAGE

| | Bump | Body Size | Bump Pitch |
|---|---|---|---|
| M5M5Y5636TG | 209(11X19) bump BGA | 14mm X 22mm | 1mm |

## PART NAME TABLE

| Part Name | Access | Cycle | Active Current (max.) | Standby Current (max.) |
|---|---|---|---|---|
| M5M5Y5636TG -25 | 2.1ns | 4.0ns | 550mA | 20mA |
| M5M5Y5636TG -22 | 2.8ns | 4.4ns | 500mA | 20mA |
| M5M5Y5636TG -20 | 3.2ns | 5.0ns | 450mA | 20mA |

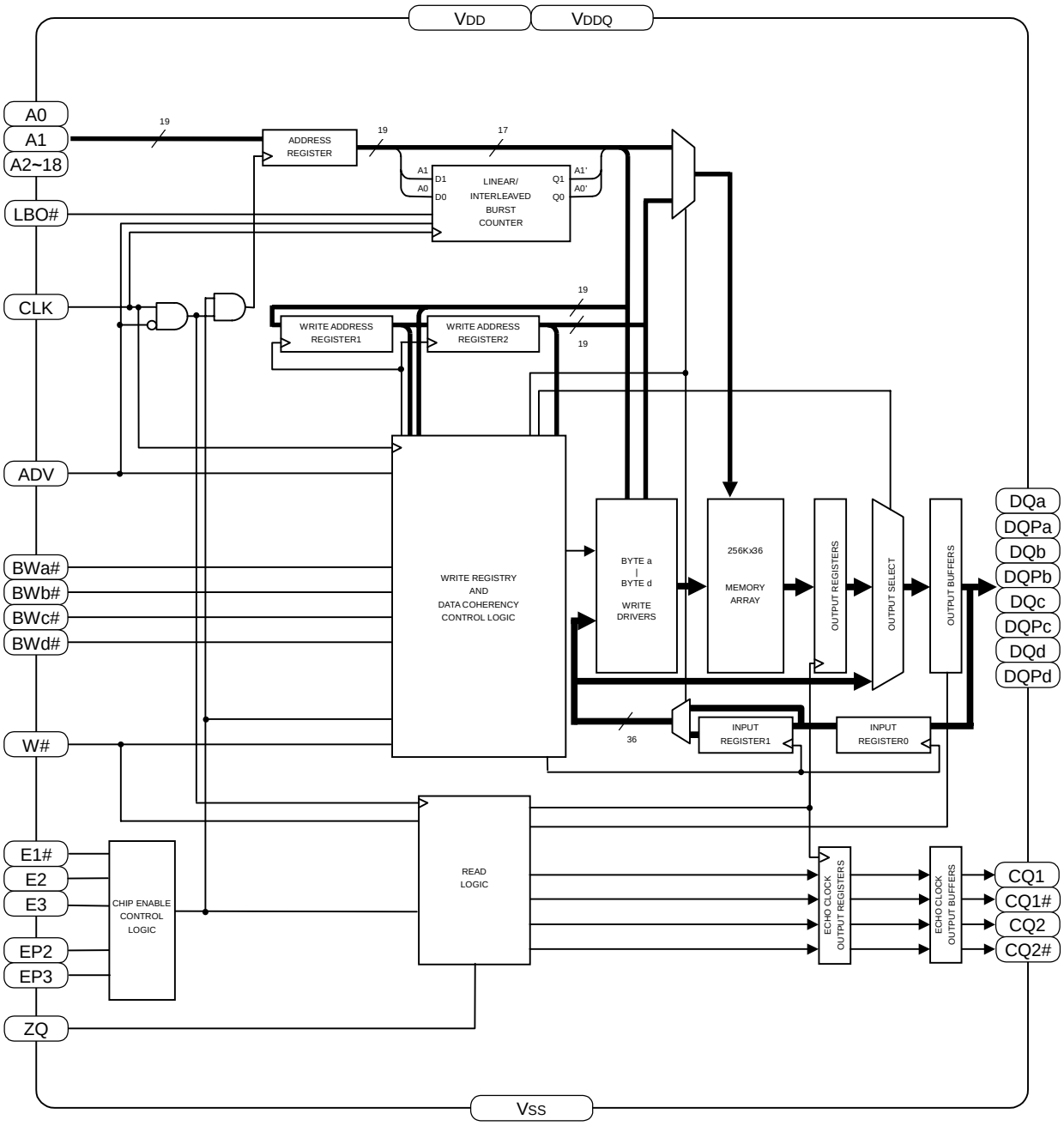
## BUMP LAYOUT(TOP VIEW)

### 209 bump BGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | NC | $A_6$ | E2 | $A_7$ | ADV | $A_8$ | E3 | $A_9$ | DQb | DQb |
| B | NC | NC | BWc# | NC | $A_{18}$ | W# | $A_{17}$ | BWb# | NC | DQb | DQb |
| C | NC | NC | NC | BWd# | NC | E1# | NC | NC | BWa# | DQb | DQb |
| D | NC | NC | $V_{SS}$ | NC | NC | MCL | NC | NC | $V_{SS}$ | DQb | DQb |
| E | NC | DQPc | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | NC | DQPb |
| F | DQc | DQc | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | ZQ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC |
| G | DQc | DQc | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | EP2 | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | NC | NC |
| H | DQc | DQc | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | EP3 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC |
| J | DQc | DQc | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | MCH | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | NC | NC |
| K | CQ2 | CQ2# | CLK | NC | $V_{SS}$ | MCL | $V_{SS}$ | NC | NC | CQ1# | CQ1 |
| L | NC | NC | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | MCH | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | DQa | DQa |
| M | NC | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | MCL | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | DQa | DQa |
| N | NC | NC | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | MCH | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | DQa | DQa |
| P | NC | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | MCL | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | DQa | DQa |
| R | DQPd | NC | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | DQPa | NC |
| T | DQd | DQd | $V_{SS}$ | NC | NC | LBO# | NC | NC | $V_{SS}$ | NC | NC |
| U | DQd | DQd | NC | $A_3$ | NC | $A_{15}$ | NC | $A_{11}$ | NC | NC | NC |
| V | DQd | DQd | $A_5$ | $A_4$ | $A_{16}$ | $A_1$ | $A_{13}$ | $A_{12}$ | $A_{10}$ | NC | NC |
| W | DQd | DQd | TMS | TDI | $A_2$ | $A_0$ | $A_{14}$ | TDO | TCK | NC | NC |

Note1. MCH means “Must Connect High”. MCH should be connected to HIGH.
Note2. MCL means “Must Connect Low”. MCL should be connected to LOW.

## BLOCK DIAGRAM




Note3. The BLOCK DIAGRAM does not include the Boundary Scan logic. See Boundary Scan chapter.
Note4. The BLOCK DIAGRAM illustrates simplified device operation. See TRUTH TABLE, PIN FUNCTION and timing diagrams for detailed information.

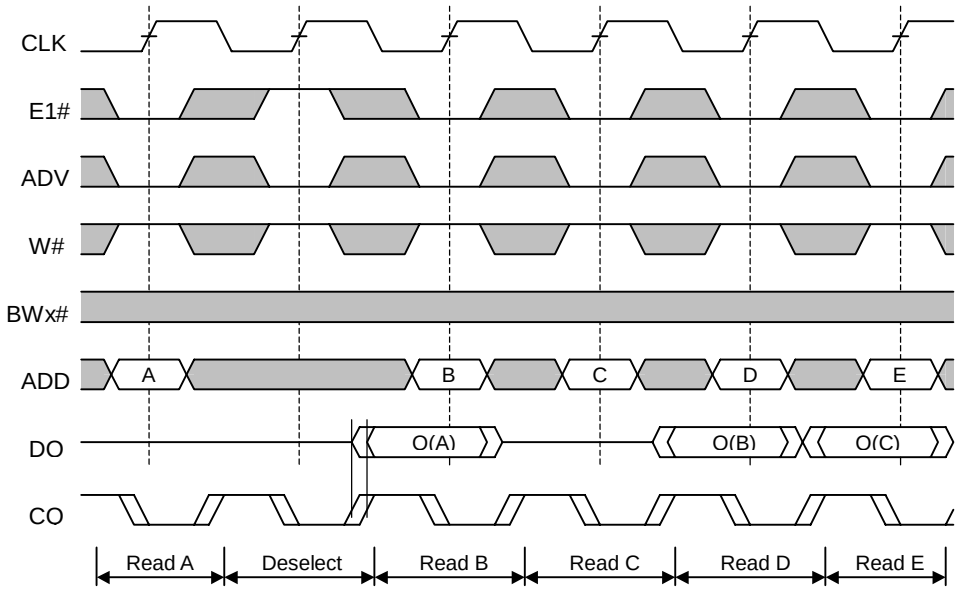
## PIN FUNCTION

| Pin | Name | Function |
|---|---|---|
| **A0~A18** | Synchronous Address Inputs | These inputs are registered and must meet the setup and hold times around the rising edge of CLK. A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired. |
| **BWa#, BWb#, BWc#, BWd#** | Synchronous Byte Write Enables | These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address. BWa are associated with addresses and apply to subsequent data. BWa# controls DQa, DQPa pins; BWb# controls DQb, DQPb pins; BWc# controls DQc, DQPc pins; BWd# controls DQd, DQPd pins. |
| **CLK** | Clock Input | This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge.<br>All synchronous inputs must meet setup and hold times around the clock's rising edge. |
| **E1#** | Synchronous Chip Enable | This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV is LOW). |
| **E2, E3** | Synchronous Chip Enable | These pins are user-programmable chip enable inputs. The sense of the inputs, whether they function as active LOW or HIGH inputs, is determined by the state of the programming inputs, EP2 and EP3. |
| **EP2, EP3** | Chip Enable Program Pin | These pins determine the sense of the user-programmable chip enable inputs, whether they function as active LOW or active HIGH inputs. |
| **ADV** | Synchronous Address Advance/Load | When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When HIGH, W# is ignored. A LOW on this pin permits a new address to be loaded at CLK rising edge. |
| **CQ1, CQ1#, CQ2, CQ2#** | Echo Clock Outputs | The Echo Clocks are delayed copies of the main RAM clock, CLK. |
| **ZQ** | Output Impedance Control | This pin allows selection between RAM nominal drive strength (ZQ low) for multi-drop bus applications and low drive strength (ZQ floating or high) point-to-point application. |
| **W#** | Synchronous Read/Write | This active input determines the cycle type when ADV is LOW. This is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on the pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus width WRITEs occur if all byte write enables are LOW. |
| **DQa,DQPa,DQb,DQPb, DQc,DQPc,DQd,DQPd** | Synchronous Data I/O | Byte “a” is DQa , DQPa pins; Byte “b” is DQb, DQPb pins; Byte “c” is DQc, DQPc pins; Byte “d” is DQd,DQPd pins. Input data must meet setup and hold times around CLK rising edge. |
| **LBO#** | Burst Mode Control | This DC operated pin allows the choice of either an interleaved burst or a linear burst. If this pin is HIGH or NC, an interleaved burst occurs. When this pin is LOW, a linear burst occurs, and input leak current to this pin. |
| **$V_{DD}$** | $V_{DD}$ | Core Power Supply |
| **$V_{SS}$** | $V_{SS}$ | Ground |
| **$V_{DDQ}$** | $V_{DDQ}$ | I/O buffer Power supply |
| **TDI** | Test Data Input | These pins are used for Boundary Scan Test. |
| **TDO** | Test Data Output | |
| **TCK** | Test Clock | |
| **TMS** | Test Mode Select | |
| **MCH** | Must Connect High | These pins should be connected to HIGH |
| **MCL** | Must Connect Low | These pins should be connected to LOW |
| **NC** | No Connect | These pins are not internally connected and may be connected to ground. |

## Read Operation

### Pipelined Read

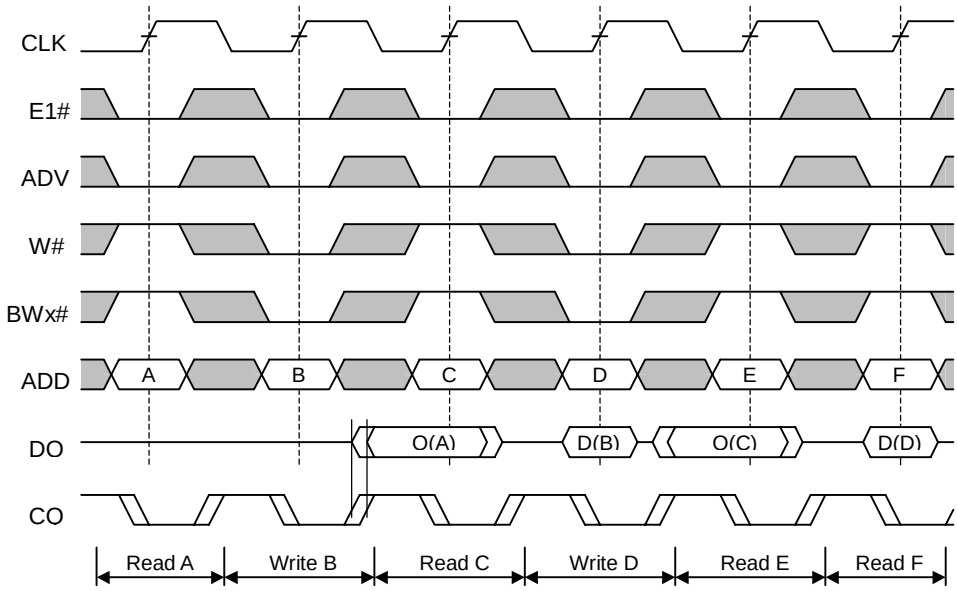
Read operation is initiated when the following conditions are satisfied at the rising edge of clock: All three chip enables (E1#, E2 and E3) are active, the write enable input signal (W#) is deasserted high, and ADV is asserted low. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the next rising edge of clock the read data is allowed to propagate through the output register and onto the output pins.



## Write Operation

### Double Late Write

Write operation occurs when the following conditions are satisfied at the rising edge of clock: All three chip enables (E1#, E2 and E3) are active and the write enable input signal (W#) is asserted low.
Double Late Write means that Data In is required on the third rising edge of clock. It is designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads.

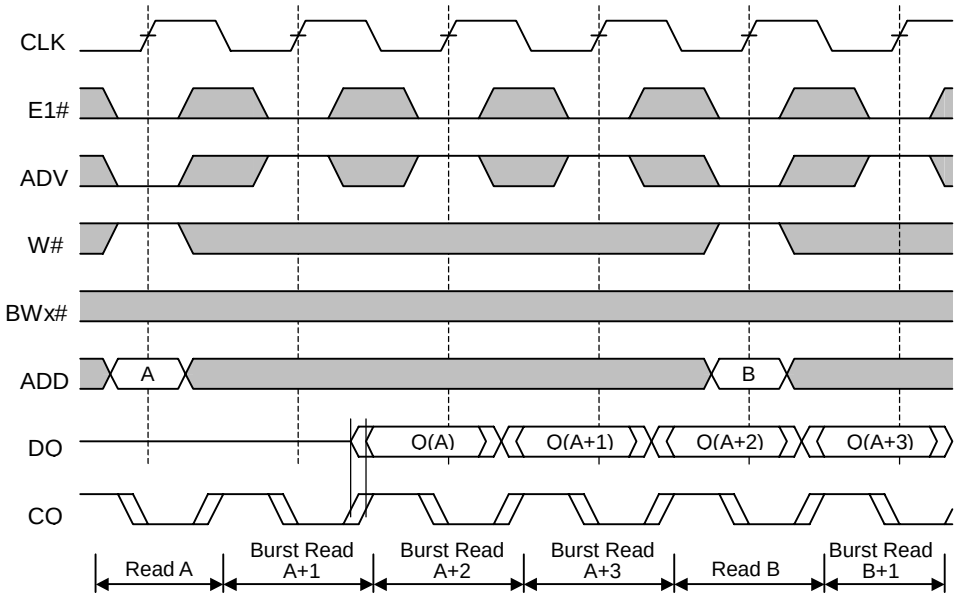


## Special Function

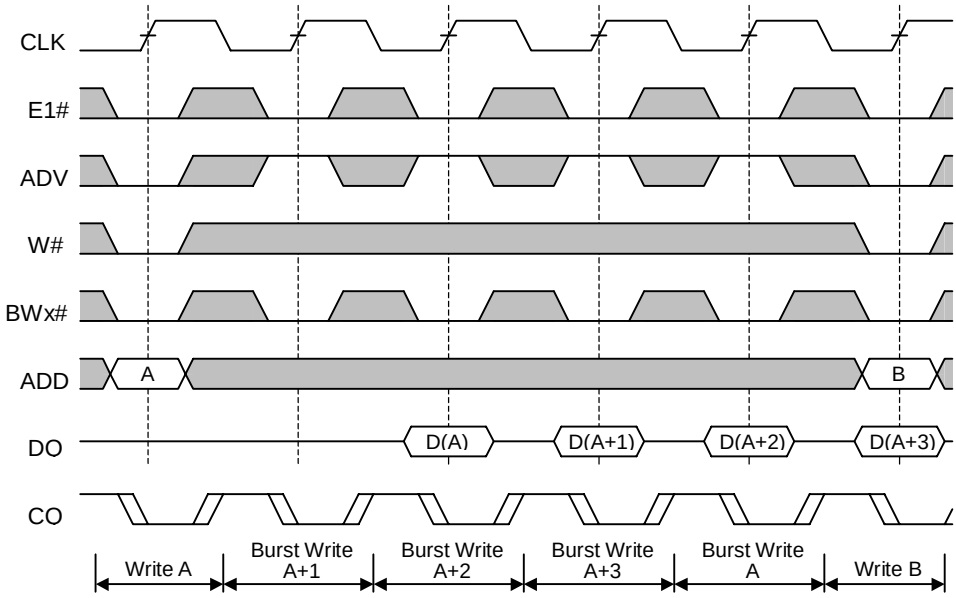
### Burst Cycles

The SRAM provides an on-chip burst address generator that can be utilized, if desired, to further simplify burst read or write implementations. The ADV control pin, when driven high, commands the SRAM to advance the internal address counter and use the counter generated address to read or write the SRAM. The starting address for the first cycle in a burst cycle series is loaded into the SRAM by driving the ADV pin low, into Load mode.

Burst Read




Burst Write



## DC OPERATED TRUTH TABLE

| Name | Input Status | Operation |
|---|---|---|
| LBO# | HIGH or NC | Interleaved Burst Sequence |
| | LOW | Linear Burst Sequence |

Note5. LBO# is DC operated pin.
Note6. NC means No Connection.
Note7. See BURST SEQUENCE TABLE about interleaved and Linear Burst Sequence.

## BURST SEQUENCE TABLE

(1) Interleaved Burst Sequence (when LBO# = HIGH or NC)

| Operation | A18~A2 | A1,A0 | | | |
|---|---|---|---|---|---|
| First access, latch external address | A18~A2 | 0 , 0 | 0 , 1 | 1 , 0 | 1 , 1 |
| Second access(first burst address) | latched A18~A2 | 0 , 1 | 0 , 0 | 1 , 1 | 1 , 0 |
| Third access(second burst address) | latched A18~A2 | 1 , 0 | 1 , 1 | 0 , 0 | 0 , 1 |
| Fourth access(third burst address) | latched A18~A2 | 1 , 1 | 1 , 0 | 0 , 1 | 0 , 0 |

(2) Linear Burst Sequence (when LBO# = LOW)

| Operation | A18~A2 | A1,A0 | | | |
|---|---|---|---|---|---|
| First access, latch external address | A18~A2 | 0 , 0 | 0 , 1 | 1 , 0 | 1 , 1 |
| Second access(first burst address) | latched A18~A2 | 0 , 1 | 1 , 0 | 1 , 1 | 0 , 0 |
| Third access(second burst address) | latched A18~A2 | 1 , 0 | 1 , 1 | 0 , 0 | 0 , 1 |
| Fourth access(third burst address) | latched A18~A2 | 1 , 1 | 0 , 0 | 0 , 1 | 1 , 0 |

Note8. The burst sequence wraps around to its initial state upon completion.

## Echo Clock

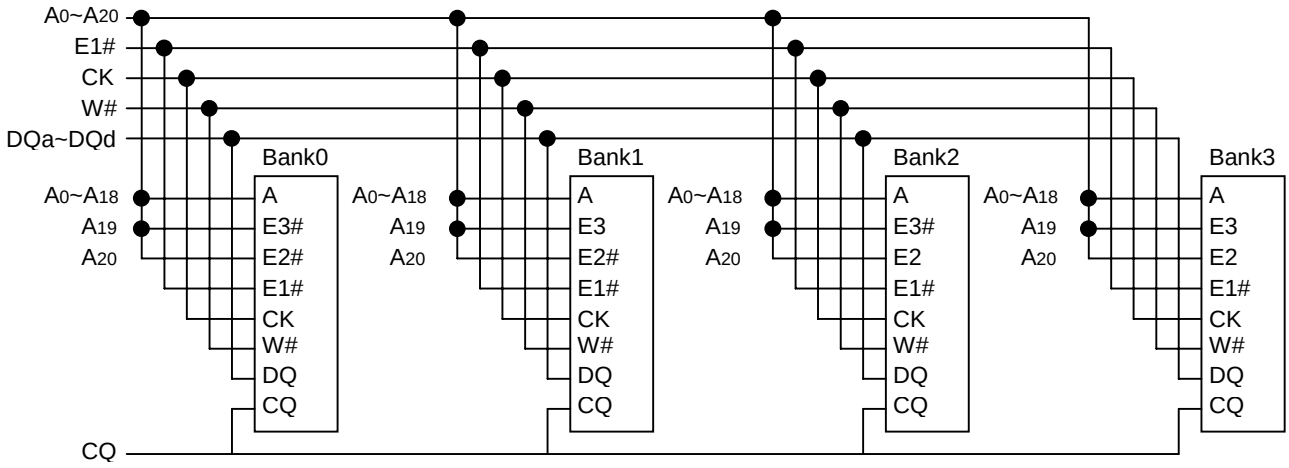
The SRAM features Echo Clocks, CQ1,CQ2, CQ1#, and CQ2# that track the performance of the output drivers. The Echo Clocks are delayed copies of the main RAM clock, CLK. Echo Clocks are designed to track changes in output driver delays due to variance in die temperature and supply voltage. The Echo Clocks are designed to fire with the rest of the data output drivers. The SRAM provide both in-phase, or true, Echo Clock outputs (CQ1 and CQ2) and inverted Echo Clock outputs (CQ1# and CQ2#).
It should be noted that deselection of the SRAM via E2 and E3 also deselects the Echo Clock output drivers. The deselection of Echo Clock drivers is always pipelined to the same degree as output data. Deselection of the SRAM via E1# does not deactivate the Echo Clocks.

## Programmable Enable

The SRAM features two user programmable chip enable inputs, E2 and E3. The sense of the inputs, whether they function as active low or active high inputs, is determined by the state of the programming inputs, EP2 and EP3. For example, if EP2 is held at HIGH, E2 functions as an active high enable. If EP2 is held to LOW, E2 functions as an active low chip enable input.

Programmability of E2 and E3 allows for banks of depth expansion to be accomplished with no additional logic. By programming the enable inputs of four SRAMs in binary sequence (00,01,10,11) and driving the enable inputs with two address inputs, four SRAMs can be made to look like one larger SRAM to the system.

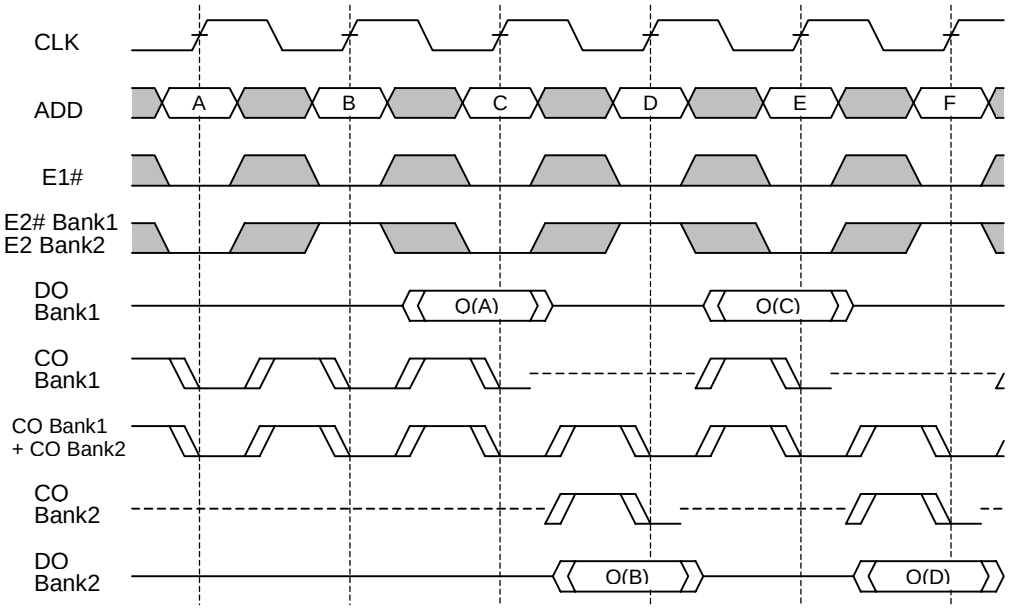
Example Four Bank Depth Schematic




**Bank Enable Truth Table**

| | EP2 | EP3 | E2 | E3 |
|---|---|---|---|---|
| Bank0 | LOW | LOW | Active Low | Active Low |
| Bank1 | LOW | HIGH | Active Low | Active High |
| Bank2 | HIGH | LOW | Active High | Active Low |
| Bank3 | HIGH | HIGH | Active High | Active High |

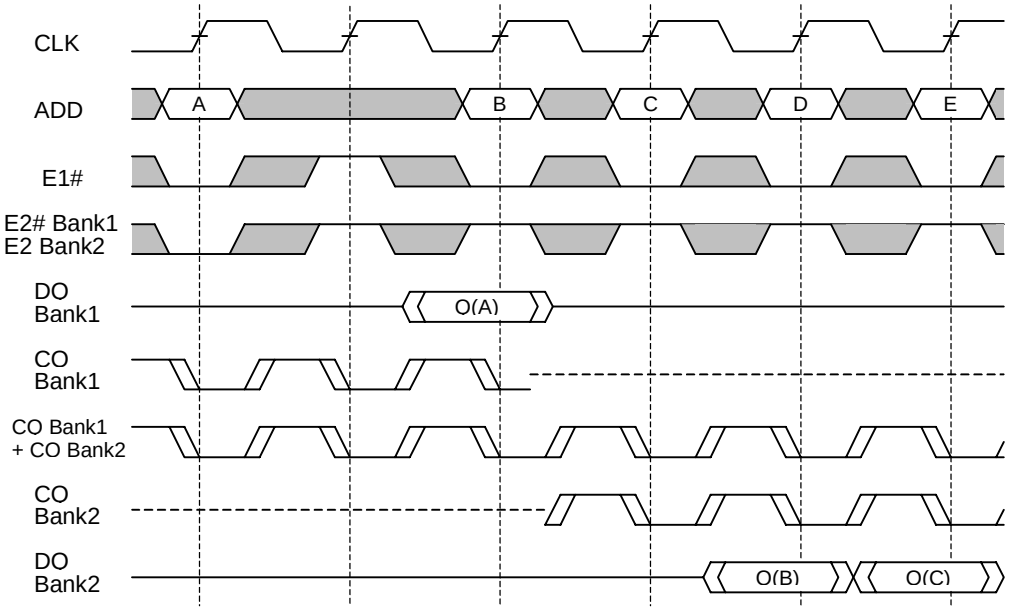
Echo Clock Control in Two Banks




Note9. E1# does not deselect the Echo Clock Outputs. Echo Clock outputs are synchronously deselected by E2 or E3 being sampled false.

It should be noted that deselection of the SRAM via E2 and E3 also deselects the Echo Clock output drivers. The deselection of Echo Clock drivers is always pipelined to the same degree as output data. Deselection of the SRAM via E1# does not deactivate the Echo Clocks.

Pipelined Read Bank Switch with E1# Deselect




Note10. E1# does not deselect the Echo Clock Outputs. Echo Clock outputs are synchronously deselected by E2 or E3 being sampled false.

In some applications it may be appropriate to pause between banks; to deselect both SRAMs with E1# before resuming read operations. An E1# deselect at a bank switch will allow at least one clock to be issued from the new bank before the first read cycle in the bank. Although the following drawing illustrates a E1# read pause upon switching from Bank 1 to Bank 2, a write to Bank 2 would have the same effect, causing the SRAM in Bank 2 to issue at least one clock before it is needed.

## Output Driver Impedance Control

The ZQ pin of SRAMs supplied with selectable impedance drivers, allows selection between SRAM nominal drive strength (ZQ low) for multi-drop bus applications and low drive strength (ZQ floating or high) point-to-point applications.

## TRUTH TABLE

| CLK | E1# ($t_n$) | E ($t_n$) | ADV ($t_n$) | W# ($t_n$) | BW# ($t_n$) | Previous Operation | Current Operation | DQ/CQ ($t_n$) | DQ/CQ ($t_{n+1}$) | DQ/CQ ($t_{n+2}$) |
|---|---|---|---|---|---|---|---|---|---|---|
| L->H | X | F | L | X | X | X | Bank Deselect | *** | High-Z | --- |
| L->H | X | X | H | X | X | Bank Deselect | Bank Deselect (Continue) | High-Z | High-Z | --- |
| L->H | H | T | L | X | X | X | Deselect | *** | High-Z / CQ | --- |
| L->H | X | X | H | X | X | Deselect | Deselect (Continue) | High-Z / CQ | High-Z / CQ | --- |
| L->H | L | T | L | L | T | X | Write<br>Loads new address<br>Stores DQx if BWx#=LOW | *** | *** | $D_n$ / CQ ($t_n$) |
| L->H | L | T | L | L | F | X | Write (Abort)<br>Loads new address<br>No data stored | *** | *** | High-Z / CQ |
| L->H | X | X | H | X | T | Write | Write Continue<br>Increments address by 1<br>Stores DQx if BWx#=LOW | *** | $D_{n-1}$ / CQ ($t_{n-1}$) | $D_n$ / CQ ($t_n$) |
| L->H | X | X | H | X | F | Write | Write Continue (Abort)<br>Increments address by 1<br>No data stored | *** | $D_{n-1}$ / CQ ($t_{n-1}$) | High-Z / CQ |
| L->H | L | T | L | H | X | X | Read<br>Loads new address | *** | $Q_n$ / CQ ($t_n$) | --- |
| L->H | X | X | H | X | X | Read | Read Continue<br>Increments address by 1 | $Q_{n-1}$ / CQ ($t_{n-1}$) | $Q_n$ / CQ ($t_n$) | --- |

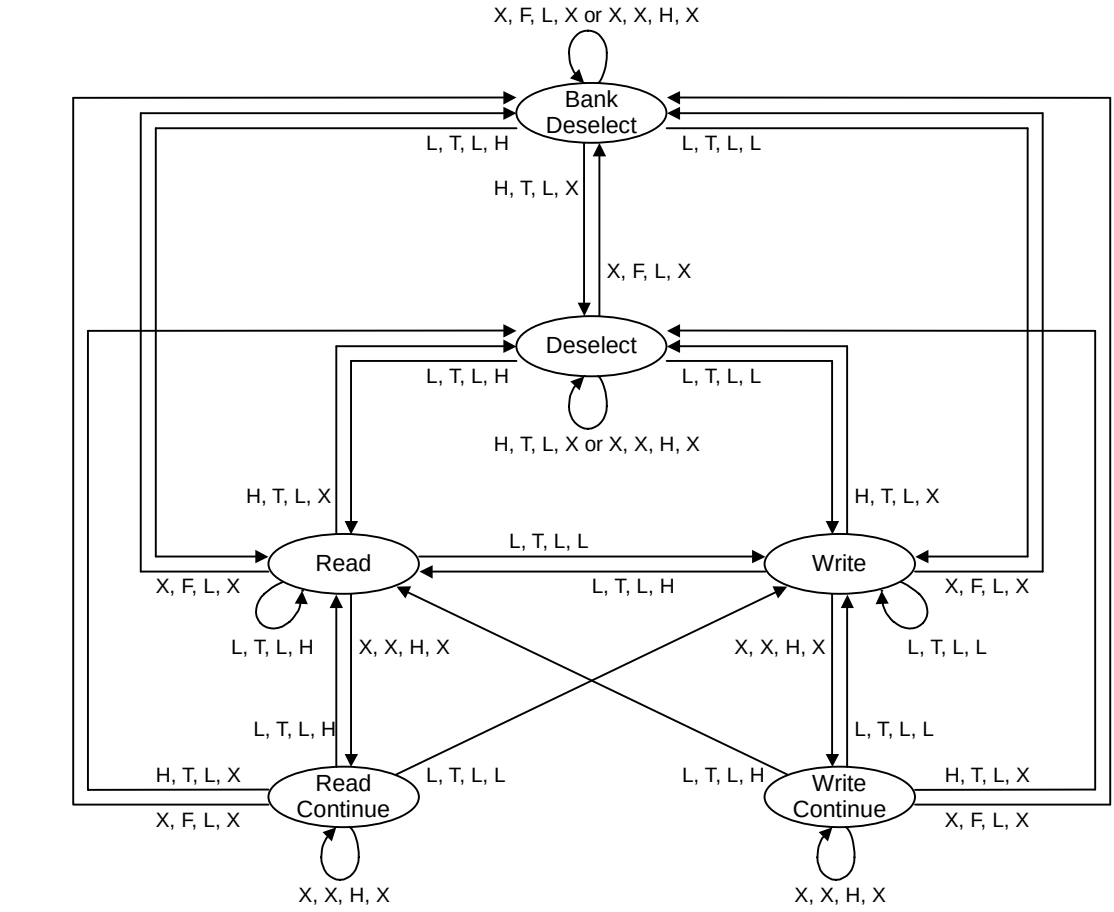
Note11. If E2=EP2 and E3=EP3 then E="T" else E="F".
Note12. If one or more BWx#=VIL and other BWx#=VIH then BW#="T". If all BWx#=VIH then BW#="F".
Note13."H" = input VIH; "L" = input VIL; "X" = input VIH or VIL; "T" = input "true"; "F" = input "false".
Note14. " *** " = indicates that the DQ input requirement / output state and CQ output state are determined by the previous operation.
Note15. " --- " = indicates that the DQ input requirement / output state and CQ output state are determined by the next operation.
Note16. DQs are tri-stated in response to Bank Deselect, Deselect and Write commands, one full cycle after the command is sampled.
Note17. CQs are tri-stated in response to Bank Deselect commands only, one full cycle after the command is sampled.
Note18. Up to three (3) Continue operations may be initiated after a Read or Write operation is initiated to burst transfer up to four (4) distinct pieces of data per single external address input. If a fourth (4) Continue operation is initiated, the internal address wraps back to the initial external (base) address.

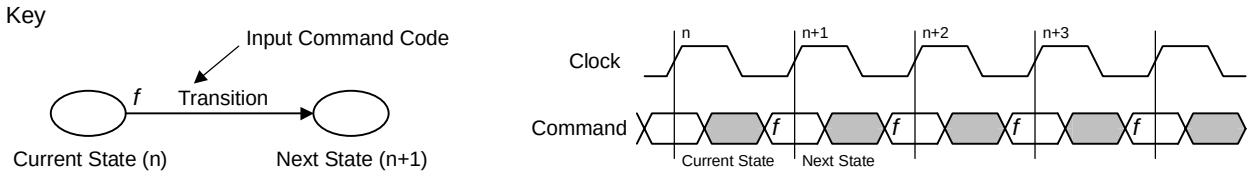
## WRITE TRUTH TABLE

| W# | BWa# | BWb# | BWc# | BWd# | Function |
|---|---|---|---|---|---|
| H | X | X | X | X | Read |
| L | L | H | H | H | Write Byte "a" |
| L | H | L | H | H | Write Byte "b" |
| L | H | H | L | H | Write Byte "c" |
| L | H | H | H | L | Write Byte "d" |
| L | L | L | L | L | Write All Bytes |
| L | H | H | H | H | Write Abort / NOP |

Note19. "H" = input VIH; "L" = input VIL; "X" = input VIH or VIL.
Note20. All inputs must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.

## STATE DIAGRAM




Current State & Next State Definition for Read/Write Control State Diagram

Note21. The notation “X, X, X, X” controlling the state transitions above indicate the states of inputs E1#, E, ADV, and W# respectively.
Note22. If (E2=EP2 and E3=EP3) then E=”T” else E=”F”.
Note23. “H” = input VIH; “L” = input VIL; “X” = input VIH or VIL; “T” = input “true”; “F” = input “false”.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | With respect to $V_{SS}$ | -0.5*~2.5 | V |
| $V_{DDQ}$ | I/O Buffer Power Supply Voltage | | -0.5*~2.5 | V |
| $V_I$ | Input Voltage | | -0.5~$V_{DDQ}$+0.5(≤2.5V max.) ** | V |
| $V_O$ | Output Voltage | | -0.5~$V_{DDQ}$+0.5(≤2.5V max.) ** | V |
| PD | Maximum Power Dissipation ($V_{DD}$) | | 780 | mW |
| $T_{OPR}$ | Operating Temperature | | 0~70 | °C |
| $T_{STG(bias)}$ | Storage Temperature(bias) | | -10~85 | °C |
| $T_{STG}$ | Storage Temperature | | -55~125 | °C |

Note24. * This is -1.0V~3.6V when pulse width≤2ns, and -0.5V~2.5V in case of DC.
** This is -1.0V~$V_{DDQ}$+1.0V(≤3.6V max.) when pulse width≤2ns, and –0.5V~$V_{DDQ}$+0.5V in case of DC.

## DC ELECTRICAL CHARACTERISTICS

### (1) Power Supplies

| Symbol | Parameter | Condition | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{DD}$ | Power Supply Voltage | | 1.70 | 1.95 | V |
| $V_{DDQ}$ | I/O Buffer Power Supply Voltage | | 1.70 | 1.95 | V |

### (2) CMOS I/O DC Input Characteristics

| Symbol | Parameter | Condition | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IH}$ | High-level Input Voltage | | 0.65*$V_{DDQ}$ | $V_{DDQ}$+0.3 | V |
| $V_{IL}$ | Low-level Input Voltage | | -0.3* | 0.35*$V_{DDQ}$ | V |

Note25. *$V_{IL}$ min is –1.0V and $V_{IH}$ max is $V_{DDQ}$+1.0V(max. 3.6V) in case of AC (Pulse width ≤ 2ns).

### (3) Input and Output Leakage Characteristics

| Symbol | Parameter | Condition | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $I_{IL}$ | Input Leakage Current (except EP2, EP3, LBO#, ZQ, MCH, MCL pins) | $V_I$ = 0V~$V_{DDQ}$ | | 10 | µA |
| | Input Leakage Current of EP2, EP3, MCH, MCL pins | $V_I$ = 0V~$V_{DDQ}$ | | 10 | µA |
| | Input Leakage Current of ZQ | $V_I$ = 0V~$V_{DDQ}$ | | 100 | µA |
| | Input Leakage Current of LBO# | $V_I$ = 0V~$V_{DDQ}$ | | 100 | µA |
| $I_{OL}$ | Output Leakage Current | $V_{I/O}$ = 0V~$V_{DDQ}$ | | 10 | µA |

### (4) Selectable Impedance Output Driver DC Electrical Characteristics

| Symbol | Parameter | Condition | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{OHL}$ | Low Drive Output High Voltage | $I_{OHL}$ = -4mA | $V_{DDQ}$-0.4V | | V |
| $V_{OLL}$ | Low Drive Output Low Voltage | $I_{OLL}$ = 4mA | | 0.4 | V |
| $V_{OHH}$ | High Drive Output High Voltage | $I_{OHH}$ = -8mA | $V_{DDQ}$-0.4V | | V |
| $V_{OLH}$ | High Drive Output Low Voltage | $I_{OLH}$ = 8mA | | 0.4 | V |

Note26. ZQ=H; High Impedance output driver setting
Note27. ZQ=L; Low Impedance output driver setting

### (5) Operating Currents

| Symbol | Parameter | Condition | | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $I_{CC1}$ | Power Supply Current : Operating | Device selected; Output open All other inputs $V_I \le V_{IL}$ or $V_I \ge V_{IH}$ | 4.0ns cycle (250MHz) | | 550 | mA |
| | | | 4.4ns cycle (225MHz) | | 500 | |
| | | | 5.0ns cycle (200MHz) | | 450 | |
| $I_{CC2}$ | Power Supply Current :Chip Disable and Bank Deselect | E1#$\ge V_{IH}$ or (E2 or E3 False) Output open All other inputs $V_I \le V_{IL}$ or $V_I \ge V_{IH}$ | 4.0ns cycle (250MHz) | | 160 | mA |
| | | | 4.4ns cycle (225MHz) | | 150 | |
| | | | 5.0ns cycle (200MHz) | | 140 | |
| $I_{CC3}$ | CMOS Standby Current (CLK stopped standby mode) | Device deselected; Output open CLK frequency=0Hz All inputs $V_I \le V_{SS}$+0.1V or $V_I \ge V_{DDQ}$-0.1V | | | 20 | mA |

### CAPACITANCE

| Symbol | Parameter | Condition | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_I$ | Input Capacitance | $V_I$=GND, $V_I$=25mVrms, f=1MHz | | | 6 | pF |
| $C_O$ | Input / Output (DQ) Capacitance | $V_O$=GND, $V_O$=25mVrms, f=1MHz | | | 8 | pF |

Note28. This parameter is sampled.

### THERMAL RESISTANCE

**4-Layer PC board mounted (70x70x1.6mmT)**

| Symbol | Parameter | Condition | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $\theta_{JA}$ | Thermal resistance Junction Ambient | Air velocity=**0**m/sec | | 25.56 | | °C/W |
| | | Air velocity=**2**m/sec | | 17.63 | | °C/W |
| $\theta_{JC}$ | Thermal resistance Junction to Case | | | 6.12 | | °C/W |

**AC ELECTRICAL CHARACTERISTICS** (Ta=0~70°C, $V_{DD}$=1.70~1.95V, unless otherwise noted)

**(1) MEASUREMENT CONDITION**

Input pulse levels ····· $V_{IH}=V_{DDQ}$, $V_{IL}$=0V
Input rise and fall times ····· faster than or equal to 1V/ns
Input timing reference levels ····· $V_{IH}=V_{IL}=V_{DDQ}$ / 2
Output reference levels ····· $V_{IH}=V_{IL}=V_{DDQ}$ / 2
Output load ····· Fig.1

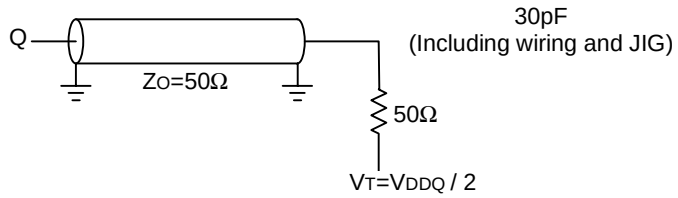



Fig.1 Output load

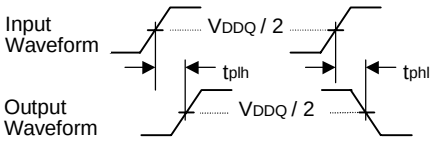



Fig.2 Tdly measurement

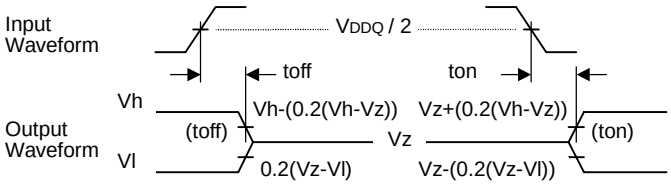



Fig.3 Tri-State measurement

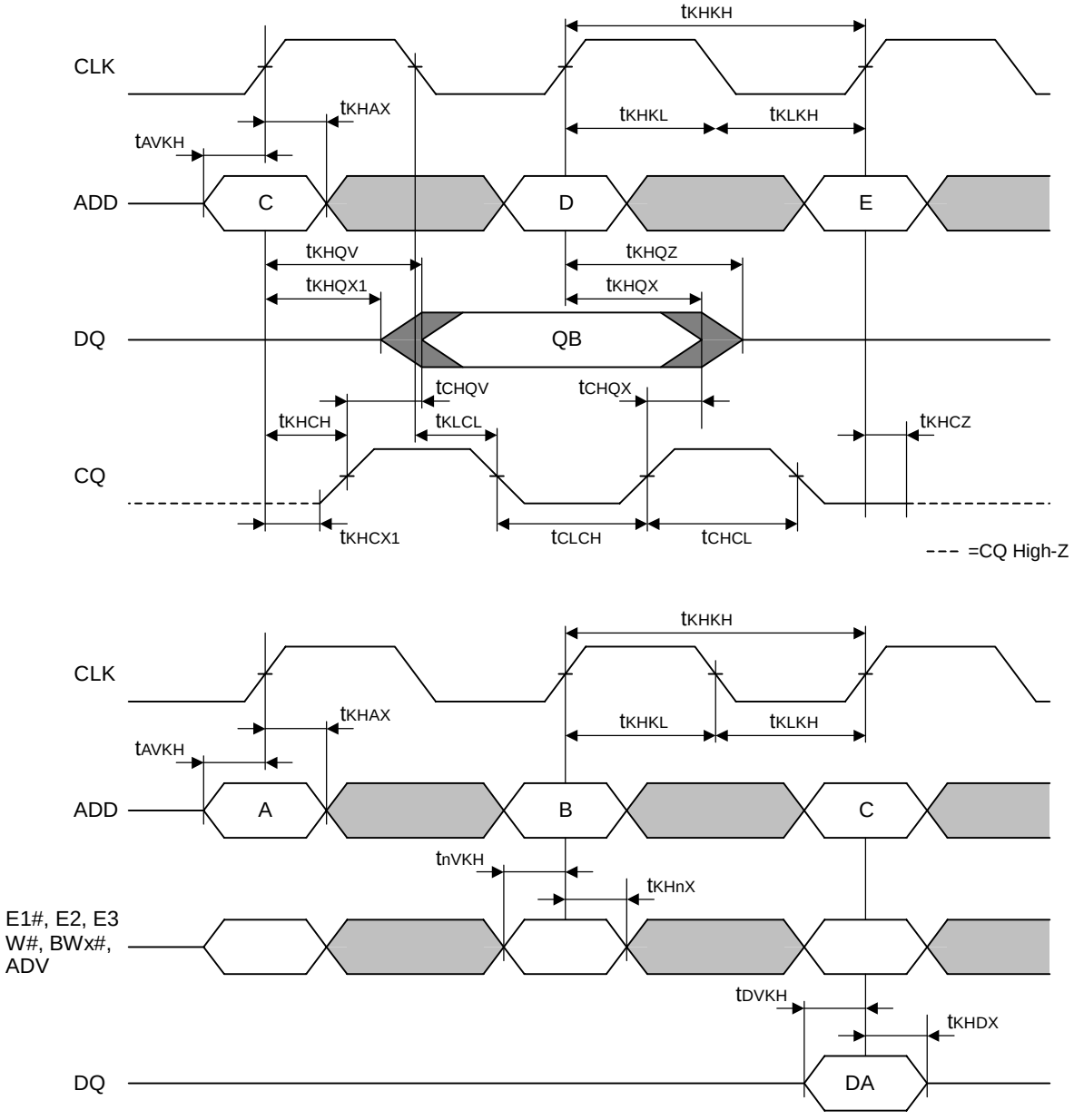
Note29.Valid Delay Measurement is made from the $V_{DDQ}$/2 on the input waveform to the $V_{DDQ}$/2 on the output waveform. Input waveform should have a slew rate of faster than or equal to 1V/ns.
Note30.Tri-state toff measurement is made from the $V_{DDQ}$/2 on the input waveform to the output waveform moving 20% from its initial to final Value $V_{DDQ}$/2.
Note:the initial value is not $V_{OL}$ or $V_{OH}$ as specified in DC ELECTRICAL CHARACTERISTICS table.
Note31. Tri-state ton measurement is made from the $V_{DDQ}$/2 on the input waveform to the output waveform moving 20% from its initial Value $V_{DDQ}$/2 to its final Value.
Note:the final value is not $V_{OL}$ or $V_{OH}$ as specified in DC ELECTRICAL CHARACTERISTICS table.
Note32.Clocks,Data,Address and control signals will be tested with a minimum input slew rate of faster than or equal to 1V/ns.

## (2)TIMING CHARACTERISTICS

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | 250MHz | | 225MHz | | 200MHz | | |
| | | -25 | | -22 | | -20 | | |
| | | Min | Max | Min | Max | Min | Max | |
| Clock | | | | | | | | |
| $t_{KHKH}$ | Clock Cycle Time | 4.0 | | 4.4 | | 5.0 | | ns |
| $t_{KHKL}$ | Clock HIGH Time | 1.5 | | 1.6 | | 1.8 | | ns |
| $t_{KLKH}$ | Clock LOW Time | 1.5 | | 1.6 | | 1.8 | | ns |
| Output times | | | | | | | | |
| $t_{KHQV}$ | Clock HIGH to Output Valid | | 2.1 | | 2.8 | | 3.2 | ns |
| $t_{KHQX}$ | Clock HIGH to Output Invalid | 0.5 | | 0.6 | | 0.7 | | ns |
| $t_{KHQX1}$ | Clock HIGH to Output in Low-Z | 0.5 | | 0.6 | | 0.7 | | ns |
| $t_{KHQZ}$ | Clock HIGH to Output in High-Z | 0.5 | 2.1 | 0.6 | 2.8 | 0.7 | 3.2 | ns |
| $t_{CHCL}$ | Echo Clock HIGH Time | $t_{KHKL}$+0.25/-0.25 | | $t_{KHKL}$+0.25/-0.25 | | $t_{KHKL}$+0.25/-0.25 | | ns |
| $t_{CLCH}$ | Echo Clock LOW Time | $t_{KLKH}$ +0.25/-0.25 | | $t_{KLKH}$ +0.25/-0.25 | | $t_{KLKH}$ +0.25/-0.25 | | ns |
| $t_{KHCH}$ | Clock HIGH to Echo Clock HIGH | 0.5 | 2.0 | 0.5 | 2.7 | 0.5 | 3.1 | ns |
| $t_{KLCL}$ | Clock LOW to Echo Clock LOW | 0.5 | 2.0 | 0.5 | 2.7 | 0.5 | 3.1 | ns |
| $t_{KHCX1}$ | Clock HIGH to Echo Clock Low-Z | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{KHCZ}$ | Clock HIGH to Echo Clock High-Z | 0.5 | 2.0 | 0.5 | 2.7 | 0.5 | 3.1 | ns |
| $t_{CHQV}$ | Echo Clock HIGH to Output Valid | | 0.5 | | 0.5 | | 0.5 | ns |
| $t_{CHQX}$ | Echo Clock HIGH to Output Invalid | -0.5 | | -0.5 | | -0.5 | | ns |
| Setup Times | | | | | | | | |
| $t_{AVKH}$ | Address Valid to Clock HIGH | 0.8 | | 1.0 | | 1.2 | | ns |
| $t_{advVKH}$ | ADV Valid to Clock HIGH | 0.8 | | 1.0 | | 1.2 | | ns |
| $t_{WVKH}$ | Write Valid to Clock HIGH | 0.8 | | 1.0 | | 1.2 | | ns |
| $t_{BxVKH}$ | Byte Write Valid to Clock HIGH (BWa#~BWd#) | 0.8 | | 1.0 | | 1.2 | | ns |
| $t_{EVKH}$ | Enable Valid to Clock HIGH (E1#,E2,E3) | 0.8 | | 1.0 | | 1.2 | | ns |
| $t_{DVKH}$ | Data In Valid Clock HIGH | 0.8 | | 1.0 | | 1.2 | | ns |
| Hold Times | | | | | | | | |
| $t_{KHAX}$ | Clock HIGH to Address don't care | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{KHadvX}$ | Clock HIGH to ADV don't care | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{KHWX}$ | Clock HIGH to Write don't care | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{KHBxX}$ | Clock HIGH to Byte Write don't care (BWa#~BWd#) | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{KHEX}$ | Clock HIGH to Enable don't care (E1#,E2,E3) | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{KHDX}$ | Clock HIGH to Data In don't care | 0.5 | | 0.5 | | 0.5 | | ns |

Note33. Test conditions is specified with the output loading shown in Fig.1 unless otherwise noted.
Note34. $t_{KHQX1}$, $t_{KHQZ}$, $t_{KHCX1}$, $t_{KHCZ}$ are sampled.
Note35. LBO#, EP2, EP3, ZQ is static and must not change during normal operation.

**Timing Parameter Key**




Note36. $t_{nVKH}$=$t_{EVKH}$, $t_{WVKH}$, $t_{BxVKH}$, $t_{advVKH}$, etc. and $t_{KHnX}$=$t_{KHEX}$, $t_{KHWX}$, $t_{KHBxX}$, $t_{KHadvX}$, etc.

## JTAG PORT OPERATION

### Overview

The JTAG Port on this SRAM operates in a manner consistent with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG), but dose not implement all of the function required for 1149.1 compliance. Unlike JTAG implementations that have been common among SRAM vendors for the last several years, this implementation dose offer a form of EXTEST, known as Clock Assisted EXTEST, reducing or eliminating the "hand coding" that has been required to overcome the test program compiler errors caused by previous non-compliant implementation. The JTAG Port interfaces with conventional CMOS logic level signaling.

### Disabling the JTAG port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. To assure normal operation of the SRAM with the JTAG Port unused, the TCK, TDI and TMS pins may be left floating or tied to High. The TDO pin should be left unconnected.

### JTAG Pin Description

**Test Clock (TCK)**

The TCK input is clock for all TAP events. All inputs are captured on the rising edge of TCK and the Test Data Out (TDO) propagates from the falling edge of TCK.

**Test Mode Select (TMS)**

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP Controller state machine. An undriven TMS input will produce the same result as a logic one input level.

**Test Data In (TDI)**

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between the TDI and TDO pins. the register placed between the TDI and TDO pins is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Resister (refer to the TAP Controller State Diagram). An undriven TDI Input will produce the same result as a logic one input level.

**Test Data Out (TDO)**

The TDO output is active depending on the state of the TAP Controller state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between the TDI and TDO pins.

**Note:**

This device dose not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automatically at power-up.

### JTAG Port Registers

**Overview**

The various JTAG registers, referred to as Test Access Port or TAP Registers, are selected (one at a time) via the sequence of 1s and 0s applied to TMS as TCK is strobed. Each of TAP Registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

**Instruction Register**

The Instruction Register holds the instructions that are executed by the TAP Controller when it is moved into the Run-Test/Idle, or the

various data register states. Instructions are 3 bits long. The Instruction Resister can be loaded when it is placed between the TDI and TDO pins. The Instruction Resister is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in the Test-Logic-Reset state.

**Bypass Register**
The Bypass resister is a single-bit register that can be placed between the TDI and TDO pins. It allows serial test data to be passed through the SRAM's JTAG Port to another device in the scan chain with as little delay as possible.

**Boundary Scan Register**
The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the SRAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pins. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the SRAM's I/O ring when the controller is in the Capture-RD state and then is placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instruction can be used to activate the Boundary Scan Register.

**Identification (ID) Register**
The ID register is a 32-bit register that is loaded with a device and vender specific 32-bit code when the controllers put in the Capture-DR state with the IDCODE Instruction loaded in the Instruction Register. The code is loaded from 32-bit on-chip ROM. It describes various attributes of the SRAM (see page 25). The register is then placed between the TDI and TDO pins when the controller is moved into the Shift-DR state. Bit 0 in the register is the LSB and the first to reach the TDO pin when shifting begins.

## TAP Controller Instruction Set

**Overview**
There are two classes of instructions defined in the Standard 1149.1-1990; standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. Although the TAP Controller in this device follows the 1149.1 conventions, it is not 1194.1-compliant because one of the mandatory instructions, EXTEST, is uniquely implemented. The TAP on this device may be used to monitor all input and I/O pads. This device will not perform INTEST but can perform the preload portion of the SAMPLE/PRELOAD command.
When the TAP controller is placed in the Capture-IR state, the two least significant bits of the instruction register are loaded with 01. When the TAP controller is moved to the Shift-IR state, the Instruction Register is placed between the TDI and TDO pins. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at the TDO output). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to the Update-IR state. The TAP Instruction Set for this device is listed in the following table.

**Instruction Descriptions**

**BYPASS**
When the BYPASS instruction is loaded in the Instruction Register, the Bypass Register is placed between the TDI and TDO pins. This occurs when the TAP Controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

**SAMPLE/PRELOAD**
SAMPLE/PRELOAD is a Standard1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the Instruction Register, moving the TAP Controller into the Capture-DR state loads the data in the SRAM's input and I/O buffers into the Boundary Scan Register. Some Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the BSDL file. Because the SRAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to

sample metastable inputs will not harm the device, repeatable results cannot be expected. SRAM input signals must be stabilized for long enough to meet the TAP's input data capture set-up plus hold time (tTS plus tTH). The SRAM's clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to the Shift-DR state then places the Boundary Scan Register between the TDI and TDO pins.

**EXTEST-A**

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the Instruction Register is loaded with all logic 0s. The EXTEST command dose not block or override the SRAM's input pins; therefore, the SRAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the SRAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the state of all SRAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the SRAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

The EXTEST implementation in this device dose not, without further user intervention, actually move the contents of the scan chain onto the SRAM's output pins. Therefore this device is not strictly 1149.1-compliant. To push data from the Boundary Scan Registers, in parallel, out onto the SRAM's I/O and output pins, the SRAM's main clock (CK) must be pulsed. A single CK transition is sufficient to transfer the data, but more transitions will do no harm.

**IDCODE**

The IDCODE instruction cause the ID ROM to be loaded into the ID register when the controller is in the Capture-DR state and places the ID Register between the TDI and TDO pins in the Shift-DR state. The IDCODE instruction is the default instruction loaded in at power-up and any time the controller is placed in the Test-Logic-Reset state.

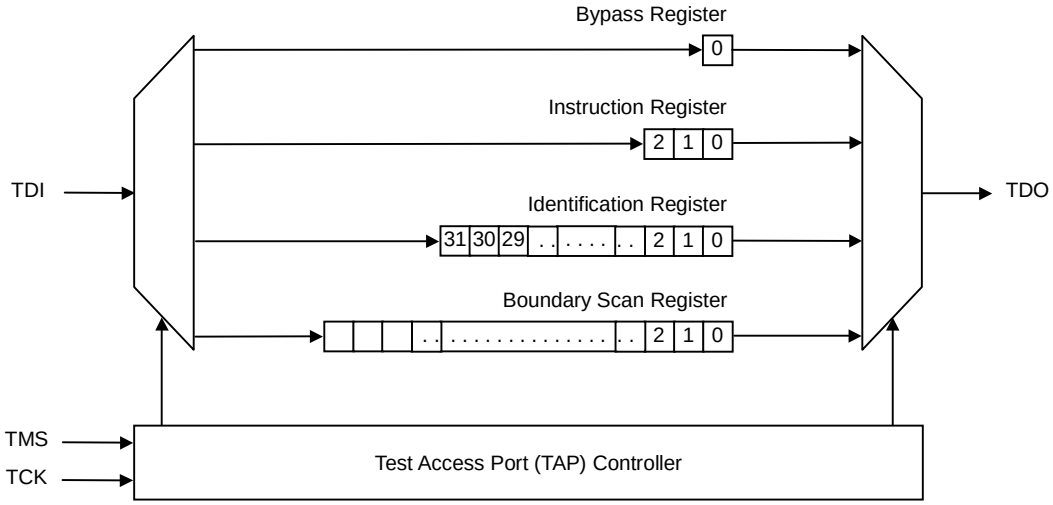
**SAMPLE-Z**

If the SAMPLE-Z instruction is loaded in the Instruction Register, all SRAM outputs are forced to an inactive drive state (High-Z) and the Boundary Scan Register is placed between the TDI and TDO pins when the TAP Controller is moved to the Shift-DR state.

**RFU**

These instructions are reserved for future use. Do not use these instructions.

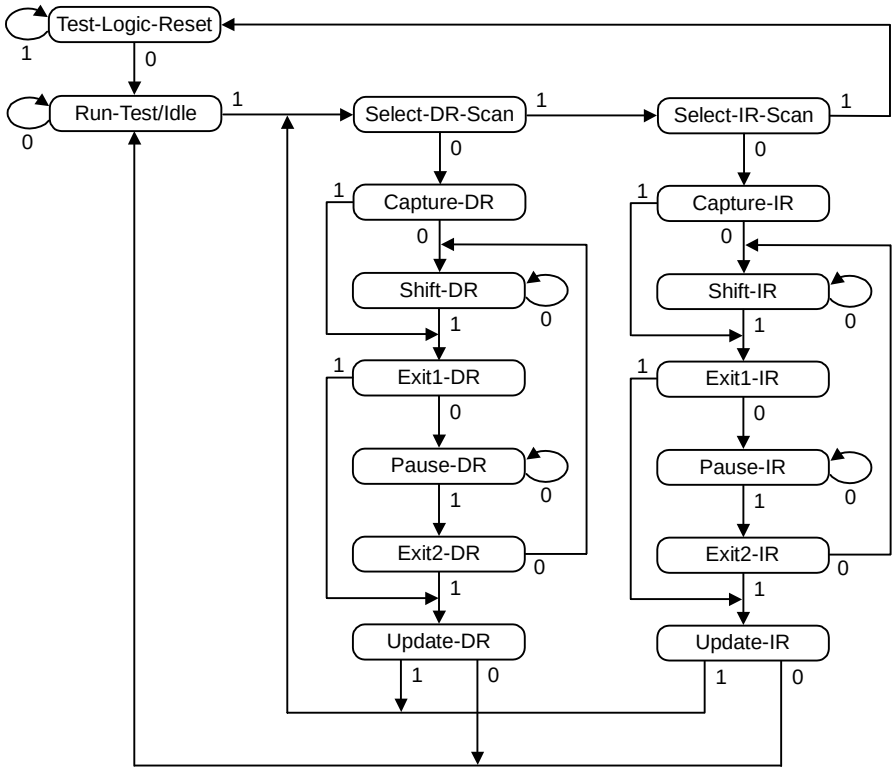
## JTAG TAP BLOCK DIAGRAM



## BOUNDARY SCAN ORDER

| Bit | Bump | Pin Name | Bit | Bump | Pin Name | Bit | Bump | Pin Name |
|---|---|---|---|---|---|---|---|---|
| 0 | 6H | EP3 | 27 | 10C | DQb | 54 | 1G | DQc |
| 1 | 6G | EP2 | 28 | 11C | DQb | 55 | 2G | DQc |
| 2 | 6N | MCH | 29 | 10B | DQb | 56 | 1H | DQc |
| 3 | 6F | ZQ | 30 | 11B | DQb | 57 | 2H | DQc |
| 4 | 5V | A16 | 31 | 10A | DQb | 58 | 1J | DQc |
| 5 | 6U | A15 | 32 | 11A | DQb | 59 | 2J | DQc |
| 6 | 8U | A11 | 33 | 9A | A9 | 60 | 2K | CQ2# |
| 7 | 7V | A13 | 34 | 7A | A8 | 61 | 6L | MCH |
| 8 | 7W | A14 | 35 | 7B | A17 | 62 | 6M | MCL |
| 9 | 8V | A12 | 36 | 5B | A18 | 63 | 1K | CQ2 |
| 10 | 9V | A10 | 37 | 6A | ADV | 64 | 1R | DQPd |
| 11 | 10R | DQPa | 38 | 6D | MCL | 65 | 2T | DQd |
| 12 | 11P | DQa | 39 | 6K | MCL | 66 | 1T | DQd |
| 13 | 10P | DQa | 40 | 6B | W# | 67 | 2U | DQd |
| 14 | 11N | DQa | 41 | 3K | CLK | 68 | 1U | DQd |
| 15 | 10N | DQa | 42 | 8A | E3 | 69 | 2V | DQd |
| 16 | 11M | DQa | 43 | 9C | BWa# | 70 | 1V | DQd |
| 17 | 10M | DQa | 44 | 8B | BWB# | 71 | 2W | DQd |
| 18 | 11L | DQa | 45 | 3B | BWc# | 72 | 1W | DQd |
| 19 | 10L | DQa | 46 | 4C | BWd# | 73 | 6T | LBO# |
| 20 | 11K | CQ1 | 47 | 4A | E2 | 74 | 3V | A5 |
| 21 | 6P | MCL | 48 | 6C | E1# | 75 | 4V | A4 |
| 22 | 6J | MCH | 49 | 5A | A7 | 76 | 4U | A3 |
| 23 | 10K | CQ1# | 50 | 3A | A6 | 77 | 5W | A2 |
| 24 | 11E | DQPb | 51 | 2E | DQPc | 78 | 6V | A1 |
| 25 | 10D | DQb | 52 | 1F | DQc | 79 | 6W | A0 |
| 26 | 11D | DQb | 53 | 2F | DQc | | | |

## JTAG TAP CONTROLLER STATE DIAGRAM




## TAP CONTROLLER DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, $V_{DD}$=1.70~1.95V, unless otherwise noted)

| Symbol | Parameter | Condition | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IHT}$ | Test Port Input High Voltage | | 0.65*$V_{DDQ}$ | $V_{DDQ}$+0.3 ** | V |
| $V_{ILT}$ | Test Port Input Low Voltage | | -0.3 ** | 0.35*$V_{DDQ}$ | V |
| $V_{OHT}$ | Test Port Output High Voltage | $I_{OH}$=-100µA | $V_{DDQ}$-0.1 | - | V |
| $V_{OLT}$ | Test Port Output Low Voltage | $I_{OL}$=+100µA | - | 0.1 | V |
| $I_{INT}$ | TMS, TCK and TDI Input Leakage Current | | -10 | 10 | µA |
| $I_{OLT}$ | TDO Output Leakage Current | Output Disable, $V_{OUT}$=0V~$V_{DDQ}$ | -10 | 10 | µA |

Note37. **Input Undershoot/Overshoot voltage must be –1.0V<Vi<$V_{DDQ}$+1V(max. 3.6V) with a pulse width not to exceed 20% tTCK.

**TAP CONTROLLER AC ELECTRICAL CHARACTERISTICS** (Ta=0~70°C, $V_{DD}$=1.70~1.95V, unless otherwise noted)

**(1)MEASUREMENT CONDITION**

Input pulse levels ····· $V_{IH}=V_{DDQ}$, $V_{IL}$=0V
Input rise and fall times ····· faster than or equal to 1V/ns
Input timing reference levels ····· $V_{IH}=V_{IL}=V_{DDQ}$ / 2
Output reference levels ····· $V_{IH}=V_{IL}=V_{DDQ}$ / 2
Output load ····· Fig.4

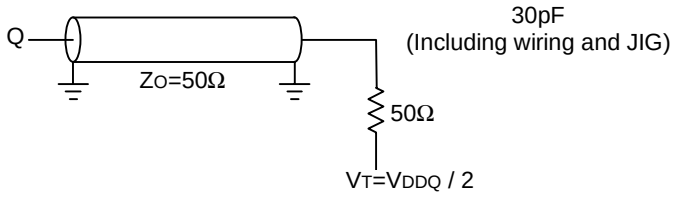
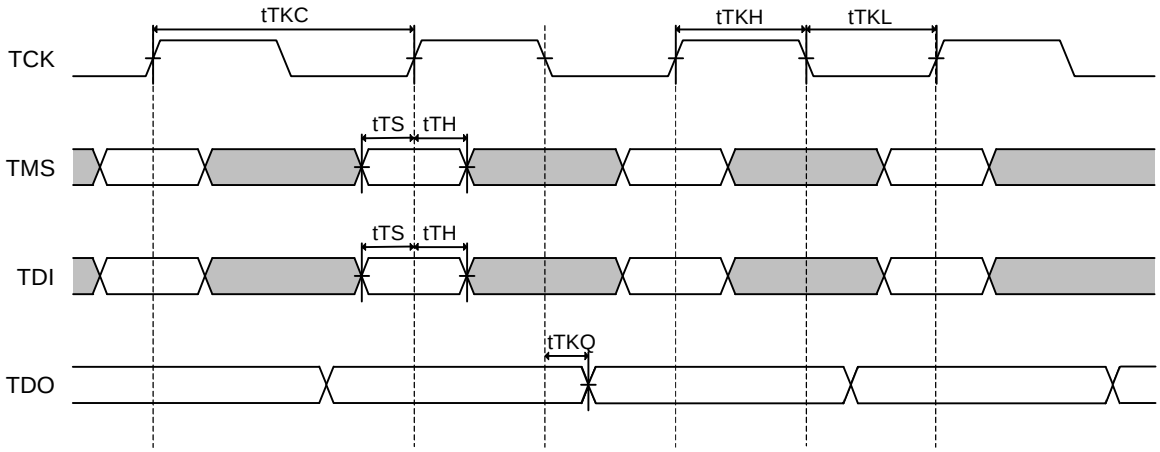



Fig.4 Output load

**(2)TIMING CHARACTERISTICS**

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| tTF | TCK Frequency | | 20 | MHz |
| tTKC | TCK Cycle Time | 50 | | ns |
| tTKH | TCK High Pulse Width | 20 | | ns |
| tTKL | TCK Low Pulse Width | 20 | | ns |
| tTS | TDI, TMS setup time | 10 | | ns |
| tTH | TDI, TMS hold time | 10 | | ns |
| tTKQ | TCK Low to TDO valid | | 20 | ns |

**(3) TIMING**



## JTAG TAP INSTRUCTION SET SUMMARY

| Instruction | Code | Description |
|---|---|---|
| EXTEST-A | 000 | Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. This SRAM implements an Clock Assisted EXTEST function. Not 1149.1 Compliant. |
| IDCODE | 001 | Preloads ID Register and places it between TDI and TDO |
| SAMPLE-Z | 010 | Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all Data and Clock output drivers to High-Z |
| RFU | 011 | Do not use this instruction; Reserved for Future Use. |
| SAMPLE/PRELOAD | 100 | Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. |
| RFU | 101 | Do not use this instruction; Reserved for Future Use. |
| RFU | 110 | Do not use this instruction; Reserved for Future Use. |
| BYPASS | 111 | Places the BYPASS Register between TDI and TDO. |

## STRUCTURE OF IDENTIFICATION REGISTER

| | Revision | | | | Device Information | | | | | | | | | | | | | | | | JEDEC Vendor Code of MITSUBISHI | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{DD}$ | | | Capacity | | | | Function | | | | Width | | | Gen. | | | | | | | | | | | | | |
| Bit No. | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| M5M5Y5636 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |

MSB LSB

Note38. Bit of Device Information “Gen.(Generation)” means

| Bit No. | 13 | 12 |
|---|---|---|
| 1st Generation | 0 | 0 |
| 2nd Generation | 0 | 1 |
| 3rd Generation | 1 | 0 |

Note39. Bit of Device Information ”Width” means

| Bit No. | 16 | 15 | 14 |
|---|---|---|---|
| X16 | 0 | 0 | 0 |
| X18 | 0 | 0 | 1 |
| X32 | 0 | 1 | 0 |
| X36 | 0 | 1 | 1 |
| X64 | 1 | 0 | 0 |
| X72 | 1 | 0 | 1 |

Note40. Bit of Device Information ”Function” means

| Bit No. | 20 | 19 | 18 | 17 |
|---|---|---|---|---|
| Network SRAM | 0 | 1 | 0 | 0 |
| PB | 0 | 0 | 0 | 1 |

Note41. Bit of Device Information ”Capacity” means

| Bit No. | 24 | 23 | 22 | 21 |
|---|---|---|---|---|
| 1M or 1.15M | 0 | 0 | 0 | 1 |
| 2M or 2.3M | 0 | 0 | 1 | 0 |
| 4M or 4.5M | 0 | 0 | 1 | 1 |
| 8M or 9M | 0 | 1 | 0 | 0 |
| 16M or 18M | 0 | 1 | 0 | 1 |
| 32M or 36M | 0 | 1 | 1 | 0 |

Note42. Bit of Device Information ”$V_{DD}$” means

| Bit No. | 27 | 26 | 25 |
|---|---|---|---|
| 3.3V | 0 | 0 | 0 |
| 2.5V | 0 | 0 | 1 |
| 1.8V | 0 | 1 | 0 |
| 1.5V | 0 | 1 | 1 |

**PACKAGE OUTLINE**

209(11x19) bump Ball Grid Array(BGA) Pin Pitch 1.0mm

Refer to JEDEC Standard MS-028, Variation BC,

which can be seen at:

http://www.jedec.org/download/search/MS-028C.pdf

**REVISION HISTORY**

| Rev.No. | History | Date | |
|---|---|---|---|
| 0.0 | First revision | June 6, 2001 | Advanced Information |
| 0.1 | AC ELECTRICAL CHARACTERISTICS<br>Changed tKHQV and tKHQZ from 2.6ns to 2.1ns<br>Changed tKHCH, tKLCL and tKHCZ from 2.5ns to 2.0ns<br>Fixed tCHCL, tCLCH and tCHQX | July 13, 2001 | Advanced Information |
| 0.2 | ABSOLUTE MAXIMUM RATINGS<br>Changed $T_{STG}$ from -65~150 to -55~125 | November 15, 2001 | Advanced Information |
| 0.3 | Added Boundary Scan Order | March 28, 2002 | Advanced Information |
| 0.4 | Fixed THERMAL RESISTANCE | July 5, 2002 | Preliminary |
| 0.5 | DC ELECTRICAL CHARACTERISTICS<br>Changed ICC1 limit from 400mA to 470mA at 250MHz(-25)<br>Changed ICC2 limit from 140mA to 160mA at 250MHz(-25)<br>Changed ICC1 limit from 380mA to 450mA at 225MHz(-22)<br>Changed ICC2 limit from 110mA to 150mA at 225MHz(-22)<br>Changed ICC1 limit from 360mA to 420mA at 200MHz(-20)<br>Changed ICC2 limit from 100mA to 140mA at 200MHz(-20) | August 7, 2002 | Preliminary |
| 0.6 | DC ELECTRICAL CHARACTERISTICS<br>Changed ILI limit from 10uA to 100uA<br>(Input Current of ZQ and LBO#)<br>Changed ICC1 limit from 470mA to 550mA at 250MHz(-25)<br>Changed ICC1 limit from 450mA to 500mA at 225MHz(-22)<br>Changed ICC1 limit from 420mA to 450mA at 200MHz(-20) | January 14, 2003 | Preliminary |

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