

To all our customers

---

## **Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.**

---

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

## M5M5J167WG - 70HI

**Preliminary**Notice: This is not a final specification.  
Some parametric limits are subject to change

16777216-BIT (1048576-WORD BY 16-BIT) CMOS STATIC RAM

**DESCRIPTION**

The M5M5J167WG is a family of low voltage 16Mbit static RAMs organized as 1048576-words by 16-bit, fabricated by Mitsubishi's high-performance 0.18 $\mu$ m CMOS technology.

The M5M5J167WG is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

The M5M5J167WG is made by stacked-micro-package technology and two chips of 8Mbits SRAMs are assembled in one package. By using this package technology, small package size can be achieved for highdensity SRAM.

The M5M5J167WG is packaged in a f-BGA (fine pitch BGA), with the outline of 7.5mm x 8.5mm, ball matrix of 6 x 8 (48ball) and ball pitch of 0.75mm. It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

The operating temperature range is -40 ~ +85°C

**FEATURES**

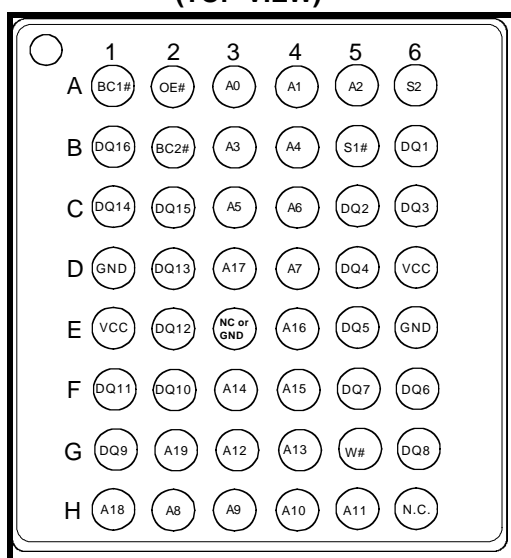
- Single 2.7~3.6V power supply
- Small stand-by current: 0.2 $\mu$ A (2.0V, typ.)
- No clocks, No refresh
- Data retention supply voltage =2.0~3.6V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by S1#, S2, BC1# and BC2#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Process technology: 0.18 $\mu$ m CMOS
- Package: 48ball 7.5mm x 8.5mm f-BGA

Operating temperature	Part name	Power Supply	Access time max.	Stand-by current						Active current Icc1 (3.3V, Typ.)
				* Typical		Ratings (max.)				
				25°C	40°C	25°C	40°C	70°C	85°C	
-40 ~ +85°C	M5M5J167WG -70HI	2.7 ~ 3.6V	70ns	2.0	2.4	10	16	40	80	30mA (10MHz) 5mA (1MHz)

\* Typical parameter indicates the value for the center of distribution, and not 100% tested.

**PIN CONFIGURATION**

(TOP VIEW)



outline : 48FHH

NC : No Connection

\*Don't connect E3 ball to voltage level more than 0V.

Pin	Function
A0 ~ A19	Address input
DQ1 ~ DQ16	Data input / output
S1#	Chip select input 1
S2	Chip select input 2
W#	Write control input
OE#	Output enable input
BC1#	Lower Byte (DQ1 ~ 8)
BC2#	Upper Byte (DQ9 ~ 16)
Vcc	Power supply
GND	Ground supply

## M5M5J167WG - 70HI

**Preliminary**

Notice: This is not a final specification.  
Some parametric limits are subject to change

16777216-BIT (1048576-WORD BY 16-BIT) CMOS STATIC RAM

**FUNCTION**

The M5M5J167WG is organized as 1048576-words by 16-bit. These devices operate on a single +2.7~3.6V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

The operation mode are determined by a combination of the device control inputs BC1# , BC2# , S1# , S2 , W#, and OE#. Each mode is summarized in the function table. A write operation is executed whenever the low level W# overlaps with the low level BC1# and/or BC2# and the low level S1# and the high level S2. The address (A0~A19) must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting W# at a high level and OE# at a low level while BC1# and/or BC2# and S1#and S2 are in an active state (S1#=L, S2=H).

When setting BC1# and BC2# at a high level or S1# at a high level or S2 at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by BC1#, BC2# and S1#, S2.

The power supply current is reduced as low as 0.2μA (25°C, typical), and the memory data can be held at +2.0V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

**FUNCTION TABLE**

S1#	S2	BC1#	BC2#	W#	OE#	Mode	DQ1~8	DQ9~16	Icc
H	H	X	X	X	X	Non selection	High-Z	High-Z	Standby
X	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
X	X	H	H	X	X	Non selection	High-Z	High-Z	Standby
L	H	L	H	L	X	Write	Din	High-Z	Active
L	H	L	H	H	L	Read	Dout	High-Z	Active
L	H	L	H	H	H	————	High-Z	High-Z	Active
L	H	H	L	L	X	Write	High-Z	Din	Active
L	H	H	L	H	L	Read	High-Z	Dout	Active
L	H	H	L	H	H	————	High-Z	High-Z	Active
L	H	L	L	L	X	Write	Din	Din	Active
L	H	L	L	H	L	Read	Dout	Dout	Active
L	H	L	L	H	H	————	High-Z	High-Z	Active

Note1: "H" and "L" in this table mean V<sub>IH</sub> and V<sub>IL</sub>, respectively.

Note2: "X" in this table should be "H" or "L".

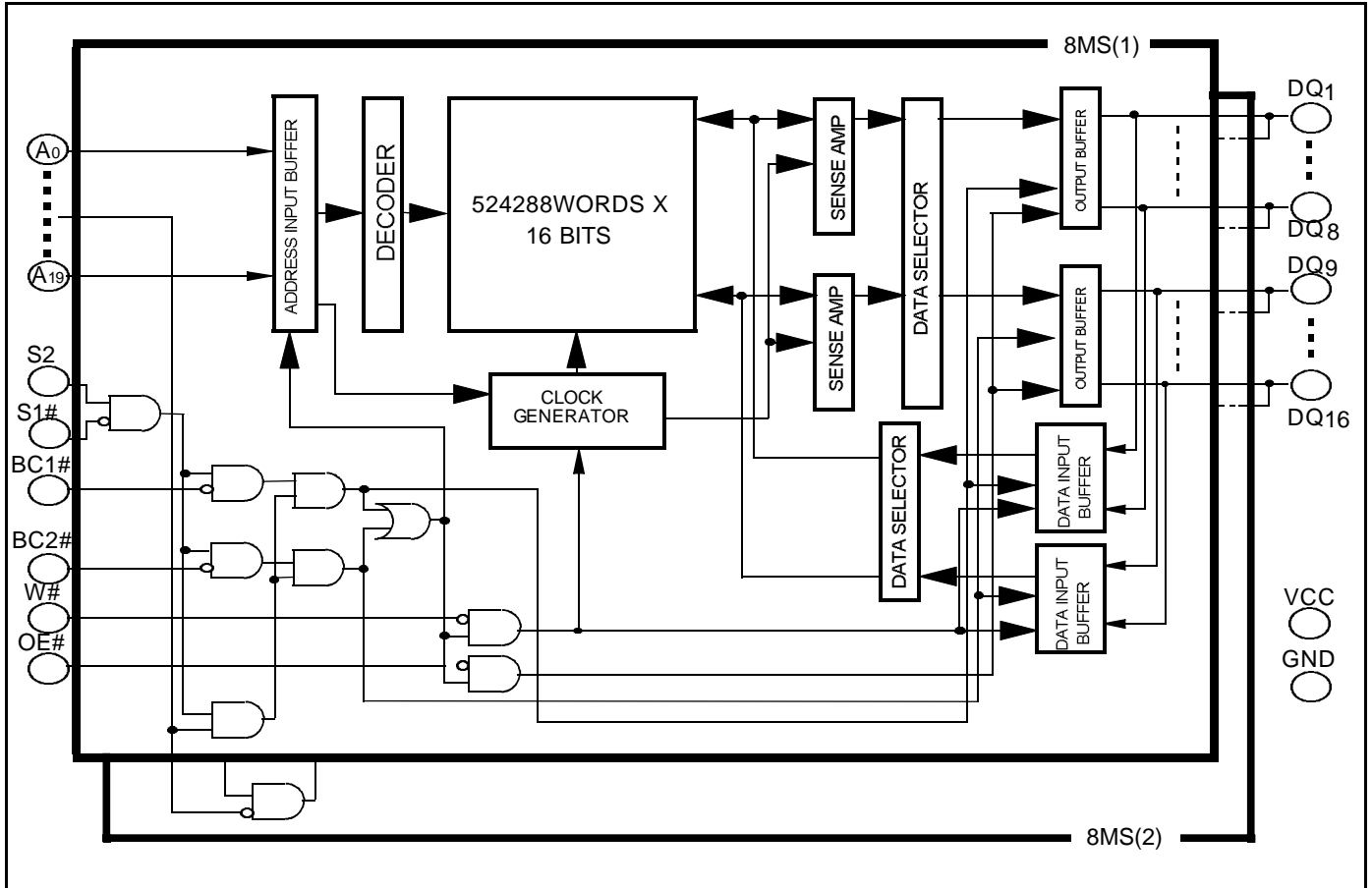
# M5M5J167WG - 70HI

## Preliminary

Notice: This is not a final specification.  
Some parametric limits are subject to change

16777216-BIT (1048576-WORD BY 16-BIT) CMOS STATIC RAM

### BLOCK DIAGRAM



## M5M5J167WG - 70HI

**Preliminary**Notice: This is not a final specification.  
Some parametric limits are subject to change

16777216-BIT (1048576-WORD BY 16-BIT) CMOS STATIC RAM

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Units
V <sub>CC</sub>	Supply voltage	With respect to GND	- 0.3* ~ +4.6	V
V <sub>I</sub>	Input voltage	With respect to GND	- 0.3* ~ V <sub>CC</sub> + 0.3 (max. 4.6V)	
V <sub>O</sub>	Output voltage	With respect to GND	0 ~ V <sub>CC</sub>	
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25°C	700	mW
T <sub>a</sub>	Operating temperature		-40 ~ +85	°C
T <sub>stg</sub>	Storage temperature		- 65 ~ +150	°C

\* -3.0V in case of AC (Pulse width ≤ 30ns)

**DC ELECTRICAL CHARACTERISTICS** (T<sub>a</sub>=-40~85°C V<sub>CC</sub>=2.7V~3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units	
			Min	Typ	Max		
V <sub>IH</sub>	High-level input voltage		2.2		V <sub>CC</sub> +0.2V	V	
V <sub>IL</sub>	Low-level input voltage		- 0.2*		0.6		
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = - 0.5mA	2.4				
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 2.0mA			0.4		
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = 0 ~ V <sub>CC</sub>			±1	μA	
I <sub>O</sub>	Output leakage current	BC1# and BC2# = V <sub>IH</sub> or S1# = V <sub>IH</sub> or S2 = V <sub>IL</sub> or OE# = V <sub>IH</sub> , V <sub>I/O</sub> = 0 ~ V <sub>CC</sub>			±1		
I <sub>CC1</sub>	Active supply current (AC, MOS level)	BC1# and BC2# ≤ 0.2V, S1# ≤ 0.2V, S2 ≥ V <sub>CC</sub> -0.2V other inputs ≤ 0.2V or ≥ V <sub>CC</sub> -0.2V Output - open (duty 100%)	f = 10MHz f = 1MHz	- -	30 5	50 15	mA
I <sub>CC2</sub>	Active supply current (AC, TTL level)	BC1# and BC2# = V <sub>IL</sub> , S1# = V <sub>IL</sub> , S2 = V <sub>IH</sub> other pins = V <sub>IH</sub> or V <sub>IL</sub> Output - open (duty 100%)	f = 10MHz f = 1MHz	- -	30 5	50 15	
I <sub>CC3</sub>	Stand by supply current (AC, MOS level)	(1) S1# ≥ V <sub>CC</sub> - 0.2V and S2 ≥ V <sub>CC</sub> - 0.2V, other inputs = 0 ~ V <sub>CC</sub> (2) S2 ≤ 0.2V, other inputs = 0 ~ V <sub>CC</sub> (3) BC1# and BC2# ≥ V <sub>CC</sub> - 0.2V S1# ≤ 0.2V, S2 ≥ V <sub>CC</sub> - 0.2V other inputs = 0 ~ V <sub>CC</sub>	~ +25°C	-	2.0	10	μA
			~ +40°C	-	2.4	16	
			~ +70°C	-	-	40	
			~ +85°C	-	-	80	
I <sub>CC4</sub>	Stand by supply current (AC, TTL level)	BC1# and BC2# = V <sub>IH</sub> or S1# = V <sub>IH</sub> or S2 = V <sub>IL</sub> Other inputs = 0 ~ V <sub>CC</sub>		-	-	2.0	mA

Note 3: Direction for current flowing into IC is indicated as positive (no mark)

\* -1.0V in case of AC (Pulse width ≤ 30ns)

Note 4: Typical parameter indicates the value for the center of distribution at 3.0V, and not 100% tested.

**CAPACITANCE** (T<sub>a</sub>=-40~+85°C V<sub>CC</sub>=2.7V~3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
C <sub>I</sub>	Input capacitance	V <sub>I</sub> =GND, V <sub>I</sub> =25mVrms, f=1MHz			20	pF
C <sub>O</sub>	Output capacitance	V <sub>O</sub> =GND, V <sub>O</sub> =25mVrms, f=1MHz			20	

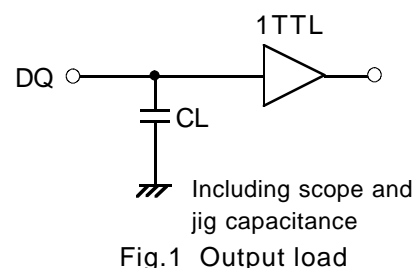
## M5M5J167WG - 70HI

**Preliminary**Notice: This is not a final specification.  
Some parametric limits are subject to change

16777216-BIT (1048576-WORD BY 16-BIT) CMOS STATIC RAM

**AC ELECTRICAL CHARACTERISTICS** ( $T_a=-40\sim+85^\circ\text{C}$ ,  $V_{cc}=2.7\text{V}\sim 3.6\text{V}$ , unless otherwise noted)**(1) TEST CONDITIONS**

Supply voltage	2.7~3.6V
Input pulse	$V_{IH}=2.7\text{V}$ , $V_{IL}=0.2\text{V}$
Input rise time and fall time	5ns
Reference level	$V_{OH}=V_{OL}=1.5\text{V}$ Transition is measured $\pm 200\text{mV}$ from steady state voltage.(for $t_{en}$ , $t_{dis}$ )
Output loads	Fig.1, $CL=30\text{pF}$ $CL=5\text{pF}$ (for $t_{en}$ , $t_{dis}$ )

**(2) READ CYCLE**

Symbol	Parameter	Limits		Units
		70HI		
		Min	Max	
$t_{CR}$	Read cycle time	70		ns
$t_{a(A)}$	Address access time		70	ns
$t_{a(S1)}$	Chip select 1 access time		70	ns
$t_{a(S2)}$	Chip select 2 access time		70	ns
$t_{a(BC1)}$	Byte control 1 access time		70	ns
$t_{a(BC2)}$	Byte control 2 access time		70	ns
$t_{a(OE)}$	Output enable access time		35	ns
$t_{dis(S1)}$	Output disable time after S1# high		25	ns
$t_{dis(S2)}$	Output disable time after S2 low		25	ns
$t_{dis(BC1)}$	Output disable time after BC1# high		25	ns
$t_{dis(BC2)}$	Output disable time after BC2# high		25	ns
$t_{dis(OE)}$	Output disable time after OE# high		25	ns
$t_{en(S1)}$	Output enable time after S1# low	10		ns
$t_{en(S2)}$	Output enable time after S2 high	10		ns
$t_{en(BC1)}$	Output enable time after BC1# low	5		ns
$t_{en(BC2)}$	Output enable time after BC2# low	5		ns
$t_{en(OE)}$	Output enable time after OE# low	5		ns
$t_{v(A)}$	Data valid time after address	10		ns

**(3) WRITE CYCLE**

Symbol	Parameter	Limits		Units
		70HI		
		Min	Max	
$t_{CW}$	Write cycle time	70		ns
$t_{w(W)}$	Write pulse width	55		ns
$t_{su(A)}$	Address setup time	0		ns
$t_{su(A-WH)}$	Address setup time with respect to W#	65		ns
$t_{su(BC1)}$	Byte control 1 setup time	65		ns
$t_{su(BC2)}$	Byte control 2 setup time	65		ns
$t_{su(S1)}$	Chip select 1 setup time	65		ns
$t_{su(S2)}$	Chip select 2 setup time	65		ns
$t_{su(D)}$	Data setup time	35		ns
$t_{h(D)}$	Data hold time	0		ns
$t_{rec(W)}$	Write recovery time	0		ns
$t_{dis(W)}$	Output disable time from W# low		25	ns
$t_{dis(OE)}$	Output disable time from OE# high		25	ns
$t_{en(W)}$	Output enable time from W# high	5		ns
$t_{en(OE)}$	Output enable time from OE# low	5		ns

M5M5J167WG - 70HI

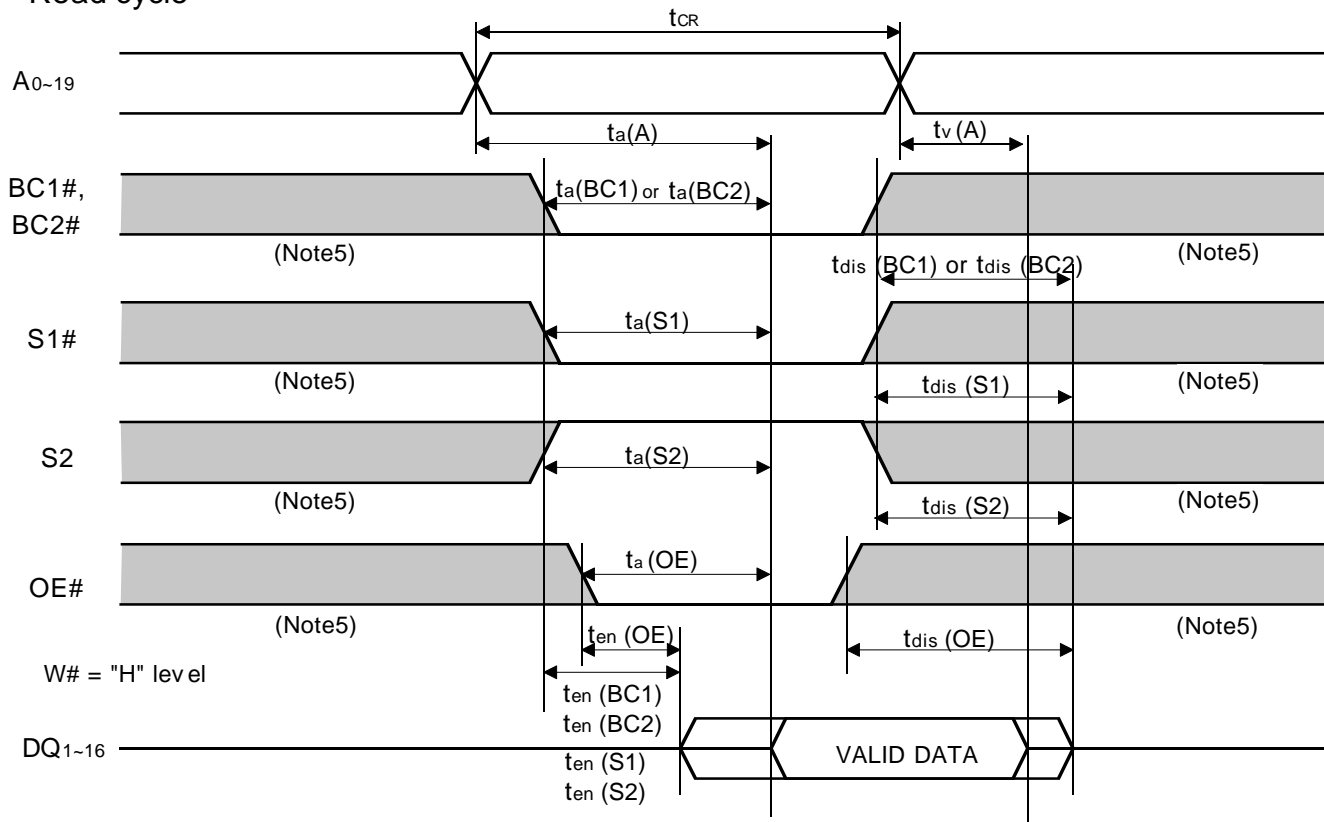
**Preliminary**

Notice: This is not a final specification.  
Some parametric limits are subject to change

16777216-BIT (1048576-WORD BY 16-BIT) CMOS STATIC RAM

(4) TIMING DIAGRAMS

Read cycle



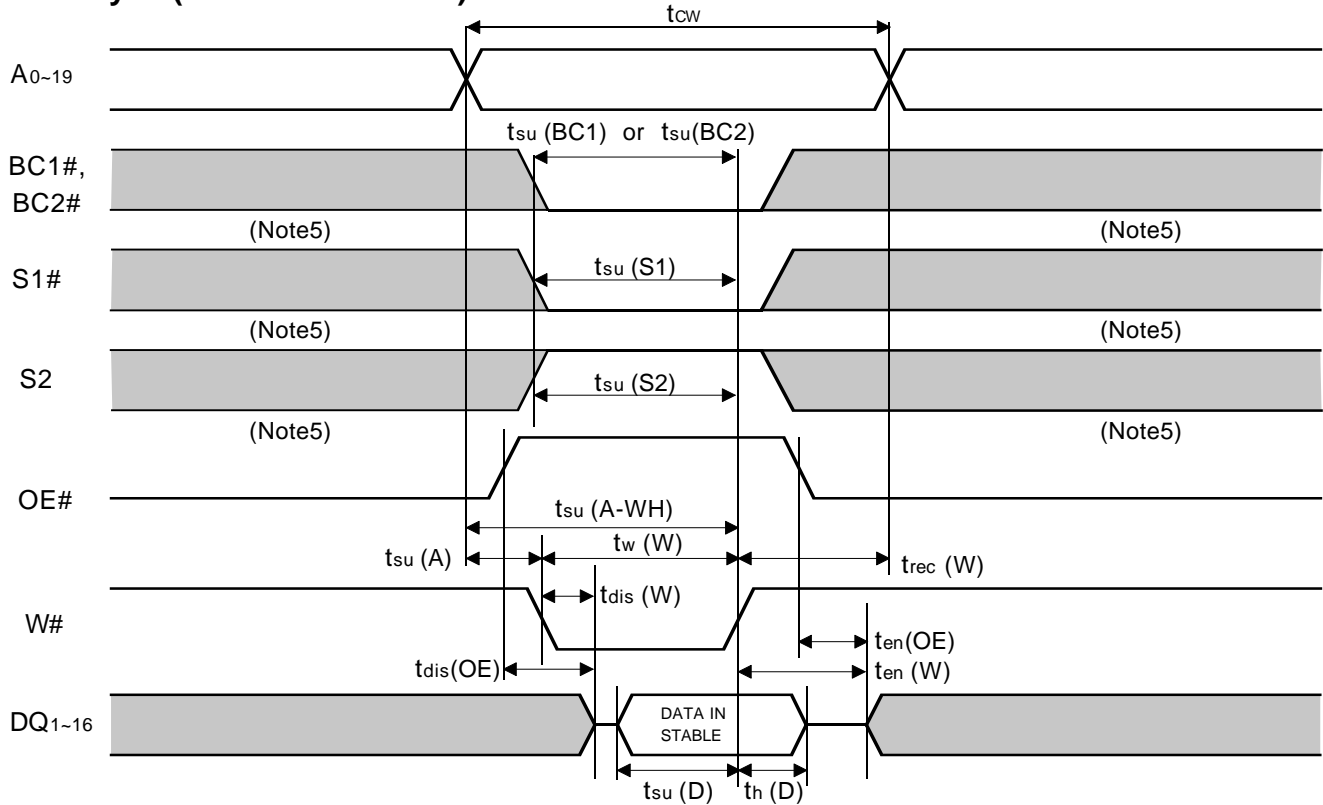
M5M5J167WG - 70HI

**Preliminary**

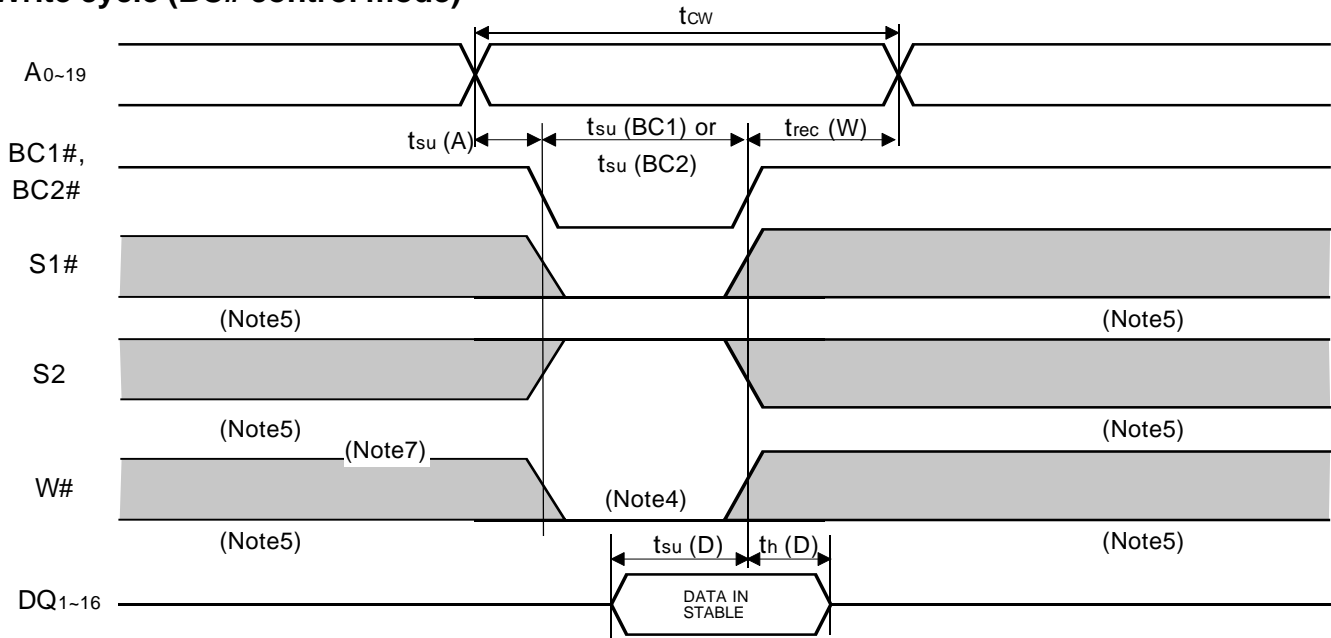
Notice: This is not a final specification.  
Some parametric limits are subject to change

16777216-BIT (1048576-WORD BY 16-BIT) CMOS STATIC RAM

**Write cycle( W# control mode )**



**Write cycle (BC# control mode)**



Note 5: Hatching indicates the state is "don't care".

Note 6: A Write occurs during S1# low, S2 high overlaps BC1# and/or BC2# low and W# low.

Note 7: When the falling edge of W# is simultaneously or prior to the falling edge of BC1# and/or BC2# or the falling edge of S1# or rising edge of S2, the outputs are maintained in the high impedance state.

Note 8: Don't apply inverted phase signal externally when DQ pin is in output mode.



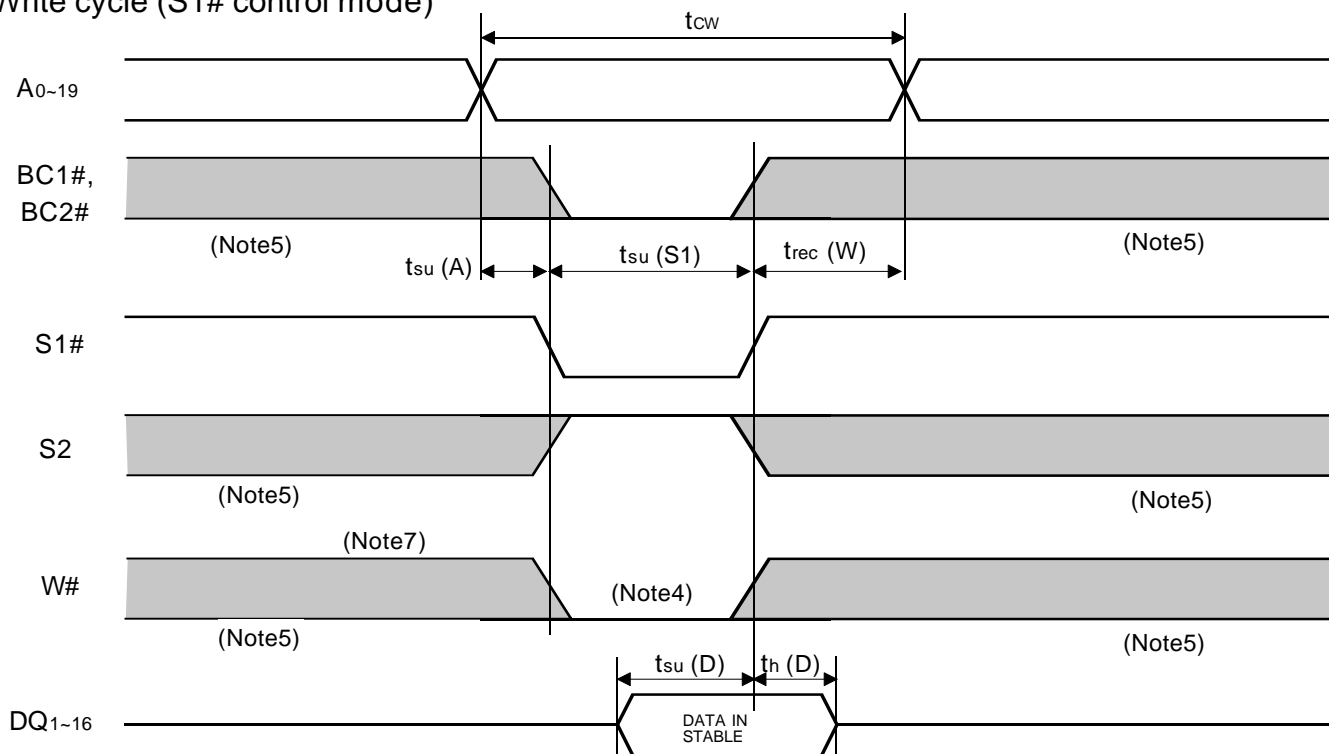
M5M5J167WG - 70HI

**Preliminary**

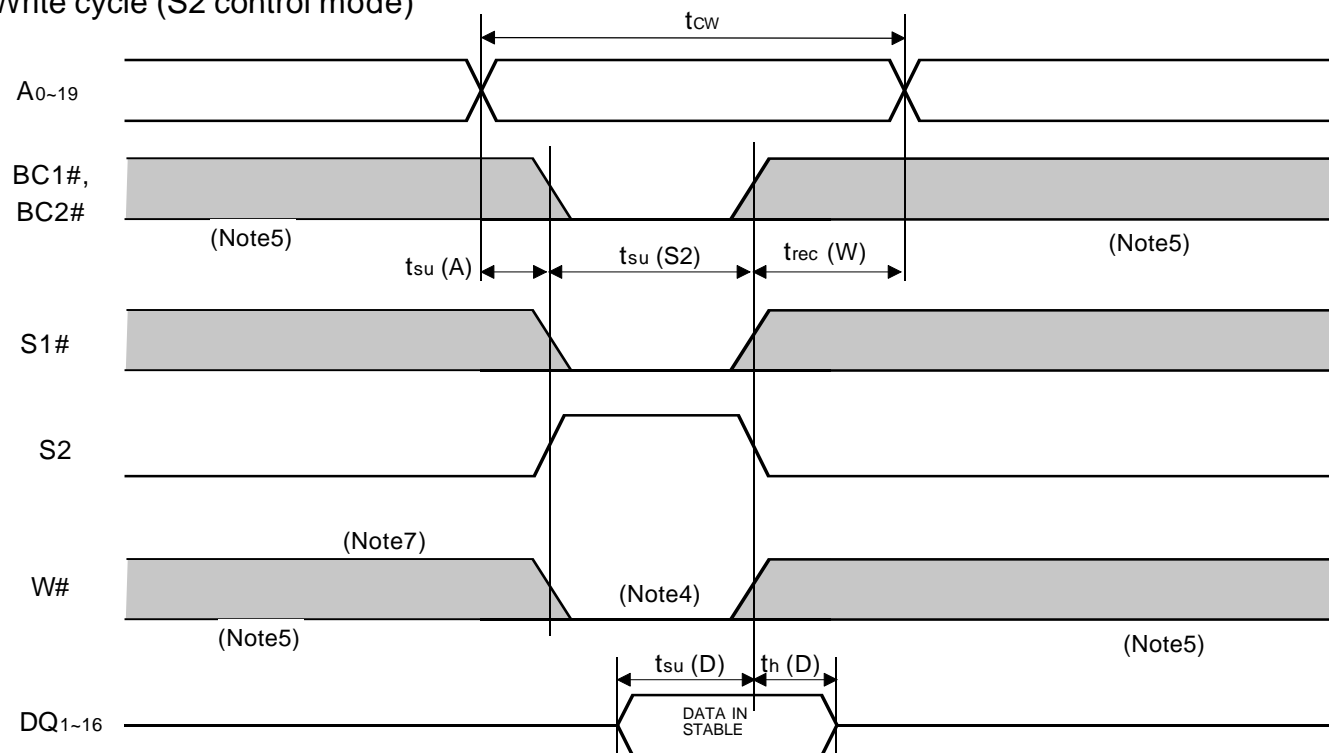
Notice: This is not a final specification.  
Some parametric limits are subject to change

16777216-BIT (1048576-WORD BY 16-BIT) CMOS STATIC RAM

Write cycle (S1# control mode)



Write cycle (S2 control mode)



# M5M5J167WG - 70HI

**Preliminary**

Notice: This is not a final specification.  
Some parametric limits are subject to change

16777216-BIT (1048576-WORD BY 16-BIT) CMOS STATIC RAM

## POWER DOWN CHARACTERISTICS

### (1) ELECTRICAL CHARACTERISTICS (Ta=-40~85°C, Vcc=2.7V~3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Units	
			Min	Typ	Max		
V <sub>CC</sub> (PD)	Power down supply voltage		2.0			V	
V <sub>I</sub> (BC)	Byte control input BC1# & BC2#		2.0			V	
V <sub>I</sub> (S1#)	Chip select input S1#		2.0			V	
V <sub>I</sub> (S2)	Chip select input S2				0.2		
I <sub>CC</sub> (PD)	Power down supply current	<b>V<sub>CC</sub>=2.0V</b> (1) S1# ≥ V <sub>CC</sub> - 0.2V, other inputs = 0 - V <sub>CC</sub> (2) S2 ≤ 0.2V, other inputs = 0 - V <sub>CC</sub> (3) BC1# and BC2# ≥ V <sub>CC</sub> - 0.2V, S1# ≤ 0.2V, S2 ≥ V <sub>CC</sub> - 0.2V, other inputs = 0 - V <sub>CC</sub>	~ +25°C	-	0.2	3.0	μA
			~ +40°C	-	0.4	6.0	
			~ +70°C	-	-	30	
			~ +85°C	-	-	60	

Note 9: Typical parameter of I<sub>CC</sub>(PD) indicates the value for the center of distribution at 2.0V, and not 100% tested.

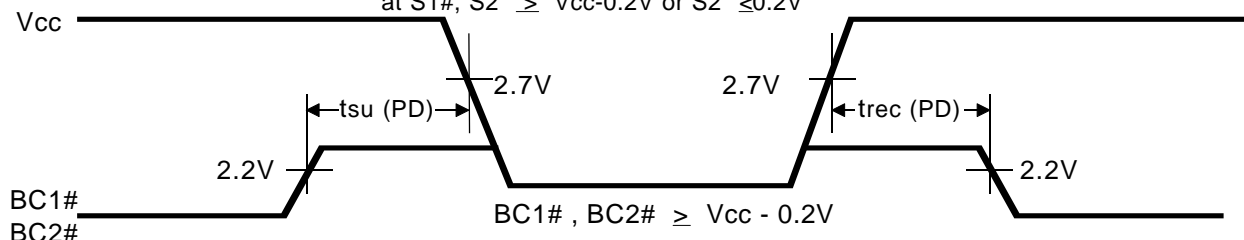
### (2) TIMING REQUIREMENTS

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
t <sub>SU</sub> (PD)	Power down set up time		0			ns
t <sub>REC</sub> (PD)	Power down recovery time		5			ms

### (3) TIMING DIAGRAM

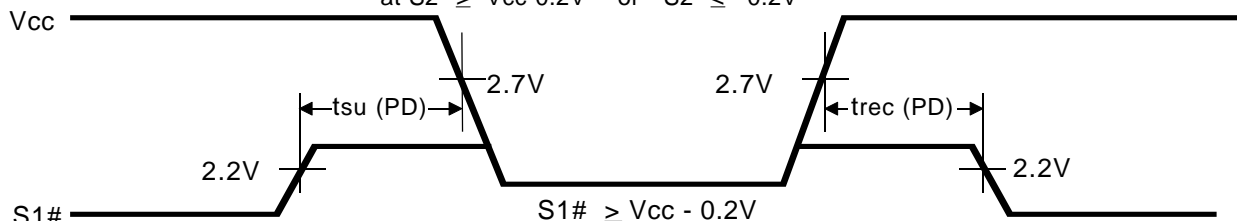
#### BC# control mode

note10: On the BC# control mode, the level of S1# and S2 must be fixed at S1#, S2 ≥ V<sub>CC</sub>-0.2V or S2 ≤ 0.2V

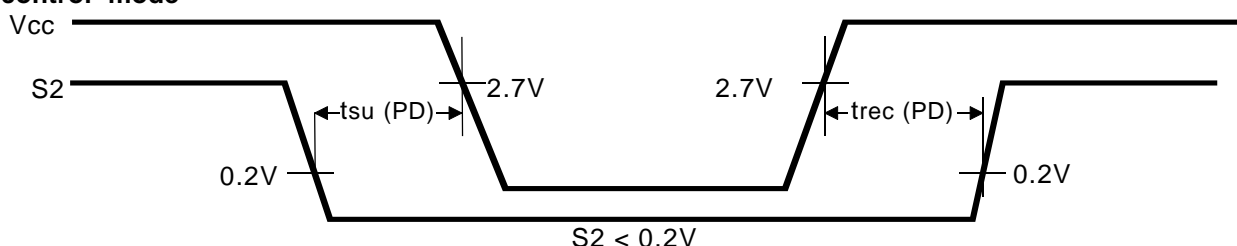


#### S1# control mode

note11: On the S1# control mode, the level of S2 must be fixed at S2 ≥ V<sub>CC</sub>-0.2V or S2 ≤ 0.2V



#### S2 control mode



# M5M5J167WG - 70HI

## **Preliminary**

Notice: This is not a final specification.  
Some parametric limits are subject to change

16777216-BIT (1048576-WORD BY 16-BIT) CMOS STATIC RAM

---

### **Keep safety first in your circuit designs!**

Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

### **Notes regarding these materials**

These materials are intended as a reference to assist our customers in the selection of the Mitsubishi semiconductor product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Mitsubishi Electric Corporation or a third party.

Mitsubishi Electric Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.

All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Mitsubishi Electric Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for the latest product information before purchasing a product listed herein.

The information described here may contain technical inaccuracies or typographical errors. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability, or other loss arising from these inaccuracies or errors.

Please also pay attention to information published by Mitsubishi Electric Corporation by various means, including the Mitsubishi Semiconductor home page (<http://www.mitsubishichips.com>).

When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.

Mitsubishi Electric Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.

The prior written approval of Mitsubishi Electric Corporation is necessary to reprint or reproduce in whole or in part these materials.

If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination. Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.

Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for further details on these materials or the products contained therein.