

M6MGD137W33TP

134,217,728-BIT (8,388,608-WORD BY 16-BIT) CMOS FLASH MEMORY &
 33,554,432-BIT (2,097,152-WORD BY 16-BIT) CMOS Mobile RAM
 Stacked- μ MCP (micro Multi Chip Package)

DESCRIPTION

The M6MGD137W33TP is a Stacked micro Multi Chip Package (S- μ MCP) that contents 128M-bit Flash memory and 32M-bit Mobile RAM in a 52-pin TSOP.

128M-bit Flash memory is a 8,388,608 words, single power supply and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR IV (Divided bit-line NOR IV) architecture for the memory cell. All memory blocks are locked and can not be programmed or erased, when F-WP# is Low. Using Software Lock Release function, program or erase operation can be executed.

32M-bit Mobile RAM is a 2,097,152 words high density RAM fabricated by CMOS technology for the peripheral circuit and DRAM cell for the memory array. The interface is compatible to an asynchronous SRAM.

The cells are automatically refreshed and the refresh control is not required for system. The device also has the partial block refresh scheme and the power down mode by writing the command.

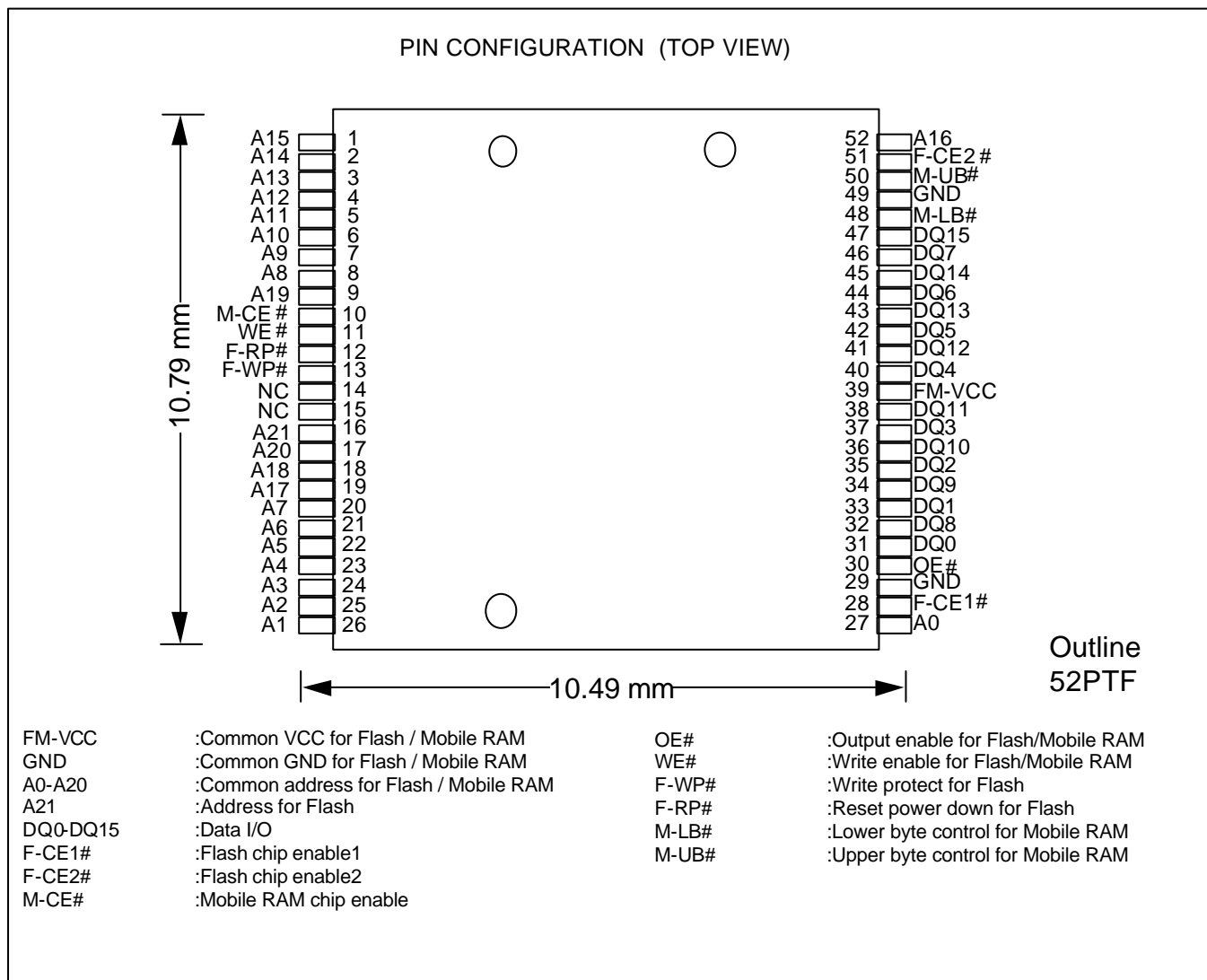
The M6MGD137W33TP is suitable for a high performance cellular phone and a mobile PC that are required to be small mounting area, weight and small power dissipation.

FEATURES

Access time	Flash	85ns (Max.)
	Mobile RAM	85ns (Max.)
Supply voltage		FM-VCC = 2.7 ~ 3.0V
Ambient temperature		Ta=-40 ~ 85 °C
Package		52pin TSOP(Type-II), Lead pitch 0.4mm

APPLICATION

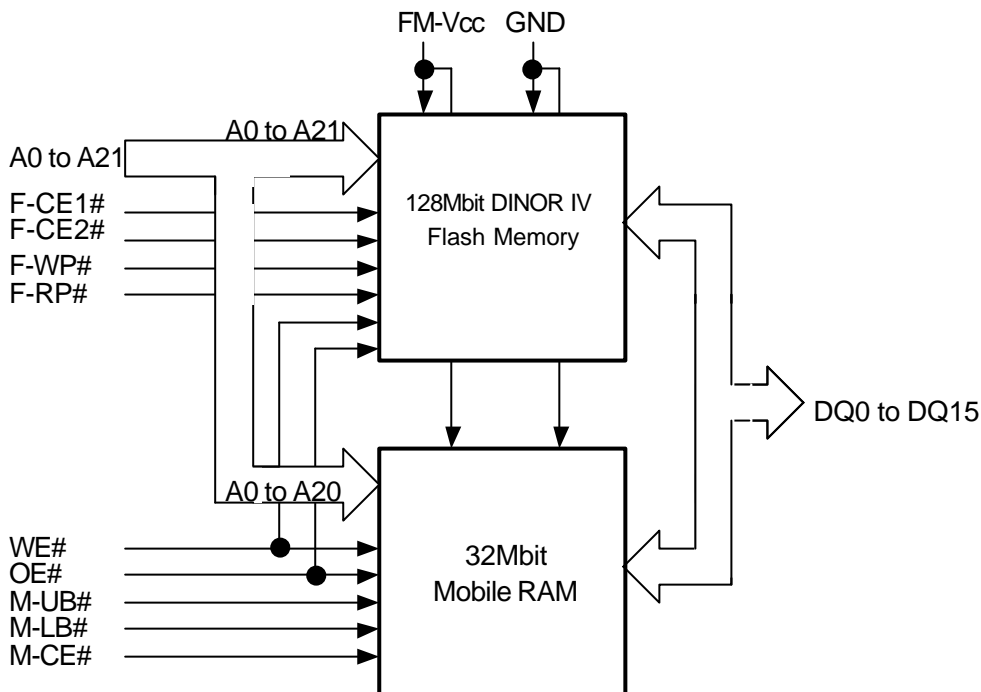
Mobile communication products



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MCP Block Diagram



Note: In the data sheet there are "VCC"s which mean "FM-VCC" (Common Vcc for Flash / Mobile RAM).

Capacitance

Symbol	Parameter		Conditions	Limits			Unit
				Min.	Typ.	Max.	
CIN	Input capacitance	A21-A0, OE#, WE#, F-WP#, F-RP#, M-CE#, M-LB#, M-UB#, F-CE1#, F-CE2#	Ta=25°C, f=1MHz, Vin=Vout=0V			26	pF
							pF
							pF
							pF
COUT	Output Capacitance	DQ15-DQ0			34	pF	

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Stacked- mMCP (micro Multi Chip Package)**

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