HN29V128A1A (3.3 V/×8)
HN29V128A0A (3.3 V/×16)
HN29A128A1A (1.8 V/×8)
HN29A128A0A (1.8 V/×16)

128M superAND Flash Memory
(with internal sector management)

REJ03C0031-0200Z
Rev. 2.00
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Description

The HN29V128A1A, HN29V128A0A, HN29A128A1A, and HN29A128A0A Series is a CMOS flash memory, which uses cost effective and high performance AND type multi-level memory cell technology. Current AND flash memory requires us to support complicated operations such as sector management for defect sector and error check correction. But this series doesn't need such operations. Beside it supports wear leveling function, which is sector replacement function in case of that certain sector, reaches certain erase/write times. And power-on-auto-read function is available. It enables to read the data of the lowest sector(2k byte) without command and address data input when power is on.

Note: This product is authorized for using consumer application such as cellular phone,
Therefore, please contact Renesas Technology's sales office before using other applications.

Features

- On-board single power supply (V_{CC}): V_{CC} = 2.7 V to 3.6 V (HN29V128A1A/HN29V128A0A)
  : V_{CC} = 1.70 V to 1.95 V (HN29A128A1A/HN29A128A0A)
- Operating temperature range: Ta = 0 to +70 °C
- Program/erase, rewrite endurance
  —10^5 times
- Access time
  —First access
    80 µs (typ) (3.3 V, ×8/×16)
    150 µs (typ) (1.8 V, ×8/×16)
  —Serial read cycle
    50 ns (min) (3.3 V, ×8/×16)
    100 ns (min) (1.8 V, ×8/×16)
  —maximum transfer rate (sequential read)
    20.0 Mbyte/s (3.3 V, ×8)
    40.0 Mbyte/s (3.3 V, ×16)
    10.0 Mbyte/s (1.8 V, ×8)
    20.0 Mbyte/s (1.8 V, ×16)
- Program time
    1.2 ms (typ) /sector (2048 byte) (3.3 V, ×8/×16)
    2.0 ms (typ) /sector (2048 byte) (1.8 V, ×8/×16)
- Erase time
    2.2 ms (typ) /sector (2048 byte) (3.3 V, ×8/×16)
    3.5 ms (typ) /sector (2048 byte) (1.8 V, ×8/×16)
- Rewrite time
    2.2 ms (typ) /sector (2048 byte) (3.3 V, ×8/×16)
    3.5 ms (typ) /sector (2048 byte) (1.8 V, ×8/×16)

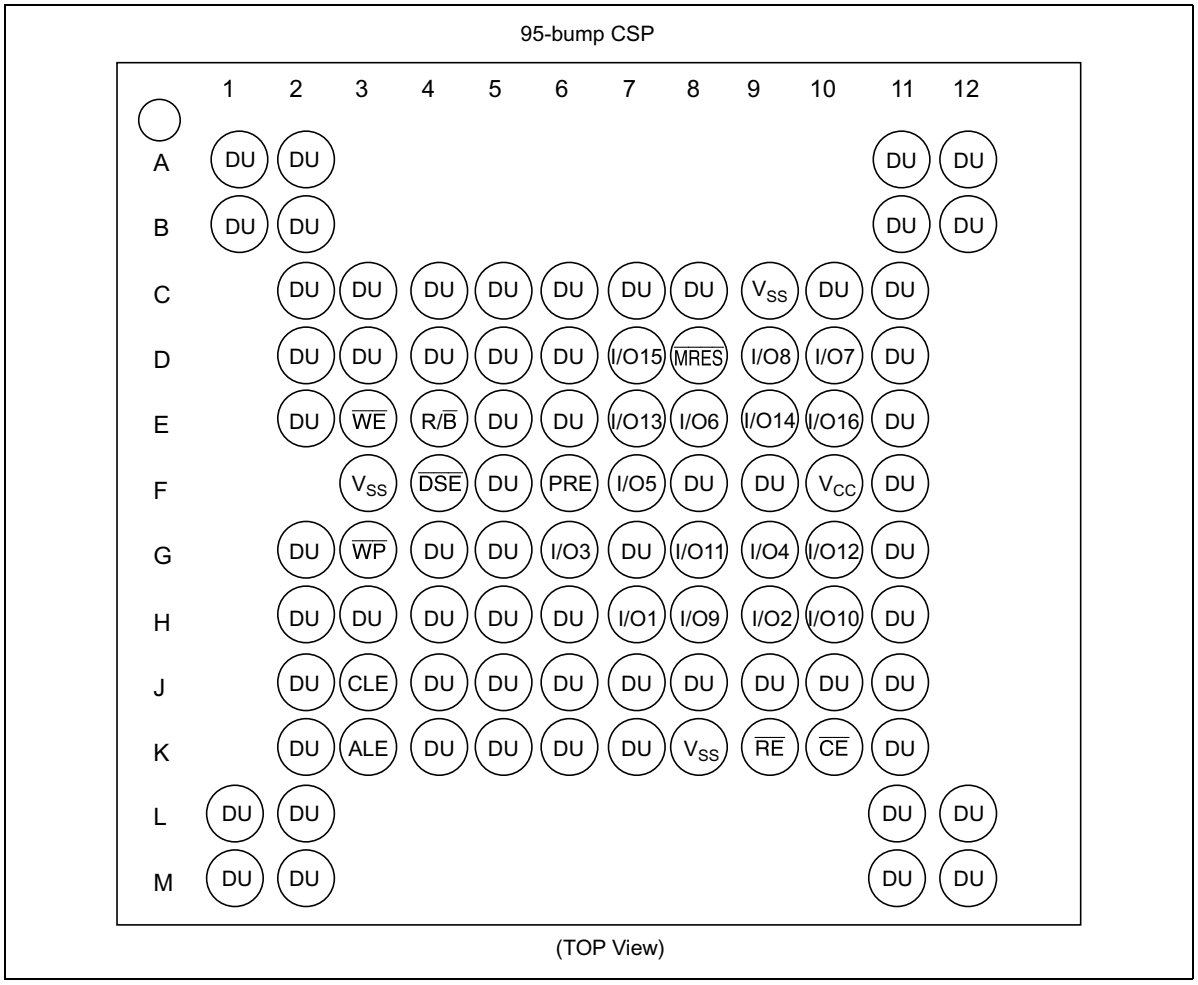
- Low power dissipation (3.3 V and 1.8 V)
  Standby current
  —I_{CCS1} = 1 mA (max)
  —I_{CCS2} = 50 µA (max) (CMOS level)
  —I_{CCS3} = 10 µA (max) (3.3 V), 15µA (max) (1.8 V) (deep standby)
  Serial read operation current
  —I_{CC1} = 30 mA (max)
  Program/erase/rewrite operation current
  —$I_{CC2/3/4}$ = 60 mA (max) (program/erase/rewrite)
- Sector management
  Following functions are build-in flash memory component.
  —Sector management:
  If certain sector had been damaged, it would be replaced by the spare sector automatically.
  Always 100% of sector number are available up to 10^5 erase/write cycles per device.
  —Error check and correction:
  ECC code is generated at the time of programming, and data error is checked at the time of read operation. If data error occurs, the data will be corrected automatically.
  (ECC: 1-byte error correction, 2-byte error detection per 512byte page)
  —Wear leveling:
  To avoid erase/program/rewrite operation converge on the particular physical sector, The number of erase/program/rewrite operation will be leveled automatically by changing internal logical sector address.

- Package line up
  —CSP: CSP 95-bump (TBP-95V)

Ordering Information

Type No.	Operating voltage (V_{CC})	Organization	Package
HN29V128A1ABP-5E	3.3 V	×8	10.0 × 11.50 mm^2, 95-bump
HN29V128A0ABP-5E	3.3 V	×16	0.8 mm ball pitch CSP (TBP-95V)
HN29A128A1ABP-8E	1.8 V	×8	Lead free
HN29A128A0ABP-8E	1.8 V	×16	

Pin Arrangement 95-bump CSP



Pin Description

Name	Description
I/O1 to I/O8	Command, address, data input/output
I/O9 to I/O16	Data input/output (×8 device: DU)
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE}$	Chip enable
$\overline{RE}$	Read enable
$\overline{WE}$	Write enable
$\overline{WP}$	Write protect
R/$\overline{B}$	Ready/$\overline{busy}$
PRE	Power on auto read enable
$\overline{MRES}$	Master reset output
$\overline{DSE}$	Deep standby enable
V_{CC}	Power supply
V_{SS}	Ground
DU	Don't use

Note: 1. All V_{SS} pins should be connected respectively.

Pin Function

Chip enable :**$\overline{CE}$**
$\overline{CE}$ is for selecting a chip and making the device in the active state.
During command waiting state, $\overline{CE}$=H makes the device standby state.
During command execution such as erase, program and rewrite, $\overline{CE}$=H can't stop command operation itself.

Read enable :**$\overline{RE}$**
$\overline{RE}$ is output enable pin and also controls read timing. Clocking $\overline{RE}$ increments the internal address and reads out each data.

Write enable :$\overline{WE}$
Commands, address, and program data are latched into the device at the rising edge of $\overline{WE}$.

Command latch enable :**CLE**
CLE specifies the command data. When CLE=H, data on I/O bus will be recognized as the command data. The command data is latched on the rising edge of $\overline{WE}$ with CLE=H.

Address latch enable :**ALE**
ALE specifies the address data. When ALE=H, data on I/O bus will be recognized as the address data. The address data is latched on the rising edge of $\overline{WE}$ with ALE=H.

Write protect :**$\overline{WP}$**
$\overline{WP}$=L disables erase, program and rewrite operation **.**

Ready/$\overline{busy}$:**R/$\overline{B}$**
R/$\overline{B}$ is the output signal. It shows the internal status of the device to be ready or busy.
It is an open-drain signal and should be pulled up to V_{CC} via suitable resistance.

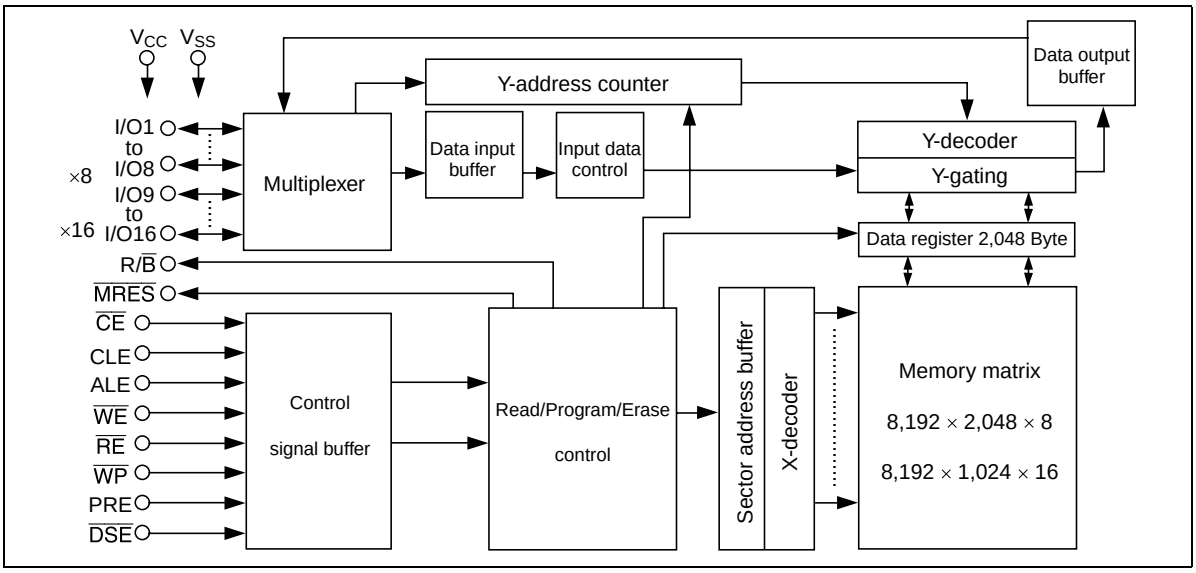
Power on auto read enable :**PRE**
PRE is control pin with active high signal. PRE active Power on auto read mode and Auto read mode. If Power on auto read mode and Auto read mode are unnecessary, PRE pin should be connected to V_{SS} or open.

Master reset output :**$\overline{MRES}$**
$\overline{MRES}$ is the output signal and for providing a reset signal to CPU when Power on auto read mode and auto read mode are activated. $\overline{MRES}$ going from low to high indicates that the data is ready for reading.
If Power on auto read mode and Auto read mode are not activated, $\overline{MRES}$ going from low to high indicates that the device initialization is completed after power is on.

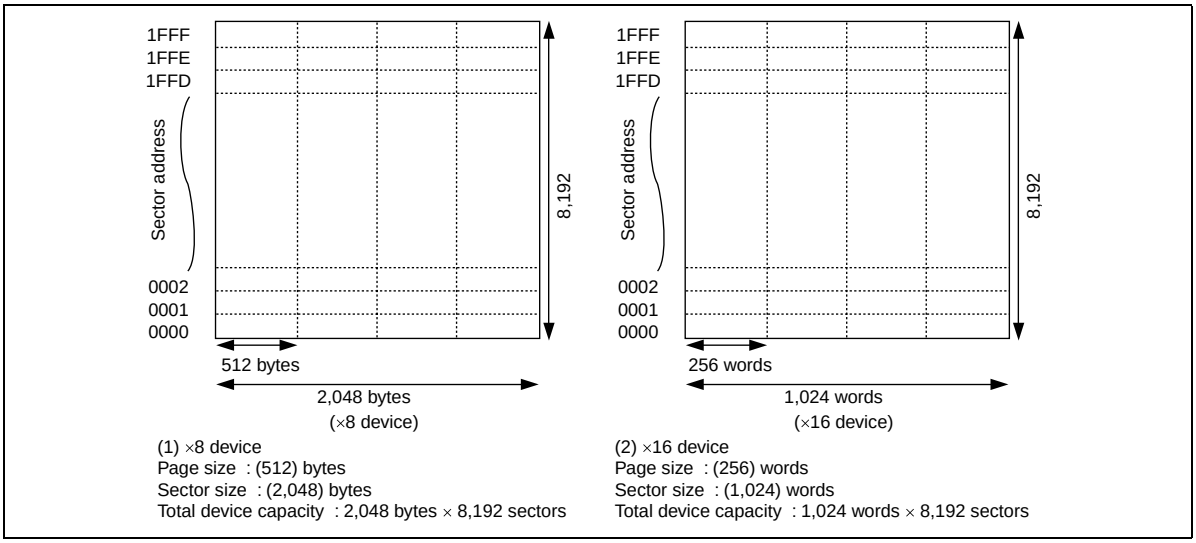
Deep standby enable :**$\overline{DSE}$**
$\overline{DSE}$ must be low when power is on. The device is initialized by $\overline{DSE}$ signal low to high after power is on. During command waiting state or standby state, $\overline{DSE}$ = L makes the device deep standby state. When DSE goes to high, the device returns from the deep standby state. During command execution, $\overline{DSE}$ = L stops command operation and makes the device deep standby state.

Input/output pins :**I/O1 to I/O16**
The I/O pins are used as input/output data and also as command and address.
I/O pins are tri-state pins and transit to the high impedance state when disabled by $\overline{CE}$ and $\overline{RE}$.
I/O9 to 16 are effective for ×16 product, but they are applied for data only.
Only I/O1 to 8 pins are used as command and address inputs for ×16 product.

Block Diagram



Memory Map and Address



Address Input

Case of HN29V128A1A/HN29A128A1A (×8 device)

Clock Cycle	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle (CA1)	A7	A6	A5	A4	A3	A2	A1	A0
Second cycle (CA2)	L*	L*	L*	L*	L*	A10	A9	A8
Third cycle (SA1)	A18	A17	A16	A15	A14	A13	A12	A11
Fourth cycle (SA2)	L*	L*	L*	A23	A22	A21	A20	A19

Notes: 1. A0 to A8: Column address A9 to A10: Page address
A11 to A23: Sector address
2. L* must be set to “Low”.

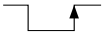
Case of HN29V128A0A/HN29A128A0A (×16 device)

Clock Cycle	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle (CA1)	A7	A6	A5	A4	A3	A2	A1	A0
Second cycle (CA2)	L*	L*	L*	L*	L*	L*	A9	A8
Third cycle (SA1)	A17	A16	A15	A14	A13	A12	A11	A10
Fourth cycle (SA2)	L*	L*	L*	A22	A21	A20	A19	A18

Notes: 1. A0 to A7: Column address A8 to A9: Page address
A10 to A22: Sector address
2. I/O9 to I/O16: V_{IH} or V_{IL}
3. L* must be set to “Low”.

Mode Selection

The address input, command input and data input/output operations of the device are controlled by CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ $\overline{WP}$ and $\overline{DSE}$ signals. The following table shows the operation logic table.

Mode	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	$\overline{DSE}$	I/O	Power
Command input	H	L	L		H	×	H	Input	Active
Address input	L	H	L		H	×	H	Input	Active
Data input	L	L	L		H	×	H	Input	Active
Data output	L	L	L	H		×	H	Output	Active
Output deselect	L	L	L	H	H	×	H	High-Z	Active
During rewriting/erasing	×	×	×	×	×	H	H	Input/ output	Active
Write protect	×	×	×	×	×	L	H	Input/ output	Active/ standby
Standby	×	×	H	×	×	×	H	High-Z	Standby*[2]
Deep standby	×	×	×	×	×	×	L	High-Z	Deep standby*[3]

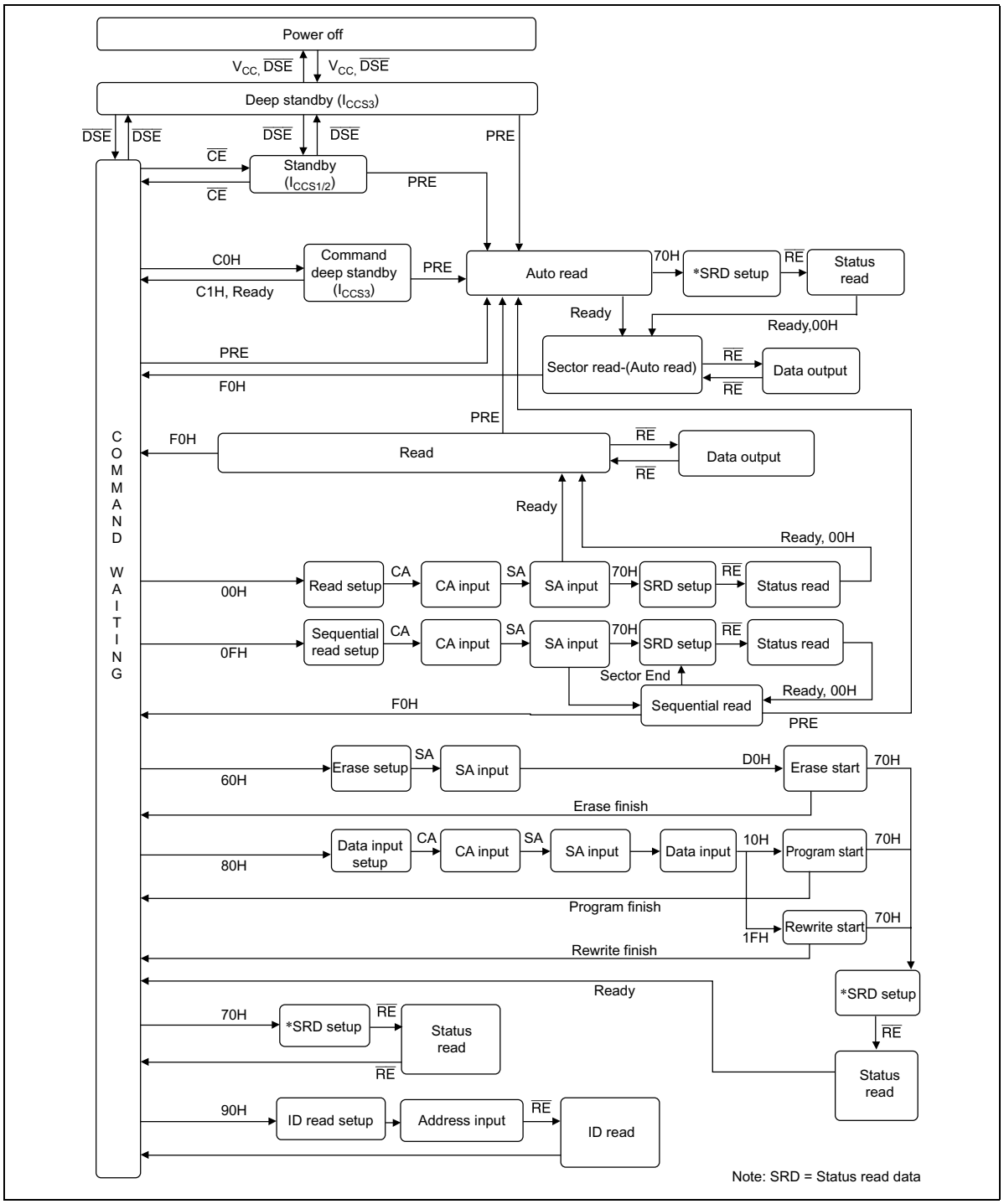
Notes: 1. H: V_{IH} ($\overline{DSE}$: V_{IHP}), L: V_{IL} ($\overline{DSE}$: V_{ILP}), ×: V_{IH} or V_{IL}

2. When setting $\overline{CE}$ = H during the read operation, even if it is in ready state, the device becomes the following data output waiting state and doesn't become standby mode. It becomes standby mode to set $\overline{CE}$ = H in ready state after read stop command execution.
3. The device can transfer only from command waiting state or standby state to deep standby state.

Command Definition

Mode	First cycle	Second cycle	Acceptance in the busy state
Data input	80H	—	
Read mode	00H	—	
Sequential read mode	0FH	—	
Read stop	F0H	—	Acceptance (in Read busy state only)
Program	10H	—	
Erase	60H	D0H	
Rewrite	1FH	—	
Status read	70H	—	Acceptance
ID read	90H	—	
Deep standby (release)	C1H	—	
Deep standby (setup)	C0H	—	

State transition diagram



Absolute Maximum Ratings

If exceeded the following specification, the device may be damaged.

		HN29V128A1A (3.3 V) HN29V128A0A (3.3 V)	HN29A128A1A (1.8 V) HN29A128A0A (1.8 V)		
Parameter	**Symbol**	**Value**	**Value**	**Unit**	**Notes**
V_{CC} voltage	V_{CC}	–0.6 to +4.6	–0.6 to +2.45	V	1
V_{SS} voltage	V_{SS}	0	0	V	
Input voltage	V_{IN}	–0.6 to +4.6	–0.6 to +2.45	V	1, 2
Input/output voltage	$V_{I/O}$	–0.6 to V_{CC} + 0.3 (≤ 4.6)	–0.6 to V_{CC} + 0.3 (≤ 2.45)	V	
Operating temperature range	Topr	0 to +70	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	–55 to +125	°C	3

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT} = –2.0 V for pulse width ≤ 20 ns
3. Device storage temperature range before programming.

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test conditions**
Input capacitance	C_{IN}	—	—	10	pF	V_{IN} = 0 V
Output capacitance	C_{OUT}	—	—	10	pF	V_{OUT} = 0 V

DC Characteristics

DC Characteristics (1)

(Ta = 0 to +70°C)

		HN29V128A1A (3.3 V) HN29V128A0A (3.3 V)			HN29A128A1A (1.8 V) HN29A128A0A (1.8 V)				Test
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**conditions**
Power supply voltage	V_{CC}	2.7	3.3	3.6	1.70	1.8	1.95	V	—
High input voltage	V_{IH}	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V	—
Low input voltage	V_{IL}	–0.3	—	$V_{CC} \times 0.2$	–0.3	—	$V_{CC} \times 0.2$	V	—
High input voltage ($\overline{DSE}$, PRE pin)	V_{IHP}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	—
Low input voltage ($\overline{DSE}$, PRE pin)	V_{ILP}	–0.3	—	$V_{CC} \times 0.1$	–0.3	—	$V_{CC} \times 0.1$	V	—
Input leakage current	I_{LI}	—	—	±2	—	—	±2	µA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	—	—	±2	—	—	±2	µA	V_{OUT} = 0 V to V_{CC}
Operating current (Serial read)	I_{CC1}	—	—	30	—	—	30	mA	$\overline{CE}$ = V_{IL} $\overline{RE}$ = V_{IH}
(Program)	I_{CC2}	—	—	60	—	—	60	mA	—
(Erase)	I_{CC3}	—	—	60	—	—	60	mA	—
(Rewrite)	I_{CC4}	—	—	60	—	—	60	mA	—

DC Characteristics (2)

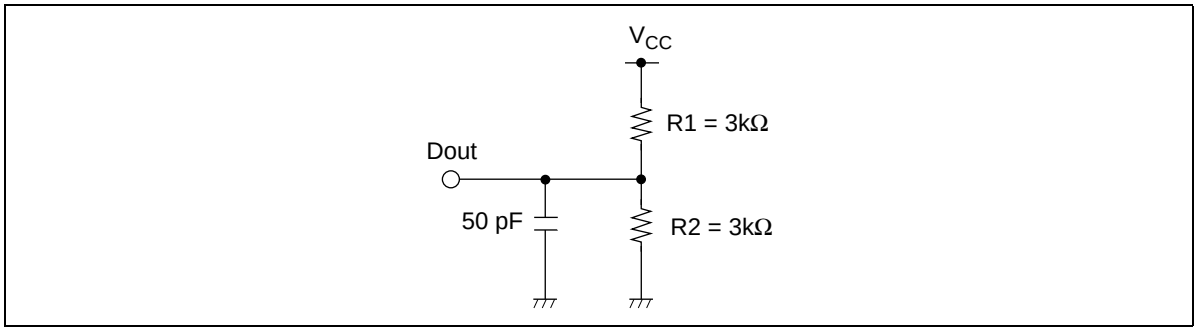
(Ta = 0 to +70°C)

		HN29V128A1A (3.3 V) HN29V128A0A (3.3 V)			HN29A128A1A (1.8 V) HN29A128A0A (1.8 V)				Test
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**conditions**
Standby current (Standby state)	I_{CCS1}	—	—	1	—	—	1	mA	$\overline{CE}$ = V_{IH}, $\overline{WP}$ = V_{IH} or V_{IL}, PRE = V_{IHP} or V_{ILP} or open, $\overline{DSE}$ = V_{IHP}
	I_{CCS2}	—	—	50	—	—	50	µA	$\overline{CE}$ = V_{CC} – 0.2 V, $\overline{WP}$ = V_{CC} ± 0.2 V or V_{SS} ± 0.2 V, PRE = V_{CC} ± 0.2 V or V_{SS} ± 0.2 V or open, $\overline{DSE}$ = V_{CC} ± 0.2 V
(Deep standby) Deep standby command	I_{CCS3}	—	—	10	—	—	15	µA	$\overline{CE}$ = V_{CC} ± 0.2 V, PRE = V_{CC} ± 0.2 V or V_{SS} ± 0.2 V or open, $\overline{DSE}$ = V_{CC} ± 0.2 V, $\overline{WP}$ = V_{CC} ± 0.2 V or V_{SS} ± 0.2 V
(Deep standby) $\overline{DSE}$ control	I_{CCS3}	—	—	10	—	—	15	µA	$\overline{CE}$ = V_{CC} ± 0.2 V, PRE = V_{CC} ± 0.2 V or V_{SS} ± 0.2 V or open, $\overline{DSE}$ = V_{SS} ± 0.2 V, $\overline{WP}$ = V_{CC} ± 0.2 V or V_{SS} ± 0.2 V
High-level output voltage	V_{OH}	V_{CC} – 0.2	—	—	V_{CC} – 0.2	—	—	V	I_{OH} = –100 µA
Low-level output voltage	V_{OL}	—	—	0.2	—	—	0.2	V	I_{OL} = 100 µA

AC Characteristics (Ta = 0 to +70°C)

Test Conditions

- V_{CC}: 2.7 V to 3.6 V (HN29V128A1A(×8)/HN29V128A0A(×16))
  : 1.70 V to 1.95 V (HN29A128A1A(×8)/HN29A128A0A(×16))
- Input pulse levels: 0 V, V_{CC}
- Input rise and fall time: 3 ns
- Input and Output reference levels: 1/2 V_{CC} / 1/2 V_{CC}
- Output load :



AC Characteristics (1)

		HN29V128A1A (3.3 V) HN29V128A0A (3.3 V)			HN29A128A1A (1.8 V) HN29A128A0A (1.8 V)				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Note**
CLE setup time	t_{CLS}	0	—	—	0	—	—	ns	
CLE hold time	t_{CLH}	10	—	—	20	—	—	ns	
$\overline{CE}$ setup time	t_{CS}	0	—	—	0	—	—	ns	
$\overline{CE}$ hold time	t_{CH}	10	—	—	20	—	—	ns	
$\overline{CE}$ high hold time	t_{CEH}	15	—	—	25	—	—	ns	
$\overline{CE}$ high hold time in Sequential read stop cycle	t_{CEHS}	500	—	—	1000	—	—	ns	1
Write pulse width	t_{WP}	25	—	—	65	—	—	ns	
ALE setup time	t_{ALS}	0	—	—	0	—	—	ns	
ALE hold time	t_{ALH}	10	—	—	20	—	—	ns	
Data setup time	t_{DS}	20	—	—	50	—	—	ns	
Data hold time	t_{DH}	10	—	—	20	—	—	ns	
Write cycle time	t_{WC}	50	—	—	100	—	—	ns	
$\overline{WE}$ high hold time	t_{WH}	15	—	—	35	—	—	ns	
$\overline{RE}$ high to $\overline{WE}$ low time	t_{RHW}	50	—	—	100	—	—	ns	
$\overline{RE}$ high to $\overline{WE}$ low time in Sequential read cycle	t_{RHWS}	1	—	—	2	—	—	µs	1
Ready to $\overline{WP}$ low time	t_{RW}	0	—	—	0	—	—	ns	
Ready to $\overline{RE}$ fall time	t_{RR}	20	—	—	20	—	—	ns	
Read pulse time	t_{RP}	35	—	—	80	—	—	ns	
Read cycle time	t_{RC}	50	—	—	100	—	—	ns	
$\overline{RE}$ access time (serial data access)	t_{REA}	—	—	35	—	—	80	ns	
$\overline{RE}$ access time (ID read)	t_{READID}	—	—	35	—	—	80	ns	
$\overline{RE}$ access time (Status read)	t_{RSTO}	—	—	35	—	—	80	ns	
Output data hold time	t_{OH}	10	—	—	10	—	—	ns	
$\overline{RE}$ high to output high-Z time	t_{RHZ}	—	—	30	—	—	80	ns	
$\overline{CE}$ high to output high-Z time	t_{CHZ}	—	—	30	—	—	80	ns	
$\overline{RE}$ high hold time	t_{REH}	15	—	—	20	—	—	ns	
$\overline{CE}$ access time	t_{CEA}	—	—	45	—	—	100	ns	
$\overline{CE}$ access time (status read)	t_{CSTO}	—	—	45	—	—	100	ns	
$\overline{WE}$ high to $\overline{CE}$ low time	t_{WHC}	30	—	—	50	—	—	ns	

Note: 1. t_{CEHS}, t_{RHWS} applies to Sequential read mode only.

AC Characteristics (2)

		HN29V128A1A (3.3 V) HN29V128A0A (3.3 V)			HN29A128A1A (1.8 V) HN29A128A0A (1.8 V)				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Note**
$\overline{WE}$ high to $\overline{RE}$ low time	t_{WHR}	30	—	—	100	—	—	ns	
ALE low to $\overline{RE}$ low time (ID read)	t_{AR1}	100	—	—	100	—	—	ns	
ALE low to $\overline{RE}$ low time (read cycle)	t_{AR2}	50	—	—	100	—	—	ns	
$\overline{CE}$ low to $\overline{RE}$ low time (ID read)	t_{CR}	100	—	—	100	—	—	ns	
Start address access from memory cell array	t_R	—	80	250	—	150	400	µs	
$\overline{WE}$ high to Busy output time	t_{WB}	—	—	200	—	—	200	ns	
$\overline{RE}$ high to Busy output time in Sequential read cycle	t_{SRB}	—	—	200	—	—	500	ns	1
Power on to $\overline{DSE}$ High time	t_{DSE}	0	—	—	0	—	—	ns	
$\overline{DSE}$ high to PRE high delay	t_{PD}	—	—	50	—	—	100	ns	
$\overline{DSE}$ high to busy time	t_{DB}	—	—	5	—	—	5	ms	
Power on busy time	t_{BSY}	—	5	30	—	5	50	ms	
Ready to $\overline{MRES}$ high time	t_{RMRES}	—	—	50	—	—	100	ns	
Deep standby busy	t_{DBSY}	—	—	300	—	—	500	µs	
Auto read busy time	t_{ARBSY}	—	—	1	—	—	1	ms	
PRE pulse width	t_{PRE}	50	—	—	100	—	—	ns	
$\overline{WP}$ setup time	t_{WPS}	100	—	—	100	—	—	ns	
$\overline{WP}$ hold time	t_{WPH}	100	—	—	100	—	—	ns	
Read stop time	t_{RSTP}	0	—	250	0	—	400	µs	
$\overline{CE}$ high to $\overline{WE}$ low setup time	t_{CHWS}	5	—	—	5	—	—	ns	
$\overline{WE}$ high to $\overline{CE}$ low hold time	t_{WHCH}	5	—	—	5	—	—	ns	
$\overline{CE}$ high to $\overline{RE}$ low setup time	t_{CHRS}	5	—	—	5	—	—	ns	
$\overline{RE}$ high to $\overline{CE}$ low hold time	t_{RHCH}	5	—	—	5	—	—	ns	

Note: 1. t_{SRB} applies to Sequential read mode only.

Program/Erase/Rewrite Characteristics

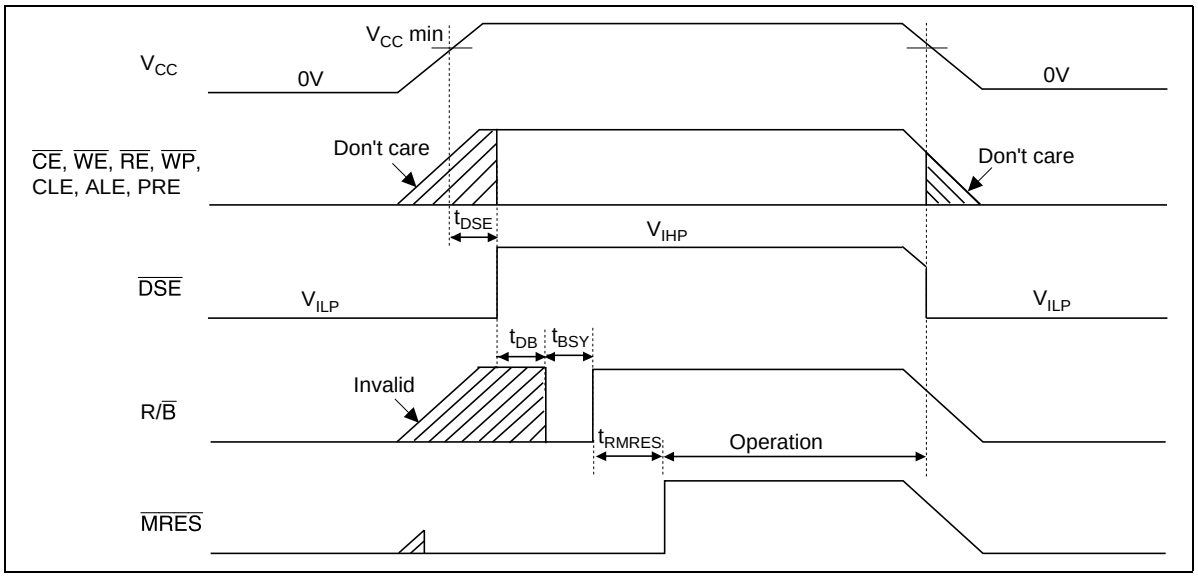
(HN29V128A1A, HN29V128A0A: 2.7 V to 3.6 V,
HN29A128A1A, HN29A128A0A: 1.70 V to 1.95 V,
Ta = 0 to +70 °C)

		HN29V128A1A (3.3 V) HN29V128A0A (3.3 V)			HN29A128A1A (1.8 V) HN29A128A0A (1.8 V)				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Note**
Rewrite time	$t_{REWRITE}$	—	2.2	100	—	3.5	150	ms	
Erase time	t_{ERS}	—	2.2	100	—	3.5	150	ms	
Program time	t_{PROG}	—	1.2	30	—	2.0	45	ms	
Number of partial program cycles in the same sector	N_{PPS}	—	—	4	—	—	4	cycles	
Number of partial program cycles in the same page	N_{PPP}	—	—	1	—	—	1	cycles	

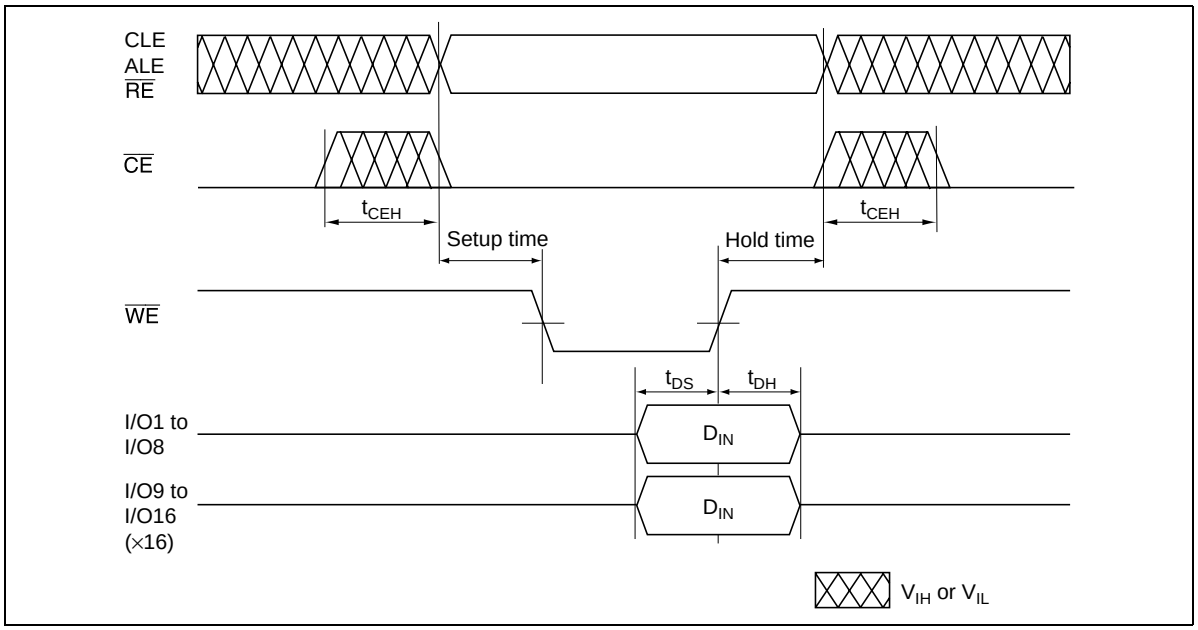
Note: 1. The data transfer time is not included.

Timing Waveforms

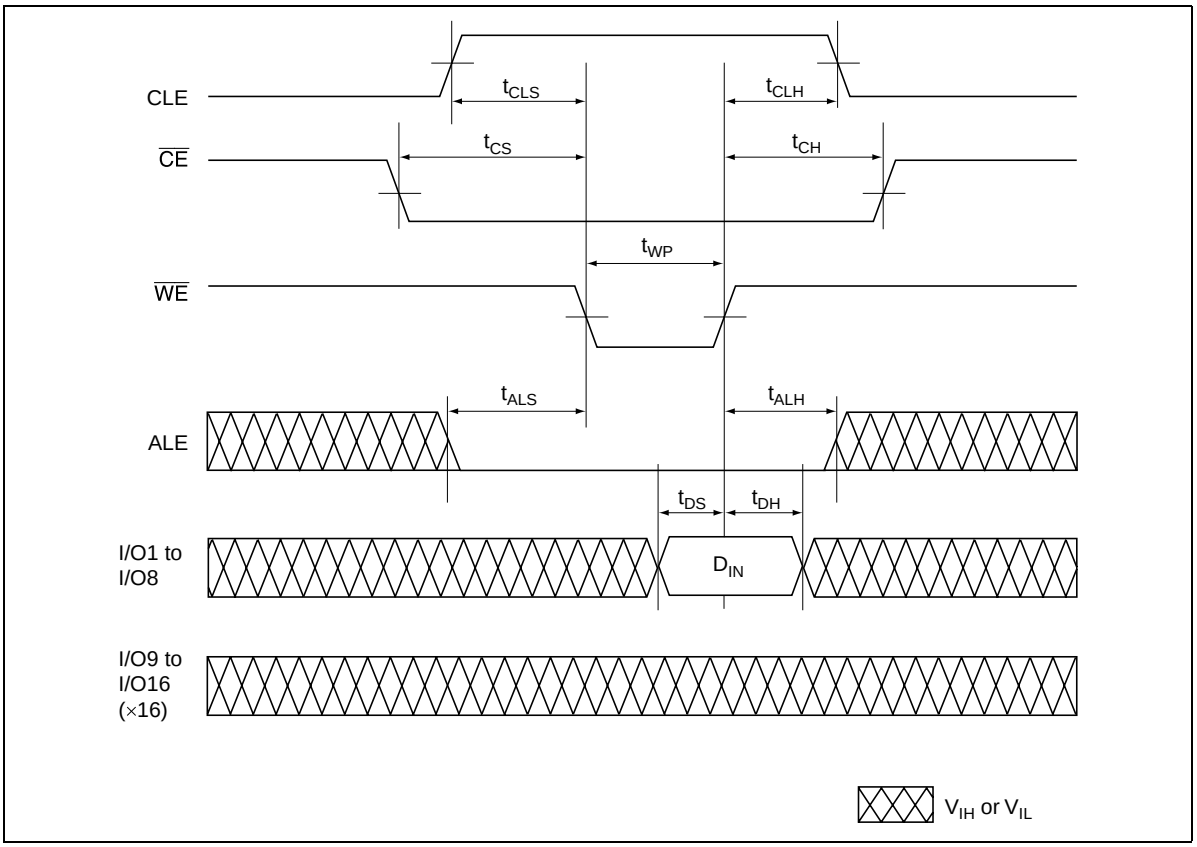
Power on and off



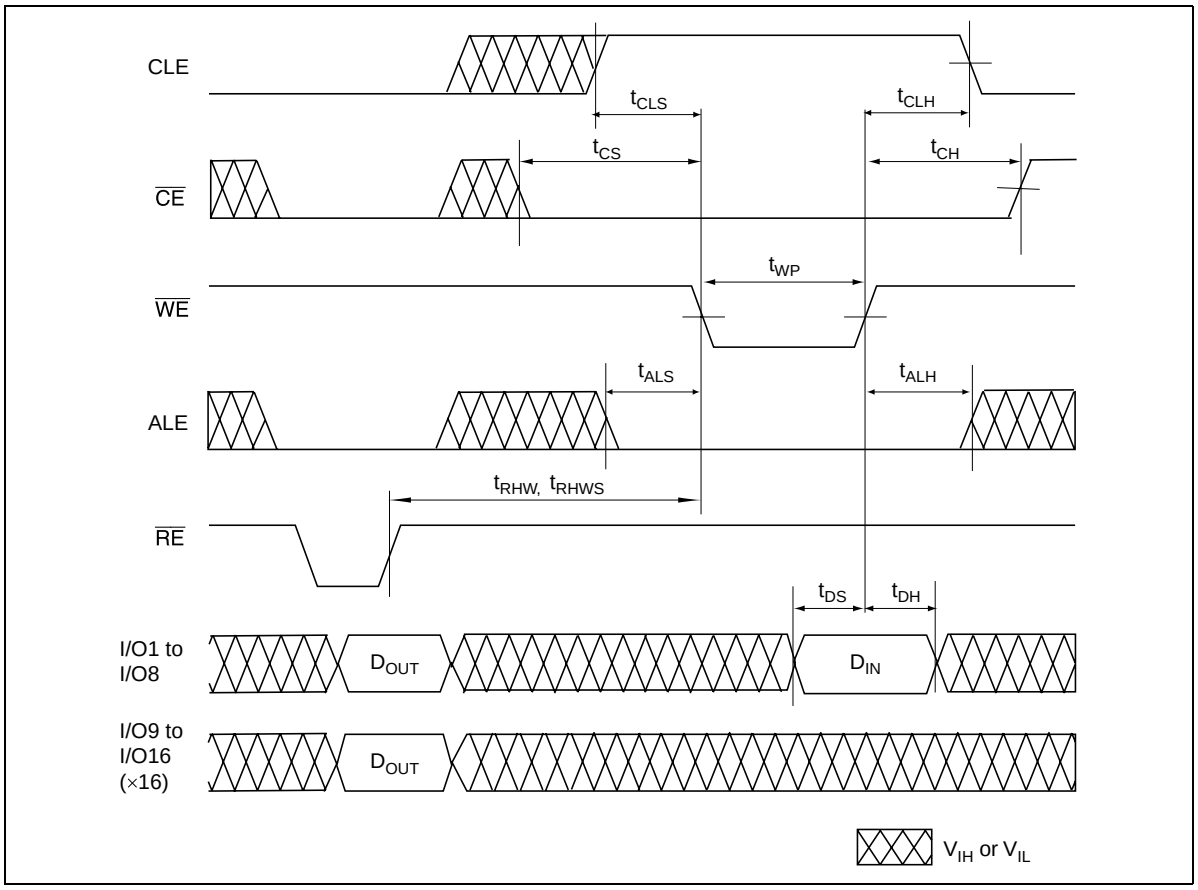
Basic timing for command, address and data latch



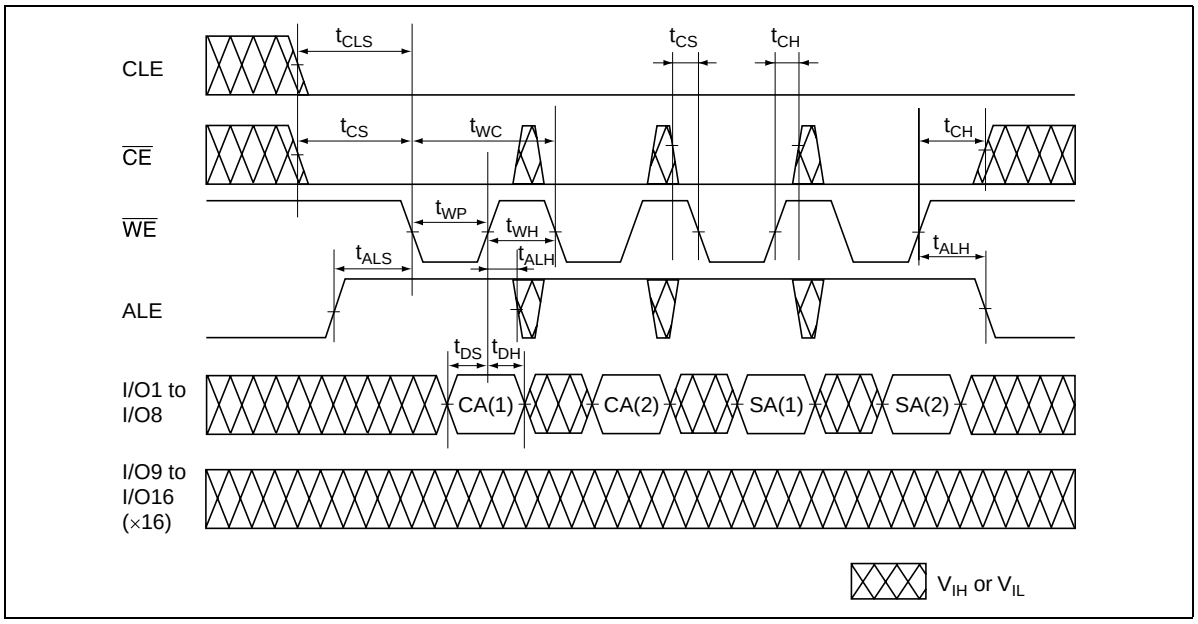
Command input cycle



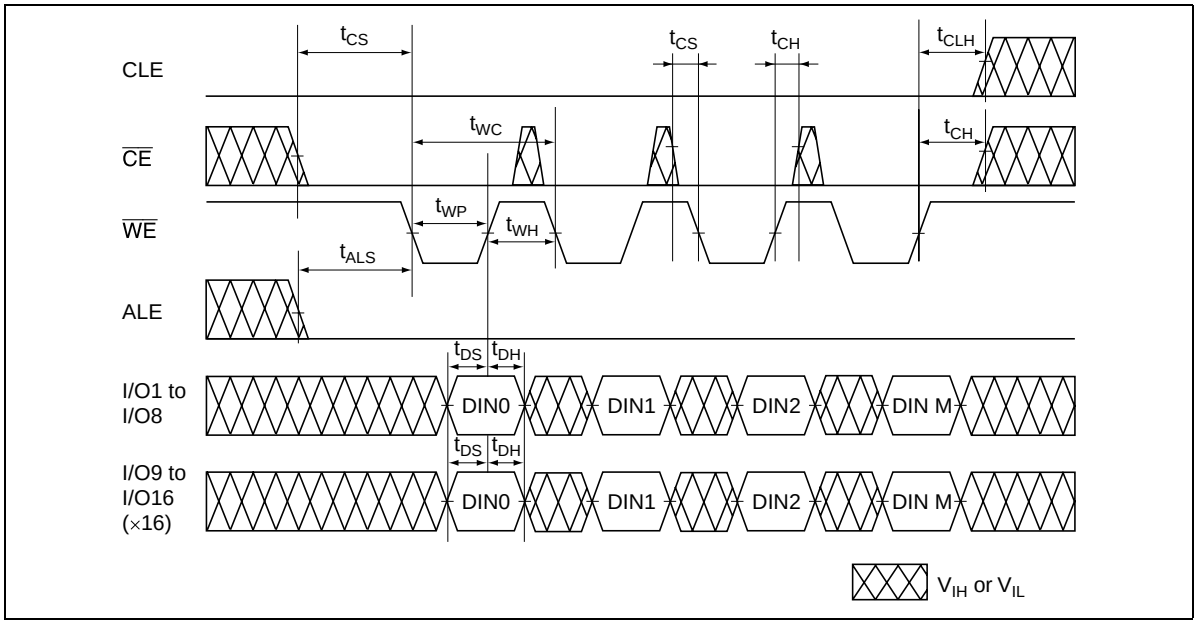
Command input cycle after data output cycle



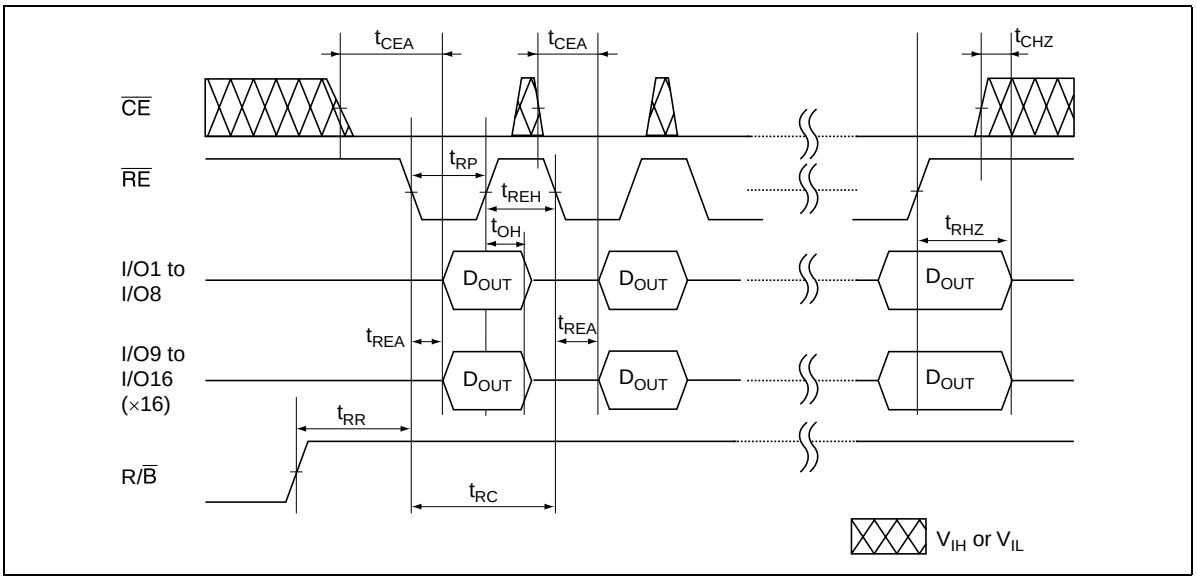
Address input cycle



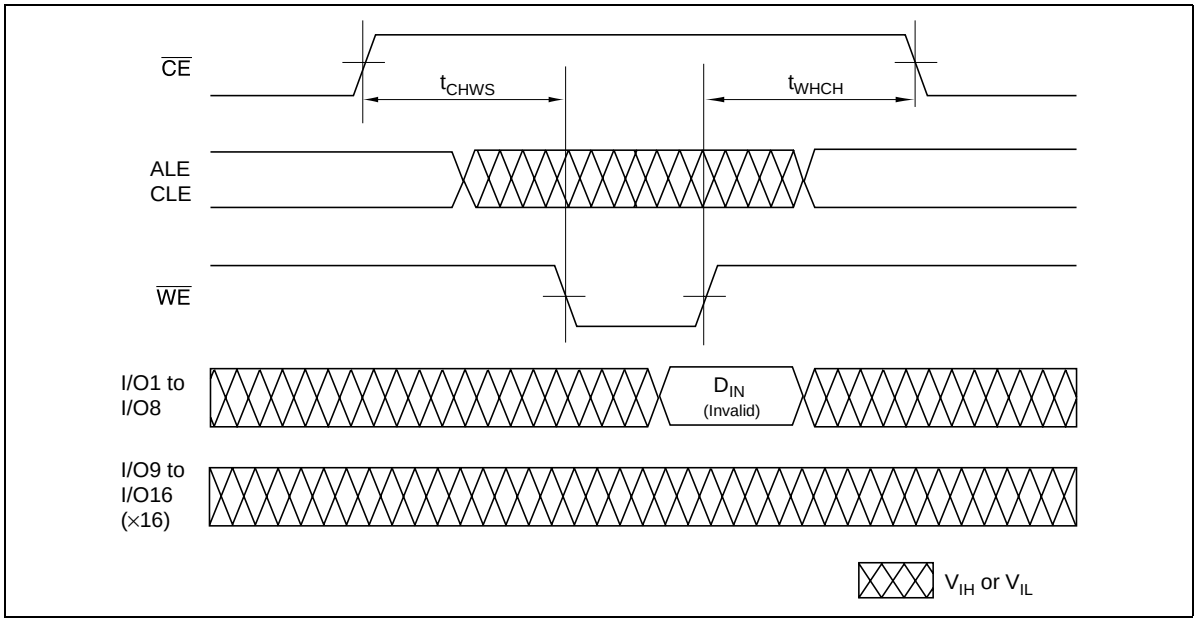
Data input cycle



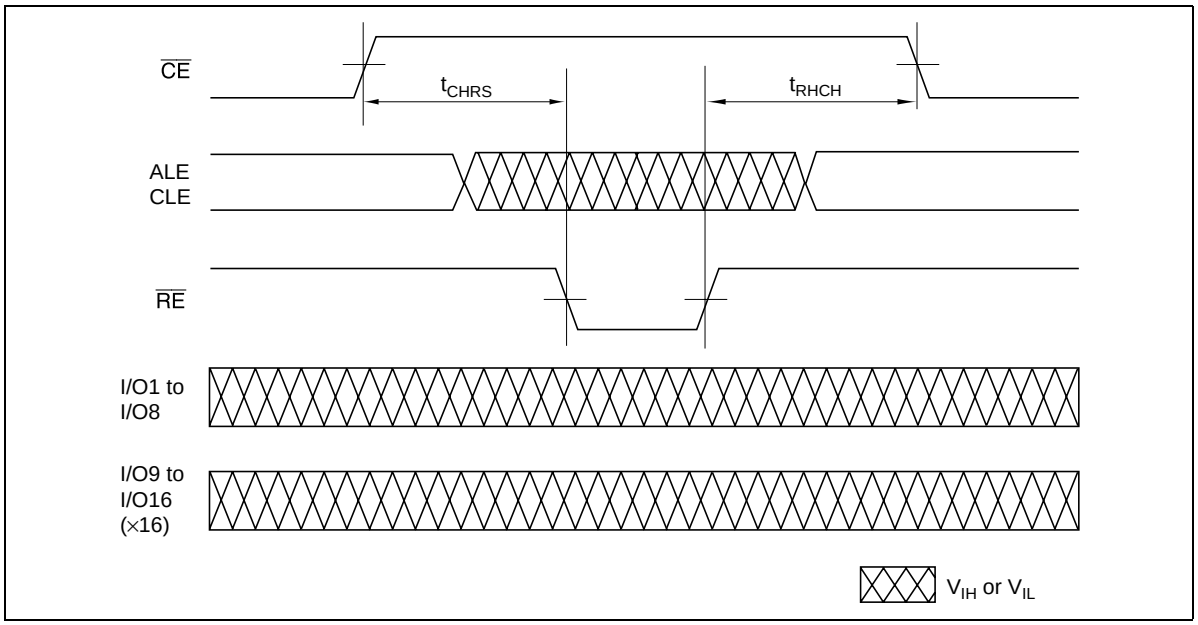
Serial read cycle



Invalid input cycle



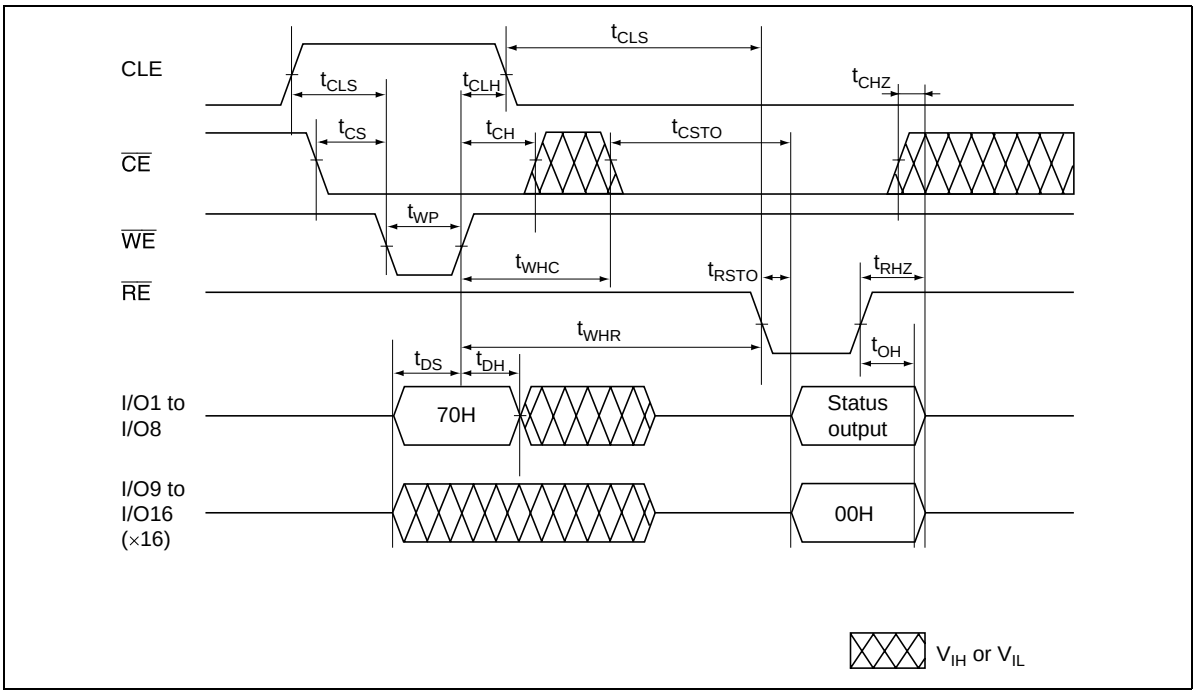
Invalid output cycle



Status read

This device automatically performs rewriting, programming, erasing, and verification after the operation. This device provides the status read function to indicate the device status and the execution result. The device status is output through the I/O pins by issuing command 70H then inputting the $\overline{RE}$ clock. The following timing shows the status as the output through the I/O pins.

Status read cycle



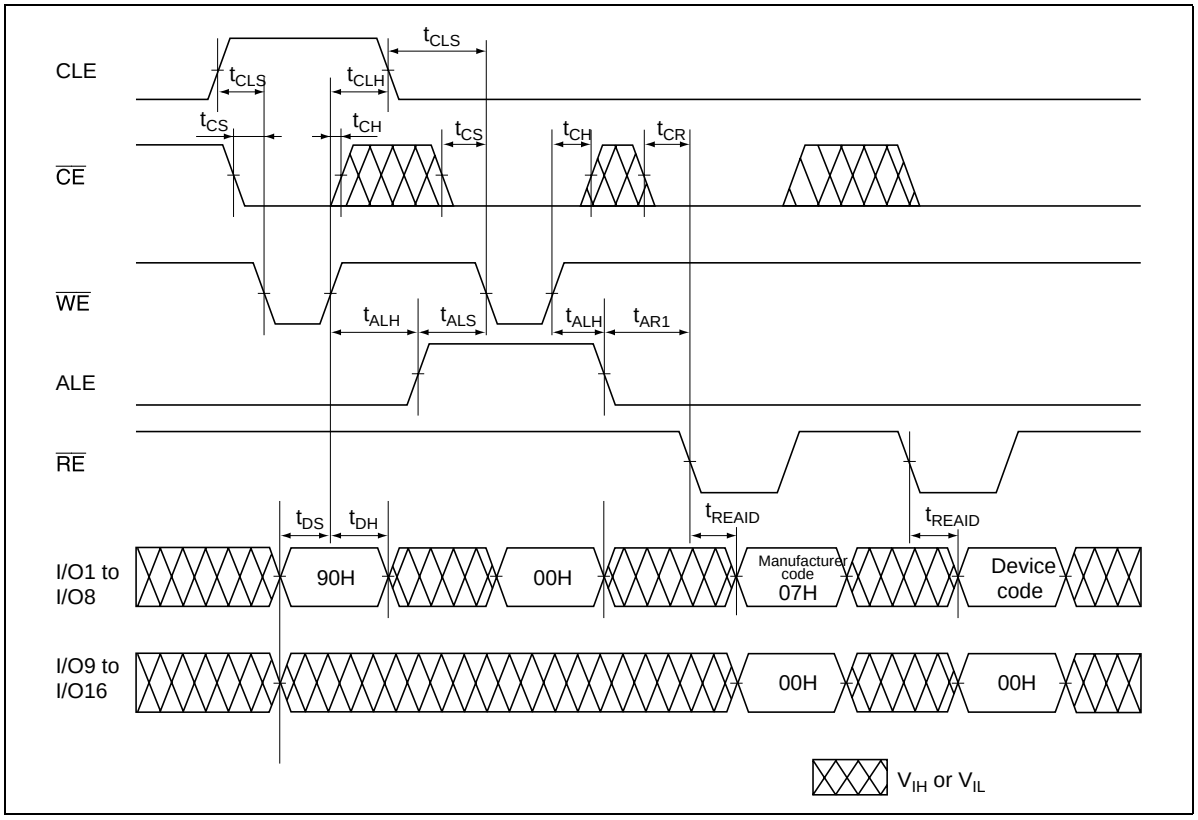
Pin	Status	Output
I/O1	Passed or failed	Passed: 0, failed: 1
I/O2	Not used. Reserved for future use	0
I/O3	Not used. Reserved for future use	0
I/O4	Not used. Reserved for future use	0
I/O5	Not used. Reserved for future use	0
I/O6	Not used. Reserved for future use	0
I/O7	Ready or busy	Ready: 1, busy: 0
I/O8	Write protection	Protected: 0, not protected: 1
I/O9 to I/O16	Not used	00H

Note: 1. The passed or failed status indicated through the I/O1 is only valid while the device is in the ready state.

ID read

This device holds the ID code which indicates the manufacturer and device information to the application system. The ID code can be read in the following timing.

ID read cycle

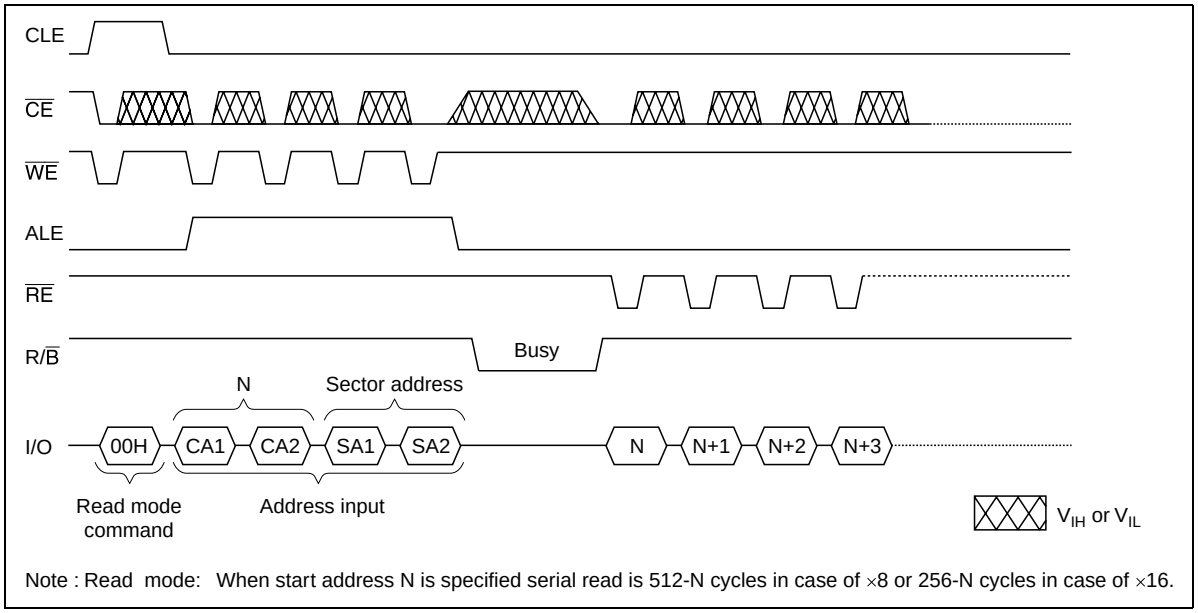


	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hexadecimal
Manufacturer code	0	0	0	0	0	1	1	1	07H
Device code I/O (×8) 3.3 V device	0	1	0	1	0	0	0	1	51H
I/O (×8) 1.8 V device	0	1	0	1	0	0	1	0	52H
I/O (×16) 3.3 V device	0	1	0	1	0	0	1	1	53H
I/O (×16) 1.8 V device	0	1	0	1	0	1	0	0	54H

Note: 1. Output of I/O9 to I/O16 at manufacture code and device code is “00H”.

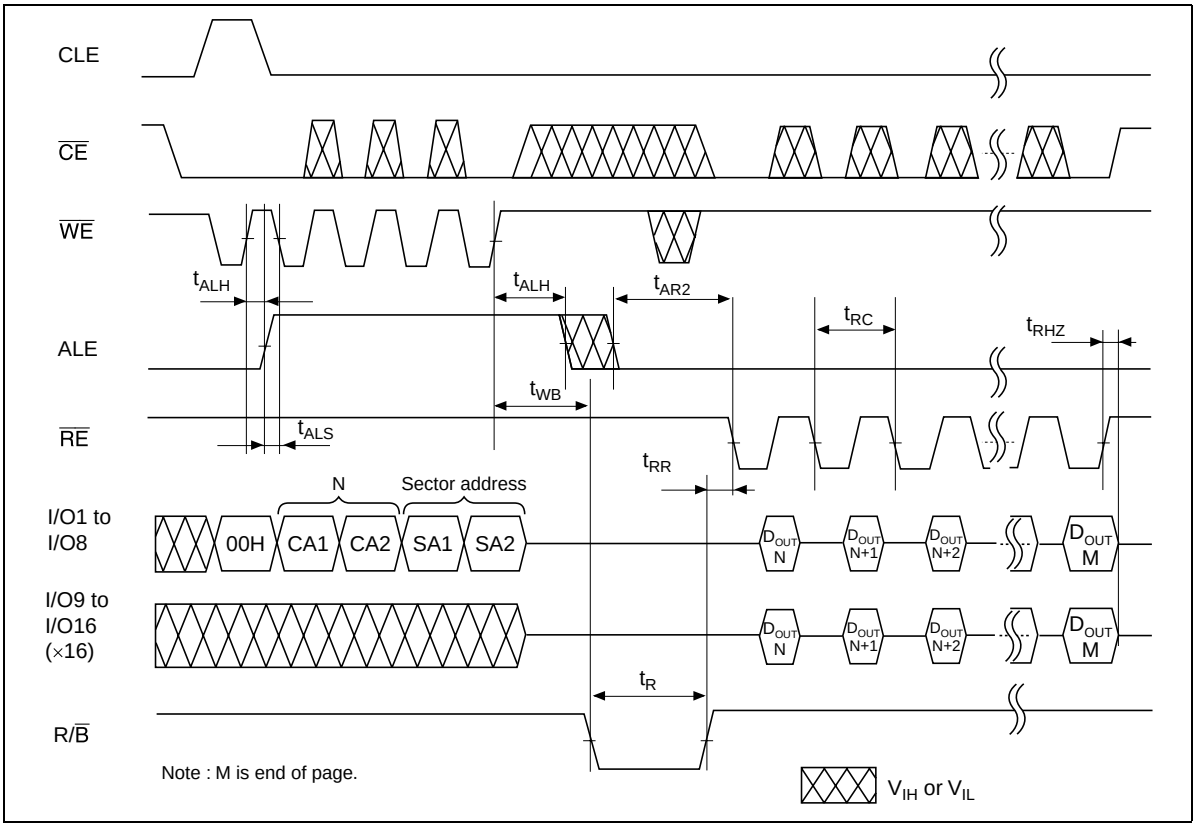
Read mode

The device enters into the read mode by command 00H. Read command operation is performed per every page. Start address in the page can be specified in a CA (Column address). The operating timing is shown below.



Note : Read mode: When start address N is specified serial read is 512-N cycles in case of ×8 or 256-N cycles in case of ×16.

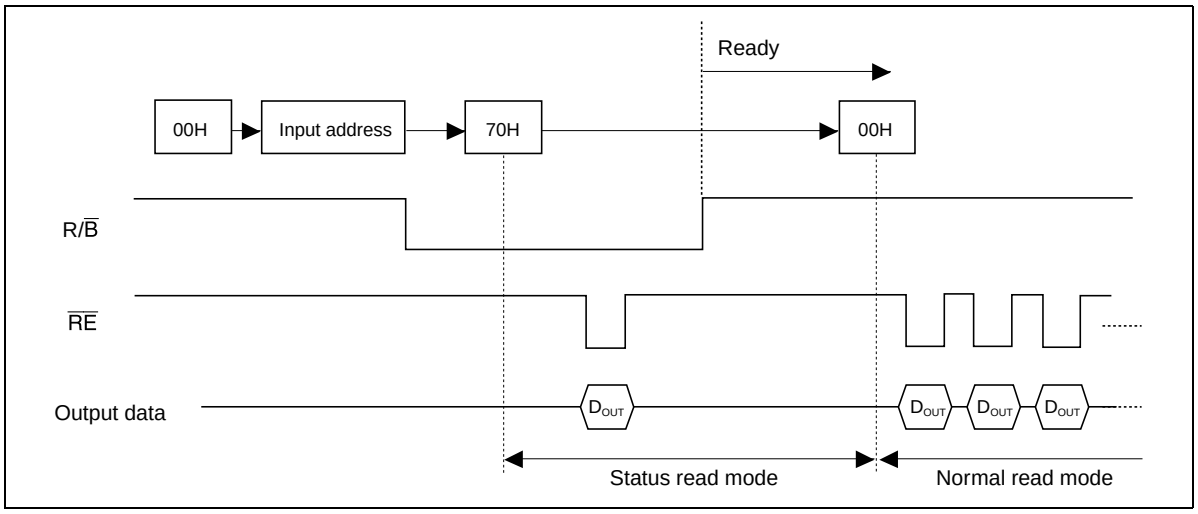
Read cycle


CLE
CE
WE
ALE
RE
I/O1 to I/O8
I/O9 to I/O16 (×16)
R/B
tALH
tALH
tAR2
tRC
tRHZ
tWB
tALS
tRR
tR
N
Sector address
00H
CA1
CA2
SA1
SA2
DOUT N
DOUT N+1
DOUT N+2
DOUT M
Note : M is end of page.
VIH or VIL

Status read during the read operation

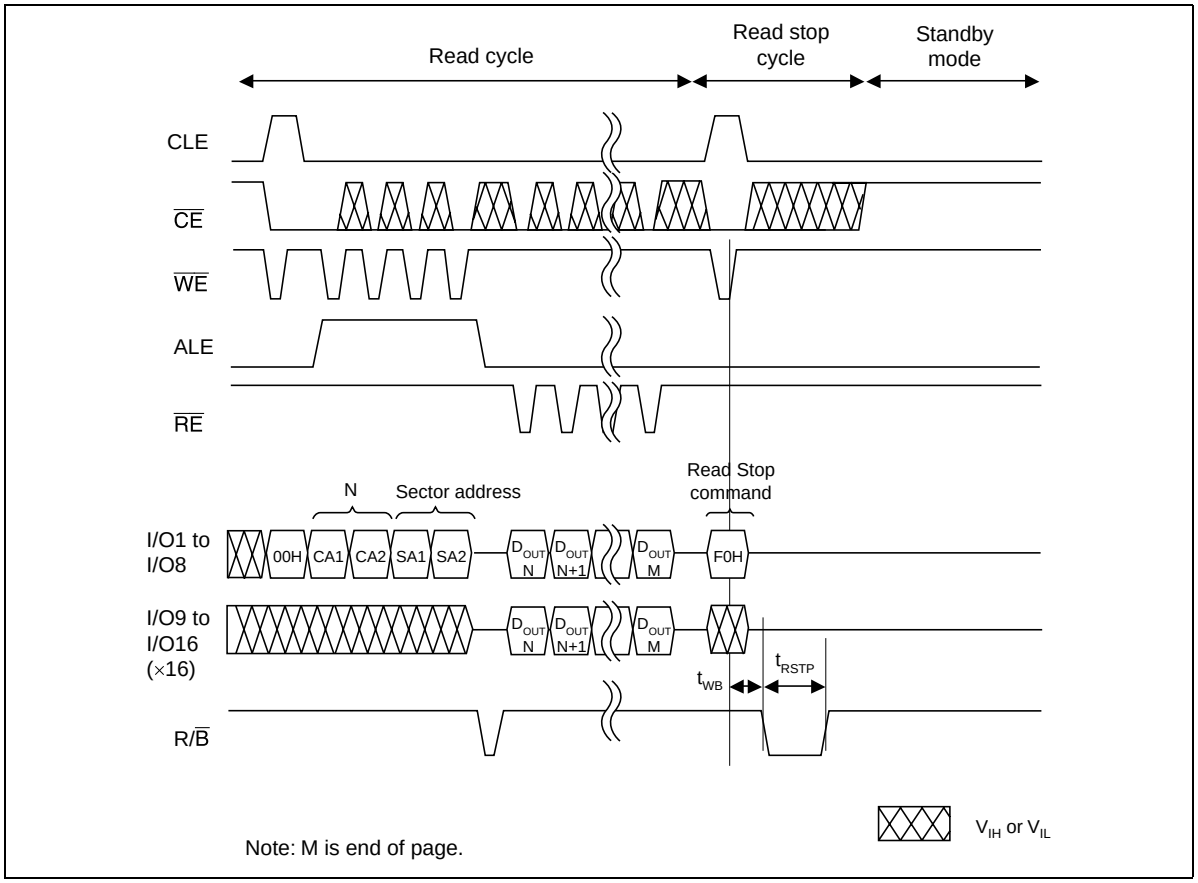
The device status can be read out by inputting the status read command 70H in the read mode. Once the device has been set to the status read mode by 70H command, the device will not return to the read mode automatically. However, when the read command 00H is input after ready, the status read mode is reset and the device returns to the read mode.

Status read during read mode



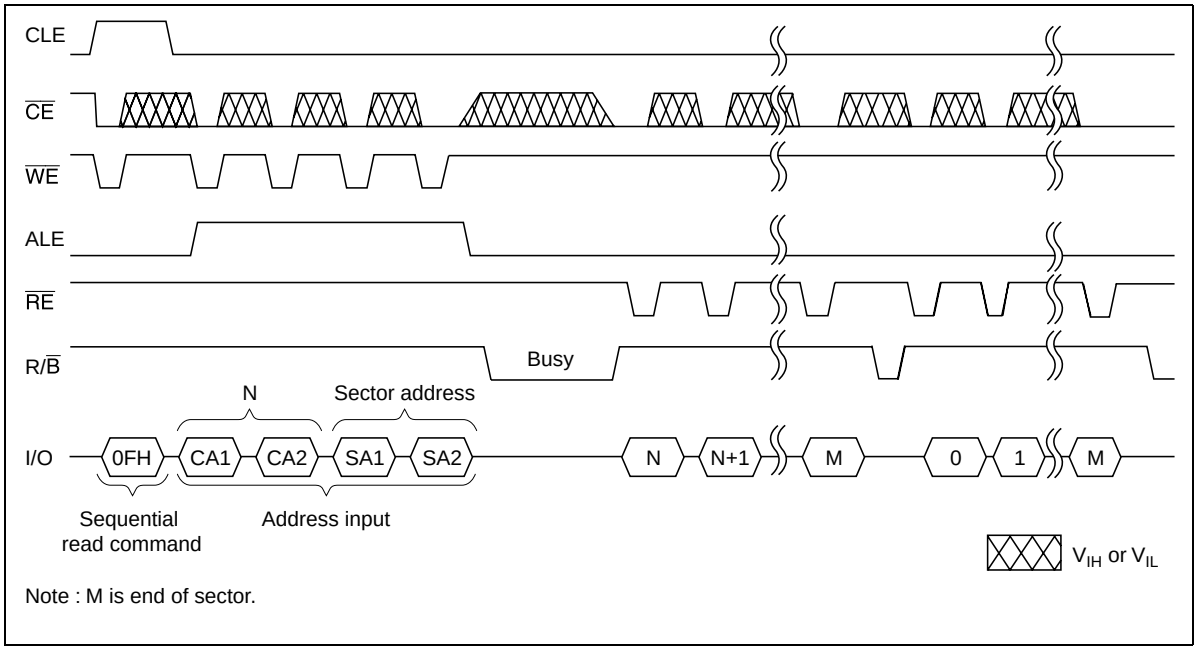
Read stop cycle

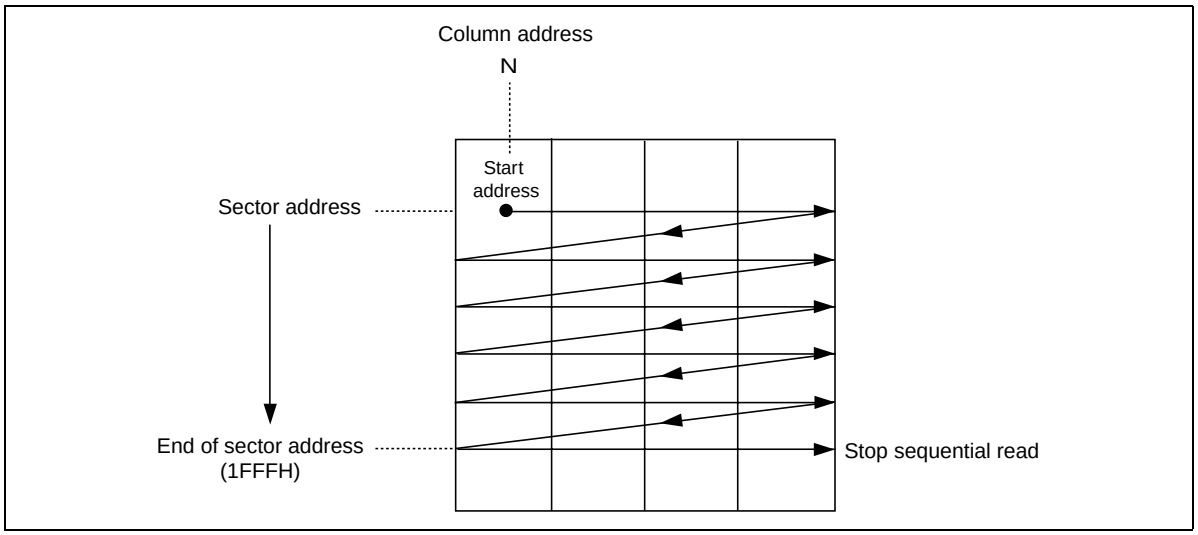
Read stop command F0H enables to finish read mode.
Read stop command F0H can be accepted in the busy state.



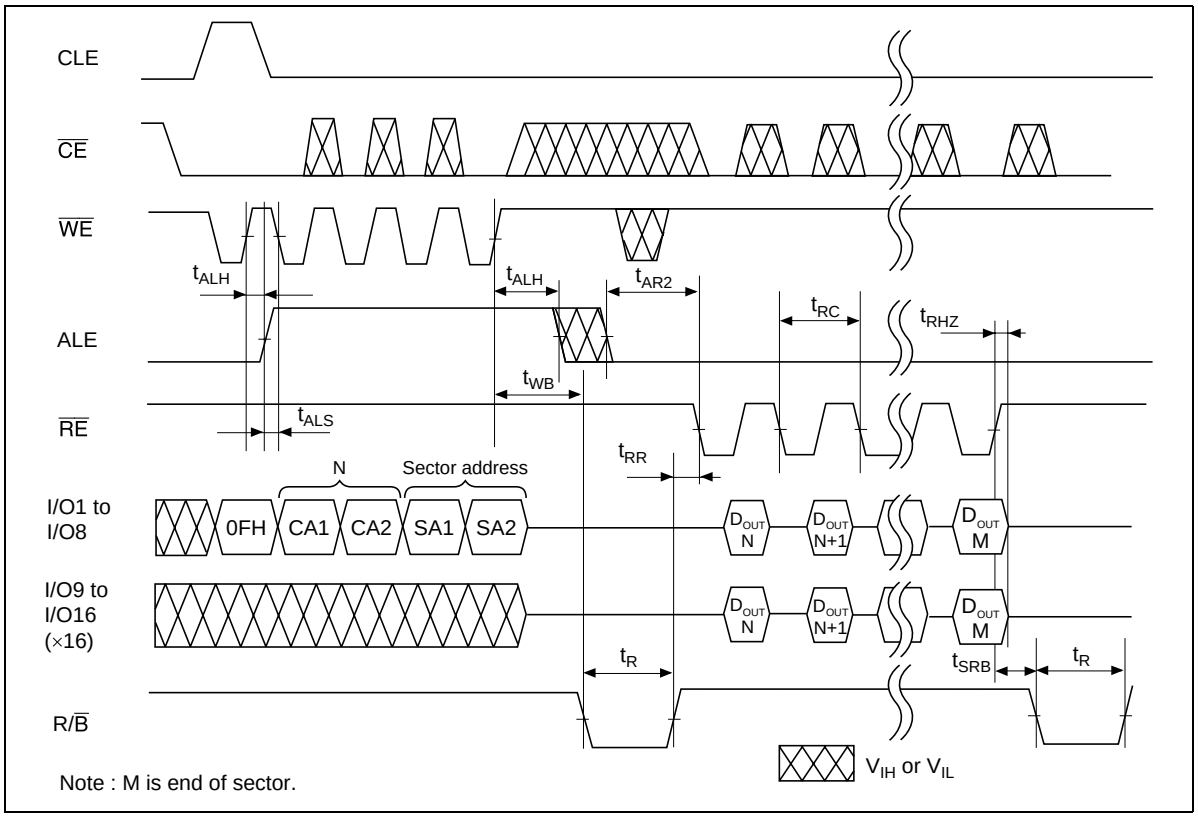
Sequential read mode

The device enters into the sequential read mode by command 0FH. This mode performs continuously reading through the pages and the sectors without additional command/address inputs. Start address in the page can be specified in a CA. The operating timing and block diagram are shown below.



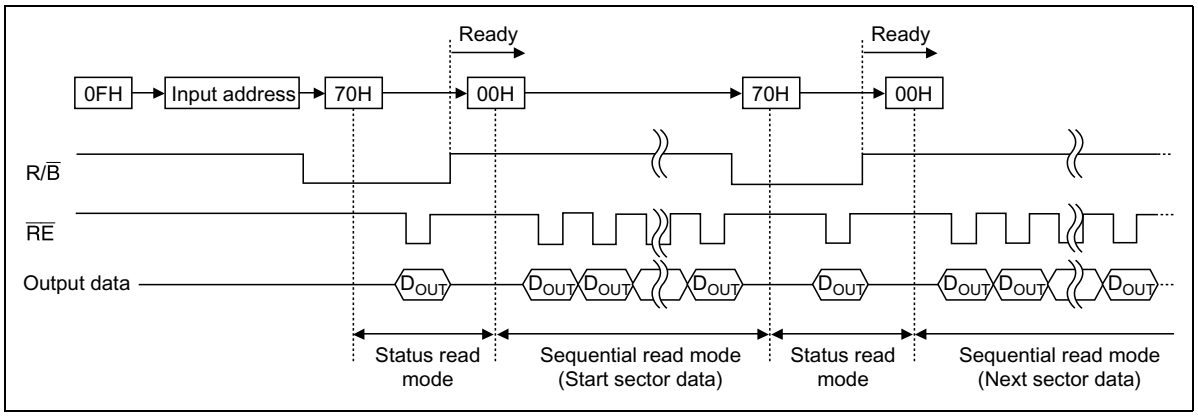


Sequential read cycle



Status read during the sequential read operation

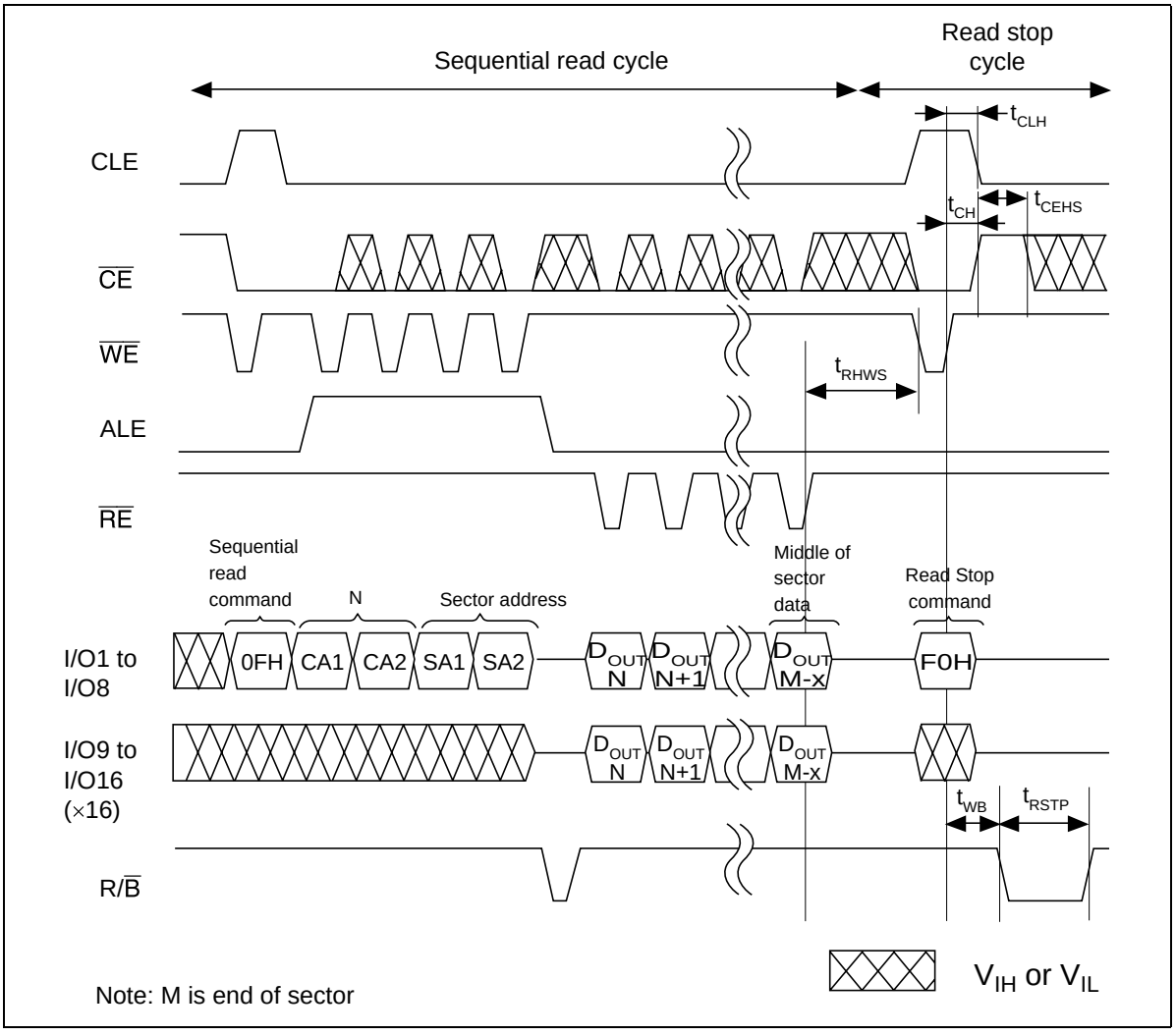
The device status can be read out by inputting the status read command 70H in the sequential read mode. Once the device has been set to the status read mode by 70H command, the device will not return to the sequential read mode automatically. However, when the read command 00H is input after ready state, the status read mode is reset and the device returns to the sequential read mode.



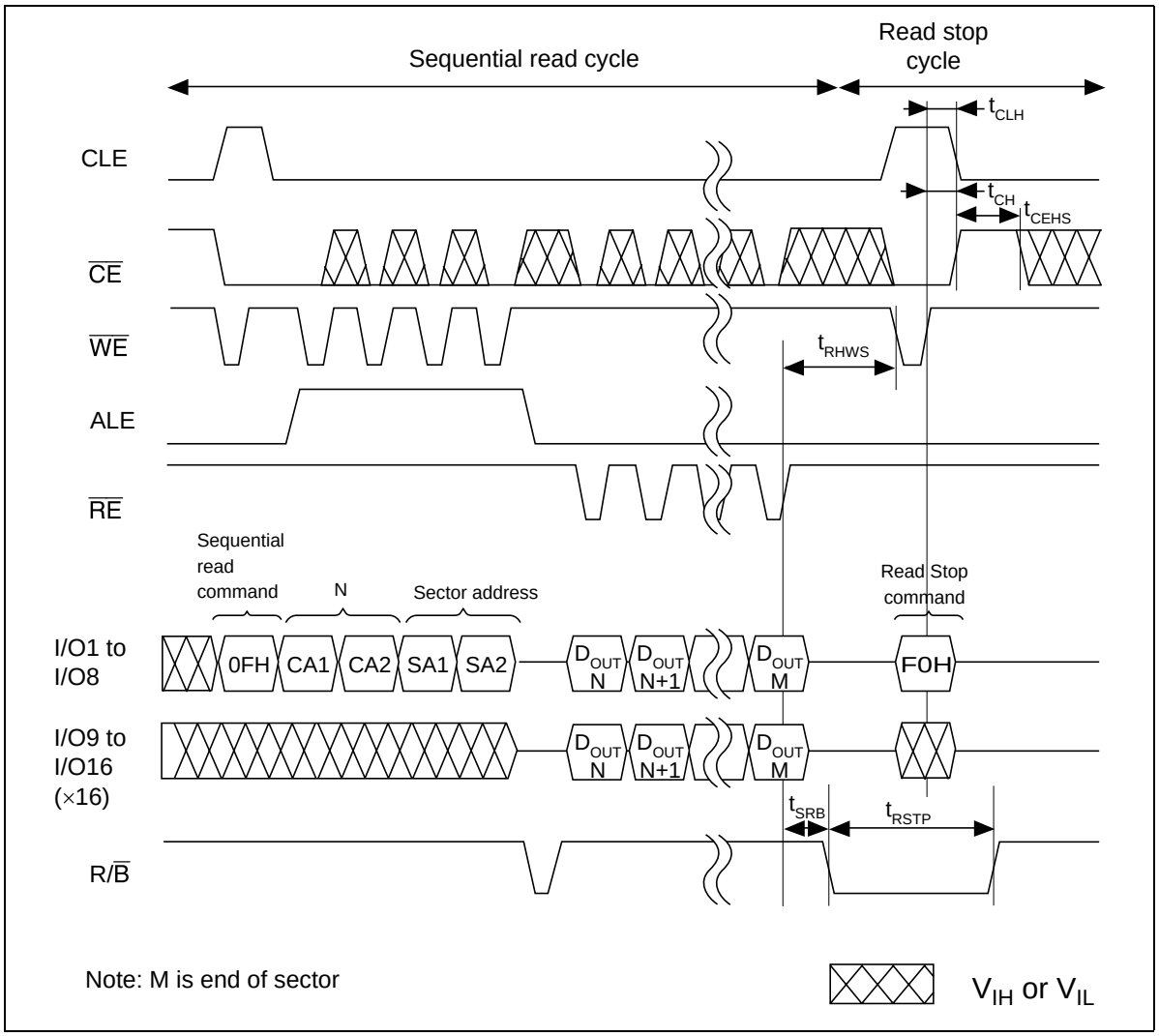
Sequential read stop cycle

Read stop command F0H enables to finish sequential read mode.
After inputting read stop command F0H, the device becomes busy state. And then, the sequential read mode ends and becomes command waiting state when the status returns to ready.
Read stop command F0H can be accepted in the busy state.

Stop in Ready state



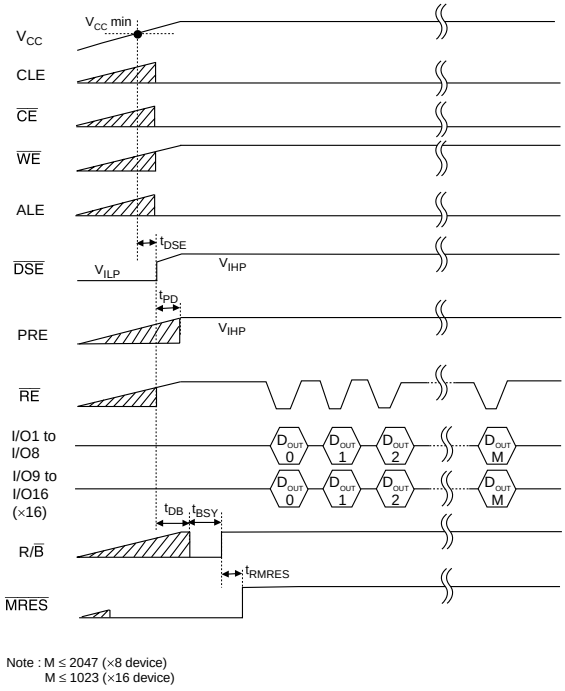
Stop in Busy state



Power on auto read / Auto read

Power on auto read mode enables to read the data of the lowest sector(2k byte) without command and address data input when power is on.
Auto read mode enables to read the data of the lowest sector (2k byte) without command and address data input in the normal operation.
Power on auto read and Auto read are activated when power is on.
Power on auto read is available and Auto read operates until power is off when these are activated.
These are activated after PRE high signal right after DSE goes high. ($\overline{DSE}$ must be low until Power reaches V_{CC}min).
$\overline{MRES}$ going low to high indicates that the data is ready for reading.
The data of the lowest sector (2k byte) can be output by $\overline{RE}$ clock without command and address input.
After power on read operation, PRE should be kept high.
During the normal operation, keeping PRE low for t_{PRE} makes the device transfer to the auto read mode and the data of the lowest sector (2k byte) can be output by $\overline{RE}$ clock without command and address input.
If power on auto read and auto read operation is unnecessary, PRE pin should be connected to V_{SS} or open.

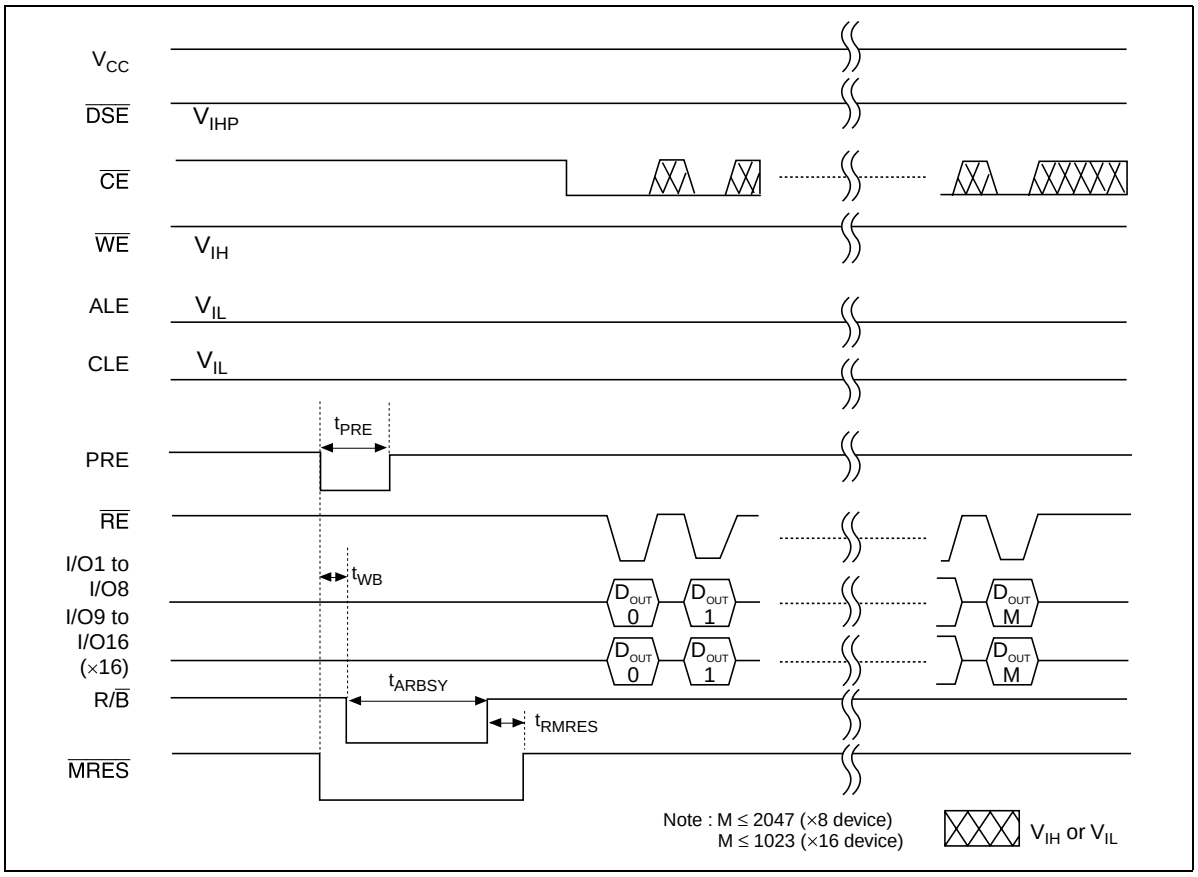
Power on auto read



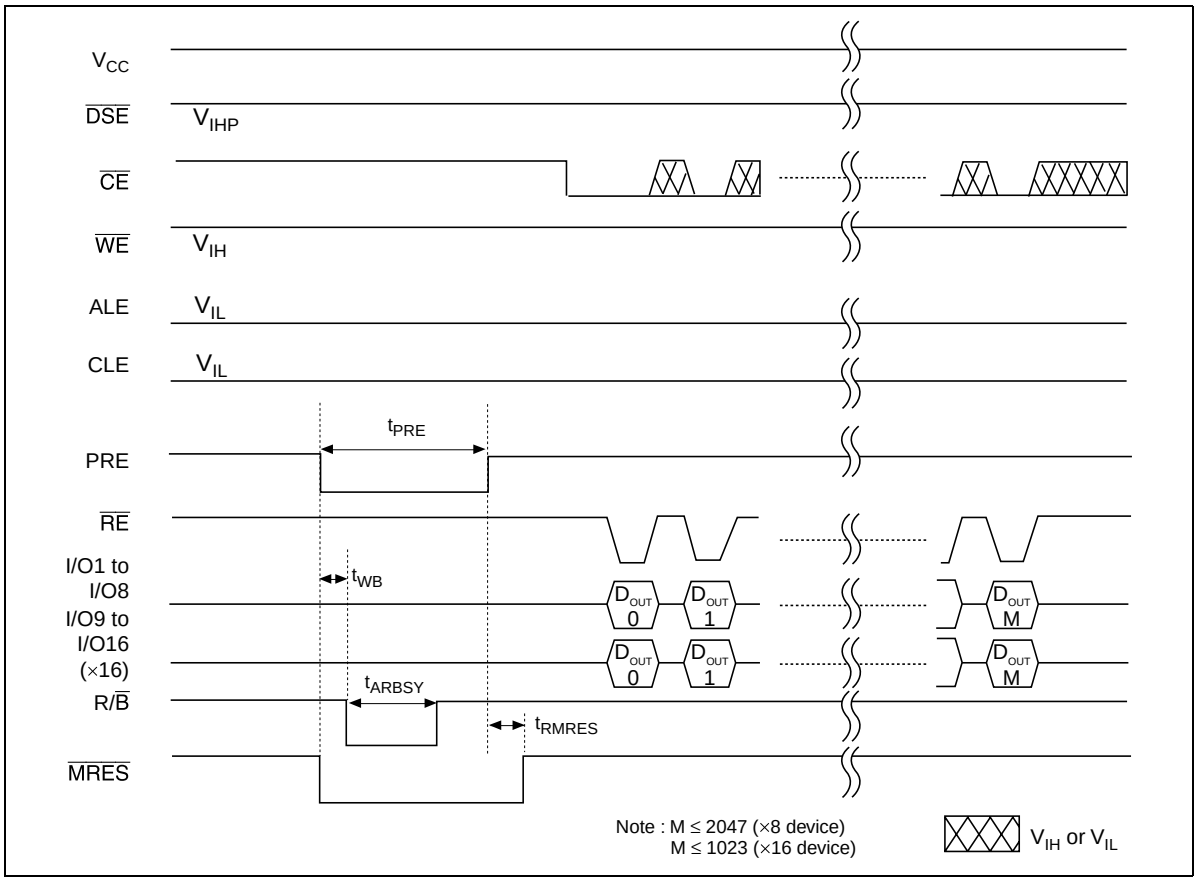
Note : M ≤ 2047 (×8 device)
M ≤ 1023 (×16 device)

Auto read

Case of $t_{PRE} < t_{ARBSY}$



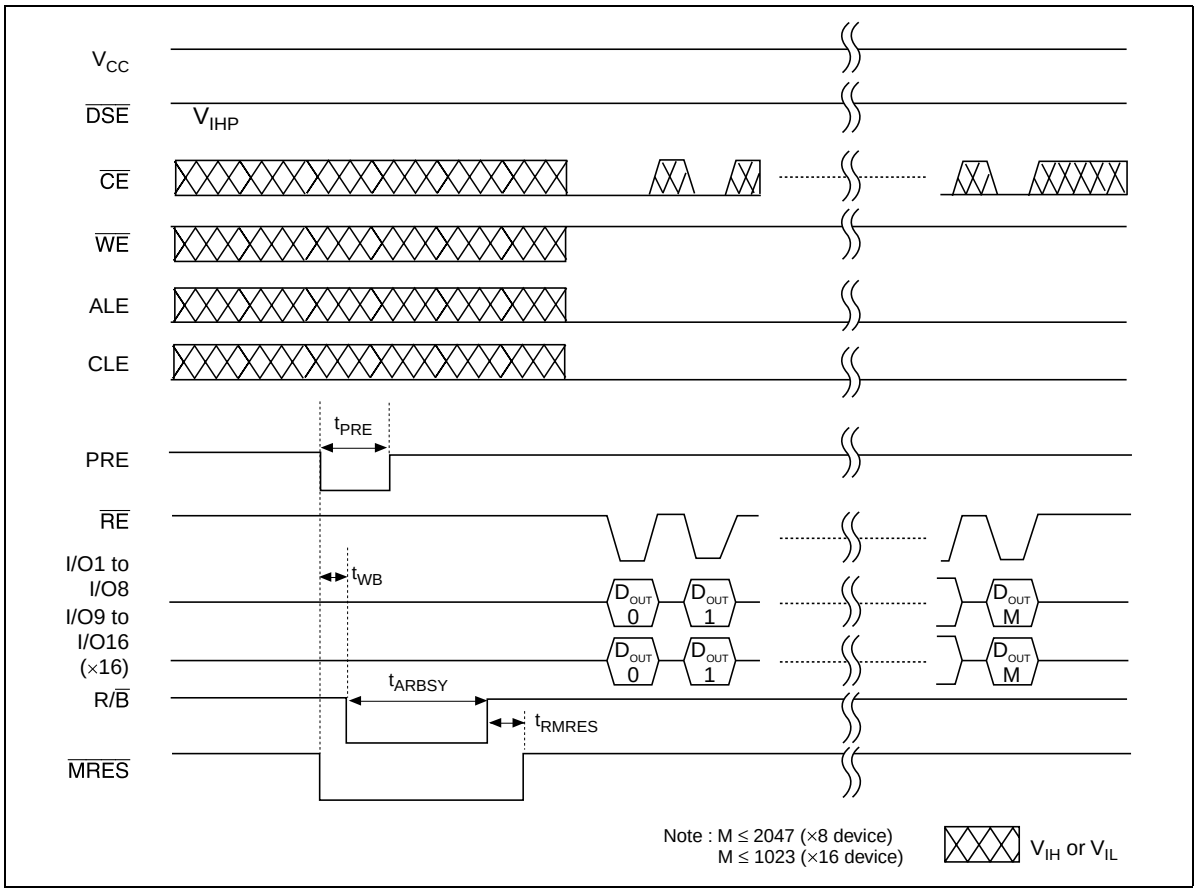
Case of $t_{PRE} \geq t_{ARBSY}$



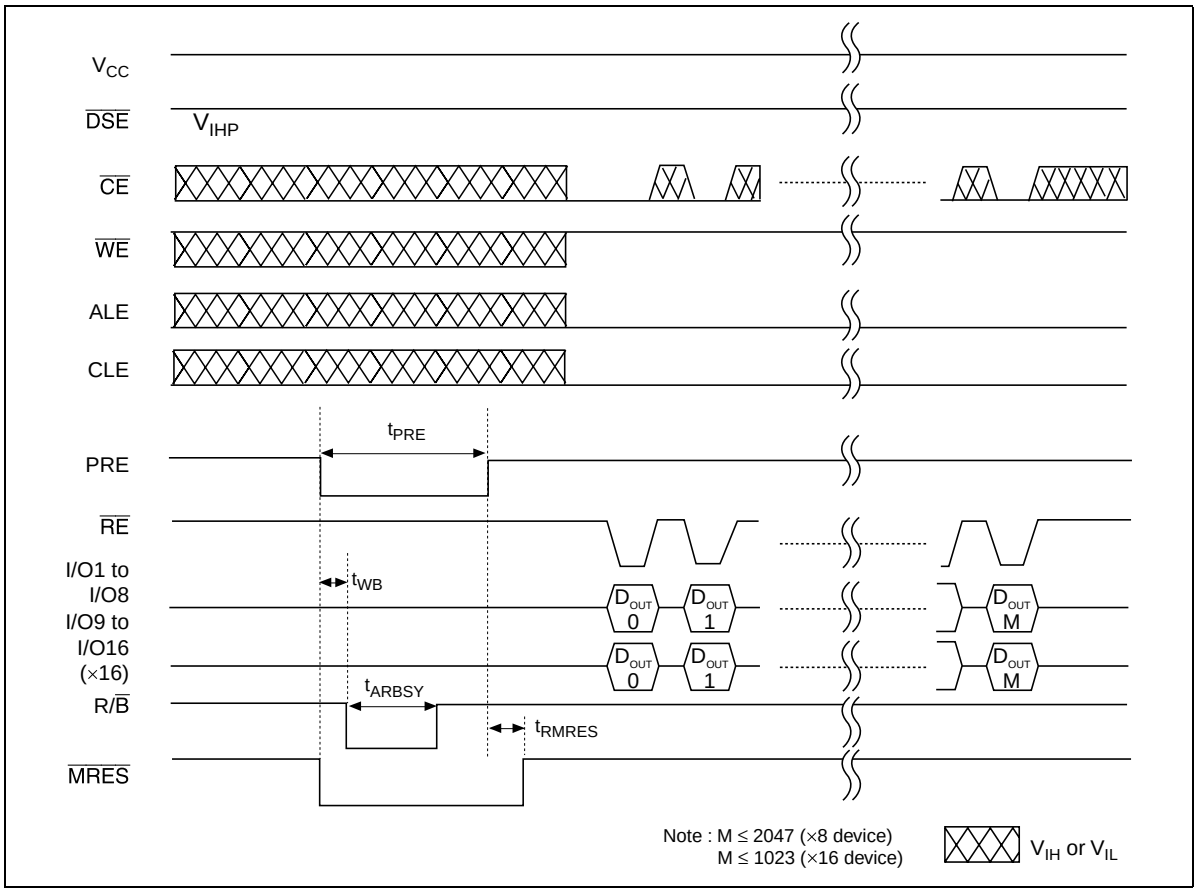
Note: 1. When PRE is turned low during busy, after the operation performed now is completed, this device transfer to the auto read mode.

Auto read (Deep standby mode which transferred by the command)

Case of $t_{PRE} < t_{ARBSY}$

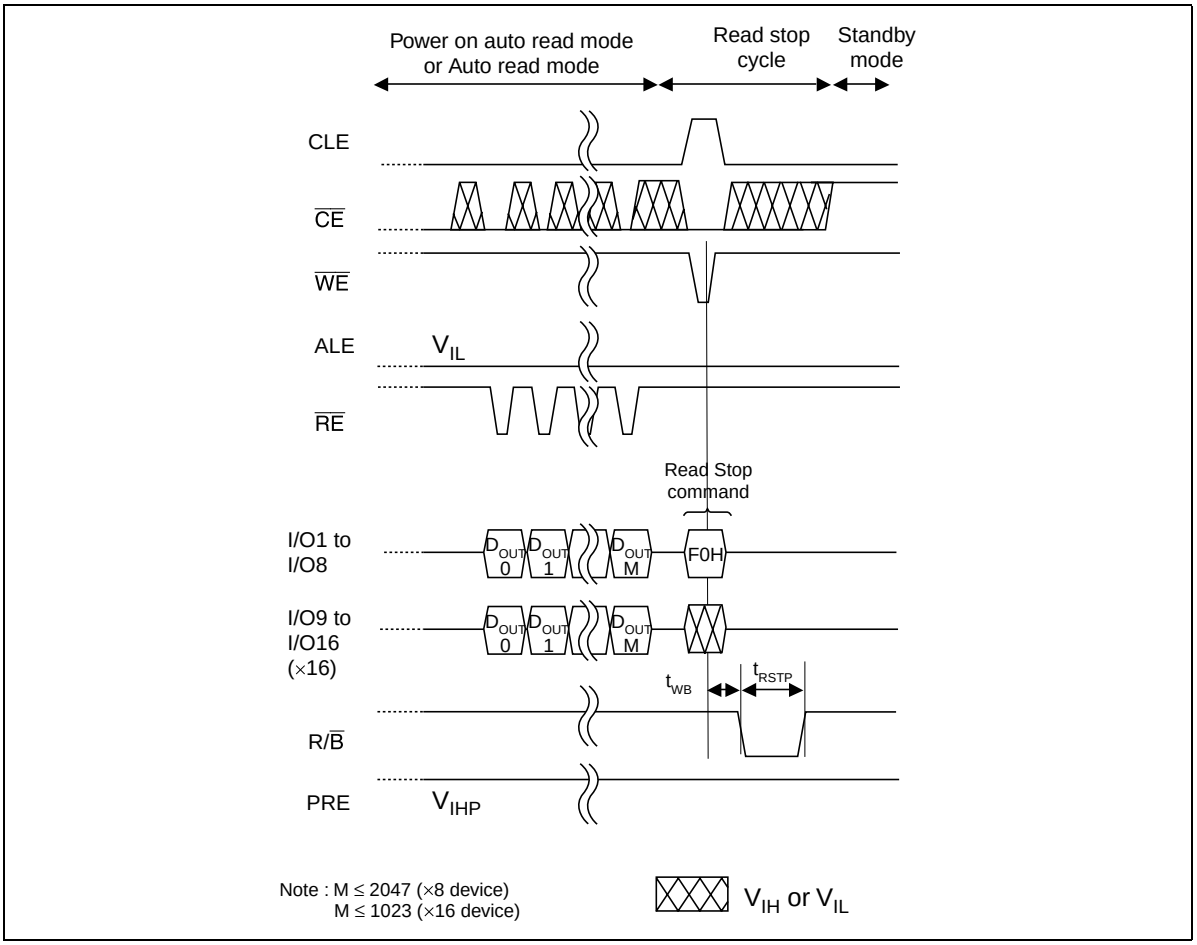


Case of $t_{PRE} \geq t_{ARBSY}$



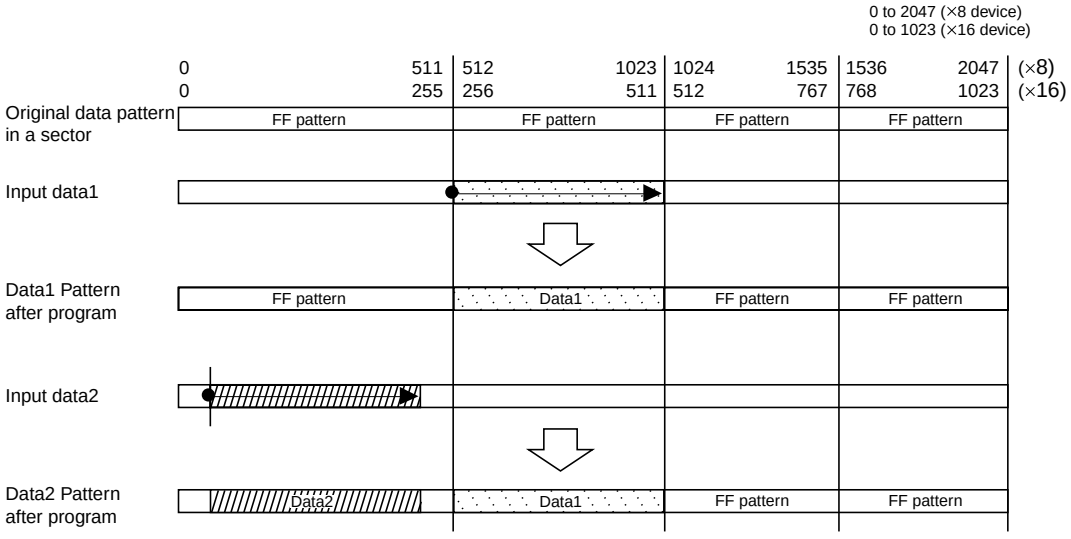
Auto read stop cycle

Read stop command F0H enables to finish power on auto read mode and auto read mode.



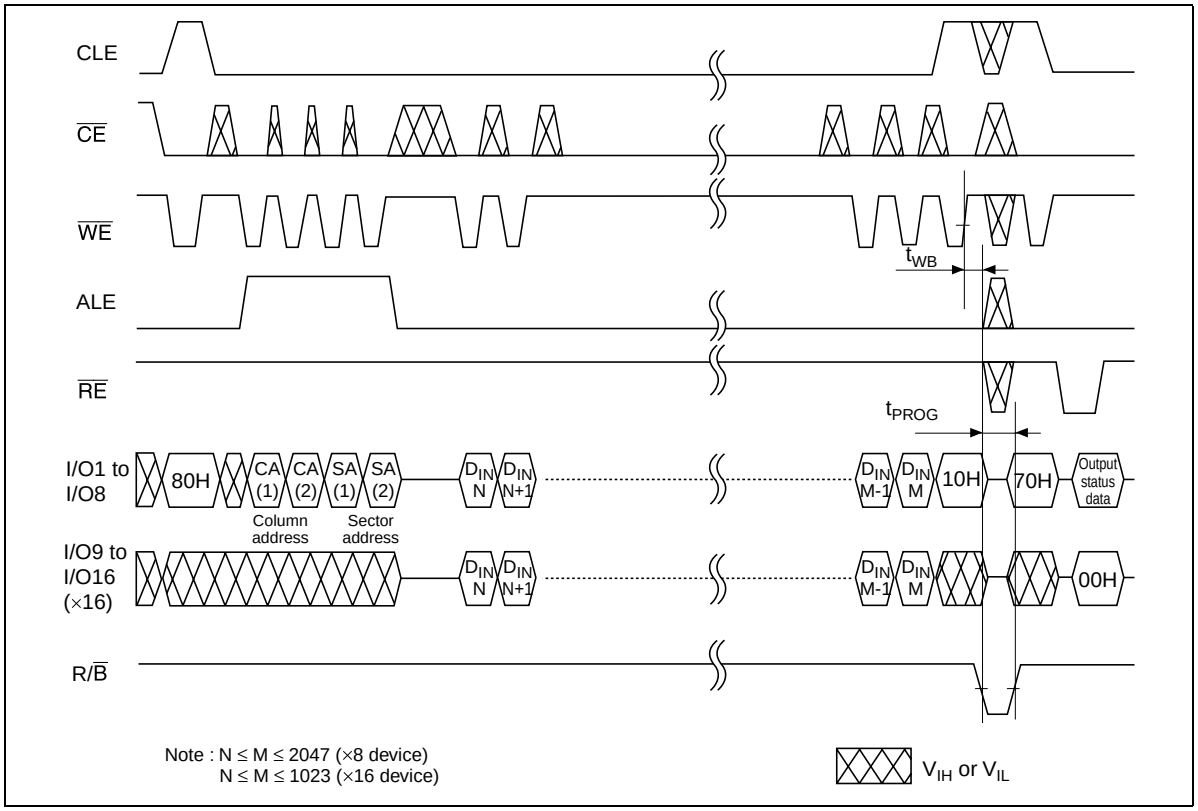
Program mode

The program mode is organized by the data input and the program. Data input command 80H is for the input address and the program data. And program command 10H makes the device start the program (Please refer to the next page). The maximum data size is 2 kbyte (1 kword for ×16 device).
One sector is divided by 4 pages. The size of page is 512byte. Each page is programmable just one time as well as the normal 2 kbyte programming (Please refer to the figure below).
The data at applied sector for program must be erased.
The data of erased sector is [FF]. The programmed bits in the sector goes “1” to “0”when they are programmed.



Note: Input only program data. It is not necessary to mask of the previous programmed data.

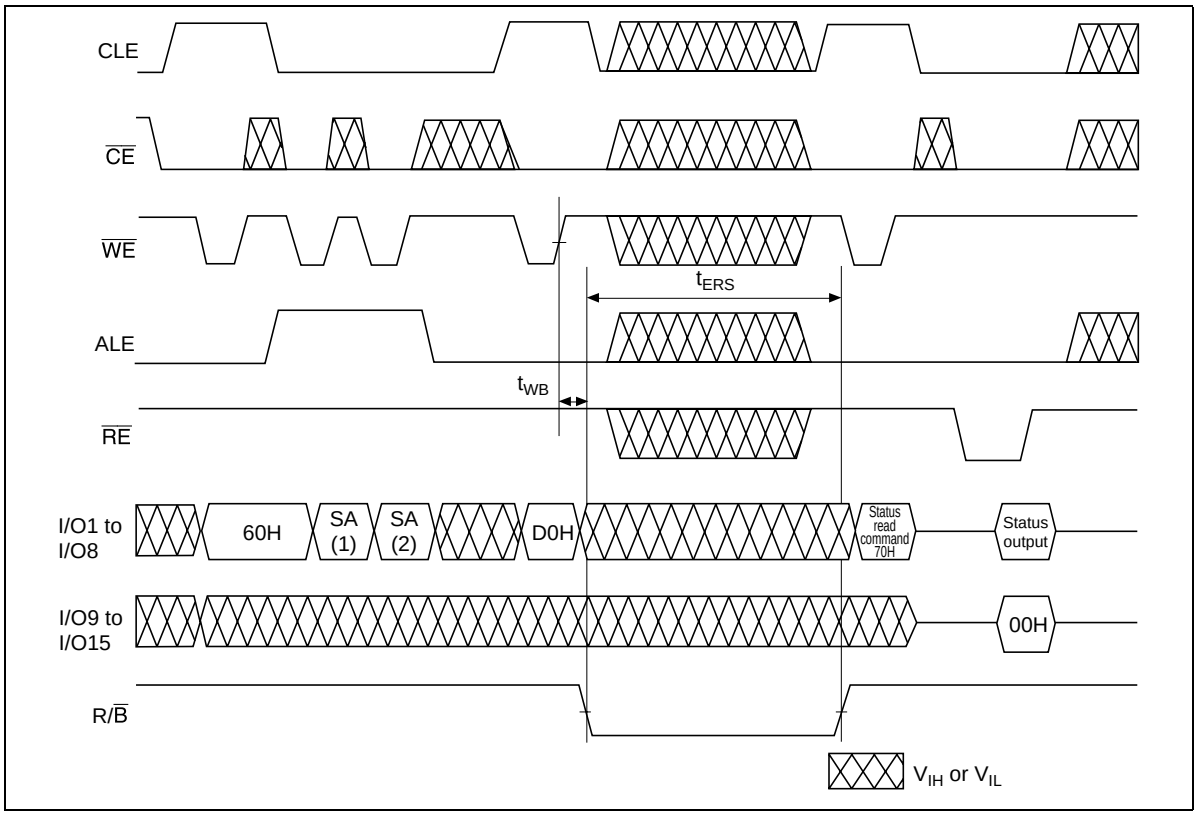
Program cycle



Erase mode

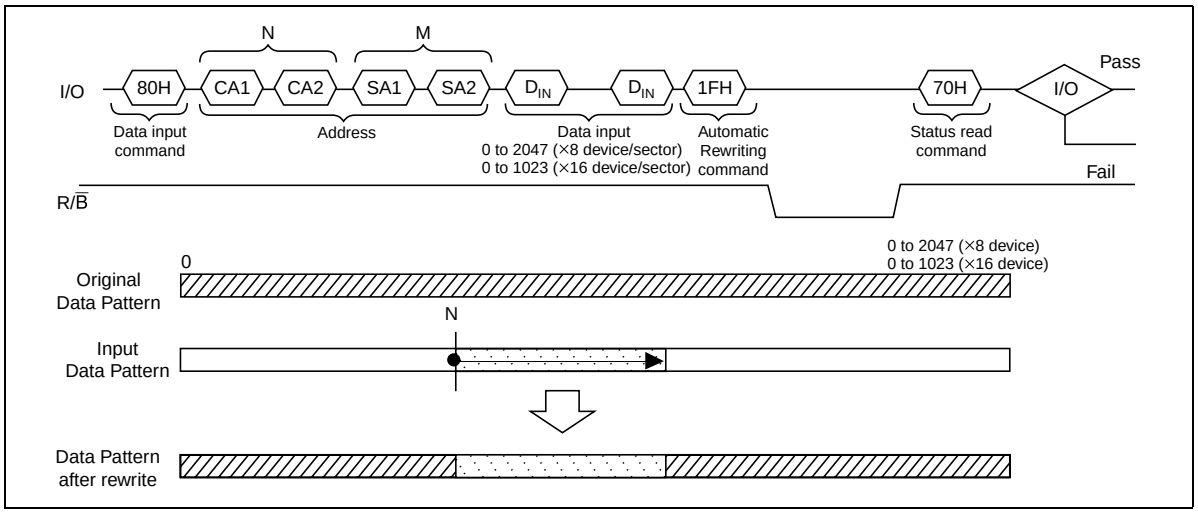
The erase mode is entered by command 60H. After inputting sector address, command D0H erases the sector data. The erase size is always 2 kbyte and the erase operation must be done in the sector.

Erase cycle

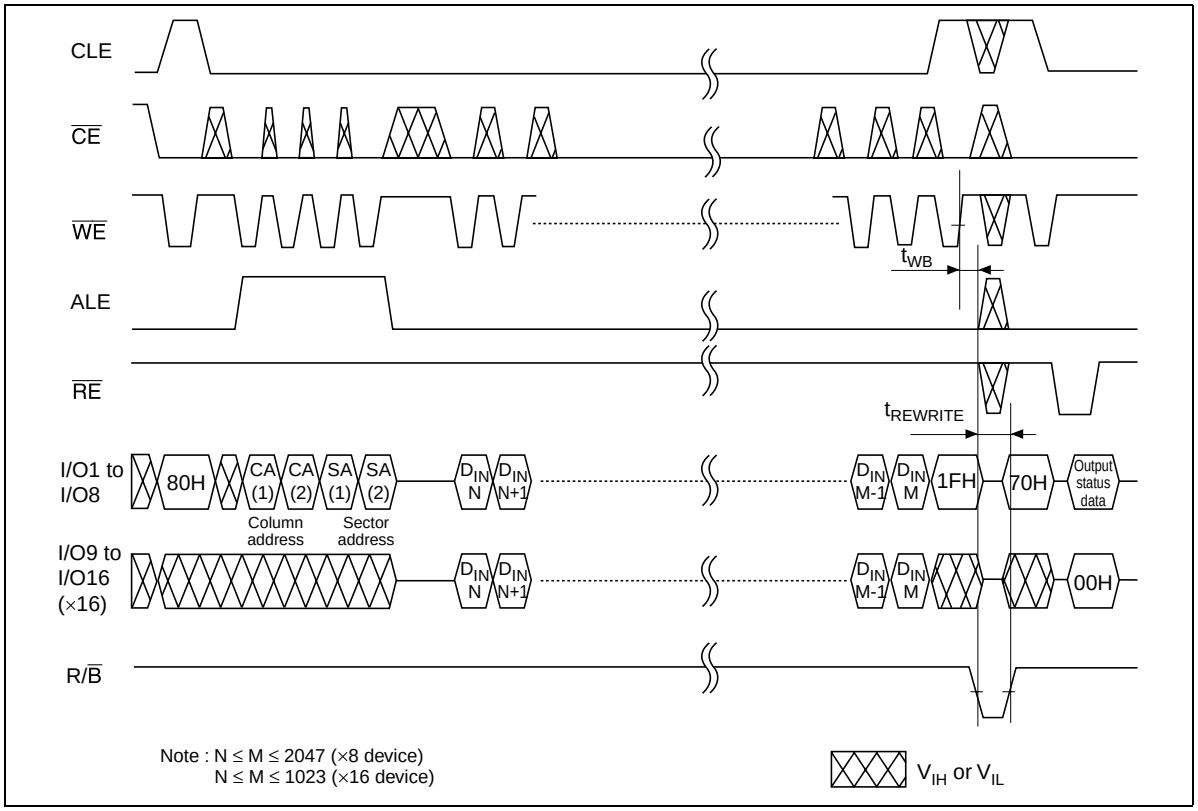


Rewrite mode

The rewrite mode is organized by the data input and the rewrite. Data input command 80H is for the input address and the rewrite data to be changed. And rewrite command 1FH makes the device start the rewrite (Please refer to the next page). The maximum data size is 2 kbyte (1 kword in case of ×16 device). By using rewrite, erase is automatically executed before programming, and the data can be rewritten for the sector. So the data before the programming operation can be either "1" or "0" (Please refer to the figure below).



Rewrite cycle



Notes on usage

1. Prohibition of undefined command input

The commands listed in the command definition can only be used in this device. It is prohibited to issue a command that is not defined in the list. If an undefined command is issued, the data held in the device may be lost.

2. Limitation of command input in the busy state

In the busy state, following two commands are acceptable. Do not issue any other command except below two commands.

- Status read 70H
- Read stop F0H (during read operation)

3. Commands that can be issued after the serial input command (80H)

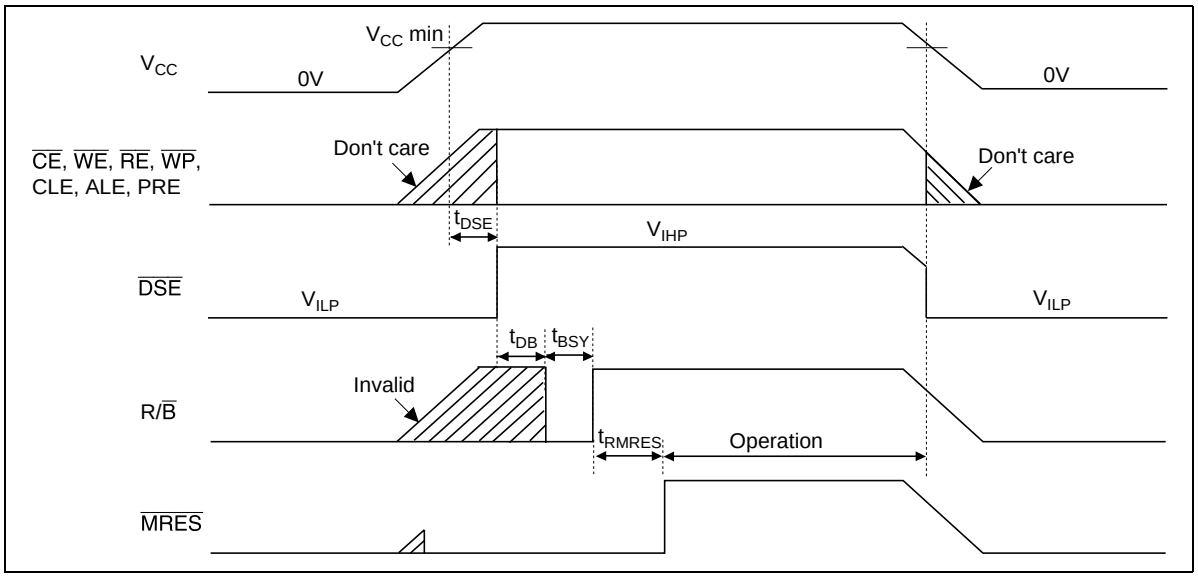
After the serial input command (80H) is issued, the rewriting and programming command (1FH, 10H) can be issued; do not issue any other command except 1FH and 10H after 80H.

4. R/$\overline{B}$(Ready/$\overline{busy}$) pin handing

R/$\overline{B}$ is an open-drain output pin, and it should be pulled up to V_{CC} with a resistance(more than 2kΩ).

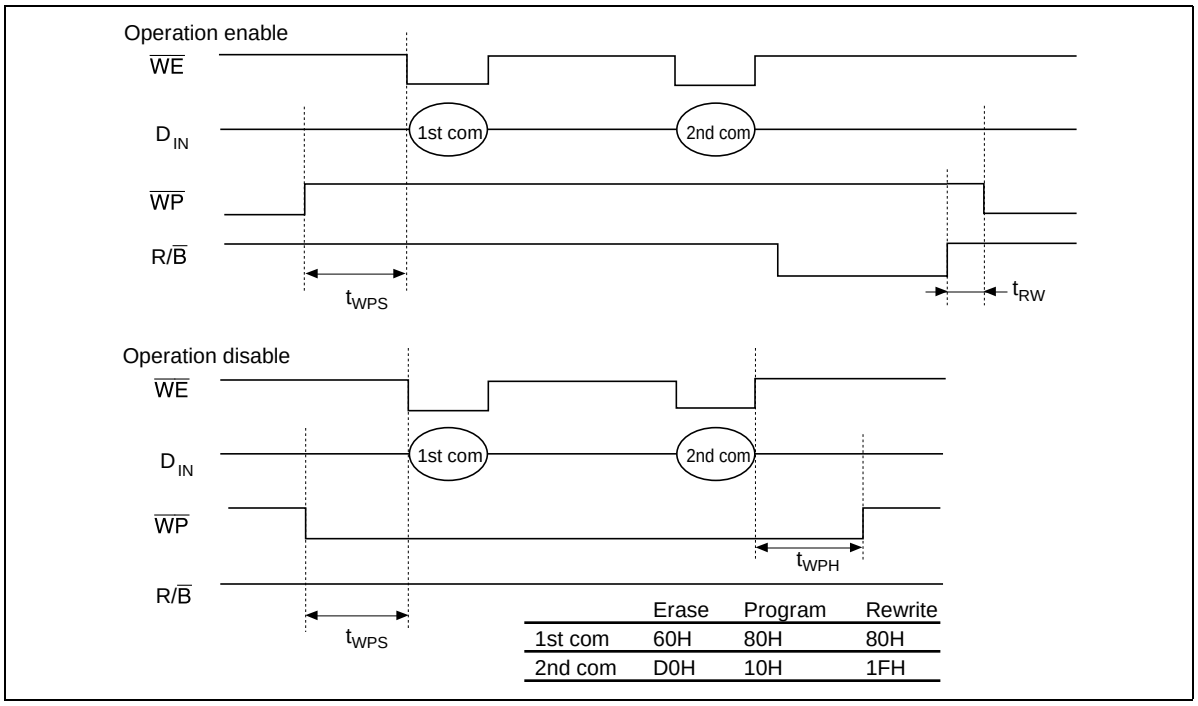
5. Notes on turning power on and off

The input signal levels may be unstable after power is on or off.
In order to prevent unexpected operation, use $\overline{DSE}$ as shown below.



6. Notes on $\overline{WP}$ signal

When $\overline{WP}$ is at the low level, the rewriting operation is disabled.
When using $\overline{WP}$ to control the operation, satisfy the timing shown below.



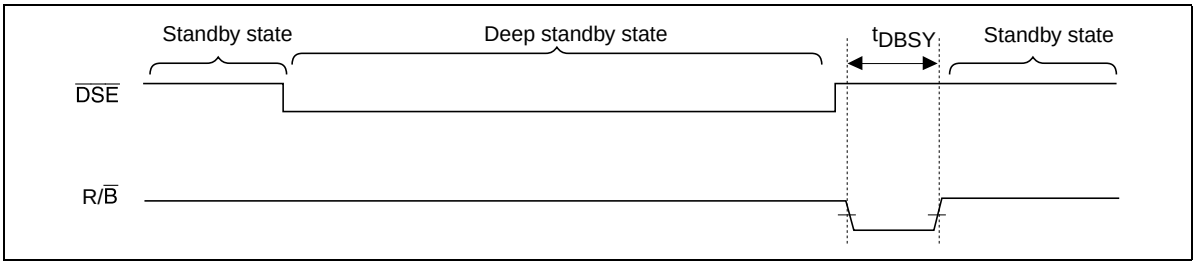
	Erase	Program	Rewrite
1st com	60H	80H	80H
2nd com	D0H	10H	1FH

7. Notes on $\overline{RE}$ signal

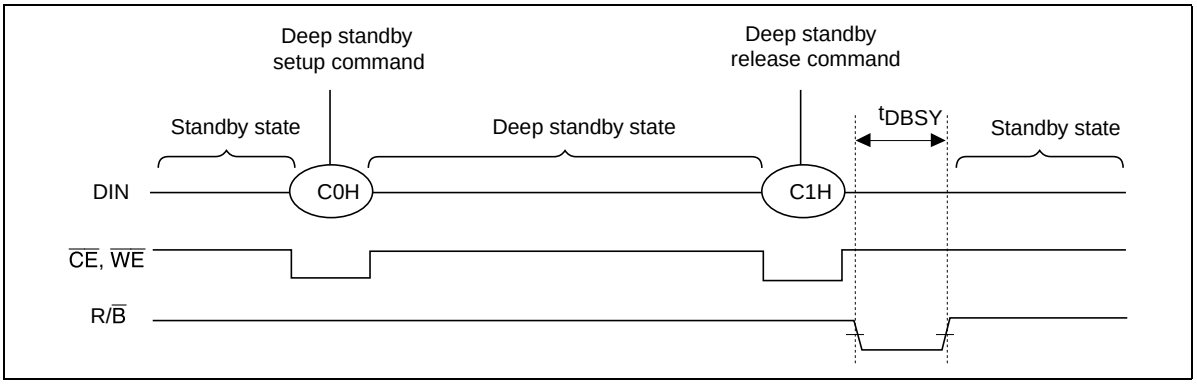
If the $\overline{RE}$ clock is sent before the address is input, the internal read operation may start unintentionally.
Be sure to send the $\overline{RE}$ clock after the address is input.

8. Deep standby mode

During command waiting or standby state, when $\overline{DSE}$ pin goes to low, the device transfers to deep standby state.
When $\overline{DSE}$ goes to high, the device returns from the deep standby state.
During command execution, going $\overline{DSE}$ low stops command operation. If $\overline{DSE}$ goes to low during erase/program/rewrite operation, the command operation is forced to terminate and the applied sector data is not guaranteed.



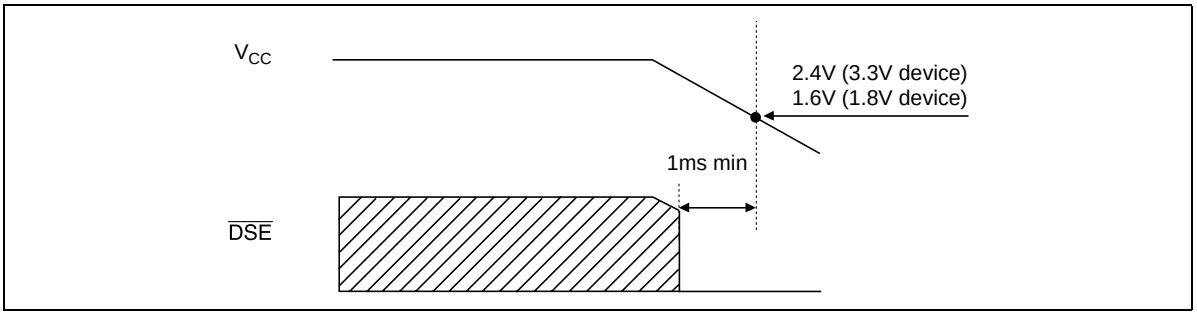
When $\overline{CE}$ becomes high after the C0H command input, the state of this device transfers to the deep standby state.
When $\overline{CE}$ becomes high after the C1H command input, the state of this device transfers from the deep standby state to the standby state.



9. Notes on the power supply down

Please do not turn off a power supply in busy status.
It is recommended to take either of following (1) or (2) measures on system side for unexpected power down.

(1) Please set $\overline{DSE}$=L when detecting the power down.
And erase any sector after the power supply is on.
The other sectors data is protected though applied sector data is invalid by doing this.

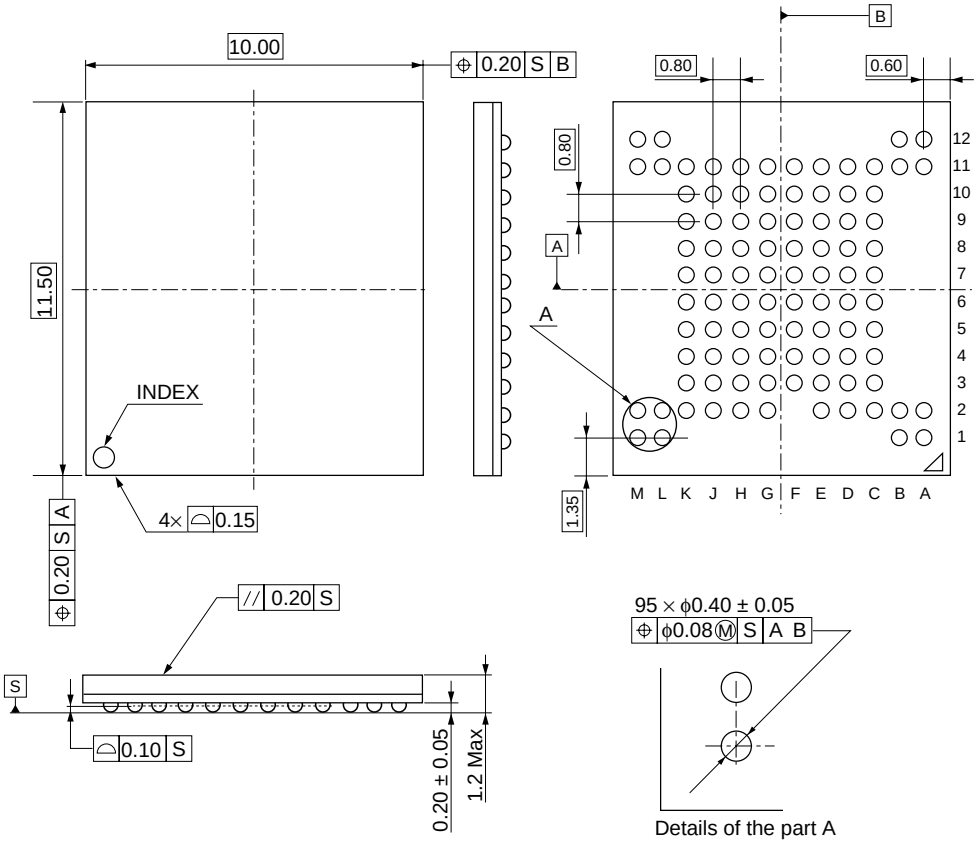


(2) Please store the operation record for back up.
When the power down is recognized to have occurred during erase/program/rewrite operation, erase applied sector after the power on.
The other sectors data is protected though applied sector data is invalid by doing this.

Package Dimensions

HN29V128A1ABP, HN29V128A0ABP, HN29A128A1ABP, HN29A128A0ABP Series (TBP-95V)

Unit: mm



Note: DatumA, B are defined as center line of terminal matrix.

Package CODE	TBP-95V
JEDEC	–
JEITA	–
Mass (reference value)	0.25 g

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

http://www.renesas.com

Colophon 0.0