RENESAS

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M6MGB/T64BS8AWG

67,108,864-BIT (4,194,304-WORD BY 16-BIT) CMOS FLASH MEMORY & 8,388,608-BIT (524,288-WORD BY 16-BIT) CMOS SRAM

Stacked-CSP (Chip Scale Package)

Description

The RENESAS M6MGB/T64BS8AWG is a Stacked Chip Scale Package (S-CSP) that contents 64M-bit Flash memory and 8M-bit SRAM in a 67-pin Stacked CSP for lead free use.

64M-bit Flash memory is a 4,194,304 words, single power supply and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR IV (Divided bit-line NOR IV) architecture for the memory cell. All memory blocks are locked and can not be programmed or erased, when F-WP# is Low. Using Software Lock Release function, program or erase operation can be executed.

8M-bit SRAM is a 524,288 words asynchronous SRAM fabricated by CMOS technology for the peripheral circuit and TFT type transistor for the memory cell.

The RENESAS M6MGB/T64BS8AWG is suitable for a high performance cellular phone and a mobile PC that are required to be small mounting area, weight and small power dissipation.

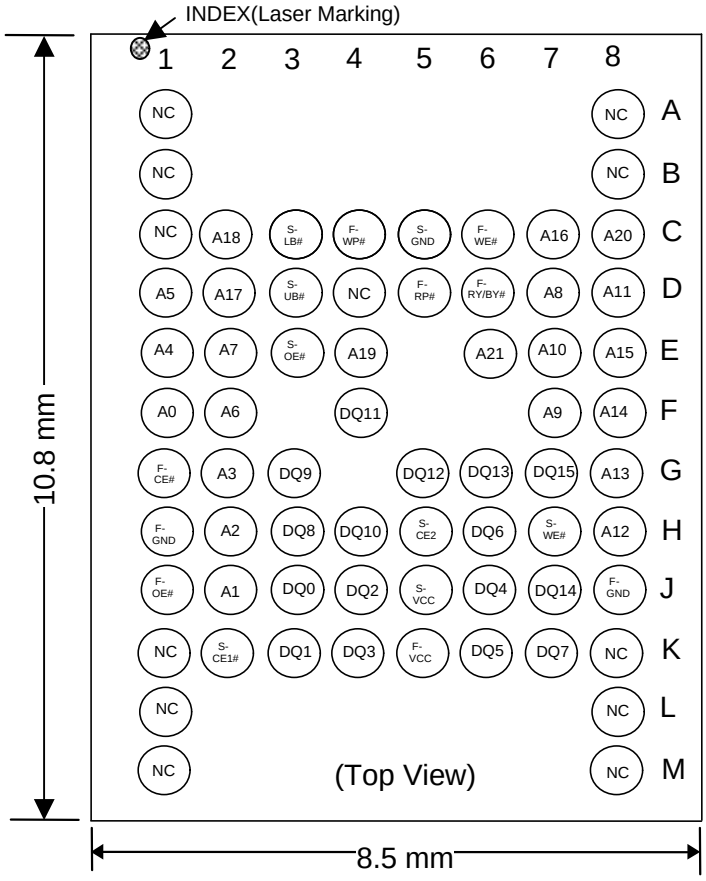
Features

Access Time	Flash	70ns (Max.)
	SRAM	85ns (Max.)
Supply Voltage		F-VCC =S-VCC=2.7 ~ 3.0V
Ambient Temperature		Ta= -40 ~ 85 degree
Package		67pin S-CSP,
		Ball pitch 0.80mm
		Outer-ball:Su-Ag-Cu

Application

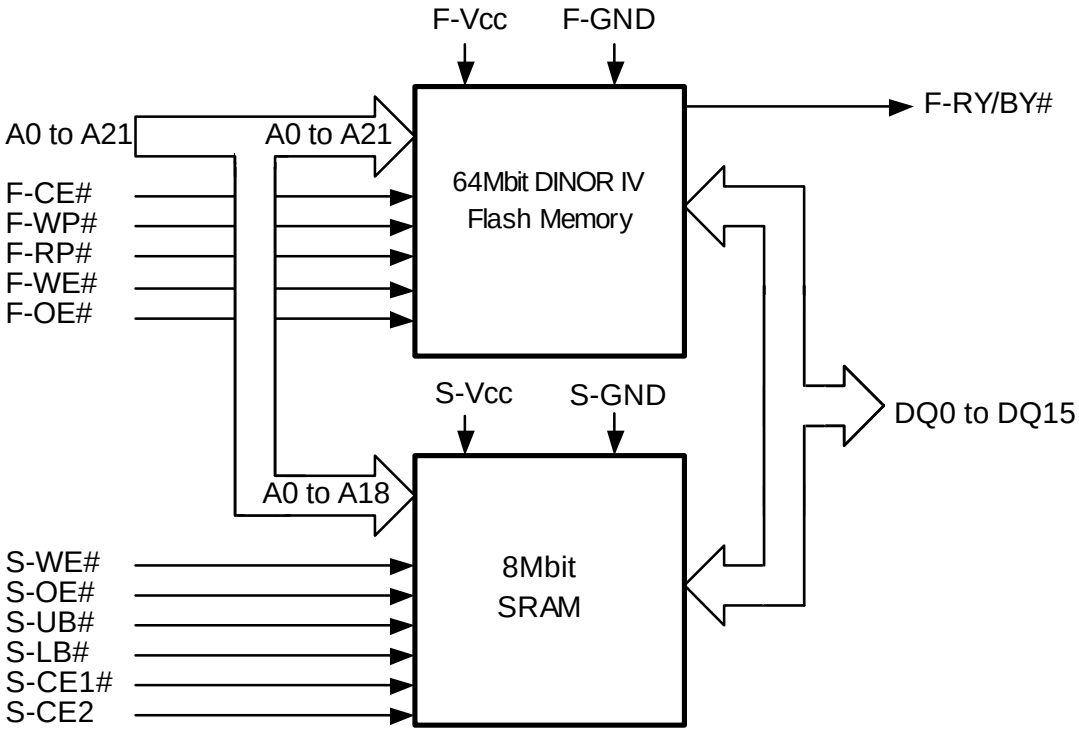
Mobile communication products

PIN CONFIGURATION (TOP VIEW)



F-VCC	: VCC for Flash Memory	F-OE#	:Output enable for Flash
S-VCC	: VCC for SRAM	S-OE#	:Output enable for SRAM
F-GND	: GND for Flash Memory	F-WE#	:Write enable for Flash
S-GND	: GND for SRAM	S-WE#	:Write enable for SRAM
A0-A18	: Common address for Flash/SRAM	F-WP#	:Write protect for Flash
A19-A21	: Address for Flash	F-RP#	:Reset power down for Flash
DQ0-DQ15	: Data I/O	F-RY/BY#	:Flash Ready/Busy
F-CE#	: Flash chip enable	S-LB#	:Lower byte control for SRAM
S-CE1#	: SRAM chip enable1	S-UB#	:Upper byte control for SRAM
S-CE2	: SRAM chip enable2	NC	:Non Connection

MCP Block Diagram



Note: In the Flash memory part there are “Vcc”, “GND”, “OE#” and “WE#” which mean “F-Vcc”, “F-GND”, “F-OE#” and “F-WE#”, respectively. In the SRAM part there are “GND”, “UB#”, “LB#”, “OE#” and “WE#” which mean “S-GND”, “S-UB#”, “S-LB#”, “S-OE#” and “S-WE#”, respectively.

Capacitance

Symbol	Parameter		Conditions	Limits			Unit
				Min.	Typ.	Max.	
CIN	Input capacitance	A21-A0, F-OE#, F-WE#, F-CE#, F-WP#, F-RP#, S-CE1#, S-CE2, S-OE#, S-WE#, S-LB#, S-UB#	Ta=25°C, f=1MHz, Vin=Vout=0V			18	pF
COUT	Output Capacitance	DQ15-DQ0, F-RY/BY#				22	pF

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