M5M5256DFP,VP -70G,-70GI,-70XG

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5256DFP,VP is 262,144-bit CMOS static RAMs organized as 32,768-words by 8-bits which is fabricated using high-performance 3 poly silicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery results in a high density and low power static RAM. Stand-by current is small enough for battery back-up application. It is ideal for the memory systems which require simple interface.

Especially the M5M5256DVP are packaged in a 28-pin thin small outline package.

FEATURE

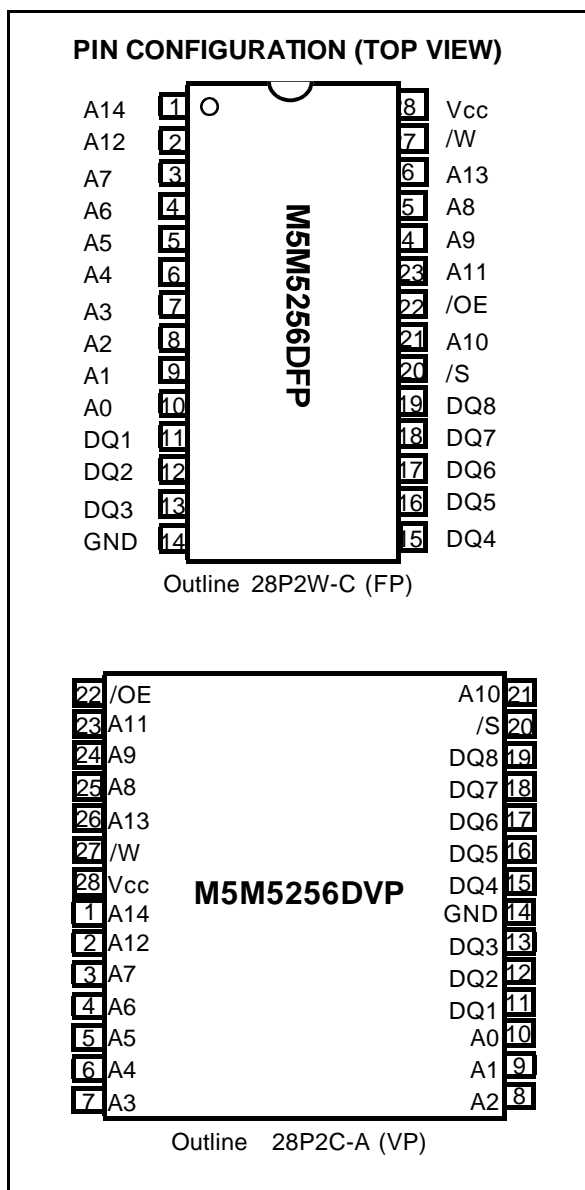| Type	Access time (max)	Oprating Temperature	Power supply current	
			Active (max)	Stand-by (max)
M5M5256DFP,VP -70G	70ns	0~70°C	45mA (Vcc=5.5V) 25mA (Vcc=3.6V)	20µA (Vcc=5.5V) 12µA (Vcc=3.6V)
M5M5256DFP,VP -70GI	70ns	-40~85°C		40µA (Vcc=5.5V) 24µA (Vcc=3.6V)
M5M5256DFP,VP -70XG	70ns	0~70°C		5µA (Vcc=5.5V) 2.4µA (Vcc=3.6V) 0.05µA (Vcc=3.0V Typical)

- Single 3.0~5.5V power supply
- No clocks, no refresh
- Data-Hold on +2.0V power supply
- Directly TTL compatible : all inputs and outputs
- Three-state outputs : OR-tie capability
- /OE prevents data contention in the I/O bus
- Common Data I/O
- Battery backup capability
- Low stand-by current .... 0.05µA(typ.)

PACKAGE

M5M5256DFP : 28 pin 450 mil SOP
M5M5256DVP : 28pin 8 X 13.4 mm^2 TSOP

APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)

A14	1		28	Vcc
A12	2		27	/W
A7	3		26	A13
A6	4		25	A8
A5	5	M5M5256DFP	24	A9
A4	6		23	A11
A3	7		22	/OE
A2	8		21	A10
A1	9		20	/S
A0	10		19	DQ8
DQ1	11		18	DQ7
DQ2	12		17	DQ6
DQ3	13		16	DQ5
GND	14		15	DQ4

Outline 28P2W-C (FP)

22	/OE		A10	21
23	A11		/S	20
24	A9		DQ8	19
25	A8		DQ7	18
26	A13	M5M5256DVP	DQ6	17
27	/W		DQ5	16
28	Vcc		DQ4	15
1	A14		GND	14
2	A12		DQ3	13
3	A7		DQ2	12
4	A6		DQ1	11
5	A5		A0	10
6	A4		A1	9
7	A3		A2	8

Outline 28P2C-A (VP)

M5M5256DFP,VP -70G,-70GI,-70XG

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5256DFP,VP is determined by a combination of the device control inputs /S, /W and /OE. Each mode is summarized in the function table.

A write cycle is executed whenever the low level /W overlaps with the low level /S. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of /W, /S, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable /OE directly controls the output stage. Setting the /OE at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting /W at a high level and /OE at a low level while /S are in an active state.

When setting /S at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by /S. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.
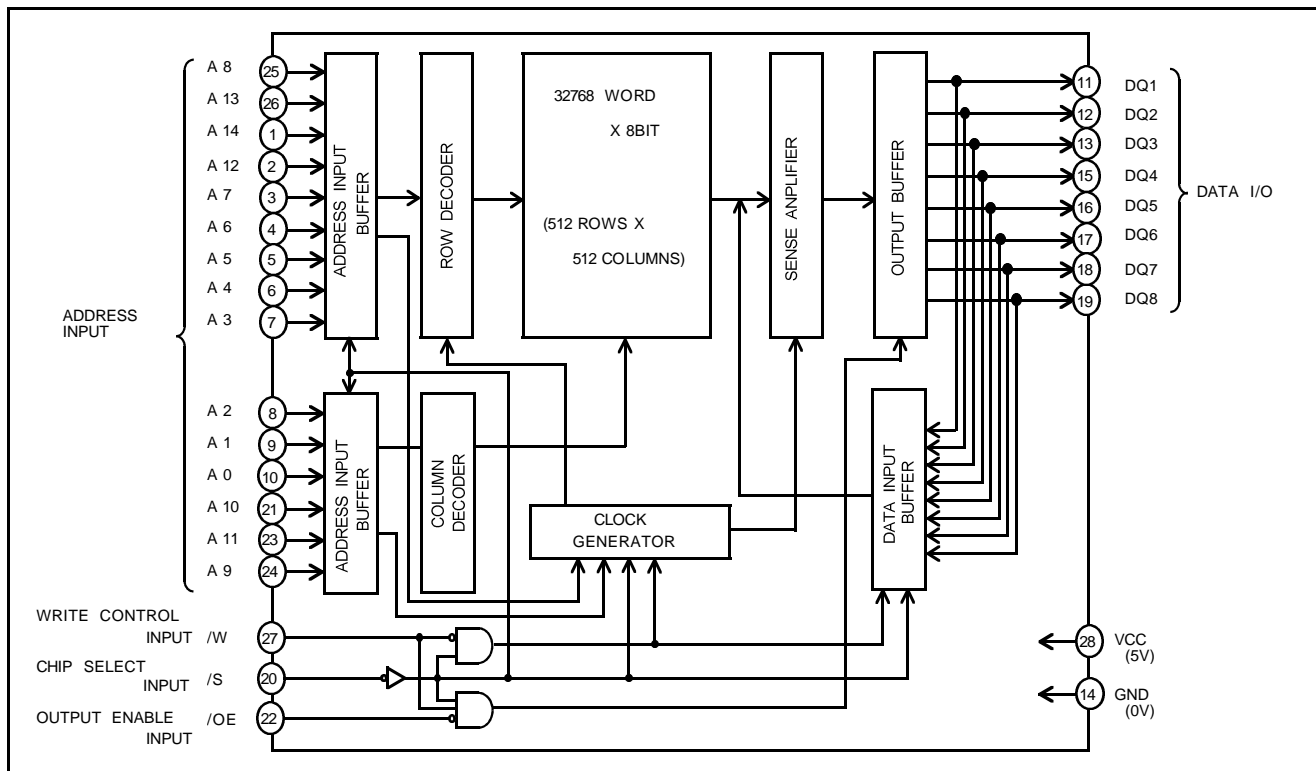
FUNCTION TABLE

/S	/W	/OE	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		High-impedance	Active

Note • "H" and "L" in this table mean VIH and VIL, respectively.
• "X" in this table should be "H" or "L".

BLOCK DIAGRAM

RENESAS
Renesas Technology Corp.

M5M5256DFP,VP -70G,-70GI,-70XG

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	-0.3*~7.0	V
V_I	Input voltage		-0.3*~Vcc+0.3 (Max 7.0)	V
V_O	Output voltage		0~Vcc	V
P_d	Power dissipation	Ta=25°C	700	mW
T_{opr}	Operating temperature	-G,-XG	0~70	°C
		-GI	-40~85	
T_{stg}	Storage temperature		-65~150	°C

* -3.0V in case of AC (Pulse width < 30ns)

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits1 (Vcc=3.3±0.3V) Min	Typ	Max	Limits2 (Vcc=5.0±0.5V) Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.0		Vcc +0.3	2.2		Vcc +0.3	V
V_{IL}	Low-level input voltage			-0.3*		0.6	-0.3*		0.8	V
V_{OH1}	High-level output voltage 1	I_{OH}=-1mA (Vcc=5.0±0.5V) I_{OH}=-0.5mA (Vcc=3.3±0.3V)		2.4			2.4			V
V_{OH2}	High-level output voltage 2	I_{OH}=-0.1mA (Vcc=5.0±0.5V) I_{OH}=-0.05mA (Vcc=3.3±0.3V)		Vcc -0.5			Vcc -0.5			V
V_{OL}	Low-level output voltage	I_{OL}=2mA (Vcc=5.0±0.5V) I_{OL}=1mA (Vcc=3.3±0.3V)				0.4			0.4	V
I_I	Input current	V_I=0~Vcc				±1			±1	µA
I_O	Output current in off-state	/S=V_{IH} or or /OE=V_{IH}, $V_{I/O}$=0~Vcc				±1			±1	µA
Icc1	Active supply current (AC, MOS level)	/S<0.2V, Output-open Other inputs<0.2V or >Vcc-0.2V	70ns		13	25		25	40	mA
			1MHz		1.5	3		2	4	
Icc2	Active supply current (AC, TTL level)	/S=V_{IL}, Output-open other inputs=V_{IH} or V_{IL}	70ns		14	25		25	45	mA
			1MHz		1.5	3		4	8	
Icc3	Stand-by current	/S>Vcc-0.2V, other inputs =0~Vcc	~25°C -G,-GI			1.2			2	µA
			~25°C -XG	0.05	0.3		0.1	0.4		
			~40°C -G,-GI			3.6			6	
			~40°C -XG		0.8			1.2		
			~70°C -G,-GI			12			20	
			~70°C -XG		2.4			5		
			~85°C -GI			24			40	
Icc4	Stand-by current	/S=V_{IH},other inputs=0~Vcc					0.33		3	mA

* -3.0V in case of AC (Pulse width ≤ 30ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			8	pF

Note 0: Direction for current flowing into an IC is positive (no mark).

1: Typical value is one at Ta = 25°C.

2: C_I, C_O are periodically sampled and are not 100% tested.

RENESAS

Renesas Technology Corp.

M5M5256DFP,VP -70G,-70GI,-70XG

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

Symbol	Parameter	Limits1 Vcc=3.3±0.3V		Limits2 Vcc=5.0±0.5V		Unit
		Min	Max	Min	Max	
t_{CR}	Read cycle time	70		70		ns
$t_a(A)$	Address access time		70		70	ns
$t_a(S)$	Chip select access time		70		70	ns
$t_a(OE)$	Output enable access time		35		35	ns
$t_{dis}(S)$	Output disable time after /S high		25		25	ns
$t_{dis}(OE)$	Output disable time after /OE high		25		25	ns
$t_{en}(S)$	Output enable time after /S low	5		5		ns
$t_{en}(OE)$	Output enable time after /OE low	5		5		ns
$t_V(A)$	Data valid time after address	10		10		ns

(2) WRITE CYCLE

Symbol	Parameter	Limits1 Vcc=3.3±0.3V		Limits2 Vcc=5.0±0.5V		Unit
		Min	Max	Min	Max	
t_{CW}	Write cycle time	70		70		ns
$t_w(W)$	Write pulse width	55		50		ns
$t_{su}(A)$	Address setup time	0		0		ns
$t_{su}(A-WH)$	Address setup time with respect to /W high	65		65		ns
$t_{su}(S)$	Chip select setup time	65		65		ns
$t_{su}(D)$	Data setup time	30		30		ns
$t_h(D)$	Data hold time	0		0		ns
$t_{rec}(W)$	Write recovery time	0		0		ns
$t_{dis}(W)$	Output disable time from /W low		25		25	ns
$t_{dis}(OE)$	Output disable time from /OE high		25		25	ns
$t_{en}(W)$	Output enable time from /W high	5		5		ns
$t_{en}(OE)$	Output enable time from /OE low	5		5		ns

(3) TIMING DIAGRAMS

Read cycle
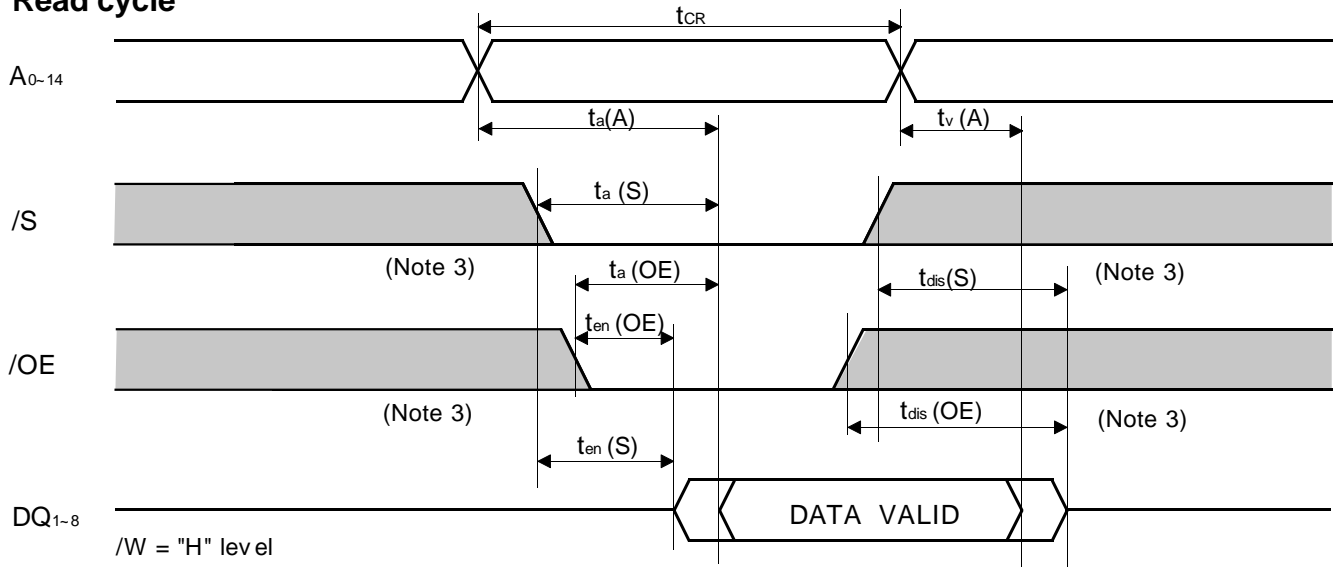
Write cycle (/W control mode)
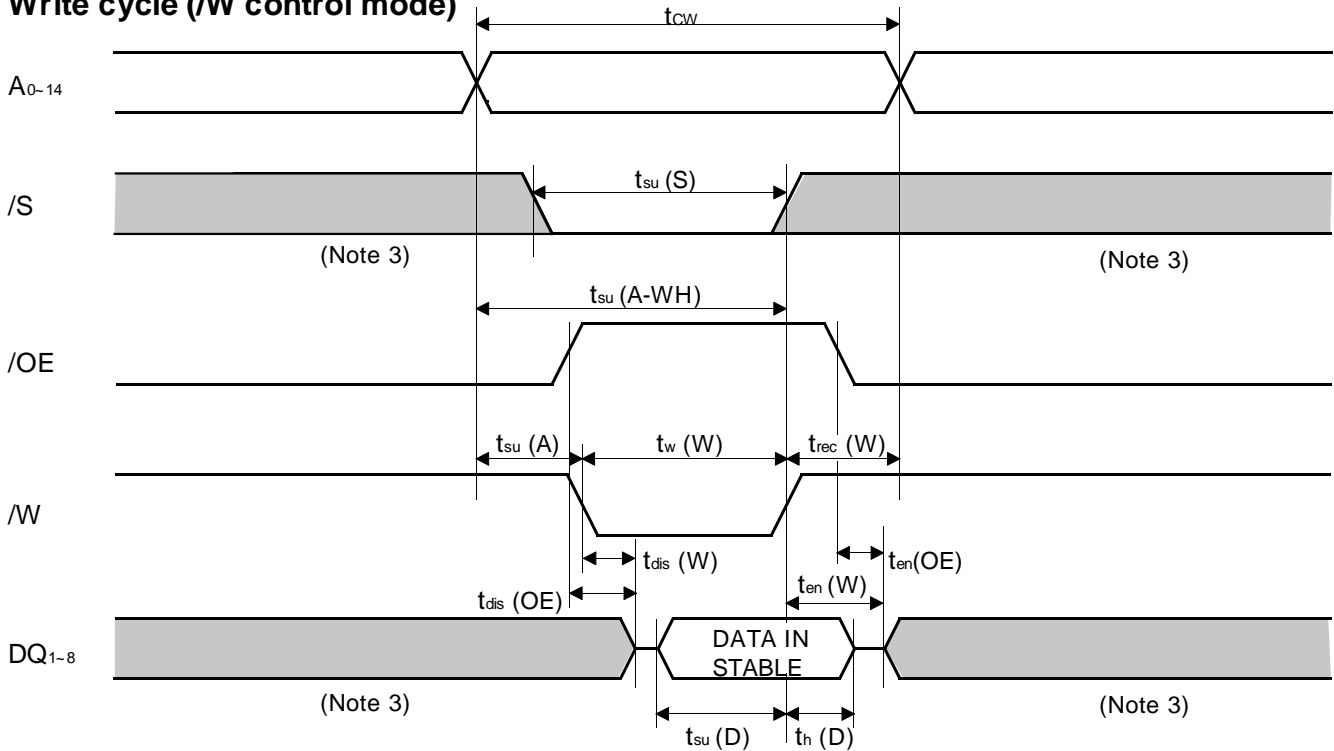
Write cycle (/S control mode)
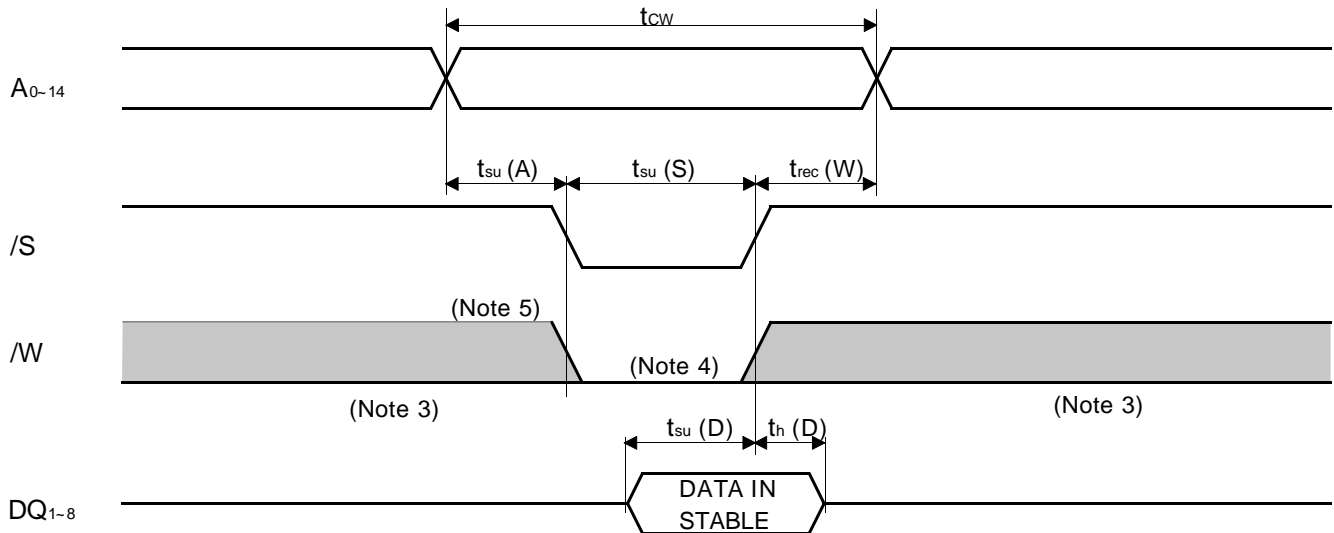
(4) MEASUREMENT CONDITIONS

Limits1:Vcc=3.3±0.3V

  Input pulse level .... V_{IH}=2.4V,V_{IL}=0.4V

  Input rise and fall time 5ns

  Reference level .... V_{OH}=V_{OL}=1.5V

  Output load .... Fig.1, CL=30pF

                      CL=5pF (for ten,tdis)

                      Transition is measured ±500mV from steady

                      state voltage. (for ten,tdis)
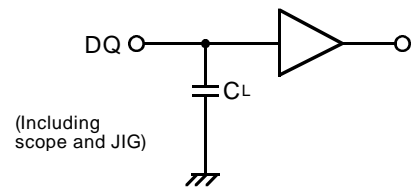
Fig.1 Output load

Limits2:Vcc=5.0±0.5V

  Input pulse level .... V_{IH}=2.4V,V_{IL}=0.6V

  Input rise and fall time 5ns

  Reference level .... V_{OH}=V_{OL}=1.5V

  Output load .... Fig.2, CL=100pF

                      CL=5pF (for ten,tdis)

                      Transition is measured ±500mV from steady

                      state voltage. (for ten,tdis)
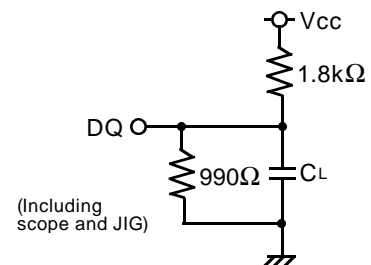
Fig.2 Output load

  Note 3 : Hatching indicates the state is "don't care".

       4 : Writing is executed in overlap of /S and /W low.

       5 : If /W goes low simultaneously with or prior to /S, the outputs remain in the high impedance state.

       6 : Don't apply inverted phase signal externally when DQ pin is output mode.

       7 : ten, tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ	Max	
$V_{CC\,(PD)}$	Power down supply voltage				2			V
$V_{I\,(/S)}$	Chip select input /S	$2.2V \leq V_{CC(PD)}$			2.2			V
		$2V \leq V_{CC(PD)} \leq 2.2V$				$V_{CC(PD)}$		V
$I_{CC\,(PD)}$	Power down supply current	$V_{CC} = 3V, /S \geq V_{CC}-0.2V,$ Other inputs=0~Vcc	~25°C	-G,-GI			1	μA
				-XG		0.05	0.2	
			~40°C	-G,-GI			3	
				-XG			0.6	
			~70°C	-G,-GI			10	
				-XG			2	
			~85°C	-GI			20	

(2) TIMING REQUIREMENTS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\,(PD)}$	Power down set up time		0			ns
$t_{rec\,(PD)}$	Power down recovery time		tCR			ns

(3) POWER DOWN CHARACTERISTICS

/S control mode
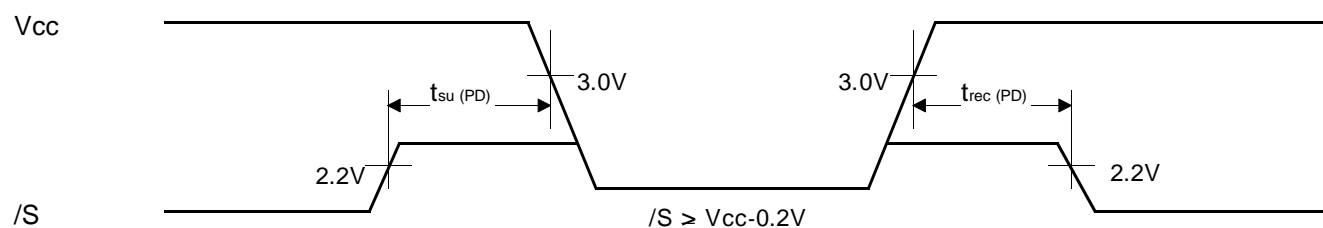
M5M5256DFP,VP -70G,-70GI,-70XG

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

RenesasTechnology Corp.

Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

RENESAS
RenesasTechnology Corp.