To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

32176 Group

Under Development

SINGLE-CHIP 32-BIT CMOS MICROCOMPUTER

Description

32176 Group is a 32-bit, single-chip RISC microcomputer with built-in flash memory, which was developed for use in general industrial and household equipment.
To make full use of microcomputer built-in mass volume flash memory, this microcomputer contains a variety of peripheral functions ranging from two independent blocks of 16-channel A-D converters to 37-channel multifunction timers, 10-channel DMAs, 4-channel serial I/Os, and 1-channel real-time debugger. Also included 2-channel Full-CAN modules and JTAG (boundary scan facility).
With lower power consumption and low noise characteris tics also considered, these microcomputers are ideal for embedded equipment applications.

Features

M32R RISC CPU core
- Uses the M32R family RISC CPU core (Instruction set common to all microcomputers in the M32R family)
- Five-stage pipelined processing
- Sixteen 32-bit general-purpose registers
- 16-bit/32-bit instructions implemented
- DSP function instructions (sum-of-products calculation using 56-bit accumulator)
- Built-in flash memory
- Built-in flash programming boot program
- Built-in RAM
- PLL clock generating circuit........................... Multiply by 4
- Oscillation stop detection function
- Maximum operating frequency of the CPU clock
  M32176F4VFP/M32176F3VFP/M32176F2VFP
  .... 32 MHz (when operating at -40°C to +125°C)
  M32176F4TFP/M32176F3TFP/M32176F2TFP
  .... 40 MHz (when operating at -40°C to +85°C)
- Single power supply: 5V (+0.5V) or 3.3V (+0.3V)

Table 1. Type Name List (32176 Group)

Type Name	RAM Size	ROM Size
M32176F4VFP/M32176F4TFP	24K bytes	512K bytes
M32176F3VFP/M32176F3TFP	24K bytes	384K bytes
M32176F2VFP/M32176F2TFP	24K bytes	256K bytes

37-channel multijunction timers (MJT)

Multifunction timers are incorporated that support various purposes of use.

16-bit output related timers........................... 11 channels
16-bit input/output related timers.................. 10 channels
16-bit input related timers .... 8 channels
32-bit input related timers .... 8 channels

- Flexible configuration is possible through interconnection of timers.
- The internal DMAC and A-D converter can be started by a timer.

Real-time Debugger

- Includes dedicated clock-synchronized serial I/O that can read and write the contents of the internal RAM independently of the CPU.
- Can look up and update the data table in real time while the program is running.
- Can generate a dedicated interrupt based on RTD communication.

Abundant internal peripheral functions

In addition to the timers and real-time debugger, the microcomputer contains the following peripheral functions.
- DMAC .... 10 channels
- A-D converters (Sample & hold function, Disconnection detector assist function, Injection current bypass circuit)
  .... 16 channels 10-bit converter
- Serial I/O .... 4 channels
- Interrupt controller ...... 23 interrupt sources, 8 priority levels
- Wait controller
- Full CAN (CAN Specification 2.0B active) .... 2 channels
- JTAG (boundary scan function, Mitsubishi original SDI debug function)
- Port input threshold level select function .... 3 levels

Designed to operate at high temperatures

To meet the need for use at high temperatures, the microcomputer is designed to be able to operate in the temperature range of -40 to +125°C when CPU clock operating frequency = 32 MHz. When CPU clock operating frequency = 40 MHz, the microcomputer can be used in the temperature range of -40 to +85°C.

Note: • This does not guarantee continuous operation at 125°C. If you are considering use of the microcomputer at 125°C, please consult Mitsubishi.

Applications

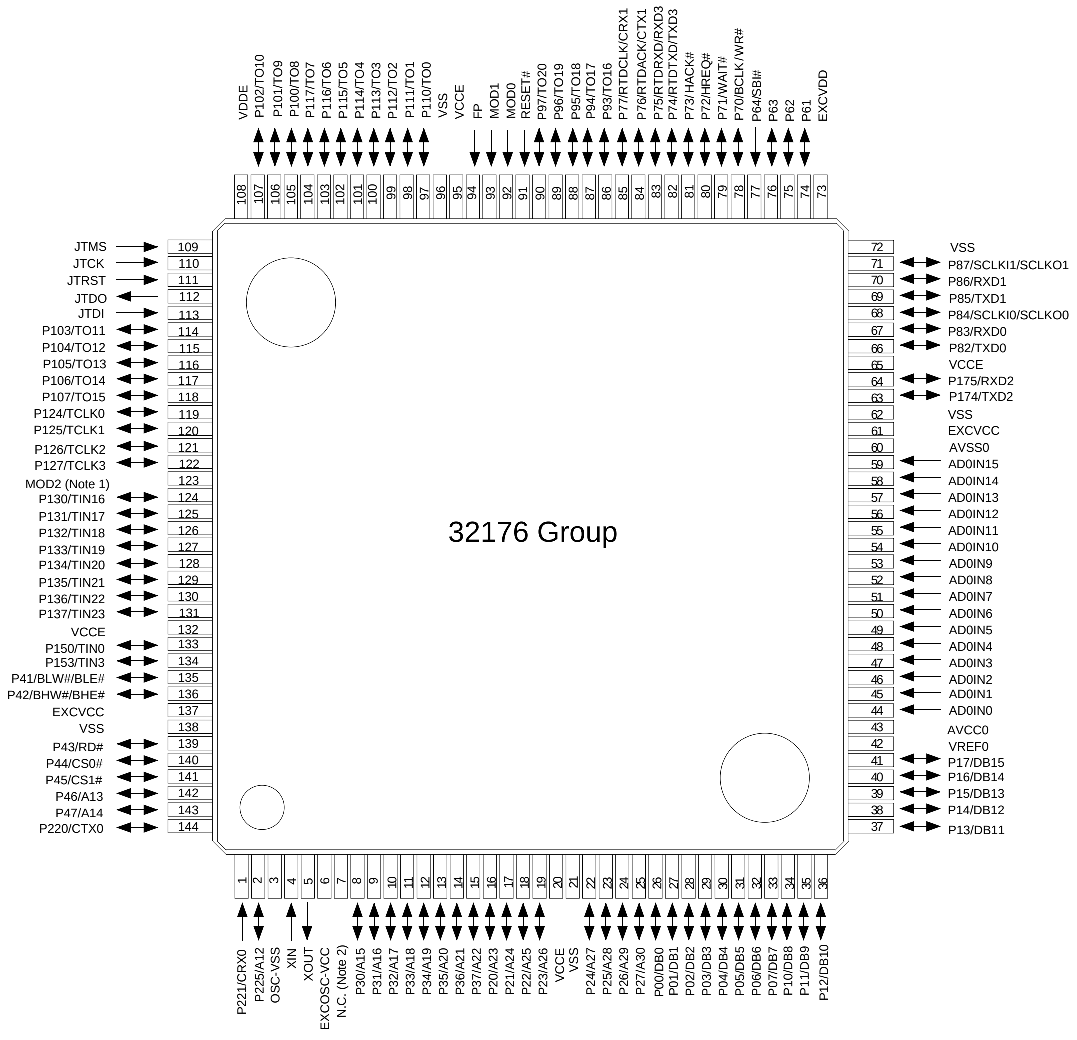
Automobile equipment control (e.g., Engine, ABS, AT), industrial equipment system control, and high-function OA equipment (e.g., PPC)

32176 Group

Under Development

SINGLE-CHIP 32-BIT CMOS MICROCOMPUTER

Pin Assignment (top view)



Package 144P6Q-A (0.5-mm pitch)

Note 1: Please be sure to connect MOD2 to ground (GND).
Note 2: The N.C. pin indicates "non connect," and is connected to ground in which no voltage change, power supply, etc.
Note: • It is shown that the pin (signal) with which "#" sticks to the last of a pin name (signal name) is "L" active pin (signal).

Figure 1. Pin Layout Diagram

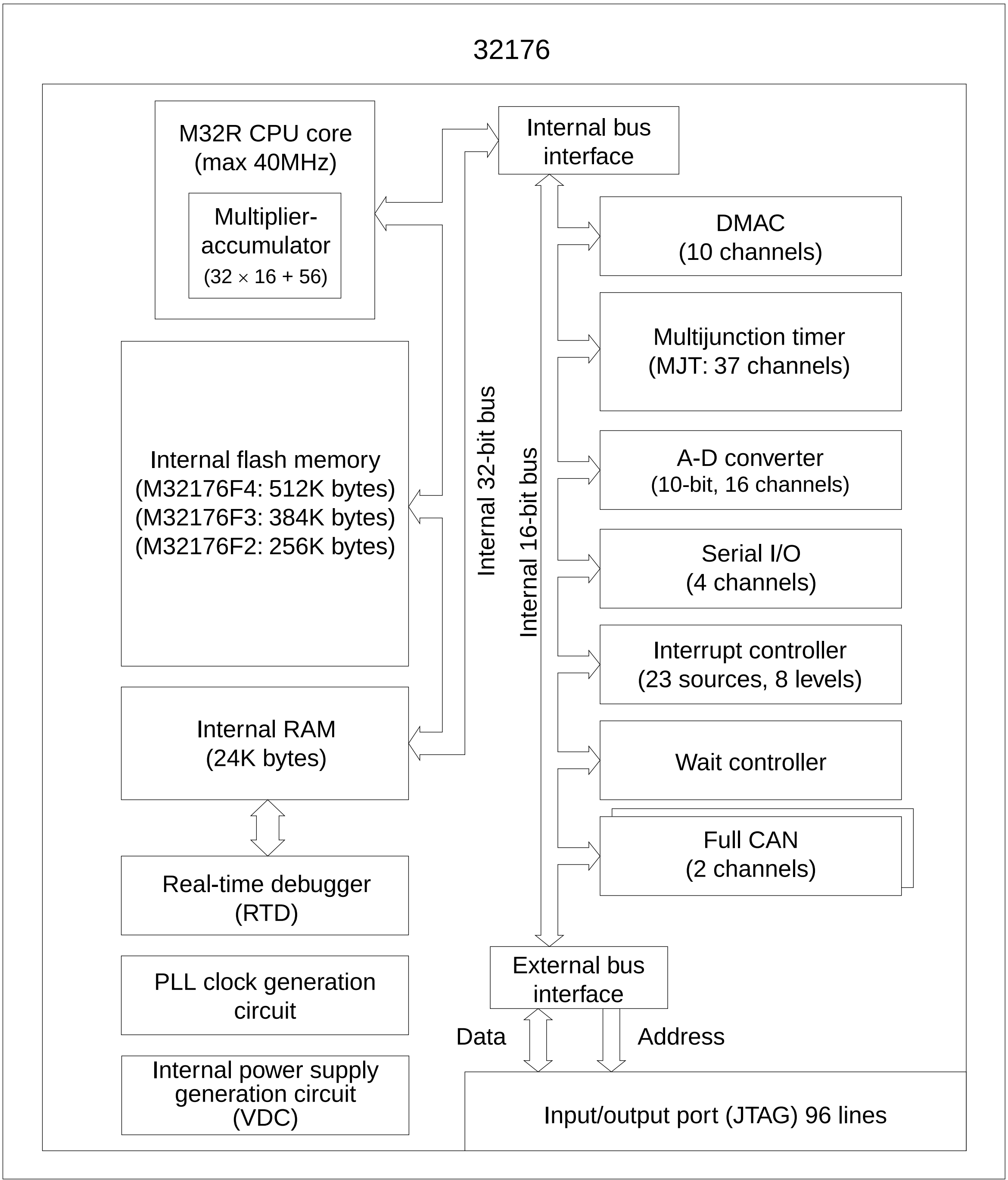


Figure 2. Block Diagram

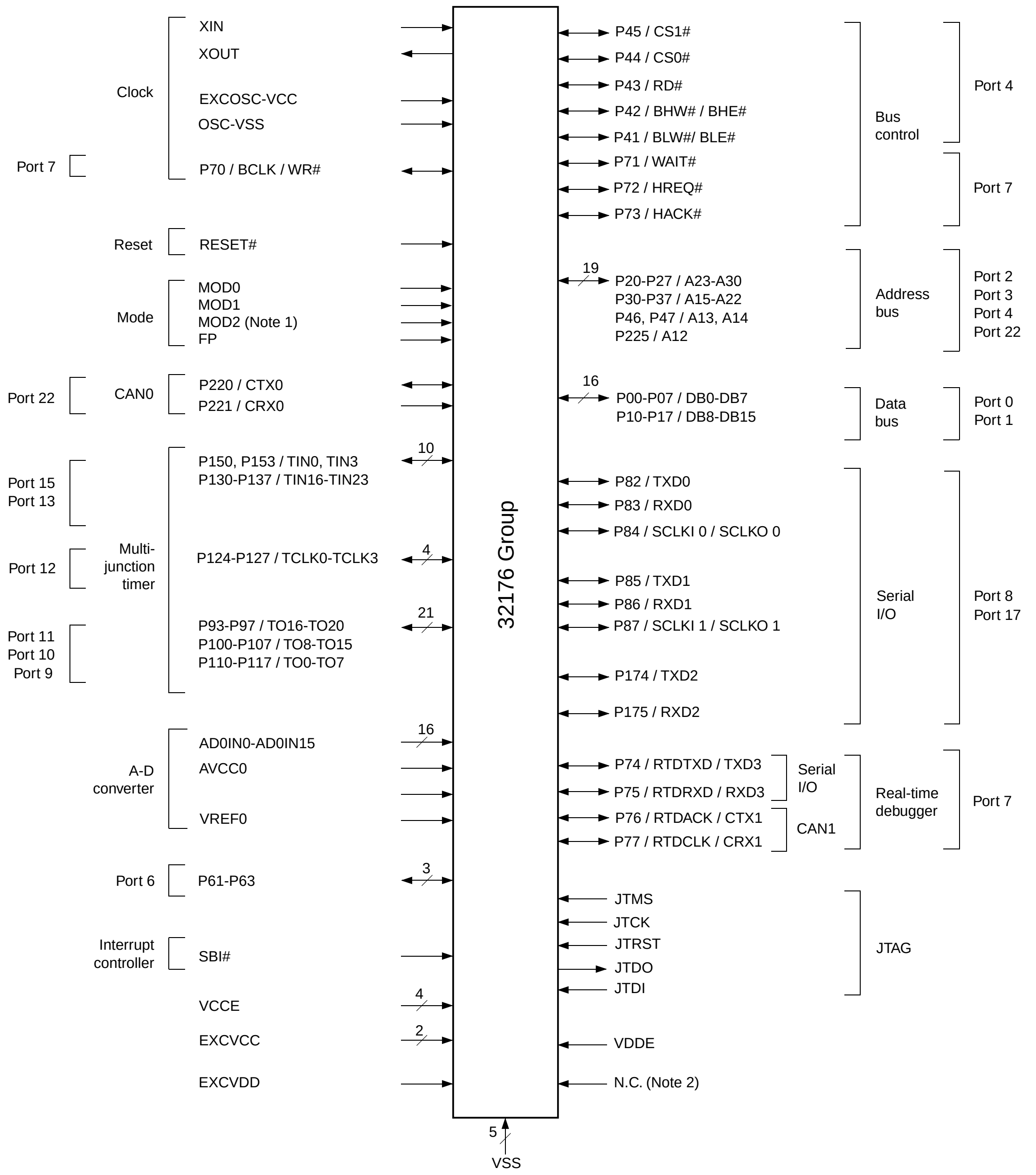
Table 2. Outline Performance (1/2)

Functional Block	Features
M32R CPU core	M32R family CPU core,internally configured in 32 bits Built-in multiplier-accumulator (32 × 16 + 56) Basic bus cycle: 25 ns (CPU clock frequency at 40 MHz, Internal peripheral clock frequency at 20 MHz) Logical address space: 4G bytes, linear General-purpose register: 32-bit register × 16, Control register: 32-bit register × 5 accumulator: 56 bits
External data bus	16 bits data bus
Instruction set	16-bit/32-bit instruction formats 83 instructions/9 addressing modes
Internal flash memory	M32176F4VFP/M32176F4TFP: 512K bytes M32176F3VFP/M32176F3TFP: 384K bytes M32176F2VFP/M32176F2TFP: 256K bytes Rewrite durability: 100 times
Internal RAM	24K bytes
DMAC	10 channels (DMA transfers between internal peripheral I/Os, between internal peripheral I/O and internal RAM, and between internal RAMs) Channels can be cascaded and can operate in combination with internal peripheral I/O
Multijunction timer	37 channels of multijunction timers • 16-bit output-related timers × 11 channels (single-shot, delayed single-shot) • 16-bit input/output-related timers × 10 channels (event count mode, single-shot, PWM, measurement) • 16-bit input-related timers × 8 channels (measurement, event count mode) • 32-bit input-related timers × 8 channels (measurement) Flexible timer configuration is possible through interconnection of channels using the event bus.
A-D converter	10-bit multifunction A-D converters • Input 16 channels • Scan-based conversion can be switched between N (N = 1-16) channels • Capable of interrupt conversion during scan • 8-bit/10-bit readout function • Sample & hold function • Disconnection detector assist function • Injection current bypass circuit
Serial I/O	4 channels (The serial I/Os can be set for synchronous serial I/O or UART. SIO2, SIO3 are UART mode only)
Real-time debugger (RTD)	1-channels dedicated clock-synchronized serial • Entire area of internal RAM • Can access the internal RAM for read/rewrite from outside independently of the CPU, and also generate an exclusive-use interrupt.
Interrupt controller	Controls interrupts from internal peripheral I/Os (Priority can be set to one of 8 levels including interrupt disabled)
Wait controller	Controls wait when accessing external extended area (1 to 4 wait cycles inserted + prolonged by external WAIT# signal input)
CAN	Two channels, each having 16-channel message slots
JTAG	Boundary-Scan function

Table 3. Outline Performance (2/2)

Function Block	Features
Clock	M32176F4VFP, M32176F3VFP, M32176F2VFP: CPU clock: maximum 32 MHz (for CPU, internal ROM, and internal RAM access) Internal peripheral clock (BCLK): maximum 16 MHz (for peripheral module access) External input clock (XIN): maximum 8 MHz, built-in × 4 PLL circuit M32176F4TFP, M32176F3TFP, M32176F2TFP: CPU clock: maximum 40 MHz (for CPU, internal ROM, and internal RAM access) Internal peripheral clock (BCLK): maximum 20 MHz (for peripheral module access) External input clock (XIN): maximum 10 MHz, built-in × 4 PLL circuit
Power Supply Voltage	5V (± 0.5V) or 3.3V (± 0.3V): single power supply voltage (The internal logic operates with 2.5V, however)
Operating temperature range (Note 1)	M32176F4VFP, M32176F3VFP, M32176F2VFP: -40 to +125°C (CPU clock 32 MHz, internal peripheral clock 16 MHz) M32176F4TFP, M32176F3TFP, M32176F2TFP: -40 to +85°C (CPU clock 40 MHz, internal peripheral clock 20 MHz)
Package	0.5mm pitches /144-pin plastic LQFP

Note 1: This does not mean that the microcomputer is guaranteed for continuous operation at 125°C. If 125°C applications are desired, please consult Mitsubishi.



Note 1: Please be sure to connect MOD2 to ground (GND).
Note 2: The N.C. pin indicates "non connect," and is connected to ground in which no voltage change, power supply, etc.
Note: • It is shown that the pin (signal) with which "#" sticks to the last of a pin name (signal name) is "L" active pin (signal).

Figure 3. Pin Function Diagram

Table 4. Description of Pin Function (1/4)

Type	Pin	Name	Input/Output	Function
Power	VCCE	Power supply	-	Power supply (5.0V ± 0.5V or 3.3V ± 0.3V).
	EXCVCC	Internal power supply	-	External capacitance connecting pin.
	VDDE	RAM power supply	-	Internal RAM backup power supply (5.0V ± 0.5V or 3.3V ± 0.3V).
	EXCVDD	Internal power supply of RAM	-	Backup power supply for the internal RAM, external capacitance connecting pin.
	VSS	Ground	-	Connect all VSS pins to ground (GND).
Clock	XIN	Clock input	Input	Clock input/output pins. These pins contain a PLL-based frequency multiply-by-4, so input the clock whose frequency is quarter the operating frequency. (XIN input = 10 MHz when CPU clock operates at 40 MHz)
	XOUT	Clock output	Output	
	BCLK	System clock	Output	Outputs a clock twice the externally sourced clock frequency, XIN (when the internal CPU memory clock is 80 MHz, BCLK output = 20 MHz). Use this output when external sync design is desired.
	EXCOSC -VCC	Internal power supply	-	External capacitance connecting pin.
	OSC-VSS	Ground	-	Connect OSC-VSS to ground.
Reset	RESET#	Reset	Input	This pin resets the internal circuits.
Mode	MOD0, MOD1	Mode	Input	These pins set an operation mode. MOD0 / MOD1 / Mode 0 / 0 / Single-chip mode 0 / 1 / Expanded external mode 1 / 0 / Processor mode (Boot mode) (Note 1) 1 / 1 / (Reserved)
	MOD2	Mode	Input	Please be sure to connect MOD2 to ground (GND).
Flash-only	FP	Flash Protect	Input	This pin protects the flash memory against E/W in hardware.
Address bus	A12-A30	Address bus	Output	19 lines of address bus (A12-A30) are provided to accommodate two channels of 1 MB memory space (max.) connected external to the chip. A31 is not output.
Data bus	DB0-DB15	Data bus	Input/output	This is a 16-bit data bus connecting to an external device. During write cycle, the microcomputer outputs BHW# or BLW# to indicate the valid byte write position of the 16-bit data bus. During read cycle, the microcomputer always reads the full 16-bit data bus. Transferred to the internal circuit of the M32R, however, is the data at only the valid byte position.

Note 1: In boot mode, the FP pin must be at the high level.

Table 5. Description of Pin Function (2/4)

Type	Pin	Name	Input/Output	Function
Bus Control	CS0#, CS1#	Chip select	Output	Chip select signals for external devices.
	RD#	Read	Output	This signal is output when reading external devices.
	WR#	Write	Output	This signal is output when writing external devices.
	BHW#	Byte High Write	Output	When writing to an external device, this signal indicates the valid byte position to which data is transferred. BHW# and BLW# correspond to the upper address side (bits 0-7 are valid) and the lower address side (bits 8-15 are valid), respectively.
	BLW#	Byte Low Write	Output	
	BHE#	Byte High Enable	Output	During an external device access, this signal indicates that the high-order data (bits 0-7) is valid.
	BLE#	Byte Low Enable	Output	During an external device access, this signal indicates that the low-order data (bits 8-15) is valid.
	WAIT#	Wait	Input	If WAIT# input is low when the M32R accesses external devices, the wait cycle extended.
	HREQ#	Hold request	Input	This pin is used by an external device to request control of the external bus. The M32R goes to a hold state when HREQ# input is pulled low.
	HACK#	Hold acknowledge	Output	This signal indicates to the external device that the M32R has entered a hold state and relinquished control of the external bus.
Multijunction timer	TIN0, TIN3 TIN16-TIN23	Timer input	Input	Input pin for multijunction timer.
	TO0 -TO20	Timer output	Output	Output pin for multijunction timer.
	TCLK0 -TCLK3	Timer clock	Input	Clock input pin for multijunction timer.
A-D converter	AVCC0	Analog power upply	-	AVCC0 is the power supply for the A-D0 converters. Connect AVCC0 to the power supply (5V or 3.3V).
	AVSS0	Analog ground	-	AVSS0 is the analog ground for the A-D0 converters. Connect to AVSS0 ground.
	AD0IN0 -AD0IN15	Analog input	Input	16-channel analog input pin for A-D0 converter.
	VREF0	Reference voltage input	Input	VREF0 is the reference voltage input pin (5V or 3.3V) for the A-D0 converters.
Interrupt controller	SBI#	System break interrupt	Input	System break interrupt (SBI) input pin of the interrupt controller.

Table 6. Description of Pin Function (3/4)

Type	Pin	Name	Input/Output	Function
Serial I/O	SCLKI0/ SCLKO0	UART transmit/ receive clock output or CSIO transmit/receive clock input/output	Input/output	When Channel 0 is in UART mode: Clock output derived from BRG output by dividing it by 2 When Channel 0 is in CSIO mode: Transmit/receive clock input when external clock is selected Transmit/receive clock output when internal clock is selected
	SCLKI1/ SCLKO1	UART transmit/ receive clock output or CSIO transmit/receive clock input/output	Input/output	When Channel 1 is in UART mode: Clock output derived from BRG output by dividing it by 2 When Channel 1 is in CSIO mode: Transmit/receive clock input when external clock is selected Transmit/receive clock output when internal clock is selected
	TXD0	Transmit data	Output	Transmit data output pin of serial I/O channel 0
	RXD0	Receive data	Input	Receive data input pin of serial I/O channel 0
	TXD1	Transmit data	Output	Transmit data output pin of serial I/O channel 1
	RXD1	Receive data	Input	Receive data input pin of serial I/O channel 1
	TXD2	Transmit data	Output	Transmit data output pin of serial I/O channel 2
	RXD2	Receive data	Input	Receive data input pin of serial I/O channel 2
	TXD3	Transmit data	Output	Transmit data output pin of serial I/O channel 3
	RXD3	Receive data	Input	Receive data input pin of serial I/O channel 3
Real-time Debugger	RTDTXD	Transmit data	Output	Serial data output pin of the Real-time Debugger
	RTDRXD	Receive data	Input	Serial data input pin of the Real-time Debugger
	RTDCLK	Clock input	Input	Serial data transmit/receive clock input pin of the Real-time Debugger
	RTDACK	Acknowledge	Output	This pin outputs a low pulse synchronously with the Real-time Debugger's first clock of serial data output word. The low pulse width indicates the type of the command/data the Real-time Debugger has received.
CAN	CTX0, CTX1	Transmit data	Output	Data output pin from CAN module.
	CRX0, CRX1	Receive data	Input	Data input pin to CAN module.
JTAG	JTMS	Test mode	Input	Test select input for controlling the test circuit's state transition.
	JTCK	Clock	Input	Clock input to the debugger module and test circuit.
	JTRST	Test reset	Input	Test reset input for initializing the test circuit asynchronously.
	JTDO	Serial output	Output	Serial output of test instruction code or test data.
	JTDI	Serial input	Input	Serial input of test instruction code or test data.

Table 7. Description of Pin Function (4/4)

Type	Pin	Name	Input/Output	Function
Input/output Port (Note 1)	P00-P07	Input/output port 0	Input/output	Programmable input/output port.
	P10-P17	Input/output port 1	Input/output	Programmable input/output port.
	P20-P27	Input/output port 2	Input/output	Programmable input/output port.
	P30-P37	Input/output port 3	Input/output	Programmable input/output port.
	P41-P47	Input/output port 4	Input/output	Programmable input/output port.
	P61-P63	Input/output port 6	Input/output	Programmable input/output port.
	P70-P77	Input/output port 7	Input/output	Programmable input/output port.
	P82-P87	Input/output port 8	Input/output	Programmable input/output port.
	P93-P97	Input/output port 9	Input/output	Programmable input/output port.
	P100-P107	Input/output port 10	Input/output	Programmable input/output port.
	P110-P117	Input/output port 11	Input/output	Programmable input/output port.
	P124-P127	Input/output port 12	Input/output	Programmable input/output port.
	P130-P137	Input/output port 13	Input/output	Programmable input/output port.
	P150, P153	Input/output port 15	Input/output	Programmable input/output port.
	P174, P175	Input/output port 17	Input/output	Programmable input/output port.
	P220, P221 P225	Input/output port 22	Input/output	Programmable input/output port. (However, P221 is an input-only port)

Note 1: Input/output port 5 is reserved for future use. Input/output ports 14, 16, 18, 19, 20 and 21 do not exist.

Outline of the CPU core

The M32176 Group uses the M32R RISC CPU core, and has an instruction set which is common to all microcomputers in the M32R family.
Instructions are processed in five pipelined stages consisting of instruction fetch, decode, execution, memory access, and write back. Thanks to its “out-of-order-completion” mechanism, the M32R CPU allows for clock cycle efficient, instruction execution control.
The M32R CPU internally contains sixteen 32-bit general-purpose registers. The instruction set consists of 83 discrete instructions, which come in either 16-bit or 32-bit instruction format. Use of the 16-bit instruction format helps to reduce the program code size. Also, the availability of 32-bit instructions facilitates programming and increases the performance at the same clock speed, as compared to architectures with segmented address spaces.

Multiply-Accumulate instructions comparable to DSP

The M32R CPU contains a multiplier/accumulator that can execute 32-bit × 16-bit in one cycle. Therefore, it executes a 32-bit × 32-bit integer multiplication instruction in three cycles.
Also, the M32R CPU supports the following four multiply-Accumulate instructions (or multiplication instructions) for DSP function use.

(1) 16 high-order register bits × 16 high-order register bits
(2) 16 low-order register bits × 16 low-order register bits
(3) All 32 register bits × 16 high-order register bits
(4) All 32 register bits × 16 low-order register bits

Furthermore, the M32R CPU has instructions for rounding the value stored in the accumulator to 16 or 32-bit, and instructions for shifting the accumulator value to adjust digits before storing in a register. Because these instructions also can be executed in one cycle, DSP comparable data processing capability can be obtained by using them in combination with high-speed data transfer instructions such as Load & Address Update or Store & Address Update.

Three operation modes

The M32176 Group has three operation modes: single-chip mode, external extended mode,and processor mode. These operation modes are changed from one to another by setting the MOD0 and MOD1 pins.

Address space

The 32176 Group’s logical address is always handled in width of 32-bit, providing a linear address space of up to 4G bytes. The 32176’s address space is divided into the following spaces.

User space

A 2G-byte area from H’0000 0000 to H’7FFF FFFF is the user space. Located in this space are the user ROM area, external extended area, internal RAM area, and SFR (Special Function Register) area (internal peripheral I/O registers). Of these, the user ROM area and external extended area are located differently depending on mode settings.

System space

A 2G-byte area from H’8000 0000 to H’FFFF FFFF is the system area. This space is reserved for use by development tools such as an in-circuit emulator and debug monitor, and cannot be used by the user.

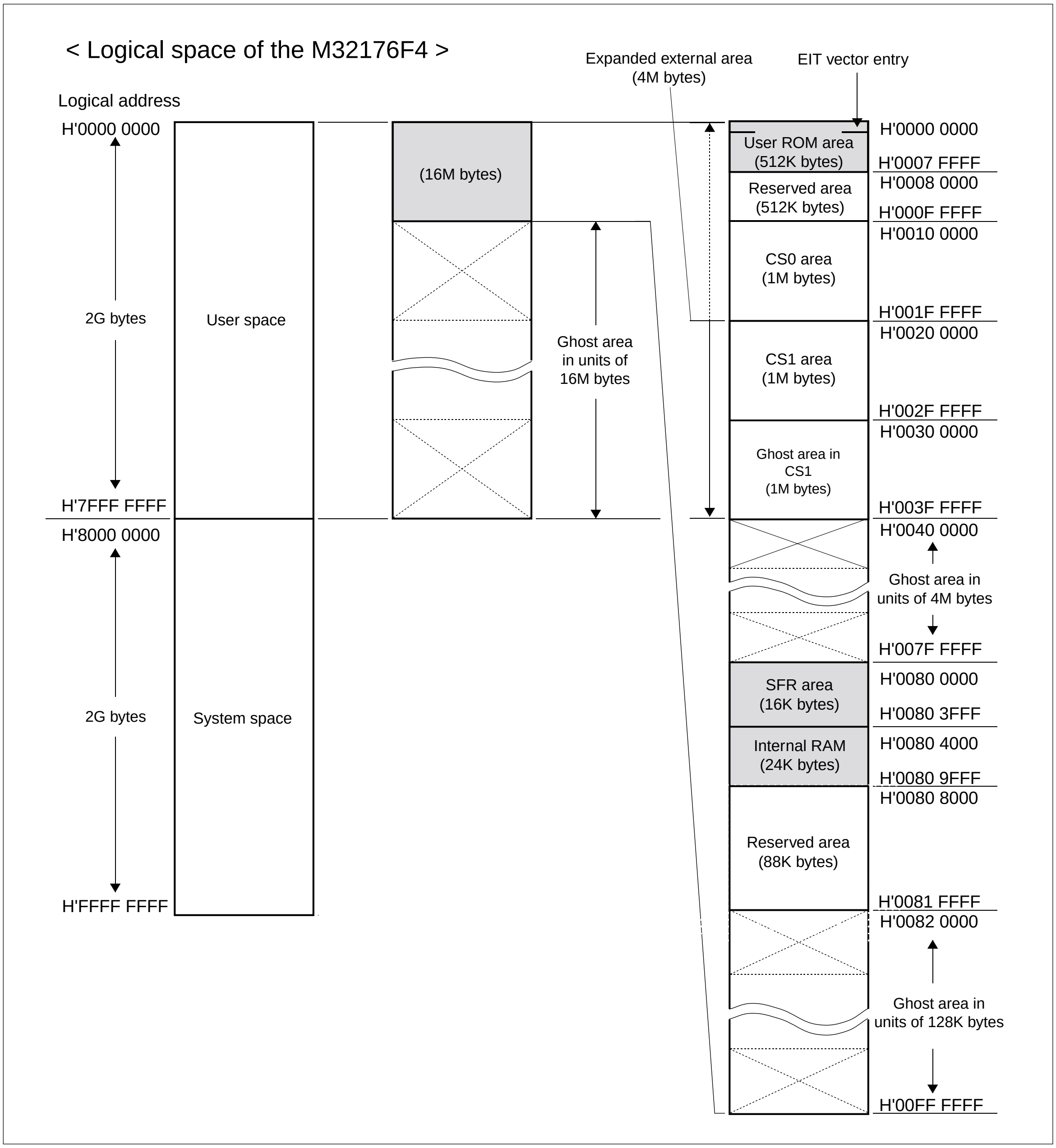


Figure 4. Address Space of the M32176F4VFP/M32176F4TFP

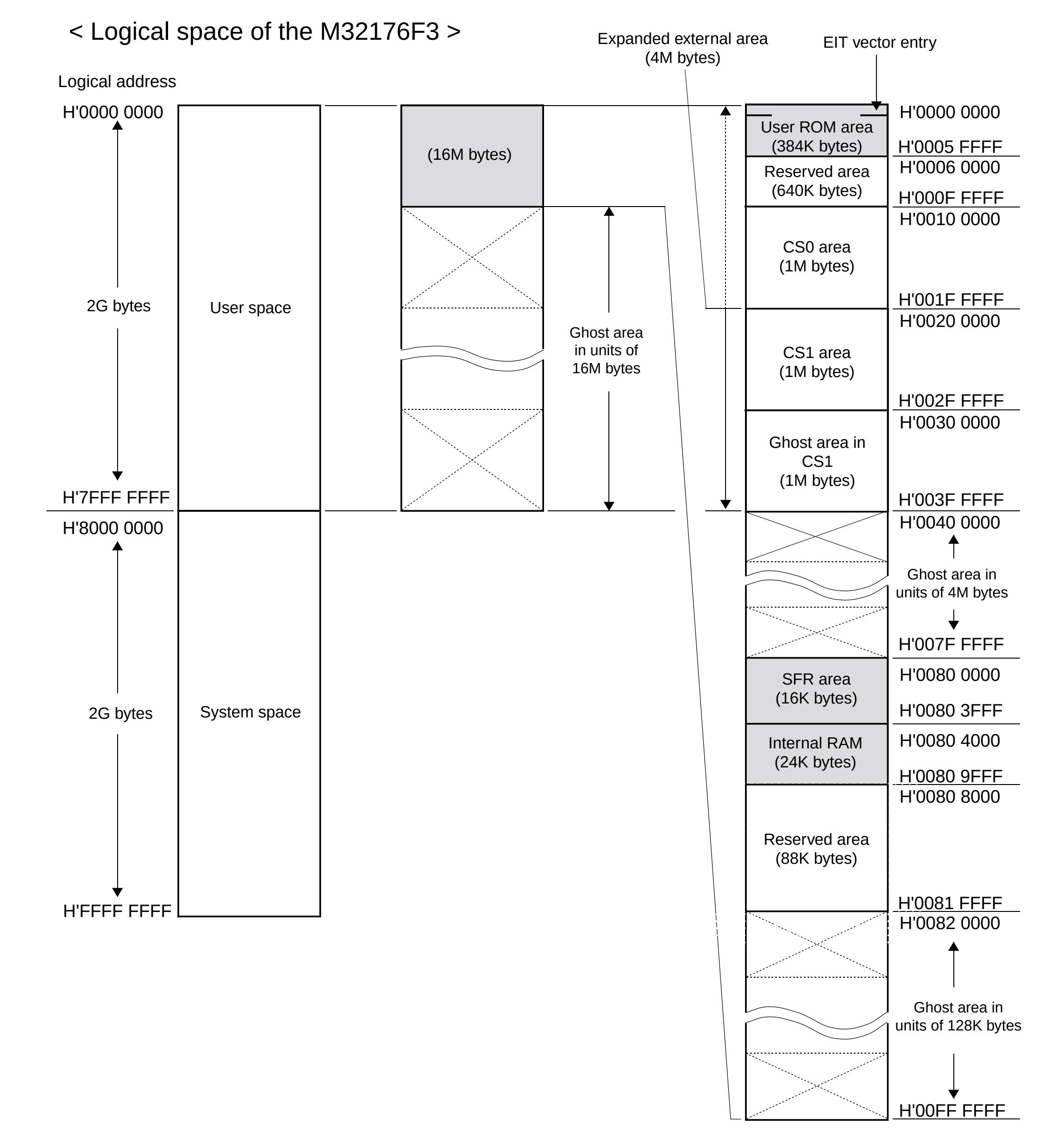


Figure 5. Address Space of the M32176F3VFP/M32176F3TFP

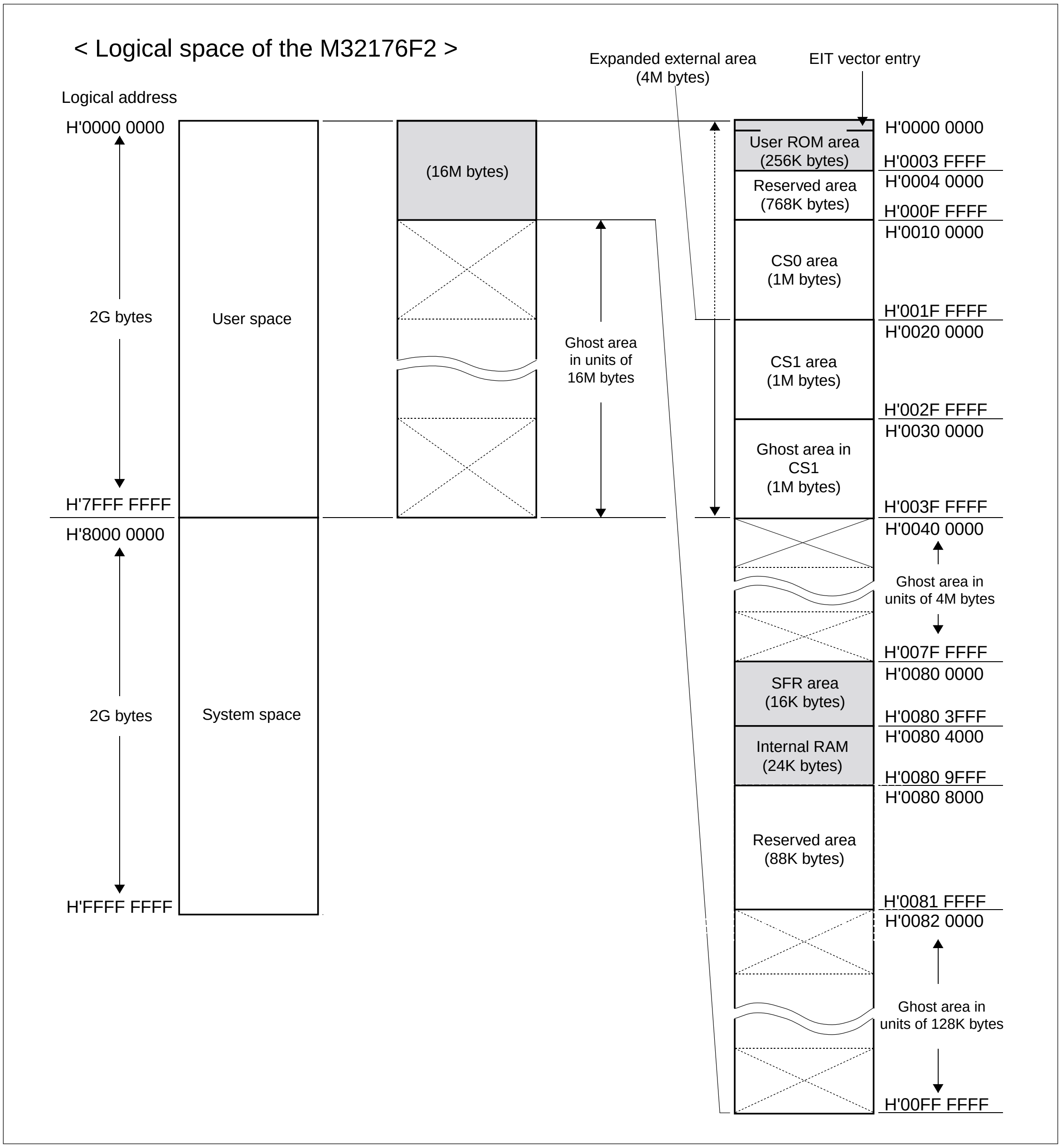
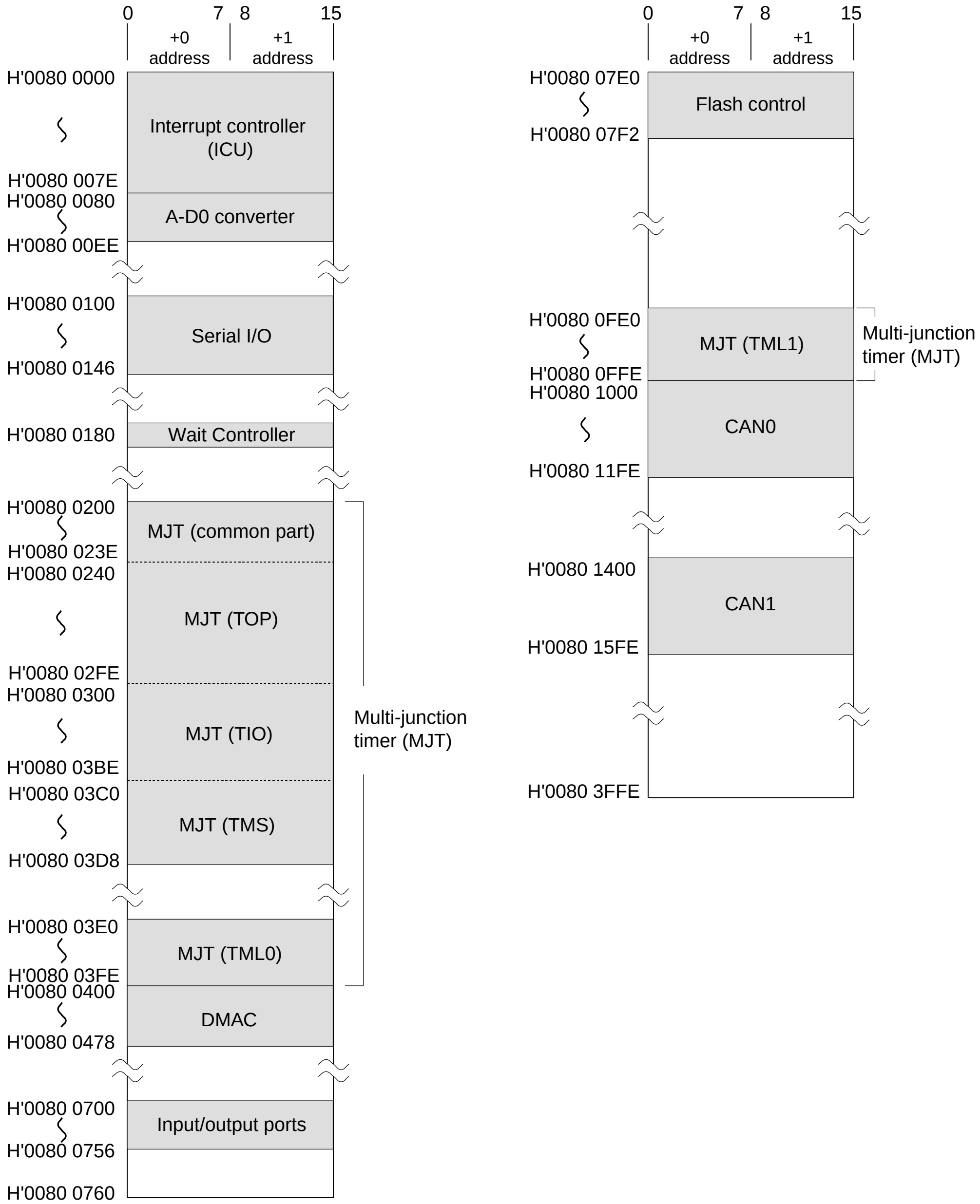


Figure 6. Address Space of the M32176F2VFP/M32176F2TFP



Note: • The Real-time debugger (RTD) is an independent module operated from external circuits, and is transparent to the CPU.

Figure 7. SFR Area

Built-in flash memory and RAM

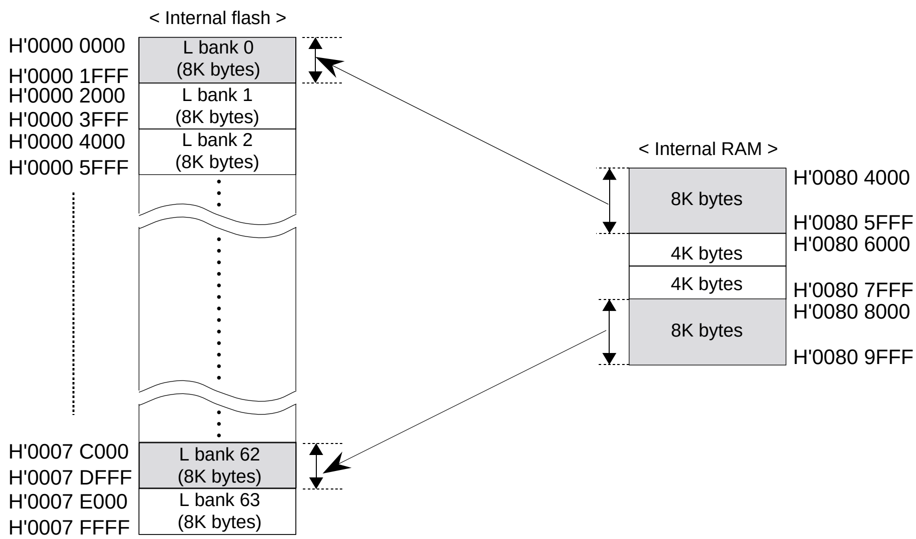
The M32176F4VFP/M32176F4TFP contains 512K bytes flash memory and 24K bytes RAM, the M32176F3VFP/ M32176F3TFP contains 384K bytes flash memory and 24K bytes RAM, the M32176F2VFP/ M32176F2TFP contains 256K bytes flash memory and 24K bytes RAM.

The internal flash memory can be programmed while being mounted on the printed circuit board (on-board programming). Use of flash memory allows the same chip as those used in mass production to be used beginning with the development stage. This means that system development can be proceeded without having to change the printed circuit boards during the entire course, from prototype to mass production.

Built-in Virtual-Flash Emulation Function

Internal flash memory, which is divided from the first address in units of 8K bytes (L banks), can be replaced in 8K bytes blocks (H’0080 4000-H’0080 5FFF, H’0080 8000-H’0080 9FFF) from the beginning of the internal RAM. And also the internal flash memory, which is divided from the first address in units of 4K bytes area (All S banks), can be replaced within two 4K bytes areas (H’0080 6000-H’0080 7FFF).

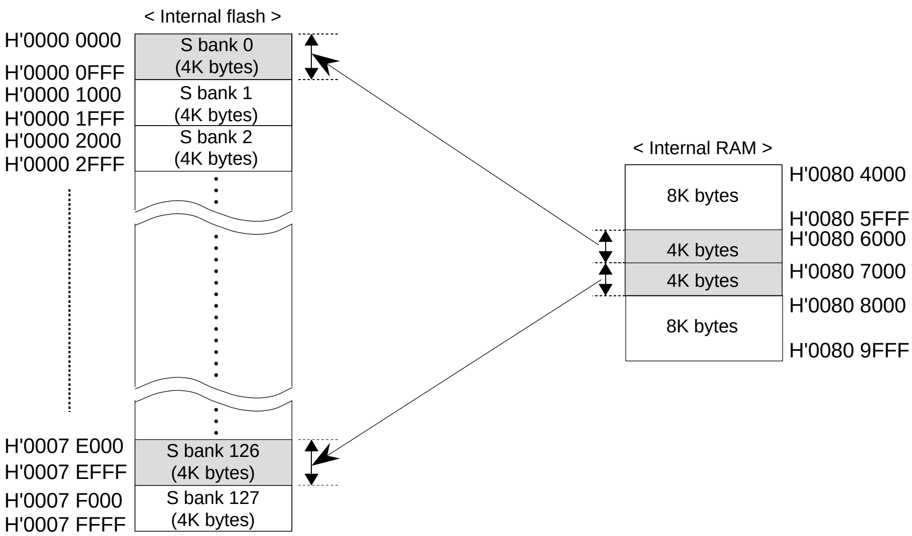
This function allows parts of the program which are frequently changed during development to be altered or evaluated without having to reset the microcomputer each time. What’s more, when combined with the realtime debugger, this function helps to reduce the program evaluation period, because data in the RAM can be rewritten without requiring any CPU load.



Notes: • If the same bank area is set in multiple virtual-flash bank registers and the virtual-flash emulation enable bit is enabled, the corresponding internal RAM area is assigned to either bank register according to the priority FELBANK0 > FESBANK0 > FESBANK1 > FELBANK1.

• When access is made to the 8K bytes area (L bank) specified with virtual-flash bank register 0, the internal RAM area is accessed. During virtual-flash emulation mode, RAM data can read and written to and from both the internal RAM area and the virtual-flash setup area.

Figure 8. Virtual-Flash Emulation Areas of the M32176F4VFP/M32176F4TFP (Replaced in Units of 8K bytes)



Notes: • If the same bank area is set in multiple virtual-flash bank registers and the virtual-flash emulation enable bit is enabled, the corresponding internal RAM area is assigned to either bank register according to the priority FELBANK0 > FESBANK0 > FESBANK1 > FELBANK1.
• When access is made to the 4K bytes area (S bank) specified with virtual-flash bank register 0 and 1, the internal RAM area is accessed. During virtual-flash emulation mode, RAM data can read and written to and from both the internal RAM area and the virtual-flash setup area.

Figure 9. Virtual-Flash Emulation Areas of the M32176F4VFP/M32176F4TFP (Replaced in Units of 4K bytes)

Virtual-Flash Emulation Areas of M32176F4VFP/M32176F4TFP, M32176F3VFP/M32176F3TFP, and M32176F2VFP/M32176F2TFP are shown as follows.

Table 8. Virtual-Flash Emulation Areas

Type Name	Virtual-Flash Emulation Areas
M32176F4VFP/M32176F4TFP	H’0000 0000-H’0007 FFFF
M32176F3VFP/M32176F3TFP	H’0000 0000-H’0005 FFFF
M32176F2VFP/M32176F2TFP	H’0000 0000-H’0003 FFFF

Input/output Ports

The microcomputer has a total of 96 input/output ports P0-P22. (However, P5 is reserved for future use, P14, P16, and P18-P21 do not exist.) The input/output ports can be used as input ports or output ports by setting uptheir direction registers.

Each input/output port is a dual-function pin shared with otherinternal peripheral I/O or external extended bus signal lines.These pin functions are selected by using the chip operation mode select or the input/output port operation mode registers.

Table 9. Outline of Input/output Ports

Item	Specification
Number of Port	Total 96 ports
	P0 : P00-P07 (8 lines)
	P1 : P10-P17 (8 lines)
	P2 : P20-P27 (8 lines)
	P3 : P30-P37 (8 lines)
	P4 : P41-P47 (7 lines)
	P6 : P61-P63 (3 lines)
	P7 : P70-P77 (8 lines)
	P8 : P82-P87 (6 lines)
	P9 : P93-P97 (5 lines)
	P10 : P100-P107 (8 lines)
	P11 : P110-P117 (8 lines)
	P12 : P124-P127 (4 lines)
	P13 : P130-P137 (8 lines)
	P15 : P150, P153 (2 lines)
	P17 : P174, P175 (2 lines)
	P22 : P220, P221, P225 (3 lines)
Port function	The input/output ports can be set for input or output mode bitwise by using the input/output port direction control register. (However, P221 is CAN input-only port.)
Pin function	Dual-functions shared with peripheral I/O or external extended signals (or multi-functions shared with peripheral I/Os which have multiple functions.)
Pin function changeover	P0-P4: Changed by setting CPU operation mode (MOD0 and MOD1 pins) P6-22: Changed by setting the input/output port operation mode register. (However, peripheral I/O pin functions are selected using the peripheral I/O register.)

Note: Input/output ports P14, P16, and P18-P21 do not exist.

Table 10. CPU Operation Modes and P0-P4 Pin Functions

MOD0	MOD1	Operation mode	Pin functions of P0-P4
VSS	VSS	Single-chip mode	Input/output port pin
VSS	VCCE	External extended mode	External extended signal pin
VCCE	VSS	Processor mode (FP pin = VSS)	
VCCE	VCCE	Reserved (use inhibited)	–

Notes: • VCCE connects to power supply, and VSS connects to GND.
• MOD2 connects to GND.

		0	1	2	3	4	5	6	7
Settings of Chip operation mode (Note 1)	P0	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
	P1	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15
	P2	A23	A24	A25	A26	A27	A28	A29	A30
	P3	A15	A16	A17	A18	A19	A20	A21	A22
	P4		BLW#/ BLE#	BHW#/ BHE#	RD#	CS0#	CS1#	A13	A14
Reserved	P5								
Settings of input/output port Operation Mode Register	P6		(P61)	(P62)	(P63)	SBI# (Note 3)			
	P7	BCLK/ WR#	WAIT#	HREQ#	HACK#	RTDTXD/ TXD3 (Note 2)	RTDRXD/ RXD3 (Note 2)	RTDACK/ CTX1 (Note 2)	RTDCLK/ CRX1 (Note 2)
	P8	MOD0 (Note 3)	MOD1 (Note 3)	TXD0	RXD0	SCLKI0/ SCLKO0	TXD1	RXD1	SCLKI1/ SCLKO1
	P9				TO16	TO17	TO18	TO19	TO20
	P10	TO8	TO9	TO10	TO11	TO12	TO13	TO14	TO15
	P11	TO0	TO1	TO2	TO3	TO4	TO5	TO6	TO7
	P12					TCLK0	TCLK1	TCLK2	TCLK3
	P13	TIN16	TIN17	TIN18	TIN19	TIN20	TIN21	TIN22	TIN23
	P14								
	P15	TIN0			TIN3				
	P16								
	P17					TXD2	RXD2		
	P18								
	P19								
	P20								
	P21								
	P22	CTX0	CRX0				A12		

Note 1: The pin function are selected by setting the MOD0 and MOD1 pins.
Note 2: It is a triple function pin. It is necessary to set up the peripheral functions outputted by the peripheral output select register.
Note 3: It cannot be used as a function of an input/output ports. The input level of SBI#, MOD0, and an MOD1 pin can be read.
Note: • P14, P16, P18, P19, P20, and P21 do not exist.

Figure 10. Input/output Ports and Pin Function Assignments

Built-in 10-Channel DMAC

The microcomputer contains 10 channels of DMAC, allowing for data transfer between internal peripheral I/Os, between internal RAM and internal peripheral I/O, and between internal RAMs.

DMA transfer requests can be issued from the user-created software, as well as can be triggered by a signal generated by the internal peripheral I/O (A-D converter, timer, or serial I/O).

The microcomputer also supports cascaded connection between DMA channels (starting DMA transfer on a channel at end of transfer on another channel). This makes advanced transfer processing possible without causing any additional CPU load.

Table 11. Outline of the DMAC

Item	Content
Number of channels	10 channels
Transfer request	• Software trigger • Request from internal peripheral I/O: A-D converter, timer, or serial I/O (reception completed, transmit buffer empty) • Cascaded connection between DMA channels possible (Note 1)
Maximum number of times transferred	256 times
Transferable address space	• 64K bytes (address space from H'0080 0000 to H'0080 FFFF) • Transfers between internal peripheral I/Os, between internal RAM and internal peripheral IO, and between internal RAMs are supported
Transfer data size	16-bit or 8-bit
Transfer method	Single transfer DMA (control of the internal bus is relinquished for each transfer performed), dual-address transfer
Transfer mode	Single transfer mode
Direction of transfer	One of three modes can be selected for the source and destination of transfer: • Address fixed • Address increment • 32-channel ring buffer
Channel priority	DMA 0 > DMA 1 > DMA 2 > DMA 3 > DMA 4 > DMA 5 > DMA 6 > DMA 7 > DMA 8 > DMA 9 (Fixed priority)
Maximum transfer rate	13.3M bytes per second (when internal peripheral clock = 20 MHz)
Interrupt request	Group interrupt request can be generated when each transfer count register underflows
Transfer area	64K bytes from H '0080 0000 to H '0080 FFFF (Transfer is possible in the entire internal RAM/ SFR area)

Note 1: The following DMA channels can be cascaded.

DMA transfer on channel 1 started at end of one DMA transfer on DMA 0
DMA transfer on channel 2 started at end of one DMA transfer on DMA 1
DMA transfer on channel 0 started at end of one DMA transfer on DMA 2
DMA transfer on channel 4 started at end of one DMA transfer on DMA 3
DMA transfer on channel 6 started at end of one DMA transfer on DMA 5
DMA transfer on channel 7 started at end of one DMA transfer on DMA 6
DMA transfer on channel 5 started at end of one DMA transfer on DMA 7
DMA transfer on channel 9 started at end of one DMA transfer on DMA 8
DMA transfer on channel 5 started at end of all DMA transfers on DMA 0 (underflow of transfer count register)

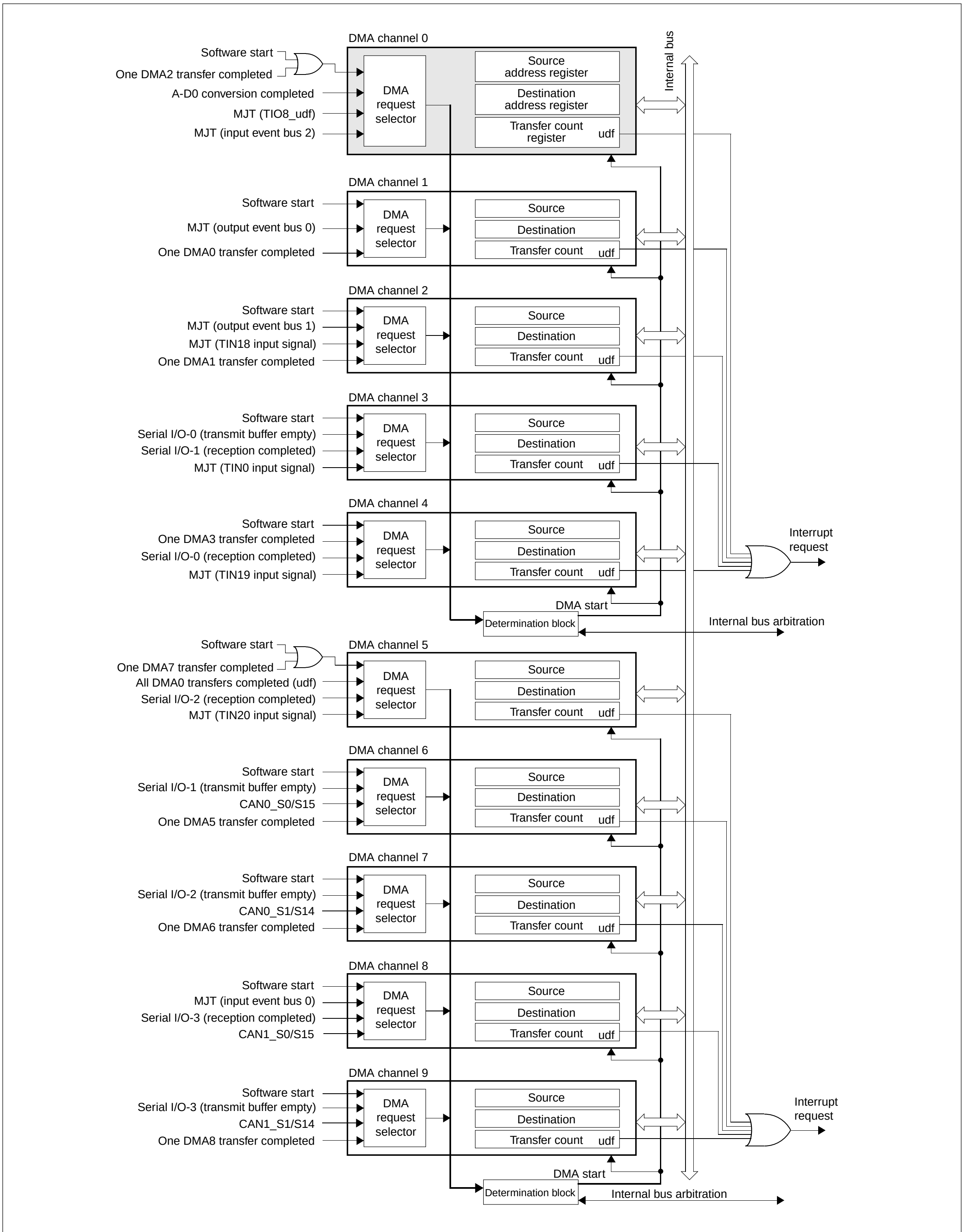
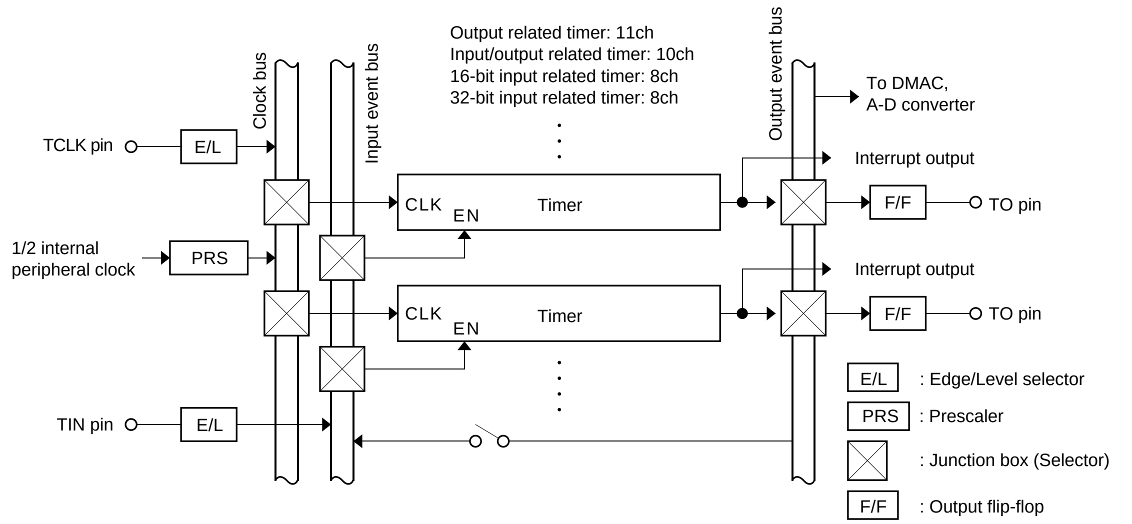


Figure 11. Block Diagram of the DMAC

Built-in 37-channel multijunction timers (MJT)

The microcomputer contains a total of 37 channels of multijunction timers consisting of 11 channels of 16-bit output related timers, 10 channels of 16-bit input/output related timers, 8 channels of 16-bit input related timers, 8 channels of 32-bit input related timers. Each timer has multiple operation modes to choose from, depending on the purposes of use.

Also, the multijunction timers internally have a clock bus, input event bus, and an output event bus, so that multiple timers can be used in combination allowing for a flexible timer configuration. The output related timers have a correcting function that allows the timer's count value to be incremented or decremented as necessary while count is in progress, making real-time output control possible.



Note: • This is a conceptual diagram and does not show the actual timer configuration.

Figure 12. Conceptual Diagram of the Multijunction Timer (MJT)

Table 12. Outline of the MJT

Name	Type	Number of channels	Contents
TOP (Timer Output)	Output related 16-bit timer (down-counter)	11	One of three output modes is selected in software. <With correcting function> • Single-shot output mode • Delayed single-shot output mode <Without correcting function> • Continuous output mode
TIO (Timer Input Output)	Input/output related 16-bit timer (down-counter)	10	One of three input modes and four output modes is selected in soft ware. <Input mode> • Measure clear input mode • Measure free-run input mode • Noise processing input mode <Output mode without correcting function> • PWM output mode • Single-shot output mode • Delayed single-shot output mode • Continuous output mode
TMS (Timer Measure Small)	Input related 16-bit timer (up-counter)	8	16-bit input measure timer.
TML (Timer Measure Large)	Input related 32-bit timer (up-counter)	8	32-bit input measure timer.

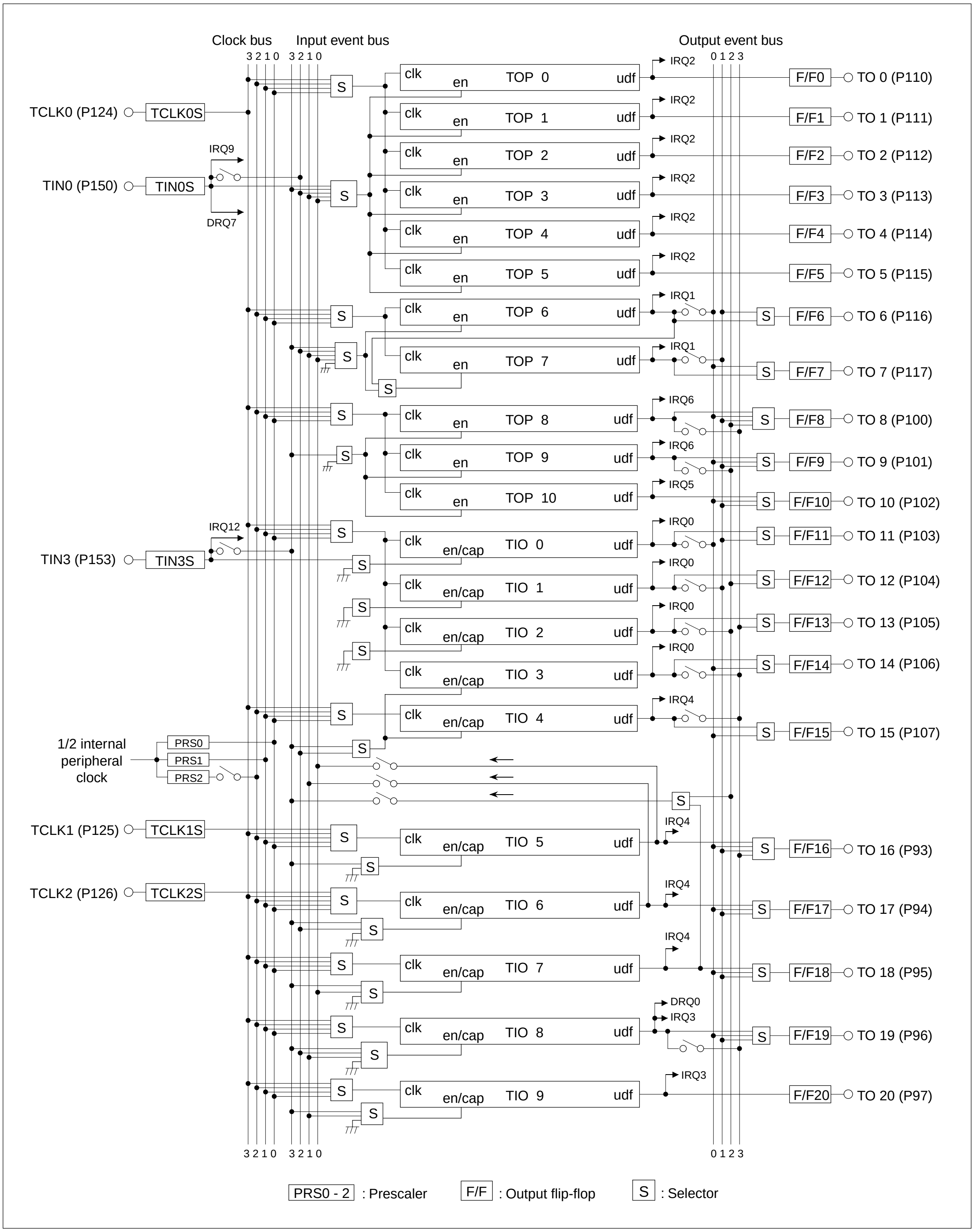


Figure 13. Block Diagram of Multijunction Timers (MJT) (1/3)

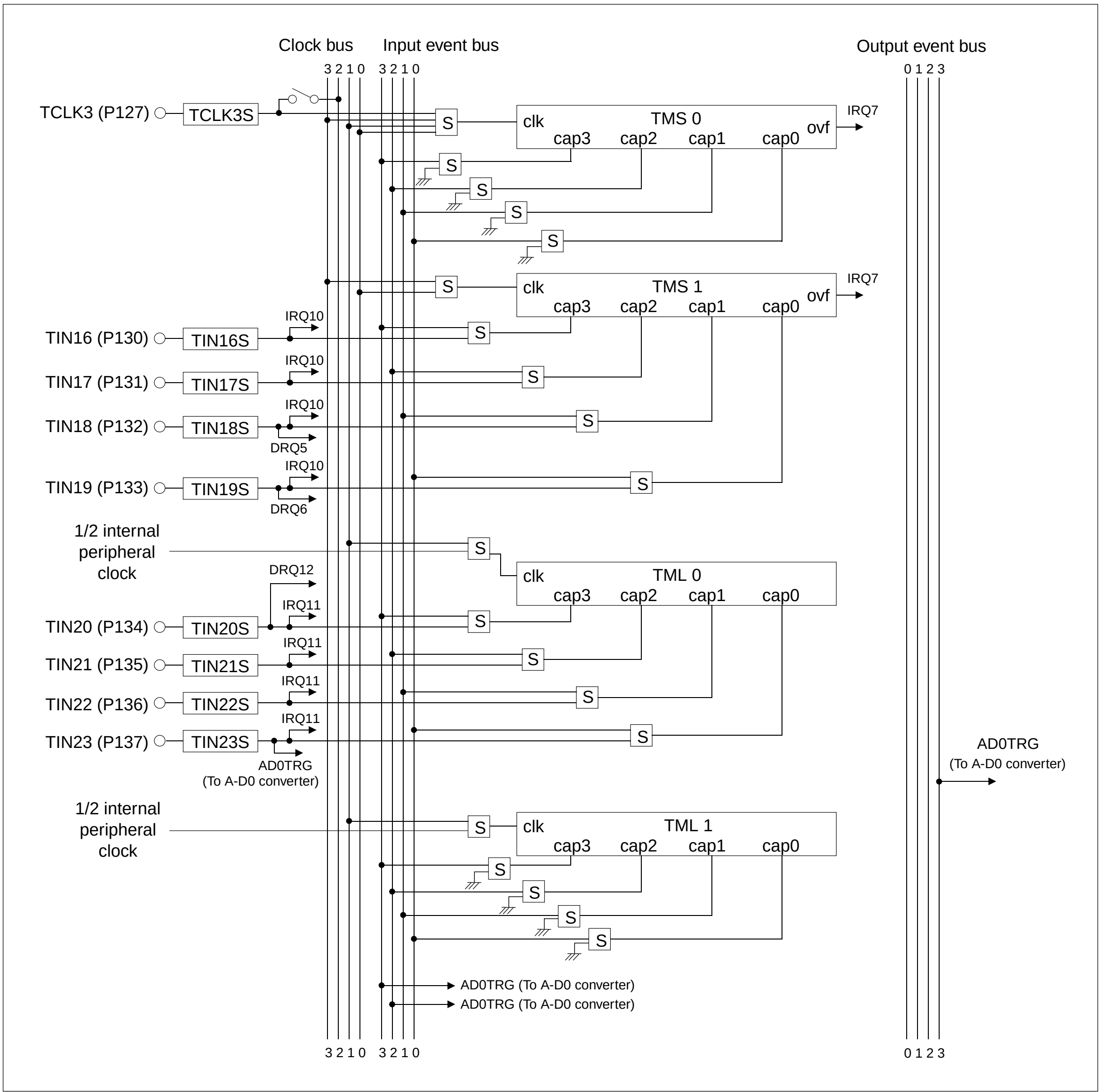


Figure 14. Block Diagram of Multijunction Timers (MJT) (2/3)

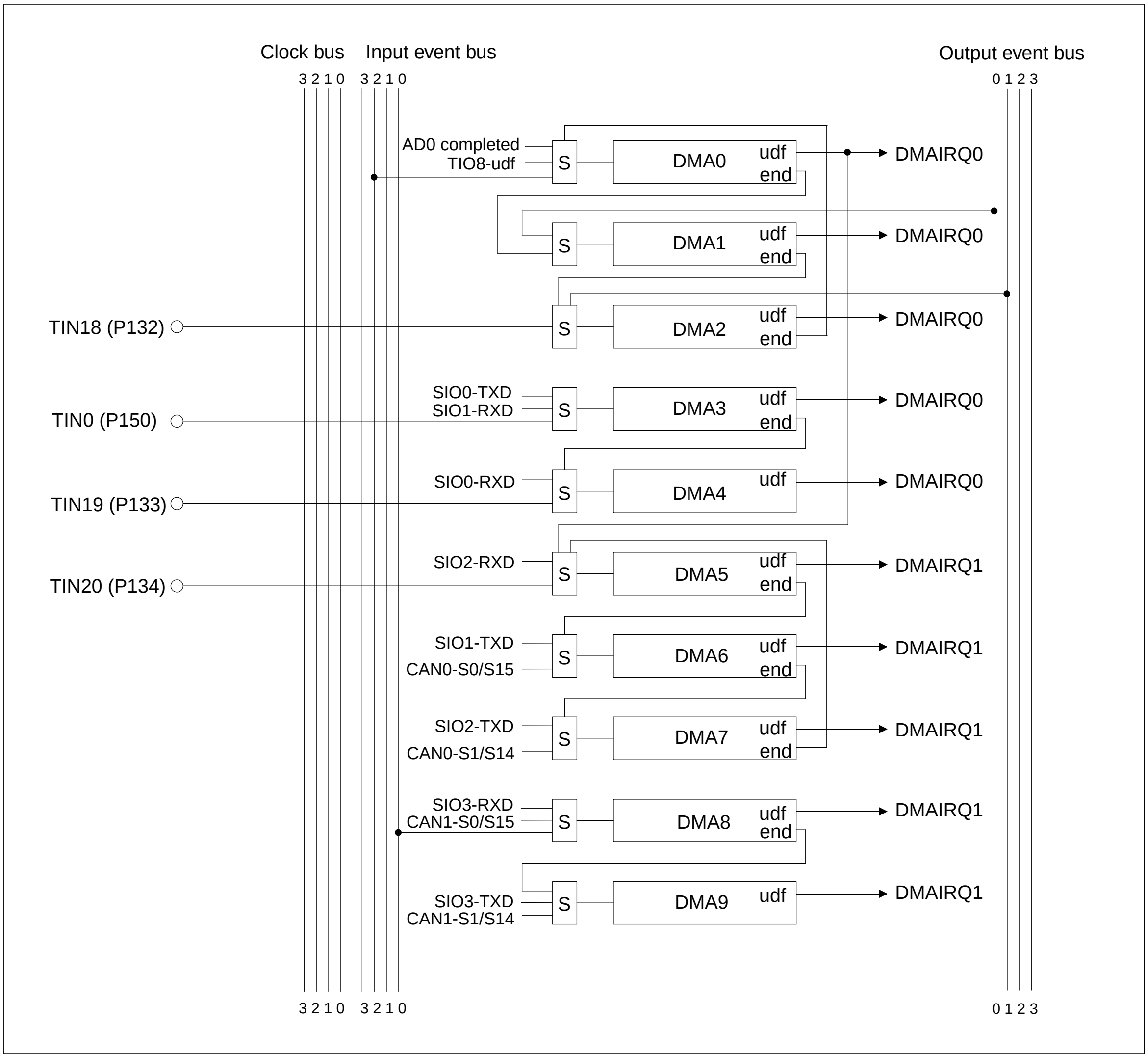


Figure 15. Block Diagram of Multijunction Timers (MJT) (3/3)

16-channel A-D Converters

The microcomputer contains 16-channel A-D0 converters with 10-bit resolution. In addition to single conversion on each channel, continuous A-D conversion on a combined group of N (N = 1-16) channels is possible. The A-D converted value can be read out in either 10-bit or 8-bit.
In addition to ordinary A-D conversion, the converters support comparator mode in which the set value and A-D converted value are compared to determine which is larger or smaller than the other.
Moreover, there is also Sample & hold function, input voltage is sampled, when A-D conversion is started, and the A-D conversion of the sampling voltage is carried out.
Since there is no invalid domain near [which becomes a problem by the external operational amplifier etc.] VCCE/VSS, conversion by the full range is possible in this sample & hold circuit.
When A-D conversion is finished, the converters can generate a DMA transfer request, as well as an interrupt.

Table 13. Outline of the A-D Converters

Item	Content				
Analog input	16-channel				
A-D conversion method	Successive approximation method				
Resolution	10-bit (Conversion results can be read out in either 10 or 8-bit)				
Absolute accuracy (Note 1)	During low speed mode : Normal mode: ± 2 LSB, double speed mode: ± 2 LSB				
(conditions: Ta = 25°C, AVCC0, 1 = VREF0, 1 = 5.12V)	During high speed mode : Normal mode: ± 3 LSB, double speed mode: ± 3 LSB Note: The performance is the same during sample & hold function.				
Conversion mode	A-D conversion mode, comparator mode				
Operation mode	Single mode, single-shot scan mode, continuous scan mode				
Conversion start trigger	Software start	Started by setting A-D conversion start bit to 1			
	Hardware start	MJT input event bus 2, MJT input event bus 3, MJT output event bus 3, and MJT (TIN23S)			
Conversion Speed f(BCLK): Internal peripheral clock operating frequency (Note 2)	During single mode (Unavailable for Sample & Hold Available for Normal Sample & Hold)	Low-speed mode	Normal	299 BCLK	14.95 µs
			Double speed	173 BCLK	8.65 µs
		High-speed mode	Normal	131 BCLK	6.55 µs
			Double speed	89 BCLK	4.45 µs
	During single mode (Available for High-speed Sample & Hold)	Low-speed mode	Normal	191 BCLK	9.55 µs
			Double speed	101 BCLK	5.05 µs
		High-speed mode	Normal	95 BCLK	4.75 µs
			Double speed	53 BCLK	2.65 µs
	During comparator mode	Low-speed mode	Normal	47 BCLK	2.35 µs
			Double speed	29 BCLK	1.45 µs
		High-speed mode	Normal	23 BCLK	1.15 µs
			Double speed	17 BCLK	0.85 µs
Sample & hold function	Validity/invalidity selectable				
A-D disconnection detection assist function	Influences of the analog input voltage wrapping around from the preceding channel are suppressed when operating scan mode.				
Interrupt request generation	When A-D conversion is finished, when comparate operation is finished When single-shot scan is finished, or when one cycle of continuous scan is finished				
DMA transfer request generation	When A-D conversion is finished, when comparate operation is finished When single-shot scan is finished, or when one cycle of continuous scan is finished				

Note 1: The rated value of conversion accuracy here is that of the microcomputer's own as a single unit which can be exhibited when themicrocomputer is used in an environment where it may not be affected by the power supply wiring or noise on the board.
Note 2: Conversion time at the time of f(BCLK) = 20 MHz operation (1 BCLK = 50 ns)

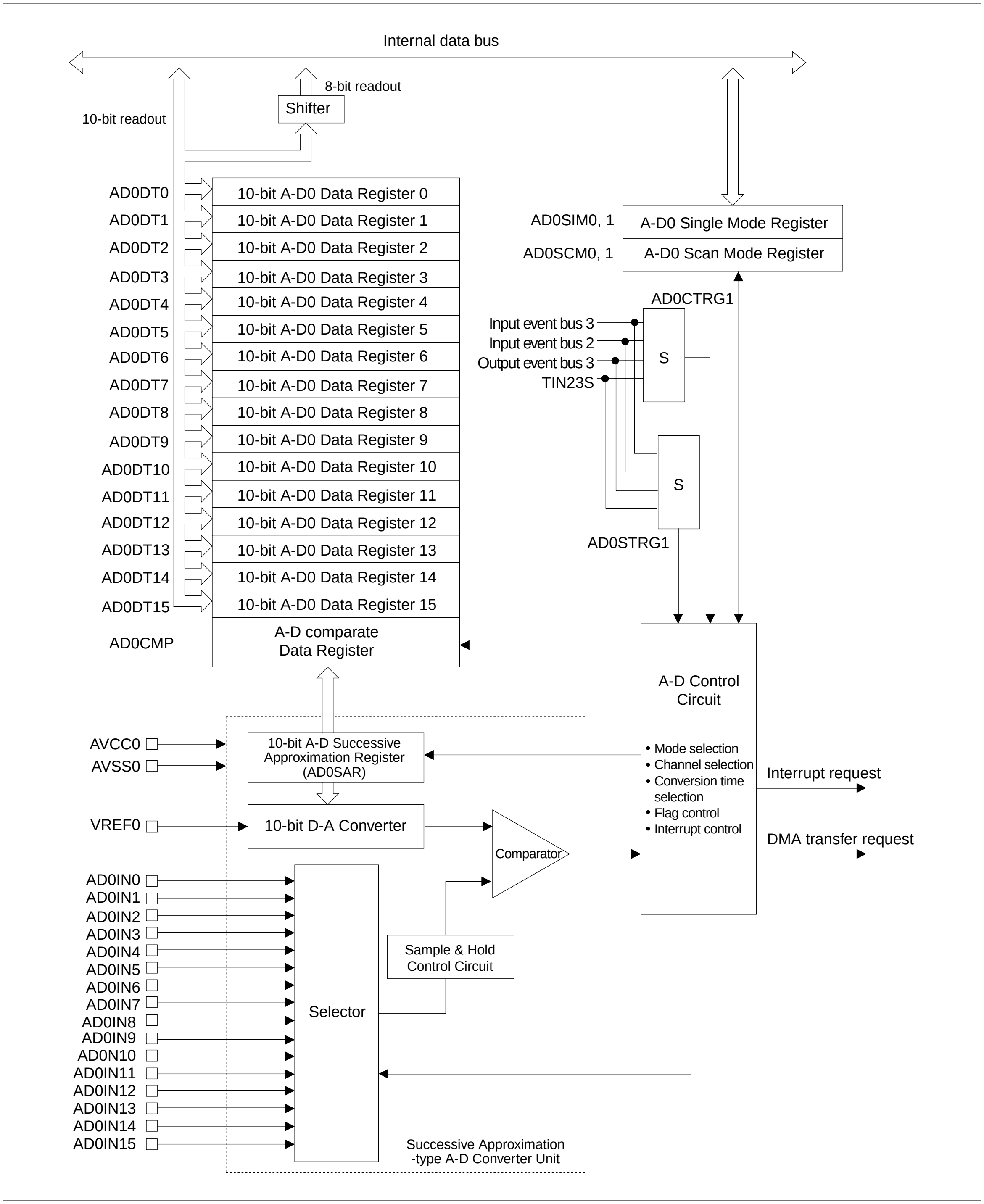


Figure 16. Block Diagram of the A-D0 Converter

4-channel High-speed Serial I/Os

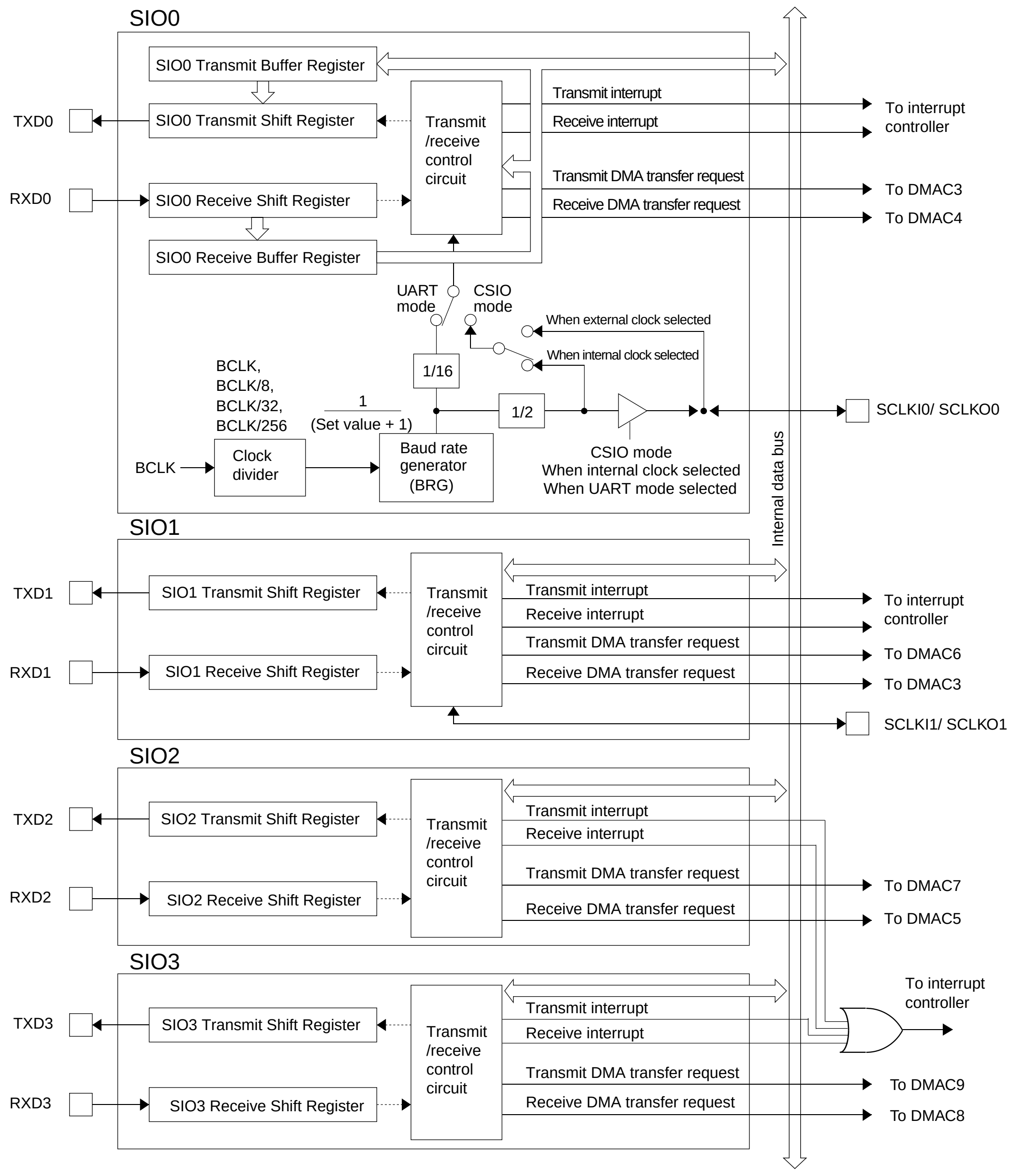
The microcomputer contains 4 channels of serial I/Os consisting of four channels that can be set for CSIO mode (clock-synchronized serial I/O) or UART mode (asynchronous serial I/O) and two other channels that can only be set for UART mode.

The SIO has the function to generate a DMA transfer request when data reception is completed or the transmit register becomes empty, and is capable of high-speed serial communication without causing any additional CPU load.

Table 14. Outline of Serial I/O

Item	Content
Number of channels	CSIO/UART : 2 channels (SIO0, SIO1) UART only : 2 channels (SIO2, SIO3)
Clock	During CSIO mode : Internal clock /external clock, selectable (Note 1) During UART mode : Internal clock only
Transfer mode	Transmit half-duplex, receive half-duplex, transmit/receive full-duplex (Transfer clock inverted mode)
BRG count sourcef	f(BCLK), f(BCLK)/8, f(BCLK)/32, f(BCLK)/256 (When internal clock is selected) (Note 2)
Data format	CSIO mode : Data length = Fixed to 8 bits Order of transfer = Fixed to LSB first UART mode : Start bit = 1 bit Character length = 7, 8, or 9 bits Parity bit = Added or not added (When added, selectable between odd and even parity) Stop bit = 1 or 2 bits Order of transfer = Fixed to LSB first
Baud rate	CSIO mode : 152 bits per second to 2 Mbits per second (when operating with f(BCLK) = 20 MHz) UART mode : 19 bits per second to 156 Kbits per second (when operating with f(BCLK) = 20 MHz)
Error detection	CSIO mode : Overrun error only UART mode : Overrun, parity, and framing errors (The error-sum bit indicates which error has occurred)
Fixed cycle clock output function	When using SIO0 and SIO1 as UART, this function outputs a divided-by-2 BRG clock from the SCLK pin.

Note 1: During CSIO mode, the maximum input frequency of an external clock is f(BCLK) divided by 16.
Note 2: When f(BCLK) is selected for the BRG count source, the BRG set value is subject to limitations.



Notes: • When BCLK is selected for the BRG count source, the BRG set value is subject to limitations.
• SIO2 and SIO3 do not have the SCLKI/SCLKO function.

Figure 17. Block Diagram of Serial I/O

CAN Modules

The M32176 Group contains two blocks of Full-CAN modules compliant with CAN Specification V2.0B active.

The CAN modules each have 16-channel message slots and three mask registers.

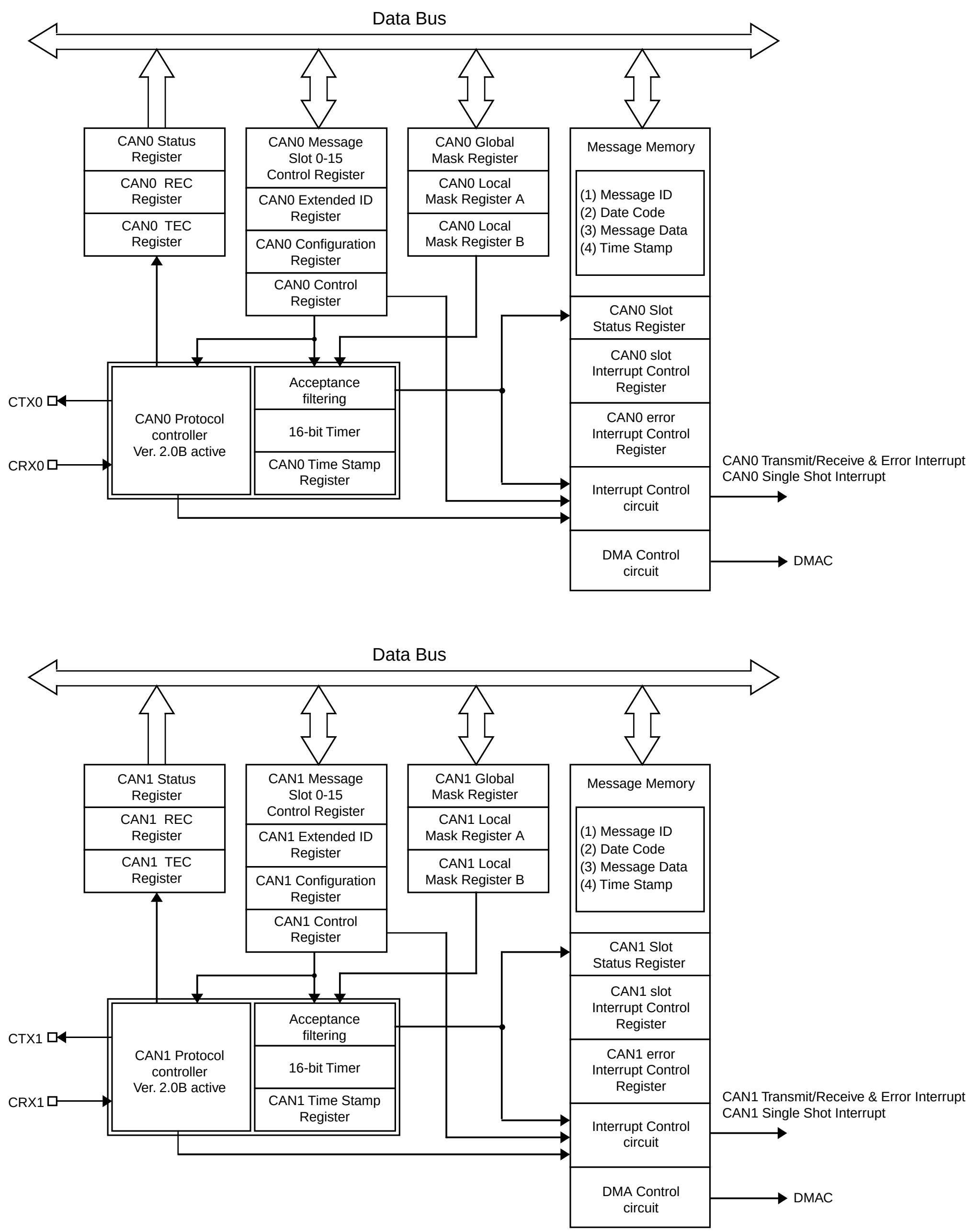


Figure 18. Block Diagram of CAN Modules

8-level Interrupt Controller

The Interrupt Controller controls interrupt requests from each internal peripheral I/O (23 sources) by using eight priority levels assigned to each interrupt source, including interrupts prohibition. In addition to these interrupts, it handles System Break Interrupt (SBI), Reserved Instruction Exception (RIE), and Address Exception (AE) as nonmaskable interrupts.

Wait Controller

The Wait Controller supports access to external devices. For access to an external extended area of up to 1Mbytes (during external extended or processor mode), the Wait Controller controls bus cycle extension by inserting one to four wait cycles and using external WAIT# signal input.

Real-time Debugger (RTD)

The Real-time Debugger (RTD) provides function for accessing directly from the outside to the internal RAM. It uses a dedicated clock-synchronized serial I/O to communicate with the outside.
Use of the RTD communicating via dedicated serial lines allows the internal RAM to be read out and rewritten without having to halt the CPU.

Port input threshold level select function

The port input level switch function sets the port threshold value to 3 different voltage levels (Schmidt ON/OFF selection also available).

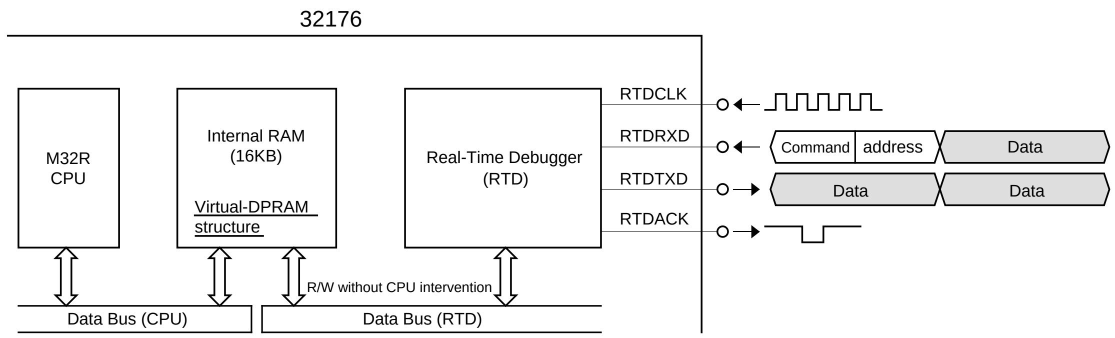


Figure 19. Conceptual Diagram of Real-time Debugger (RTD)

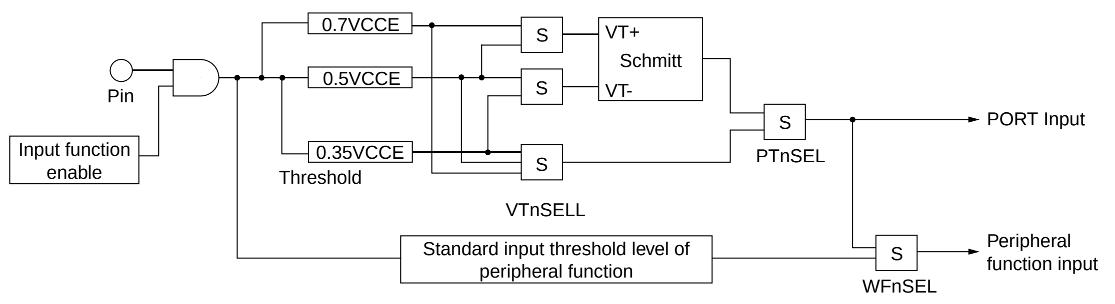


Figure 20. Port input threshold level select function

CPU Instruction Set

The M32R employs a RISC architecture, supporting a total of 83 discrete instructions.

(1) Load/store instructions

Perform data transfer between memory and registers.

LD	Load
LDB	Load byte
LDUB	Load unsigned byte
LDH	Load halfword
LDUH	Load unsigned halfword
LOCK	Load locked
ST	Store
STB	Store byte
STH	Store halfword
UNLOCK	Store unlocked

(2) Transfer instructions

Perform register to register transfer or register to immediate transfer.

LD24	Load 24-bit immediate
LDI	Load immediate
MV	Move register
MVFC	Move from control register
MVTC	Move to control register
SETH	Set high-order 16-bit

(3) Branch instructions

Used to change the program flow.

BC	Branch on C-bit
BEQ	Branch on equal
BEQZ	Branch on equal zero
BGEZ	Branch on greater than or equal zero
BGTZ	Branch on greater than zero
BL	Branch and link
BLEZ	Branch on less than or equal zero
BLTZ	Branch on less than zero
BNC	Branch on not C-bit
BNE	Branch on not equal
BNEZ	Branch on not equal zero
BRA	Branch
JL	Jump and link
JMP	Jump
NOP	No operation

(4) Arithmetic/logic instructions

Perform comparison, arithmetic/logic operation, multiplication/division, or shift between registers.

• Comparison

CMP	Compare
CMPI	Compare immediate
CMPU	Compare unsigned
CMPUI	Compare unsigned immediate

• Logical operation

AND	AND
AND3	AND 3-operand
NOT	Logical NOT
OR	OR
OR3	OR 3-operand
XOR	Exclusive OR
XOR3	Exclusive OR 3-operand

• Arithmetic operation

ADD	Add
ADD3	Add 3-operand
ADDI	Add immediate
ADDV	Add (with overflow checking)
ADDV3	Add 3-operand
ADDX	Add with carry
NEG	Negate
SUB	Subtract
SUBV	Subtract (with overflow checking)
SUBX	Subtract with borrow

• Multiplication/division

DIV	Divide
DIVU	Divide unsigned
MUL	Multiply
REM	Remainder
REMU	Remainder unsigned

• Shift

SLL	Shift left logical
SLL3	Shift left logical 3-operand
SLLI	Shift left logical immediate
SRA	Shift right arithmetic
SRA3	Shift right arithmetic 3-operand
SRAI	Shift right arithmetic immediate
SRL	Shift right logical
SRL3	Shift right logical 3-operand
SRLI	Shift right logical immediate

(5) Instructions for the DSP function

Perform 32-bit × 16-bit or 16-bit × 16-bit multiplication or multiply-Accumulate calculation. These instructions also perform rounding of the accumulator data or transfer between accumulator and general-purpose register.

MACHI	Multiply-accumulate high-order halfwords
MACLO	Multiply-accumulate low-order halfwords
MACWHI	Multiply-accumulate word and high-order halfword
MACWLO	Multiply-accumulate word and low-order halfword
MULHI	Multiply high-order halfwords
MULLO	Multiply low-order halfwords
MULWHI	Multiply word and high-order halfword
MULWLO	Multiply word and low-order half word
MVFACHI	Move from accumulator high-order word
MVFACLO	Move from accumulator low-order word
MVFACMI	Move from accumulator middle-order word
MVTACHI	Move to accumulator high-order word
MVTACLO	Move to accumulator low-order word
RAC	Round accumulator
RACH	Round accumulator halfword

(6) EIT related instructions

Start trap or return from EIT processing.

RTE	Return from EIT
TRAP	Trap

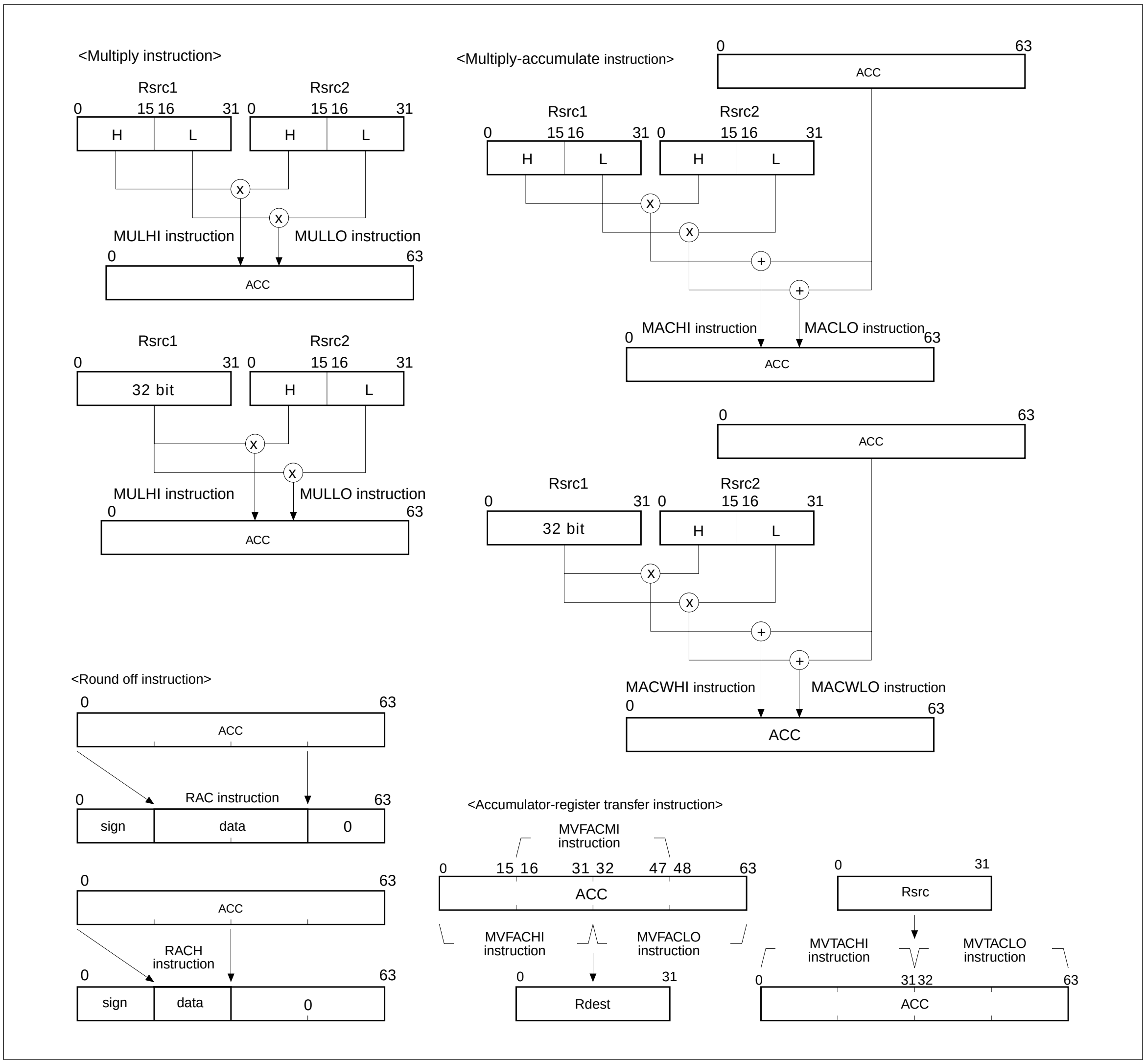


Figure 21. Instructions for the DSP Function

32176 Group

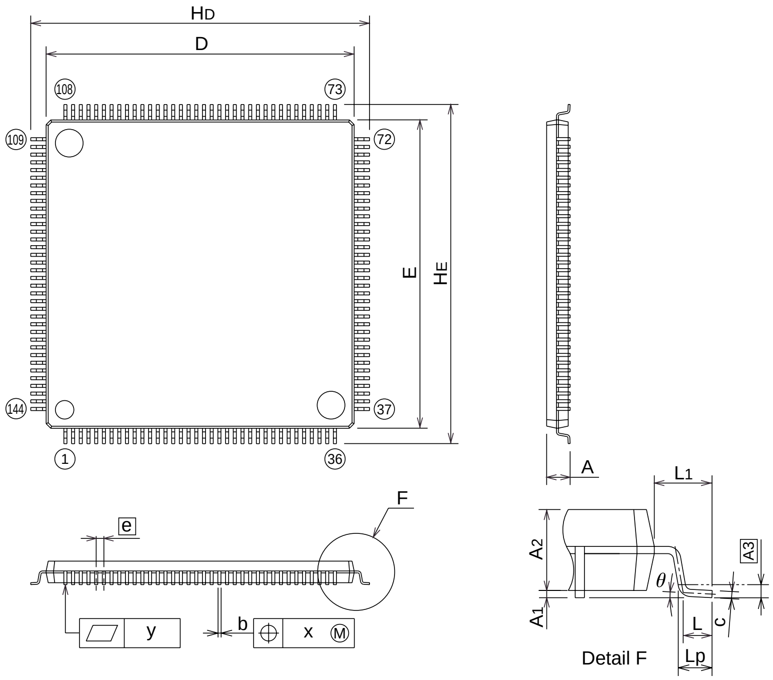
Under Development

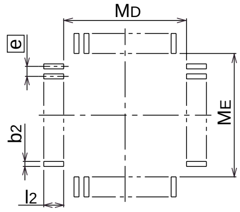
SINGLE-CHIP 32-BIT CMOS MICROCOMPUTER

Package Dimensions Diagram

144P6Q-A (MMP) **Plastic 144pin 20 × 20mm body LQFP**

EIAJ Package Code	JEDEC Code	Weight (g)	Lead Material
LQFP144-P-2020-0.50	-	1.23	Cu Alloy





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A_1	0.05	0.125	0.2
A_2	-	1.4	-
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	-	0.5	-
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
L	0.35	0.5	0.65
L_1	-	1.0	-
Lp	0.45	0.6	0.75
A_3	-	0.25	-
x	-	-	0.08
y	-	-	0.1
θ	0°	-	8°
b_2	-	0.225	-
I_2	0.95	-	-
M_D	-	20.4	-
M_E	-	20.4	-

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REVISION HISTORY	32176 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
1.3	Oct. 15, 02	-	First edition
1.4	Jan. 30, 03	P2, P6	The “VCNT pin” is altered to “N.C. pin”.
		P2	In Figure 1, “Pin Layout Diagram,” name of the pins are corrected.
		P6	In Figure 3, “Pin Function Diagram,” the numbers of the VCCE and VSS are corrected.
		P31	In Figure 18, “Block Diagram of CAN Modules,” DMA control circuit is added to CAN1.