M16C/28 Group

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0026-0020Z
Rev.0.20
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1. Overview

The M16C/28 group of single-chip microcomputers is built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and is packaged in a 64-pin and 80-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, office/communications/portable/industrial equipment, etc

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Table 1.2.1 lists performance outline of M16C/28 group 80-pin device.

Table 1.2.2 lists performance outline of M16C/28 group 64-pin device.

Table 1.2.1. Performance outline of M16C/28 group (80-pin device)

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V) (Normal-ver./T-ver.) 100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V) (Normal-ver.) 50 ns (f(BCLK)= 20MHz, Vcc= 4.2V to 5.5V -40 to 105°C) (V-ver.) 62.5 ns (f(BCLK)= 16MHz, Vcc= 4.2V to 5.5V -40 to 125°C) (V-ver.)
Memory capacity	ROM	(See the product list)
	RAM	(See the product list)
I/O port		71 lines
Multifunction timer		TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
Serial I/O		2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I2C bus1 (option3), or IE bus2 (option3) 2 channels (SI/O3, SI/O4) Clock synchronous 1 channel (Multi-Master I2C bus1 (option3))
A-D converter		10 bits x 24 channels
DMAC		2 channels (trigger: 31 sources)
Watchdog timer		15 bits x 1 (with prescaler)
Interrupt		25 internal and 8 external sources, 4 software sources, 7 levels
Clock generation circuit		4 circuits • Main clock, • Sub-clock (These circuits contain a built-in feedback resistor and external ceramic/quartz oscillator) • Ring oscillator(main-clock oscillation stop detect function) • PLL frequency synthesizer
Voltage detection circuit		Present (option3)
Power supply voltage		Vcc=3.0V to 5.5V (f(BCLK)=20MHz) (Normal-ver.) Vcc=2.7V to 5.5V (f(BCLK)=10MHz)
		Vcc=3.0V to 5.5V (T-ver.)
		Vcc=4.2V to 5.5V (V-ver.)
Flash memory	Program/erase voltage	2.7V to 5.5V (Normal-ver.) 3.0V to 5.5V (T-ver.) 4.2V to 5.5V (V-ver.)
	Number of program/erase	100 times (Block A ,Block B : 10,000 times (option3))
Power consumption		16mA (Vcc=5V, f(BCLK)=20MHz) 25 µA (Vcc=3V, f(BCLK)=f(XCIN)=32KHz on RAM) 1.8 µA (Vcc=3V, f(BCLK)=f(XCIN)=32KHz, when wait mode) 0.7 µA (Vcc=3V, when stop mode)
Operating ambient temperature		-20 to 85°C / -40 to 85°C (option3) (Normal-ver.)
		-40 to 85°C (T-ver.)
		-40 to 105°C / -40 to 125°C (V-ver.)
Package		80-pin plastic mold QFP

Notes:
1. I2C Bus is a registered trademark of PHILIPS.
2. IE Bus is a registered trademark of NEC.
3. If you desire this option, please so specify.

Table 1.2.2. Performance outline of M16C/28 group (64-pin device)

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V) (Normal-ver./T-ver.) 100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V) (Normal-ver.) 50 ns (f(BCLK)= 20MHz, Vcc= 4.2V to 5.5V -40 to 105°C) (V-ver.) 62.5 ns (f(BCLK)= 16MHz, Vcc= 4.2V to 5.5V -40 to 125°C) (V-ver.)
Memory capacity	ROM	(See the product list)
	RAM	(See the product list)
I/O port		55 lines
Multifunction timer		TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
Serial I/O		2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I2C bus1 (option3), or IE bus2 (option3) 1 channel (SI/O3) Clock synchronous 1 channel (Multi-Master I2C bus1 (option3))
A-D converter		10 bits x 13 channels
DMAC		2 channels (trigger: 30 sources)
Watchdog timer		15 bits x 1 (with prescaler)
Interrupt		24 internal and 8 external sources, 4 software sources, 7 levels
Clock generation circuit		4 circuits • Main clock, • Sub-clock (These circuits contain a built-in feedback resistor and external ceramic/quartz oscillator) • Ring oscillator(main-clock oscillation stop detect function) • PLL frequency synthesizer
Voltage detection circuit		Present (option3)
Power supply voltage		Vcc=3.0V to 5.5V (f(BCLK)=20MHz) (Normal-ver.) Vcc=2.7V to 5.5V (f(BCLK)=10MHz)
		Vcc=3.0V to 5.5V (T-ver.)
		Vcc=4.2V to 5.5V (V-ver.)
Flash memory	Program/erase voltage	2.7V to 5.5V (Normal-ver.) 3.0V to 5.5V (T-ver.) 4.2V to 5.5V (V-ver.)
	Number of program/erase	100 times (Block A ,Block B : 10,000 times (option3))
Power consumption		16mA (Vcc=5V, f(BCLK)=20MHz) 25 µA (Vcc=3V, f(BCLK)=f(XCIN)=32KHz on RAM) 1.8 µA (Vcc=3V, f(BCLK)=f(XCIN)=32KHz, when wait mode) 0.7 µA (Vcc=3V, when stop mode)
Operating ambient temperature		-20 to 85°C / -40 to 85°C (option3) (Normal-ver.)
		-40 to 85°C (T-ver.)
		-40 to 105°C / -40 to 125°C (V-ver.)
Package		64-pin plastic mold QFP

Notes:
1. I2C Bus is a registered trademark of PHILIPS.
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3. If you desire this option, please so specify.

1.3 Block Diagram

Figure 1.3.1 is a block diagram of the M16C/28 group, 80-pin device.

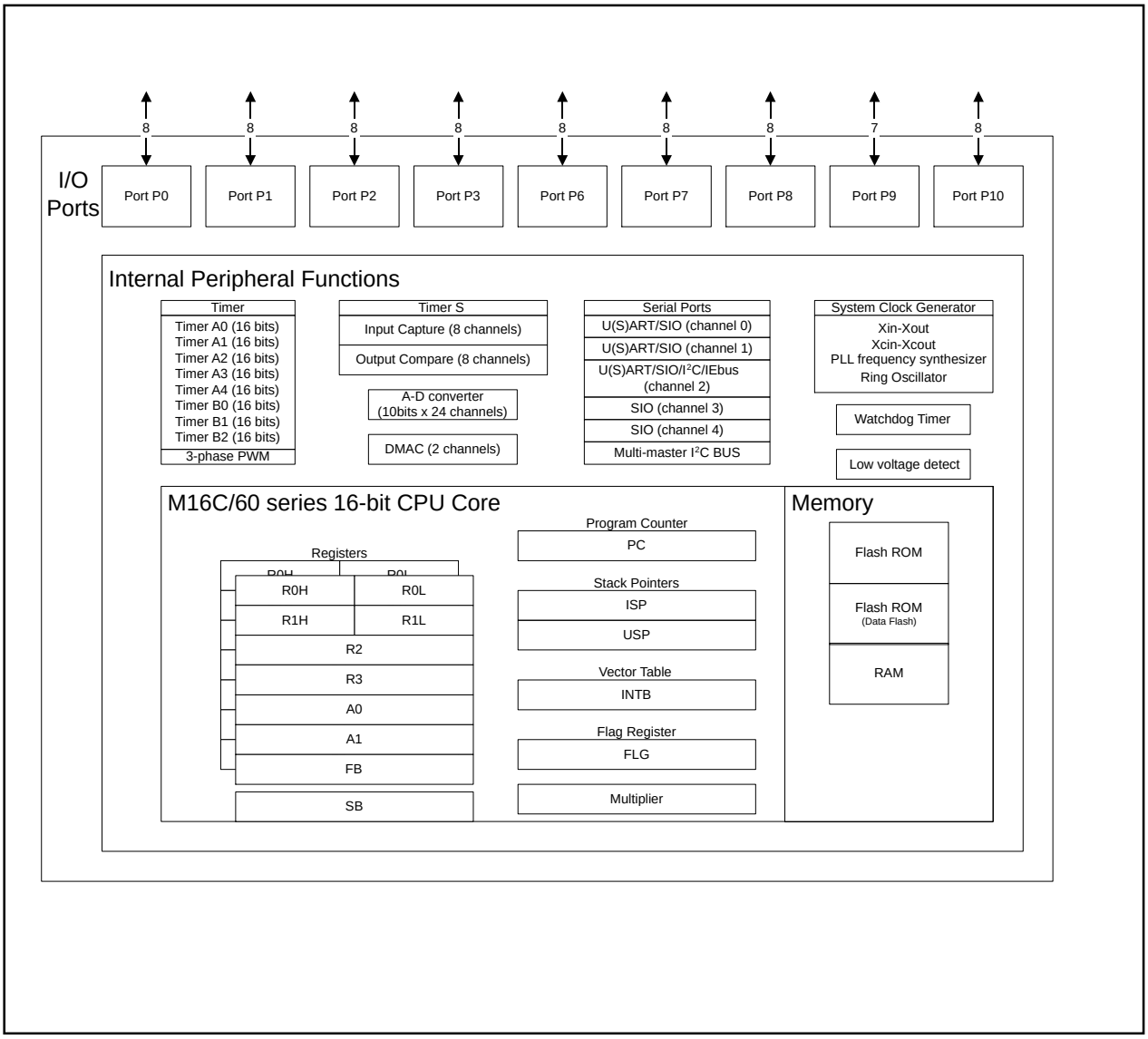


Figure 1.3.1. M16C/28 Group, 80-pin Block Diagram

Figure 1.3.2 is a block diagram of the M16C/28 group, 64-pin device.

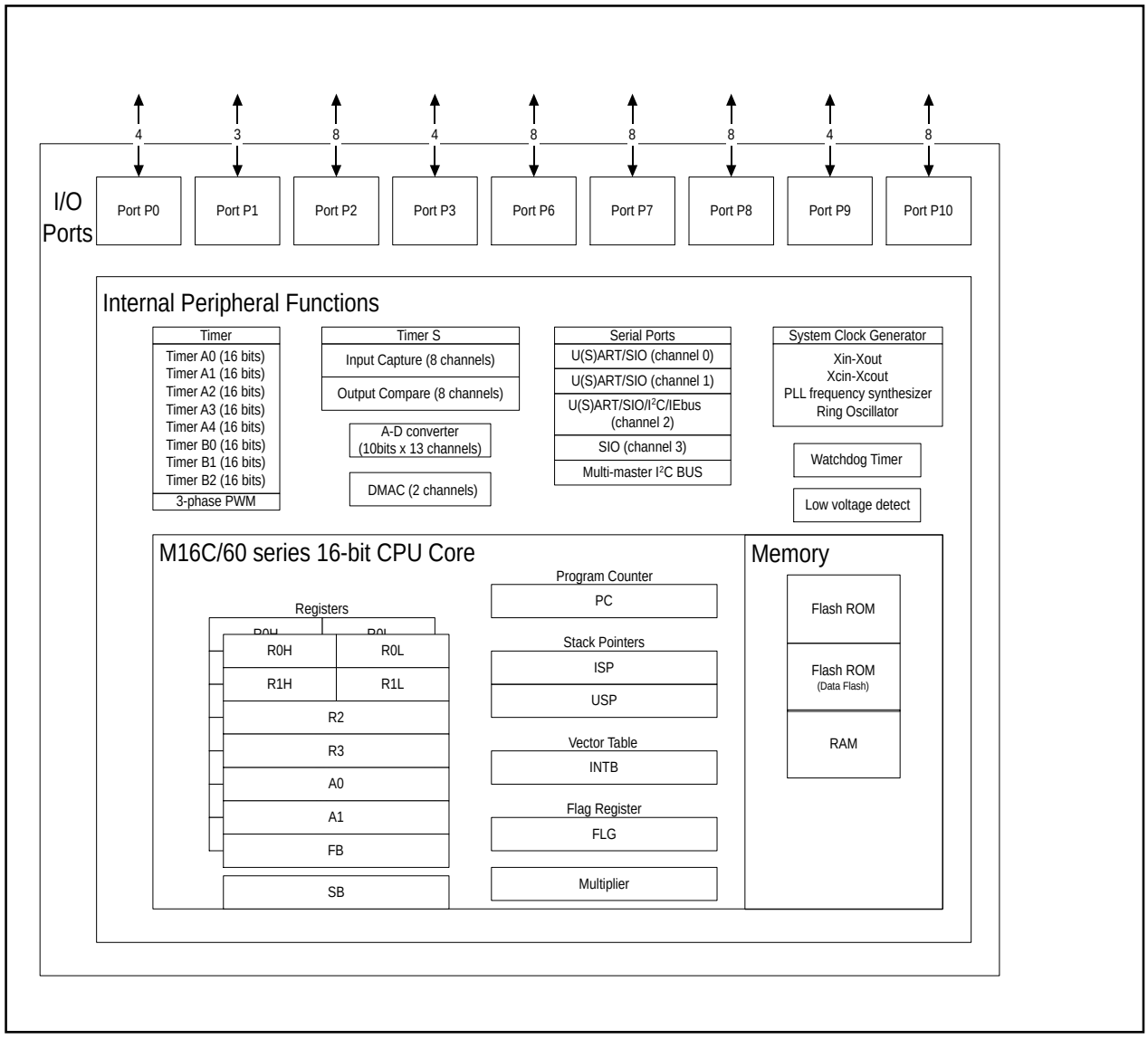


Figure 1.3.2. M16C/28 Group, 64-pin Block Diagram

1.4 Product List

Tables 1.4.1 to 1.4.3 list the M16C/28 group products and Figure 1.4.1 shows the type numbers, memory sizes and packages.

Table 1.4.1. Product List (1) -Normal Version

As of November 2003

Type No.		ROM capacity	RAM capacity	Package type	Remarks
M30280F6HP	**	48K + 4K byte	4K byte	80P6Q-A	Flash ROM Version
M30280F8HP	**	64K + 4K byte	4K byte		
M30280FAHP	**	96K + 4K byte	8K byte		
M30281F6HP	**	48K + 4K byte	4K byte	64P6Q-A	
M30281F8HP	**	64K + 4K byte	4K byte		
M30281FAHP	**	96K + 4K byte	8K byte		
M30280M4-XXXHP	*	32K byte	2K byte	80P6Q-A	Mask ROM Version
M30280M6-XXXHP	*	48K byte	4K byte		
M30280M8-XXXHP	*	64K byte	4K byte		
M30281M4-XXXHP	*	32K byte	2K byte	64P6Q-A	
M30281M6-XXXHP	*	48K byte	4K byte		
M30281M8-XXXHP	*	64K byte	4K byte		

* : under planning

** : under development

Table 1.4.2. Product List (2) -T Version

As of November 2003

Type No.		ROM capacity	RAM capacity	Package type	Remarks
M30280F6THP	**	48K + 4K byte	4K byte	80P6Q-A	Flash ROM Version (T-version)
M30280F8THP	**	64K + 4K byte	4K byte		
M30280FATHP	**	96K + 4K byte	8K byte		
M30281F6THP	**	48K + 4K byte	4K byte	64P6Q-A	
M30281F8THP	**	64K + 4K byte	4K byte		
M30281FATHP	**	96K + 4K byte	8K byte		
M30280M4T-XXXHP	*	32K byte	2K byte	80P6Q-A	Mask ROM Version (T-version)
M30280M6T-XXXHP	*	48K byte	4K byte		
M30280M8T-XXXHP	*	64K byte	4K byte		
M30281M4T-XXXHP	*	32K byte	2K byte	64P6Q-A	
M30281M6T-XXXHP	*	48K byte	4K byte		
M30281M8T-XXXHP	*	64K byte	4K byte		

* : under planning

** : under development

Table 1.4.2. Product List (3) -V Version

As of November 2003

Type No.		ROM capacity	RAM capacity	Package type	Remarks
M30280F6VHP	**	48K + 4K byte	4K byte	80P6Q-A	Flash ROM Version (V-version)
M30280F8VHP	**	64K + 4K byte	4K byte		
M30280FAVHP	**	96K + 4K byte	8K byte		
M30281F6VHP	**	48K + 4K byte	4K byte	64P6Q-A	
M30281F8VHP	**	64K + 4K byte	4K byte		
M30281FAVHP	**	96K + 4K byte	8K byte		
M30280M4V-XXXHP	*	32K byte	2K byte	80P6Q-A	Mask ROM Version (V-version)
M30280M6V-XXXHP	*	48K byte	4K byte		
M30280M8V-XXXHP	*	64K byte	4K byte		
M30281M4V-XXXHP	*	32K byte	2K byte	64P6Q-A	
M30281M6V-XXXHP	*	48K byte	4K byte		
M30281M8V-XXXHP	*	64K byte	4K byte		

* : under planning

** : under development

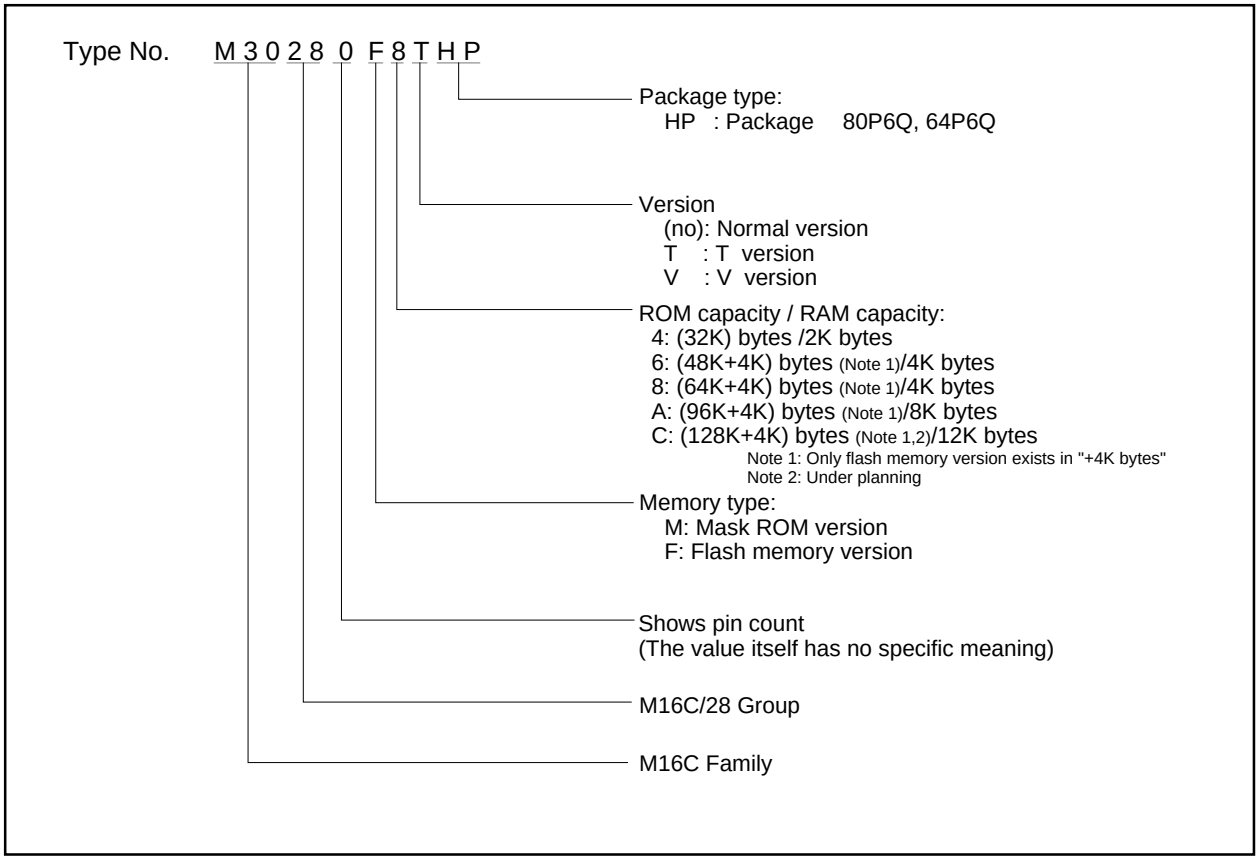


Figure 1.4.1. Type No., Memory Size, and Package

1.5 Pin Configuration

Figures 1.5.1 and 1.5.2 show the pin configurations (top view).

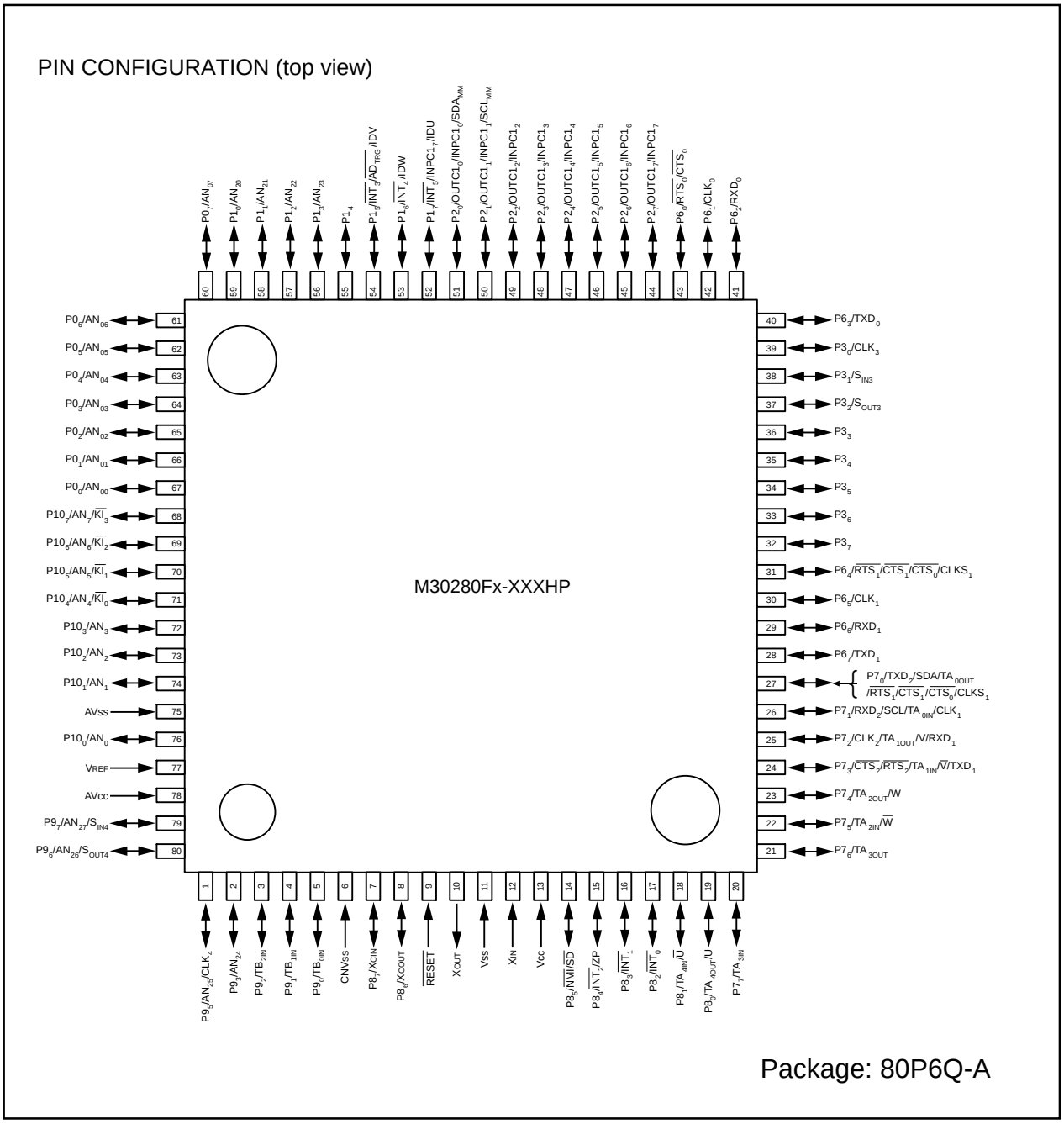


Figure 1.5.1. Pin Configuration (Top View) of M16C/28 Group, 80-pin Package

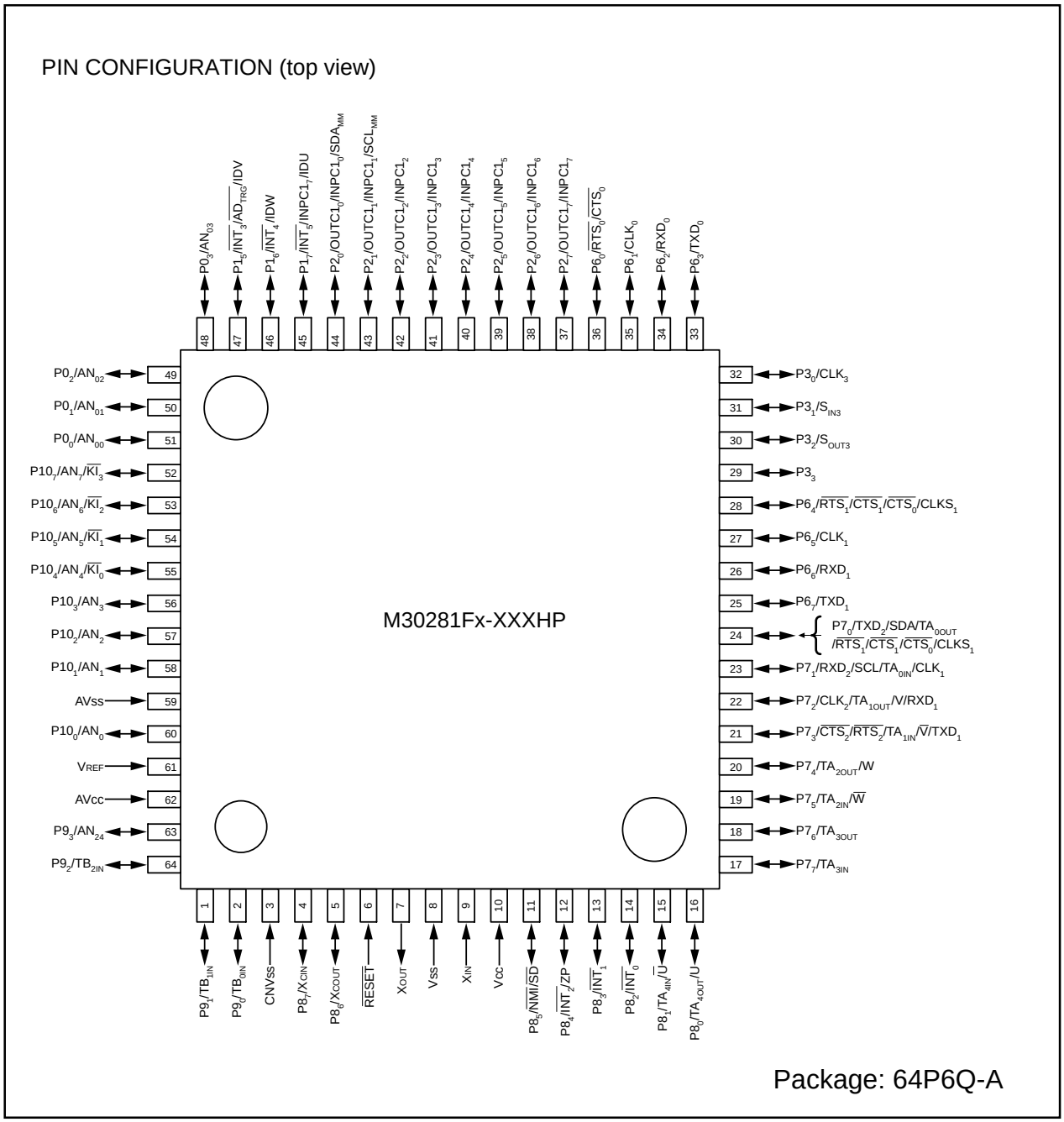


Figure 1.5.2. Pin Configuration (Top View) of M16C/28 Group, 64-pin Package

1.6 Pin Description

Table 1.6.1 and 1.6.2 describes the available pins.

Table 1.6.1 Pin Description(1)

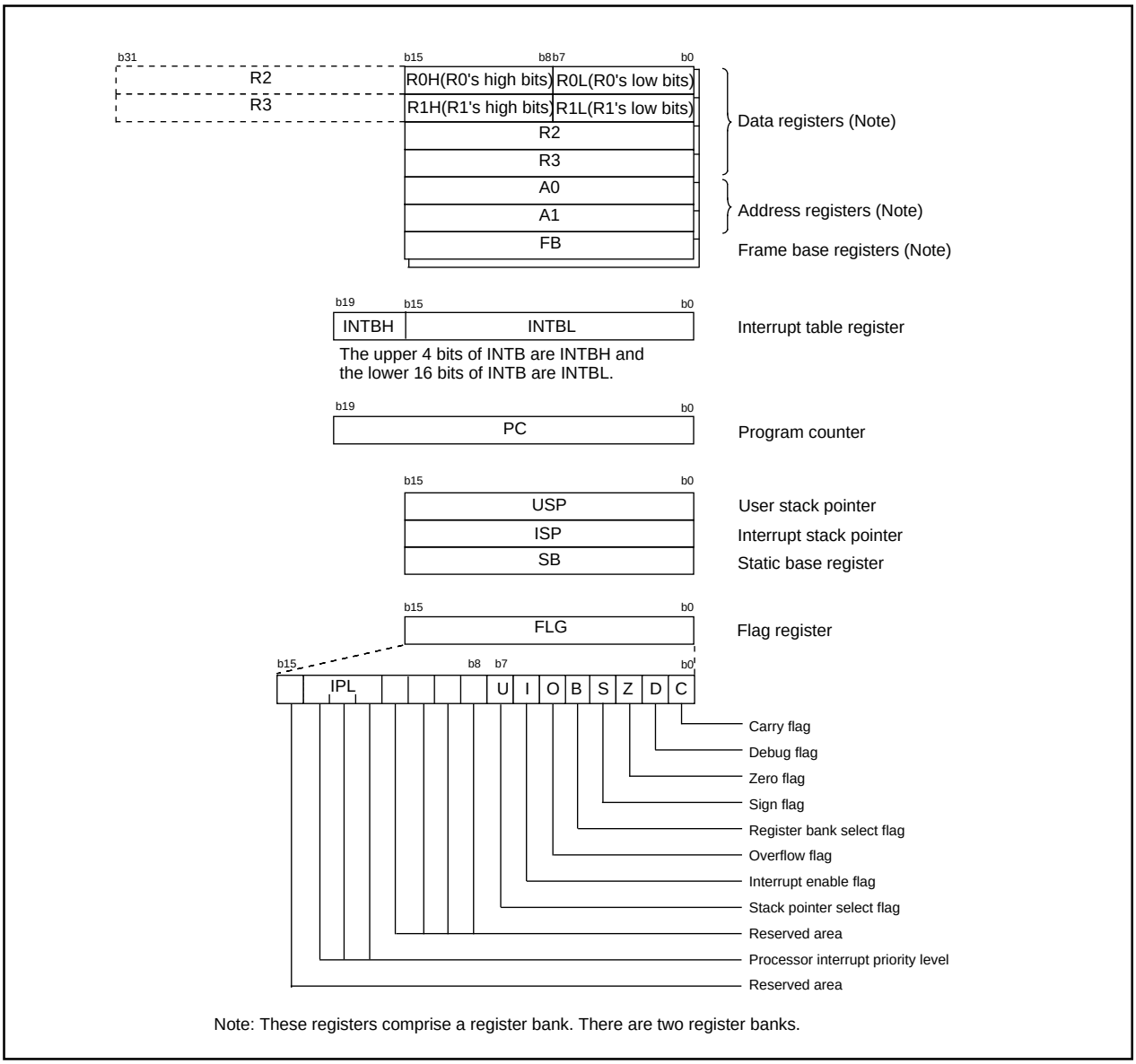
Pin name	Signal name	I/O type	Function
V_{CC},V_{SS}	Power supply input		Apply 0V to the Vss pin, and the following voltage to the Vcc pin. 2.7 to 5.5V (Normal-ver.) 3.0 to 5.5V (T-ver.) 4.2 to 5.5V (V-ver.)
CNV_{SS}	CNV_{SS}	Input	Connect this pin to Vss.
$\overline{RESET}$	Reset input	Input	"L" on this input resets the microcomputer.
X_{IN} X_{OUT}	Clock input Clock output	Input Output	These pins are provided for the main clock generating circuit input/ output. Connent a ceramic resonator or crystal between the X_{IN} and the X_{OUT} pins. To use an externally derived clock, input it to the X_{IN} pin and leave the X_{OUT} pin open. If X_{IN} is not used (for external oscillator or external clock) connect X_{IN} pin to V_{CC} and leave X_{OUT} pin open.
AV_{CC}	Analog power supply input		This pin is a power supply input for the A-D converter. Connect this pin to V_{CC}.
AV_{SS}	Analog power supply input		This pin is a power supply input for the A-D converter. Connect this pin to V_{SS}.
V_{REF}	Reference Voltage input	Input	This pin is a reference voltage input for the A-D converter.
$P0_0$~$P0_7$	I/O port P0	Input/output	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input, a pull-up resister option can be selected for the entire group of four pins.Software can also select this port to function as A-D converter input pins. $P0_4$~$P0_7$ is not in 64 pin version.
$P1_0$~$P1_7$	I/O port P1	Input/output	This is an 8-bit I/O port equivalent to P0. Additional software-select able secondary functions are: 1) $P1_0$ to $P1_3$ can act as A-D converter input pins; 2) $P1_5$ to $P1_7$ can be configured as external interrupt pins; 3) $P1_5$ to $P1_7$ can be configured as position-data-retain function input pins,and; 4) $P1_5$ can input a trigger for the A-D converter. $P1_0$~$P1_4$ is not in 64 pin version.
$P2_0$~$P2_7$	I/O port P2	Input/output	This is an 8-bit I/O port equivalent to P0. Software can also select this port to perform as I/O for the Timer S (all pins), and MultiMaster I^2C Bus ($P2_0$ and $P2_1$ only)
$P3_0$~$P3_7$	I/O port P3	Input/output	This is an 8-bit I/O port equivalent to P0. $P3_0$ to $P3_2$ also function as SIO3 I/O, as selected by software. $P3_4$~$P3_7$ is not in 64 pin version.
$P6_0$~$P6_7$	I/O port P6	Input/output	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as UART0 and UART1 I/O, as selected by software.
$P7_0$~$P7_7$	I/O port P7	Input/output	This is an 8-bit I/O port equivalent to P0. P7 can also function as I/O for timer A0-A3, as selected by software. Additional programming options are: $P7_0$ to $P7_3$ can assume UART1 and UART2 I/O capabilities, and $P7_2$ to $P7_5$ can function as output pins for the three-phase motor control timer.

Table 1.6.2 Pin Description(2)

Pin name	Signal name	I/O type	Function
$P8_0$~$P8_7$	I/O port P8	Input/output	This is an 8-bit I/O port equivalent to P0. Additional software-select able secondary functions are: 1) $P8_0$ and $P8_1$ can act as either I/O for Timer A4, or as output pins for the three-phase motor control timer; 2) $P8_2$ to $P8_4$ can be configured as external interrupt pins. $P8_4$ can be used for Timer A Zphase function; 3) $P8_5$ can be used as $\overline{NMI}/\overline{SD}$. $P8_5$ can not be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $P8_5$ after setting the direction register for $P8_5$ to "0" when the three-phase motor control is enabled, and; 4) $P8_6$ and $P8_7$ can serve as I/O pins for the sub-clock generation circuit. In this latter case, a quartz oscillator must be connented between $P8_6$ (X_{COUT} pin) and $P8_7$ (X_{CIN} pin).
$P9_0$~$P9_3$, $P9_5$~$P9_7$	I/O port P9	Input/output	This is an 7-bit I/O port equivalent to P0. Additional software-select able secondary functions are: 1) $P9_0$ to $P9_2$ can act as Timer B0~B2 input pins; 2) $P9_3$, $P9_5$ to $P9_7$ can act as A-D converter input pins, and; 3) $P9_6$ to $P9_7$ can assume SI/O4 I/O. $P9_5$ to $P9_7$ is not in 64 pin version.
$P10_0$~$P10_7$	I/O port P10	Input/output	This is an 8-bit I/O port equivalent to P0. This port can also function as A-D converter input pins, as selected by software. Furthermore, $P10_4$-$P10_7$ can also function as input pins for the key input interrupt function.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.



Note: These registers comprise a register bank. There are two register banks.

Figure 2.1. Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is cleared to “0” when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.

The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of the M16C/28 group. The linear address space of 1M bytes extends from address 00000$_{16}$ to FFFFF$_{16}$. From FFFFF$_{16}$ down is ROM. For example, in the M30280F8HP,there are 64 Kbytes of internal ROM from F0000$_{16}$ to FFFFF$_{16}$.

The vector table for fixed interrupts, such as Reset and NMI, is mapped from FFFDC$_{16}$ to FFFFF$_{16}$. The starting address of the interrupt routine is stored here.

The address of the vector table for timer interrupts,etc.,can be set as desired using the interrupt table register(INTB). See the section on interrupts for details.

From 00400$_{16}$ up is RAM. For example, in the M30280F8HP, 4K bytes of internal RAM is mapped to the space from 00400$_{16}$ to 013FF$_{16}$. In addition to storing data, the RAM also stores the stack used when calling subroutines and when interrupts are generated.

These devices also contain two blocks of Flash ROM as Data Flash memory to store data. These two blocks of 2K bytes are located from 0F000$_{16}$ to 0FFFF$_{16}$ on all versions.

The SFR area is mapped from 00000$_{16}$ to 003FF$_{16}$. This area accommodates the control registers for peripheral devices such as I/O ports, A-D converter, serial I/O, and timers, etc. Any part of the SFR area that is not occupied is reserved and cannot be used for other purposes.

The special page vector table is allocated to the address from FFE00$_{16}$ to FFFDB$_{16}$. This vector is used by the JMPS or JSRS instruction. For details, refer to the "M16C/60 and M16C/20 Series Software Manual".

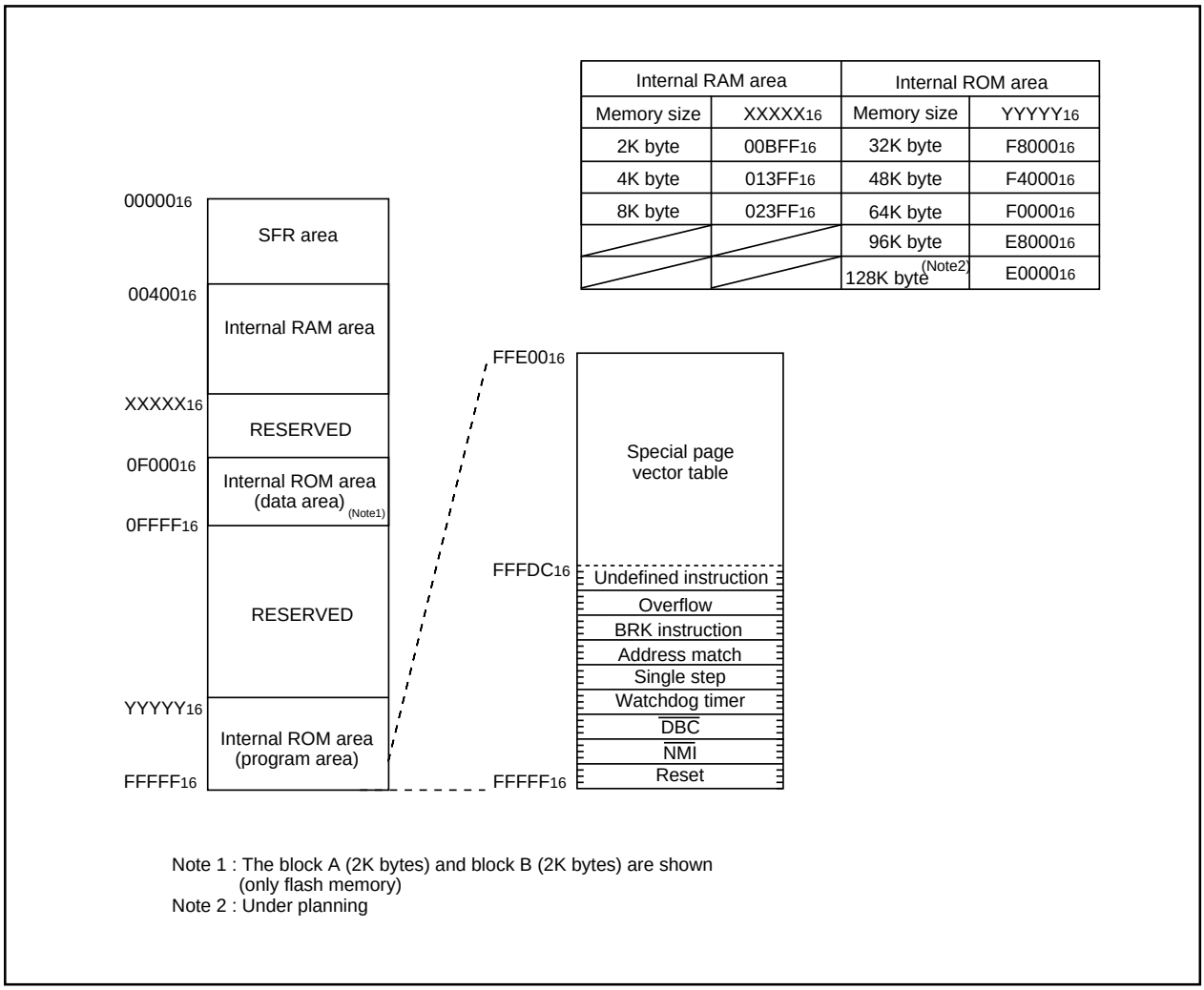


Figure 3.1. Memory Map

4. Special Function Register (SFR) Map

Address	Register Name	Acronym	Value after Reset
0000$_{16}$			
0001$_{16}$			
0002$_{16}$			
0003$_{16}$			
0004$_{16}$	Processor mode register 0	PM0	00$_{16}$
0005$_{16}$	Processor mode register 1	PM1	00001000$_2$
0006$_{16}$	System clock control register 0	CM0	01001000$_2$
0007$_{16}$	System clock control register 1	CM1	00100000$_2$
0008$_{16}$			
0009$_{16}$	Address match interrupt enable register	AIER	XXXXXX00$_2$
000A$_{16}$	Protect register	PRCR	XX000000$_2$
000B$_{16}$			
000C$_{16}$	Oscillation stop detection register (Note 2)	CM2	0X000010$_2$
000D$_{16}$			
000E$_{16}$	Watchdog timer start register	WDTS	??$_{16}$
000F$_{16}$	Watchdog timer control register	WDC	00??????$_2$(Note 3)
0010$_{16}$	Address match interrupt register 0	RMAD0	00$_{16}$
0011$_{16}$			00$_{16}$
0012$_{16}$			X0$_{16}$
0013$_{16}$			
0014$_{16}$	Address match interrupt register 1	RMAD1	00$_{16}$
0015$_{16}$			00$_{16}$
0016$_{16}$			X0$_{16}$
0017$_{16}$			
0018$_{16}$			
0019$_{16}$	Voltage detection register 1 (Note 4)	VCR1	00001000$_2$
001A$_{16}$	Voltage detection register 2 (Note 4)	VCR2	00$_{16}$
001B$_{16}$			
001C$_{16}$	PLL control register 0	PLC0	0001X010$_2$
001D$_{16}$			
001E$_{16}$	Processor mode register 2	PM2	XXX00000$_2$
001F$_{16}$	Voltage down detection interrupt register	D4INT	00$_{16}$
0020$_{16}$	DMA0 source pointer	SAR0	??$_{16}$
0021$_{16}$			??$_{16}$
0022$_{16}$			X?$_{16}$
0023$_{16}$			
0024$_{16}$	DMA0 destination pointer	DAR0	??$_{16}$
0025$_{16}$			??$_{16}$
0026$_{16}$			X?$_{16}$
0027$_{16}$			
0028$_{16}$	DMA0 transfer counter	TCR0	??$_{16}$
0029$_{16}$			??$_{16}$
002A$_{16}$			
002B$_{16}$			
002C$_{16}$	DMA0 control register	DM0CON	00000?00$_2$
002D$_{16}$			
002E$_{16}$			
002F$_{16}$			
0030$_{16}$	DMA1 source pointer	SAR1	??$_{16}$
0031$_{16}$			??$_{16}$
0032$_{16}$			X?$_{16}$
0033$_{16}$			
0034$_{16}$	DMA1 destination pointer	DAR1	??$_{16}$
0035$_{16}$			??$_{16}$
0036$_{16}$			X?$_{16}$
0037$_{16}$			
0038$_{16}$	DMA1 transfer counter	TCR1	??$_{16}$
0039$_{16}$			??$_{16}$
003A$_{16}$			
003B$_{16}$			
003C$_{16}$	DMA1 control register	DM1CON	00000?00$_2$
003D$_{16}$			
003E$_{16}$			
003F$_{16}$			

Note 1: The blank areas are reserved and cannot be accessed by users.
Note 2: The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
Note 3: Tjhe WDC5 bit is "0" (cold start) immediately after power-on. It can only be set to "1" in a program. It is set to "0" when the input voltage at the Vcc pin drops to Vdet2 or less while the VC25 bit in the VCR2 register is set to "1"(RAM retention limit detection circuit enable).
Note 4: This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.

X : Noting is mapped to this bit
? : Value indeterminate at reset

Figure 4.1. SFR Map (1 of 7)

Address	Register Name	Acronym	Value after Reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆	INT3 interrupt control register	INT3IC	XX00?000₂
0045₁₆	IC/OC interrupt control register	ICOCIC	XXXX?000₂
0046₁₆	IC/OC interrupt control register 1, I²C-BUS interface interrupt control register	ICOC1IC, IICIC	XXXX?000₂
0047₁₆	IC/OC interrupt control register 2, SCLSDA interrupt control register	ICOC2IC, SCLDAIC	XXXX?000₂
0048₁₆	SI/O4 interrupt control register, INT5 interrupt control register	S4IC, INT5IC	XX00?000₂
0049₁₆	SI/O3 interrupt control register, INT4 interrupt control register	S3IC, INT4IC	XX00?000₂
004A₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXX?000₂
004B₁₆	DMA0 interrupt control register	DM0IC	XXXX?000₂
004C₁₆	DMA1 interrupt control register	DM1IC	XXXX?000₂
004D₁₆	Key input interrupt control register	KUPIC	XXXX?000₂
004E₁₆	A-D conversion interrupt control register	ADIC	XXXX?000₂
004F₁₆	UART2 transmit interrupt control register	S2TIC	XXXX?000₂
0050₁₆	UART2 receive interrupt control register	S2RIC	XXXX?000₂
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXX?000₂
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXX?000₂
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXX?000₂
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXX?000₂
0055₁₆	Timer A0 interrupt control register	TA0IC	XXXX?000₂
0056₁₆	Timer A1 interrupt control register	TA1IC	XXXX?000₂
0057₁₆	Timer A2 interrupt control register	TA2IC	XXXX?000₂
0058₁₆	Timer A3 interrupt control register	TA3IC	XXXX?000₂
0059₁₆	Timer A4 interrupt control register	TA4IC	XXXX?000₂
005A₁₆	Timer B0 interrupt control register	TB0IC	XXXX?000₂
005B₁₆	Timer B1 interrupt control register	TB1IC	XXXX?000₂
005C₁₆	Timer B2 interrupt control register	TB2IC	XXXX?000₂
005D₁₆	INT0 interrupt control register	INT0IC	XX00?000₂
005E₁₆	INT1 interrupt control register	INT1IC	XX00?000₂
005F₁₆	INT2 interrupt control register	INT2IC	XX00?000₂
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

Note 1: The blank areas are reserved and cannot be accessed by users.

X : Noting is mapped to this bit
? : Value indeterminate at reset

Figure 4.2. SFR Map (2 of 7)

Address	Register Name	Acronym	Value after Reset
0080₁₆			
0081₁₆			
0082₁₆			
0083₁₆			
0084₁₆			
0085₁₆			
0086₁₆			
≈			≈
01B0₁₆			
01B1₁₆			
01B2₁₆			
01B3₁₆	Flash memory control register 4 (Note 2)	FMR4	01000000₂
01B4₁₆			
01B5₁₆	Flash memory control register 1 (Note 2)	FMR1	000???0?₂
01B6₁₆			
01B7₁₆	Flash memory control register 0 (Note 2)	FMR0	??000001₂
01B8₁₆			
01B9₁₆			
01BA₁₆			
01BB₁₆			
01BC₁₆			
01BD₁₆			
01BE₁₆			
01BF₁₆			
≈			≈
0250₁₆			
0251₁₆			
0252₁₆			
0253₁₆			
0254₁₆			
0255₁₆			
0256₁₆			
0257₁₆			
0258₁₆			
0259₁₆			
025A₁₆			
025B₁₆			
025C₁₆	Ring oscillator control register	ROCR	00000101₂
025D₁₆	Pin assignment control register	PACR	00₁₆
025E₁₆	Peripheral clock select register	PCLKR	00000011₂
025F₁₆			
≈			≈
02E0₁₆	I^2C0 data shift register	S00	??₁₆
02E1₁₆	I^2C0 address register 2	S0D02	00₁₆
02E2₁₆	I^2C0 address register	S0D0	00₁₆
02E3₁₆	I^2C0 control register 0	S1D0	00₁₆
02E4₁₆	I^2C0 clock control register	S20	00₁₆
02E5₁₆	I^2C0 start/stop condition control register	S2D0	00011010₂
02E6₁₆	I^2C0 control register 1	S3D0	00110000₂
02E7₁₆	I^2C0 control register 2	S4D0	00₁₆
02E8₁₆	I^2C0 status register	S10	0001000X₂
02E9₁₆			
02EA₁₆			
≈			≈
02FE₁₆			
02FF₁₆			

Note 1:The blank areas are reserved and cannot be accessed by users.
Note 2:This register is included in the flash memory version.

X : Noting is mapped to this bit
? : Value indeterminate at reset

Figure 4.3. SFR Map (3 of 7)

Address	Register Name	Acronym	Value after Reset
0300₁₆	TM/WG register 0	G1TM0/G1PO0	??₁₆
0301₁₆			??₁₆
0302₁₆	TM/WG register 1	G1TM1/G1PO1	??₁₆
0303₁₆			??₁₆
0304₁₆	TM/WG register 2	G1TM2/G1PO2	??₁₆
0305₁₆			??₁₆
0306₁₆	TM/WG register 3	G1TM3/G1PO3	??₁₆
0307₁₆			??₁₆
0308₁₆	TM/WG register 4	G1TM4/G1PO4	??₁₆
0309₁₆			??₁₆
030A₁₆	TM/WG register 5	G1TM5/G1PO5	??₁₆
030B₁₆			??₁₆
030C₁₆	TM/WG register 6	G1TM6/G1PO6	??₁₆
030D₁₆			??₁₆
030E₁₆	TM/WG register 7	G1TM7/G1PO7	??₁₆
030F₁₆			??₁₆
0310₁₆	WG control register 0	G1POCR0	0X00X000₂
0311₁₆	WG control register 1	G1POCR1	0X00X000₂
0312₁₆	WG control register 2	G1POCR2	0X00X000₂
0313₁₆	WG control register 3	G1POCR3	0X00X000₂
0314₁₆	WG control register 4	G1POCR4	0X00X000₂
0315₁₆	WG control register 5	G1POCR5	0X00X000₂
0316₁₆	WG control register 6	G1POCR6	0X00X000₂
0317₁₆	WG control register 7	G1POCR7	0X00X000₂
0318₁₆	TM control register 0	G1TMCR0	00₁₆
0319₁₆	TM control register 1	G1TMCR1	00₁₆
031A₁₆	TM control register 2	G1TMCR2	00₁₆
031B₁₆	TM control register 3	G1TMCR3	00₁₆
031C₁₆	TM control register 4	G1TMCR4	00₁₆
031D₁₆	TM control register 5	G1TMCR5	00₁₆
031E₁₆	TM control register 6	G1TMCR6	00₁₆
031F₁₆	TM control register 7	G1TMCR7	00₁₆
0320₁₆	Base timer register	G1BT	??₁₆
0321₁₆			??₁₆
0322₁₆	Base timer control register 0	G1BCR0	00₁₆
0323₁₆	Base timer control register 1	G1BCR1	00₁₆
0324₁₆	TM prescaler register 6	G1TPR6	00₁₆
0325₁₆	TM prescaler register 7	G1TPR7	00₁₆
0326₁₆	Function enable register	G1FE	00₁₆
0327₁₆	Function select register	G1FS	00₁₆
0328₁₆	Base timer reset register	G1BTRR	??₁₆
0329₁₆			??₁₆
032A₁₆	Divider register	G1DV	00₁₆
032B₁₆			
032C₁₆			
032D₁₆			
032E₁₆			
032F₁₆			
0330₁₆	Interrupt request register 0	G1IR	??₁₆
0331₁₆	Interrupt enable register 0	G1IE0	00₁₆
0332₁₆	Interrupt enable register 1	G1IE1	00₁₆
0333₁₆			
0334₁₆			
0335₁₆			
0336₁₆			
0337₁₆			
0338₁₆			
0339₁₆			
033A₁₆			
033B₁₆			
033C₁₆			
033D₁₆			
033E₁₆	NMI digital debounce register	NDDR	FF₁₆
033F₁₆	P17 digital debounce register	P17DDR	FF₁₆

Note 1:The blank areas are reserved and cannot be accessed by users.

X : Noting is mapped to this bit
? : Value indeterminate at reset

Figure 4.4. SFR Map (4 of 7)

Address	Register Name	Acronym	Value after Reset
0340₁₆			
0341₁₆			
0342₁₆	Timer A1-1 register	TA11	??16
0343₁₆			??16
0344₁₆	Timer A2-1 register	TA21	??16
0345₁₆			??16
0346₁₆	Timer A4-1 register	TA41	??16
0347₁₆			??16
0348₁₆	Three-phase PWM control register 0	INVC0	0016
0349₁₆	Three-phase PWM control register 1	INVC1	0016
034A₁₆	Three-phase output buffer register 0	IDB0	0016
034B₁₆	Three-phase output buffer register 1	IDB1	0016
034C₁₆	Dead time timer	DTT	??16
034D₁₆	Timer B2 interrupt occurrence frequency set counter	ICTB2	X?16
034E₁₆	Position-data-retain function contol register	PDRF	XXXX00002
034F₁₆			
0350₁₆			
0351₁₆			
0352₁₆			
0353₁₆			
0354₁₆			
0355₁₆			
0356₁₆			
0357₁₆			
0358₁₆			
0359₁₆			
035A₁₆			
035B₁₆			
035C₁₆			
035D₁₆			
035E₁₆	Interrupt request cause select register 2	IFSR2A	00XXXXXX2(Note 2)
035F₁₆	Interrupt request cause select register	IFSR	0016
0360₁₆	SI/O3 transmit/receive register	S3TRR	??16
0361₁₆			
0362₁₆	SI/O3 control register	S3C	010000002
0363₁₆	SI/O3 bit rate generator	S3BRG	??16
0364₁₆	SI/O4 transmit/receive register	S4TRR	??16
0365₁₆			
0366₁₆	SI/O4 control register	S4C	010000002
0367₁₆	SI/O4 bit rate generator	S4BRG	??16
0368₁₆			
0369₁₆			
036A₁₆			
036B₁₆			
036C₁₆			
036D₁₆			
036E₁₆			
036F₁₆			
0370₁₆			
0371₁₆			
0372₁₆			
0373₁₆			
0374₁₆	UART2 special mode register 4	U2SMR4	0016
0375₁₆	UART2 special mode register 3	U2SMR3	000X0X0X2
0376₁₆	UART2 special mode register 2	U2SMR2	X0000000₂
0377₁₆	UART2 special mode register	U2SMR	X0000000₂
0378₁₆	UART2 transmit/receive mode register	U2MR	0016
0379₁₆	UART2 bit rate generator	U2BRG	??16
037A₁₆	UART2 transmit buffer register	U2TB	????????2
037B₁₆			XXXXXXX?2
037C₁₆	UART2 transmit/receive control register 0	U2C0	000010002
037D₁₆	UART2 transmit/receive control register 1	U2C1	000000102
037E₁₆	UART2 receive buffer register	U2RB	????????2
037F₁₆			?????XX?2

Note 1: The blank areas are reserved and cannot be accessed by users.
Note 2: Write "1" to bit 0 after reset.

X : Noting is mapped to this bit
? : Value indeterminate at reset

Figure 4.5. SFR Map (5 of 7)

Address	Register Name	Acronym	Value after Reset
0380₁₆	Count start flag	TABSR	00₁₆
0381₁₆	Clock prescaler reset flag	CPSRF	0XXXXXXX₂
0382₁₆	One-shot start flag	ONSF	00₁₆
0383₁₆	Trigger select register	TRGSR	00₁₆
0384₁₆	Up-down flag	UDF	00₁₆
0385₁₆			
0386₁₆	Timer A0 register	TA0	??₁₆
0387₁₆			??₁₆
0388₁₆	Timer A1 register	TA1	??₁₆
0389₁₆			??₁₆
038A₁₆	Timer A2 register	TA2	??₁₆
038B₁₆			??₁₆
038C₁₆	Timer A3 register	TA3	??₁₆
038D₁₆			??₁₆
038E₁₆	Timer A4 register	TA4	??₁₆
038F₁₆			??₁₆
0390₁₆	Timer B0 register	TB0	??₁₆
0391₁₆			??₁₆
0392₁₆	Timer B1 register	TB1	??₁₆
0393₁₆			??₁₆
0394₁₆	Timer B2 register	TB2	??₁₆
0395₁₆			??₁₆
0396₁₆	Timer A0 mode register	TA0MR	00₁₆
0397₁₆	Timer A1 mode register	TA1MR	00₁₆
0398₁₆	Timer A2 mode register	TA2MR	00₁₆
0399₁₆	Timer A3 mode register	TA3MR	00₁₆
039A₁₆	Timer A4 mode register	TA4MR	00₁₆
039B₁₆	Timer B0 mode register	TB0MR	00??0000₂
039C₁₆	Timer B1 mode register	TB1MR	00?X0000₂
039D₁₆	Timer B2 mode register	TB2MR	00?X0000₂
039E₁₆	Timer B2 special mode register	TB2SC	X0000000₂
039F₁₆			
03A0₁₆	UART0 transmit/receive mode register	U0MR	00₁₆
03A1₁₆	UART0 bit rate generator	U0BRG	??₁₆
03A2₁₆	UART0 transmit buffer register	U0TB	????????₂
03A3₁₆			XXXXXXX?₂
03A4₁₆	UART0 transmit/receive control register 0	U0C0	00001000₂
03A5₁₆	UART0 transmit/receive control register 1	U0C1	00000010₂
03A6₁₆	UART0 receive buffer register	U0RB	????????₂
03A7₁₆			?????XX?₂
03A8₁₆	UART1 transmit/receive mode register	U1MR	00₁₆
03A9₁₆	UART1 bit rate generator	U1BRG	??₁₆
03AA₁₆	UART1 transmit buffer register	U1TB	????????₂
03AB₁₆			XXXXXXX?₂
03AC₁₆	UART1 transmit/receive control register 0	U1C0	00001000₂
03AD₁₆	UART1 transmit/receive control register 1	U1C1	00000010₂
03AE₁₆	UART1 receive buffer register	U1RB	????????₂
03AF₁₆			?????XX?₂
03B0₁₆	UART transmit/receive control register 2	UCON	X0000000₂
03B1₁₆			
03B2₁₆			
03B3₁₆			
03B4₁₆			
03B5₁₆			
03B6₁₆			
03B7₁₆			
03B8₁₆	DMA0 request cause select register	DM0SL	00₁₆
03B9₁₆			
03BA₁₆	DMA1 request cause select register	DM1SL	00₁₆
03BB₁₆			
03BC₁₆			
03BD₁₆			
03BE₁₆			
03BF₁₆			

Note 1:The blank areas are reserved and cannot be accessed by users.

X : Noting is mapped to this bit
? : Value indeterminate at reset

Figure 4.6. SFR Map (6 of 7)

Address	Register Name	Acronym	Value after Reset
03C0₁₆	A-D register 0	AD0	????????₂
03C1₁₆			XXXXXX??₂
03C2₁₆	A-D register 1	AD1	????????₂
03C3₁₆			XXXXXX??₂
03C4₁₆	A-D register 2	AD2	????????₂
03C5₁₆			XXXXXX??₂
03C6₁₆	A-D register 3	AD3	????????₂
03C7₁₆			XXXXXX??₂
03C8₁₆	A-D register 4	AD4	????????₂
03C9₁₆			XXXXXX??₂
03CA₁₆	A-D register 5	AD5	????????₂
03CB₁₆			XXXXXX??₂
03CC₁₆	A-D register 6	AD6	????????₂
03CD₁₆			XXXXXX??₂
03CE₁₆	A-D register 7	AD7	????????₂
03CF₁₆			XXXXXX??₂
03D0₁₆			
03D1₁₆			
03D2₁₆	A-D trigger control register	ADTRGCON	XXXX0000₂
03D3₁₆	A-D convert status register 0	ADSTAT0	00000X00₂
03D4₁₆	A-D control register 2	ADCON2	00₁₆
03D5₁₆			
03D6₁₆	A-D control register 0	ADCON0	00000???₂
03D7₁₆	A-D control register 1	ADCON1	00₁₆
03D8₁₆			
03D9₁₆			
03DA₁₆			
03DB₁₆			
03DC₁₆			
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 register	P0	??₁₆
03E1₁₆	Port P1 register	P1	??₁₆
03E2₁₆	Port P0 direction register	PD0	00₁₆
03E3₁₆	Port P1 direction register	PD1	00₁₆
03E4₁₆	Port P2 register	P2	??₁₆
03E5₁₆	Port P3 register	P3	??₁₆
03E6₁₆	Port P2 direction register	PD2	00₁₆
03E7₁₆	Port P3 direction register	PD3	00₁₆
03E8₁₆			
03E9₁₆			
03EA₁₆			
03EB₁₆			
03EC₁₆	Port P6 register	P6	??₁₆
03ED₁₆	Port P7 register	P7	??₁₆
03EE₁₆	Port P6 direction register	PD6	00₁₆
03EF₁₆	Port P7 direction register	PD7	00₁₆
03F0₁₆	Port P8 register	P8	??₁₆
03F1₁₆	Port P9 register	P9	???X????₂
03F2₁₆	Port P8 direction register	PD8	00₁₆
03F3₁₆	Port P9 direction register	PD9	000X0000₂
03F4₁₆	Port P10 register	P10	??₁₆
03F5₁₆			
03F6₁₆	Port P10 direction register	PD10	00₁₆
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆	Pull-up control register 0	PUR0	00₁₆
03FD₁₆	Pull-up control register 1	PUR1	00₁₆
03FE₁₆	Pull-up control register 2	PUR2	00₁₆
03FF₁₆	Port control register	PCR	00₁₆

Note 1:The blank areas are reserved and cannot be accessed by users.

X : Noting is mapped to this bit
? : Value indeterminate at reset

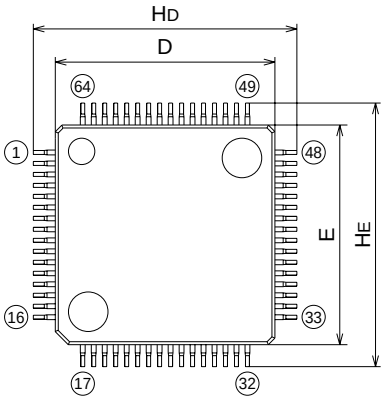
Figure 4.7. SFR Map (7 of 7)

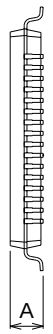
5. Package

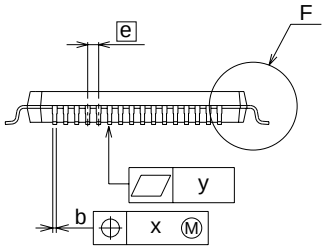
64P6Q-A (MMP)

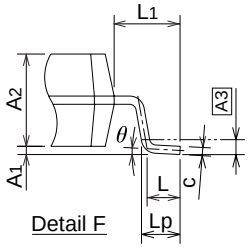
Plastic 64pin 10×10mm body LQFP

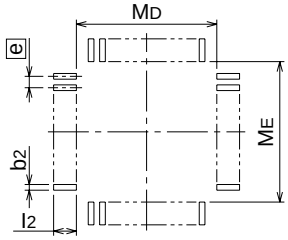
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1010-0.50	–	–	Cu Alloy











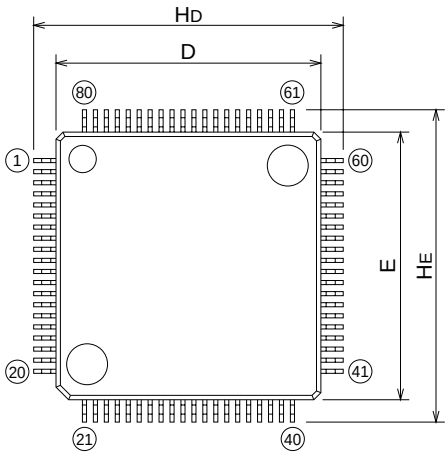
Recommended Mount Pad

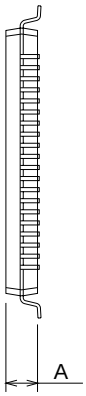
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	9.9	10.0	10.1
E	9.9	10.0	10.1
e	–	0.5	–
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	1.0	–	–
MD	–	10.4	–
ME	–	10.4	–

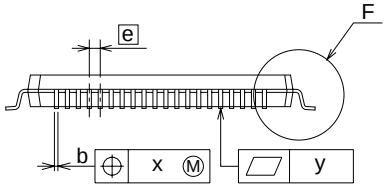
80P6Q-A (MMP)

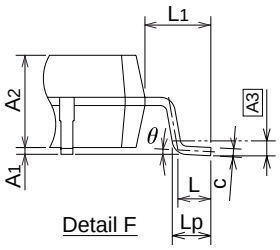
Plastic 80pin 12×12mm body LQFP

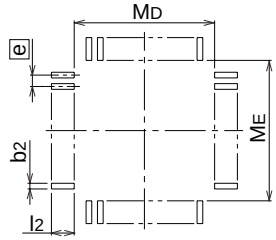
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.5	–	0.47	Cu Alloy











Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	–	0.5	–
HD	13.8	14.0	14.2
HE	13.8	14.0	14.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	12.4	–
ME	–	12.4	–

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