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1. Overview

The M32C/81 is a single-chip microcomputer that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/81 group is available in 144-pin and 100-pin plastic molded QFP/LQFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It incorporates a multiplier and DMAC adequate for office automation, communication devices and industrial equipments and other high-speed processing applications.

1.1 Applications

Audio, cameras, office equipment, communications equipment, portable equipment, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error.
Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Difference between the M32C/81 Group and the M32C/83 Group

The M32/C81 group microcomputer has less peripheral functions than the M32C/83 group miccrocomputer. The intelligent I/O group 3 and the A-D1 converter are not provided in the M32C/81 group. Interrupt requests, and as a result interrupts, DMAC, and DMACII, caused by intelligent I/O group 3 are not available in the M32C/81 group. However, the A-D1 conversion interrupt is generated in place of the A-D0 conversion interrupt when input voltage applied to $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$ pins are converted.

1.3 Performance Outline

Tables 1.1 and 1.2 list performance outlines of the M32C/81 group.

Table 1.1 M32C/81 Group Performance (144-Pin Package)

Item		Performance
CPU	Basic instructions	108 instructions
	Shortest instruction execution time	31.3 ns (f(BCLK)=32 MHz, VCC=4.2 V to 5.5 V) 50ns (f(BCLK)=20MHz, VCC=3.0 V to 5.5 V)
	Operation mode	Single-chip, memory expansion and microprocessor modes
	Address space	16 Mbytes
	Memory capacity	See Table 1.3.
Peripheral function	Port	123 I/O pins and 1 input pin
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function: 16 bits x 12 channels Waveform generating function: 16 bits x 20 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus(1))
	Serial I/O	5 channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I2C bus(2)
	CAN module	1 channel Supporting CAN 2.0B specification
	A-D converter	10-bit A-D converter: 1 circuit, 34 channels
	D-A converter	8-bit x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt factors Immediate transfer, calculation transfer and chain transfer functions
	DRAMC	$\overline{CAS}$-before-$\overline{RAS}$ refresh, self-refresh, EDO, FP
	CRC calculation circuit	CRC-CCITT
	X-Y converter	16 bits X 16 bits
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	42 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock generating circuit	4 circuits Main clock oscillation circuit(*), sub clock oscillation circuit(*), ring oscillator, PLL frequency synthesizer (*)Oscillation circuits include an internal feedback resistor and external ceramic resonator/crystal oscillator.
	Oscillator stop detect function	Main clock oscillator stop detect function
Electric characteristics	Supply voltage	4.2 V to 5.5 V (f(BCLK)=32 MHz) 3.0 V to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 V to 3.6 V (f(BCLK)=20 MHz, not through VDC)
	Power consumption	28 mA (VCC=5 V, f(BCLK)=32 MHz) 17 mA (VCC=3.3 V, f(BCLK)=20 MHz) 470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode) 340 µA (VCC=3.3 V, f(XCIN)=32 kHz, through VDC in wait mode) 5.0 µA (VCC=3.3 V, f(XCIN)=32 kHz, not through VDC in wait mode) 0.4 µA (VCC=5 V, f(XCIN)=32 kHz, in stop mode) 0.4 µA (VCC=3.3 V, f(XCIN)=32 kHz, in stop mode)
Operating ambient temperature		–20 to 85°C, –40 to 85°C (option)
Package		144-pin plastic mold QFP

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I2C bus is a trademark of Koninklijke Philips Electronics N. V.

All options are on a request basis.

Table 1.2 M32C/81 Group Performance (100-Pin Package)

Item		Performance
CPU	Basic instructions	108 instructions
	Shortest instruction execution time	31.3 ns (f(BCLK)=32 MHz, VCC=4.2 V to 5.5 V) 50ns (f(BCLK)=20MHz, VCC=3.0 V to 5.5 V)
	Operation mode	Single-chip, memory expansion and microprocessor modes
	Address space	16 Mbytes
	Memory capacity	See Table 1.3.
Peripheral function	Port	87 I/O pins and 1 input pin
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function: 16 bits x 5 channels Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus(1))
	Serial I/O	5 channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I2C bus(2)
	CAN module	1 channel Supporting CAN 2.0B specification
	A-D converter	10-bit A-D converter: 1 circuit, 26 channels
	D-A converter	8-bit x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt factors Immediate transfer, calculation transfer and chain transfer functions
	DRAMC	$\overline{CAS}$-before-$\overline{RAS}$ refresh, self-refresh, EDO, FP
	CRC calculation circuit	CRC-CCITT
	X-Y converter	16 bits X 16 bits
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	42 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock generating circuit	4 circuits Main clock oscillation circuit(*), sub clock oscillation circuit(*), ring oscillator, PLL frequency synthesizer (*)Oscillation circuits include an internal feedback resistor and external ceramic resonator/crystal oscillator.
	Oscillator stop detect function	Main clock oscillator stop detect function
Electric charact-eristics	Supply voltage	4.2 V to 5.5 V (f(XIN)=32 MHz) 3.0 V to 5.5 V (f(XIN)=20 MHz, through VDC) 3.0 V to 3.6 V (f(XIN)=20 MHz, not through VDC)
	Power consumption	28 mA (VCC=5 V, f(BCLK)=32 MHz) 17 mA (VCC=3.3 V, f(BCLK)=20 MHz) 470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode) 340 µA (VCC=3.3 V, f(XCIN)=32 kHz, through VDC in wait mode) 5.0 µA (VCC=3.3 V, f(XCIN)=32 kHz, not through VDC in wait mode) 0.4 µA (VCC=5 V, f(XCIN)=32 kHz, in stop mode) 0.4 µA (VCC=3.3 V, f(XCIN)=32 kHz, in stop mode)
Operating ambient temperature		–20 to 85°C, –40 to 85°C (option)
Package		100-pin plastic mold QFP

NOTES:
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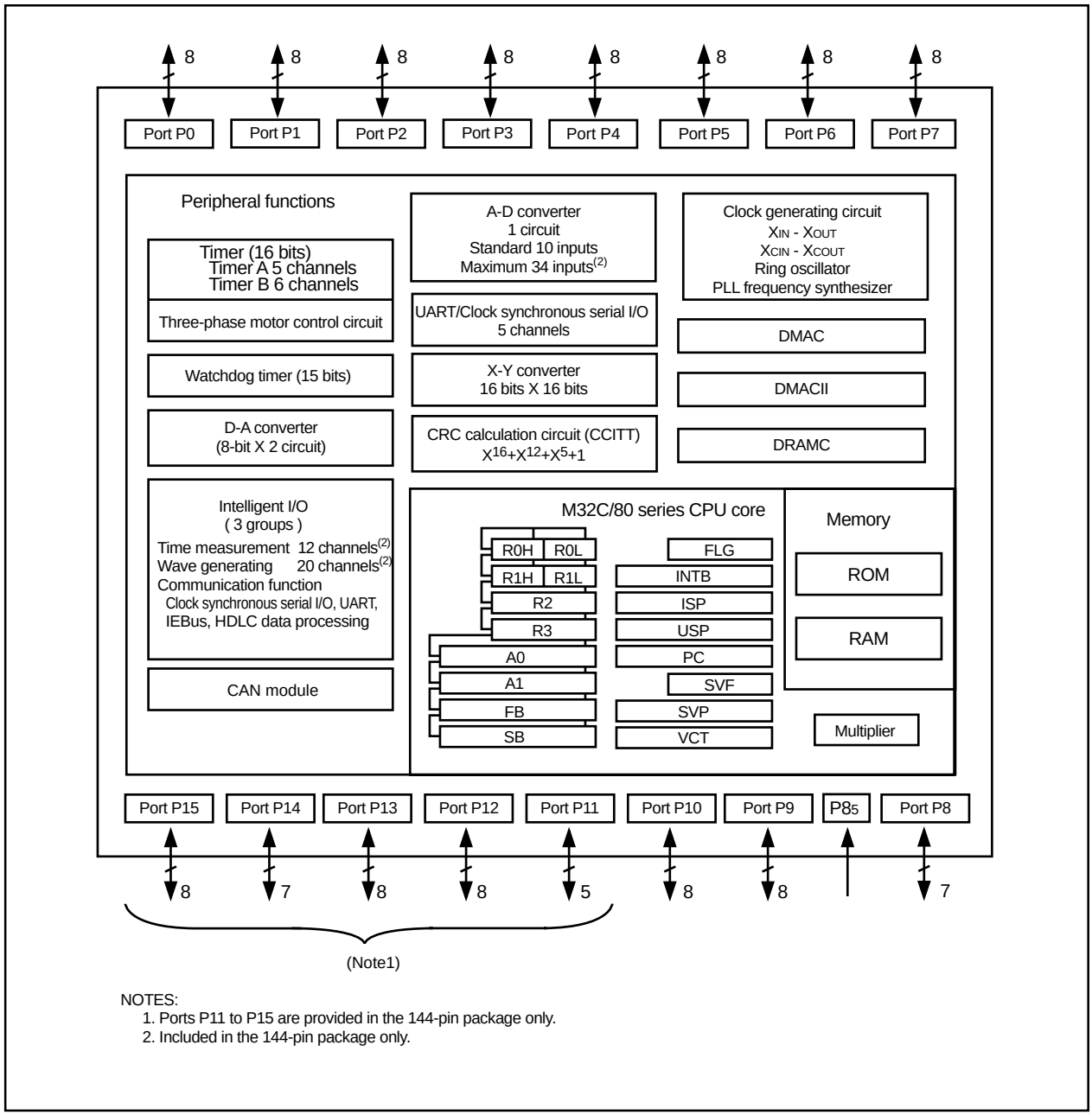
2. I2C bus is a trademark of Koninklijke Philips Electronics N. V.

All options are on a request basis.

1.4 Block Diagram

Figure 1.1 shows a block diagram of the M32C/81 group microcomputer.

The M32C/81 group microcomputer contains ROM and RAM as memory to store instructions and data, CPU to execute calculations and peripheral functions such as interrupt, timer, serial I/O, DMAC, CRC calculation circuit, A-D converter, D-A converter, DRAMC, intelligent I/O and ports.



NOTES:
1. Ports P11 to P15 are provided in the 144-pin package only.
2. Included in the 144-pin package only.

Figure 1.1 M32C/81 Group Block Diagram

1.5 Product Information

Renesas plans to release the following products in the M32C/81 group:

(1) Support for the masked ROM version

(2) ROM/RAM capacity

(3) Package

100P6S-A : Plastic molded QFP

100P6Q-A : Plastic molded QFP

144P6Q-A : Plastic molded QFP

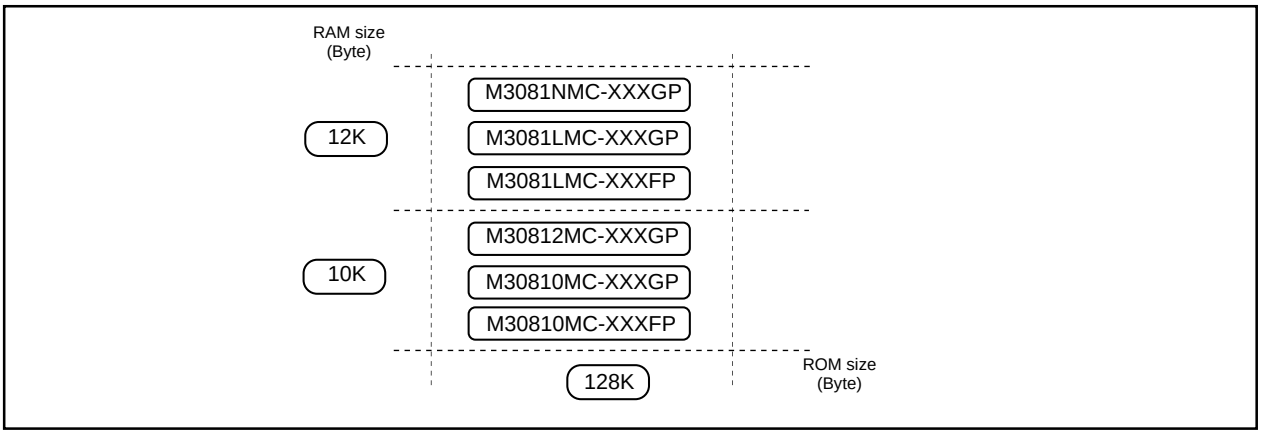


Figure 1.2 ROM/RAM Capacity

Table 1.3 M32C/81 Group **As of September, 2003**

Type number	ROM capacity	RAM capacity	Package type	Remarks
M30810MC-XXXFP (D)	128 Kbytes	10 Kbytes	100P6S-A	Masked ROM
M30810MC-XXXGP (D)			100P6Q-A	
M30812MC-XXXGP (D)			144P6Q-A	
M3081LMC-XXXFP (D)		12 Kbytes	100P6S-A	
M3081LMC-XXXGP (D)			100P6Q-A	
M3081NMC-XXXGP (D)			144P6Q-A	

(D): Under development

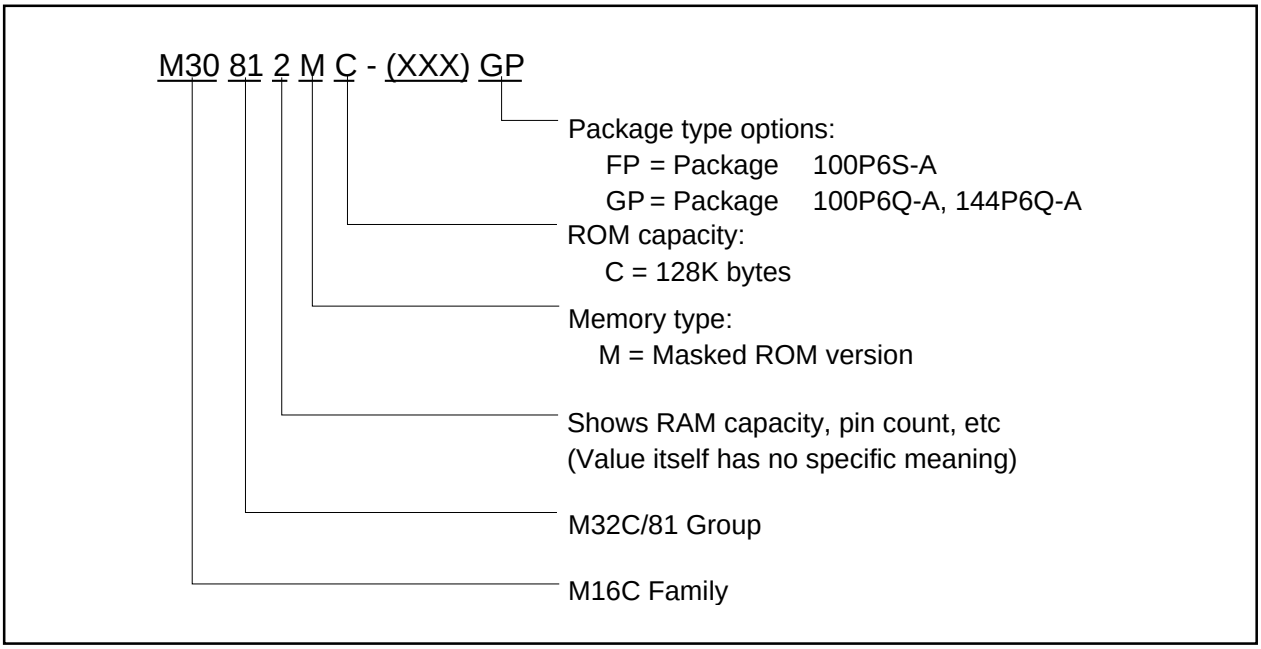


Figure 1.3 Product Numbering System

1.6 Pin Assignments

Figures 1.4 to 1.6 show pin assignments (top view).

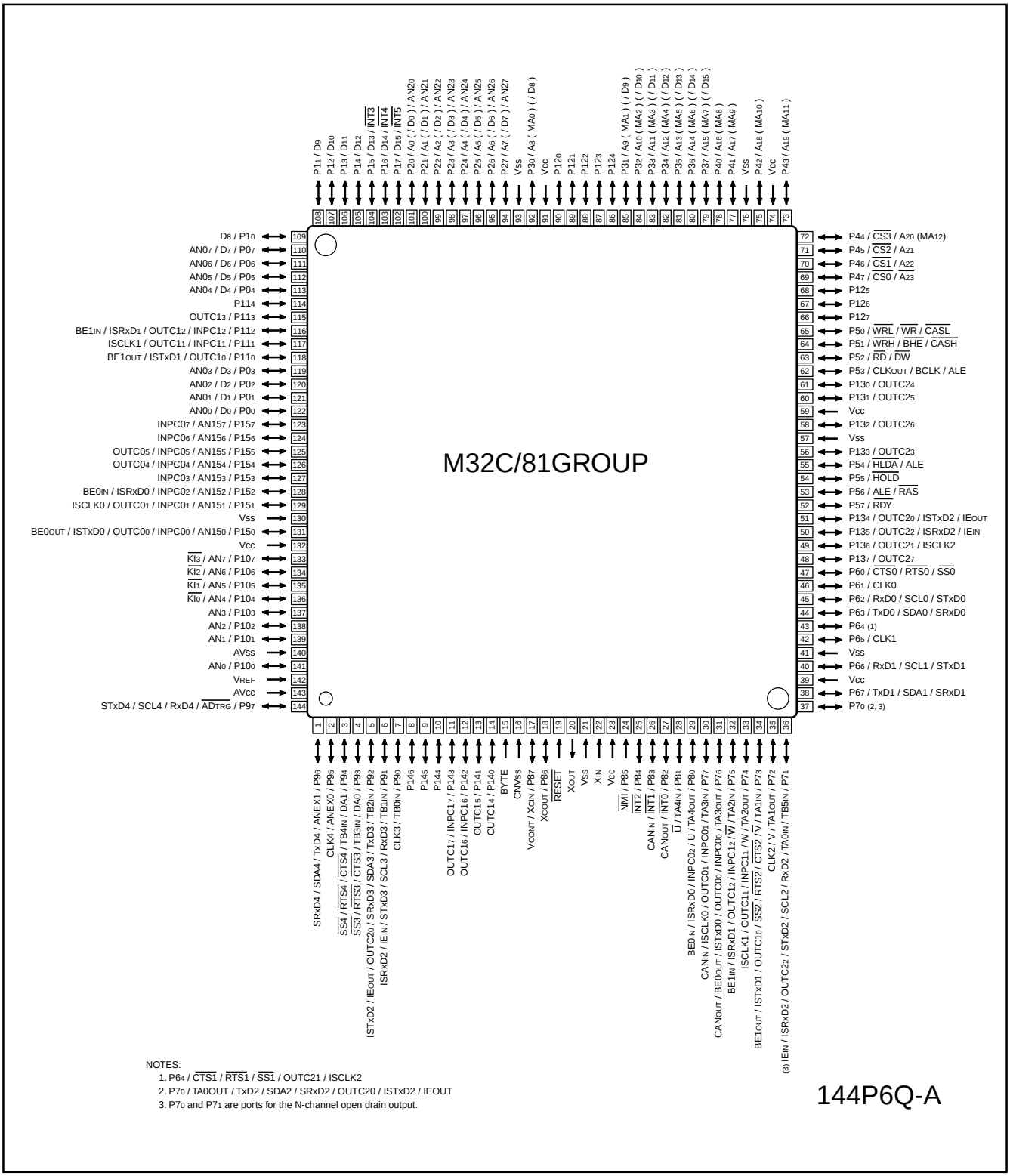


Figure 1.4 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
1		$P9_6$			TxD4/SDA4/SRxD4		ANEX1	
2		$P9_5$			CLK4		ANEX0	
3		$P9_4$		$TB4_{IN}$	$\overline{CTS4}/\overline{RTS4}/\overline{SS4}$		DA1	
4		$P9_3$		$TB3_{IN}$	$\overline{CTS3}/\overline{RTS3}/\overline{SS3}$		DA0	
5		$P9_2$		$TB2_{IN}$	TxD3/SDA3/SRxD3	$OUTC2_0/IE_{OUT}$/ISTxD2		
6		$P9_1$		$TB1_{IN}$	RxD3/SCL3/STxD3	IE_{IN}/ISRxD2		
7		$P9_0$		$TB0_{IN}$	CLK3			
8		$P14_6$						
9		$P14_5$						
10		$P14_4$						
11		$P14_3$				$INPC1_7/OUTC1_7$		
12		$P14_2$				$INPC1_6/OUTC1_6$		
13		$P14_1$				$OUTC1_5$		
14		$P14_0$				$OUTC1_4$		
15	BYTE							
16	CNV_{SS}							
17	X_{CIN}/V_{CONT}	$P8_7$						
18	X_{COUT}	$P8_6$						
19	$\overline{RESET}$							
20	X_{OUT}							
21	V_{SS}							
22	X_{IN}							
23	V_{CC}							
24		$P8_5$	$\overline{NMI}$					
25		$P8_4$	$\overline{INT2}$					
26		$P8_3$	$\overline{INT1}$		CAN_{IN}			
27		$P8_2$	$\overline{INT0}$		CAN_{OUT}			
28		$P8_1$		$TA4_{IN}/\overline{U}$				
29		$P8_0$		$TA4_{OUT}/U$		$INPC0_2/ISRxD0/BE0_{IN}$		
30		$P7_7$		$TA3_{IN}$	CAN_{IN}	$INPC0_1/OUTC0_1$/ISCLK0		
31		$P7_6$		$TA3_{OUT}$	CAN_{OUT}	$INPC0_0/OUTC0_0$/ISTxD0/$BE0_{OUT}$		
32		$P7_5$		$TA2_{IN}/\overline{W}$		$INPC1_2/OUTC1_2$/ISRxD1/$BE1_{IN}$		
33		$P7_4$		$TA2_{OUT}$/W		$INPC1_1/OUTC1_1$/ISCLK1		
34		$P7_3$		$TA1_{IN}/\overline{V}$	$\overline{CTS2}/\overline{RTS2}/\overline{SS2}$	$OUTC1_0$/ISTxD1/$BE1_{OUT}$		
35		$P7_2$		$TA1_{OUT}/V$	CLK2			
36		$P7_1$		$TB5_{IN}/TA0_{IN}$	RxD2/SCL2/STxD2	$OUTC2_2$/ISRxD2/IE_{IN}		
37		$P7_0$		$TA0_{OUT}$	TxD2/SDA2/SRxD2	$OUTC2_0$/ISTxD2/IE_{OUT}		
38		$P6_7$			TxD1/SDA1/SRxD1			
39	V_{CC}							
40		$P6_6$			RxD1/SCL1/STxD1			
41	V_{SS}							
42		$P6_5$			CLK1			
43		$P6_4$			$\overline{CTS1}/\overline{RTS1}/\overline{SS1}$	$OUTC2_1$/ISCLK2		
44		$P6_3$			TxD0/SDA0/SRxD0			
45		$P6_2$			RxD0/SCL0/STxD0			
46		$P6_1$			CLK0			
47		$P6_0$			$\overline{CTS0}/\overline{RTS0}/\overline{SS0}$			
48		$P13_7$				$OUTC2_7$		

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
49		$P13_6$				$OUTC2_1$/ISCLK2		
50		$P13_5$				$OUTC2_2$/ISRxD2/IE_{IN}		
51		$P13_4$				$OUTC2_0$/ISTxD2/IE_{OUT}		
52		$P5_7$						$\overline{RDY}$
53		$P5_6$						ALE/$\overline{RAS}$
54		$P5_5$						$\overline{HOLD}$
55		$P5_4$						$\overline{HLDA}$/ALE
56		$P13_3$				$OUTC2_3$		
57	V_{SS}							
58		$P13_2$				$OUTC2_6$		
59	V_{CC}							
60		$P13_1$				$OUTC2_5$		
61		$P13_0$				$OUTC2_4$		
62		$P5_3$						CLK_{OUT}/BCLK/ALE
63		$P5_2$						$\overline{RD}$/$\overline{DW}$
64		$P5_1$						$\overline{WRH}$/$\overline{BHE}$/$\overline{CASH}$
65		$P5_0$						$\overline{WRL}$/$\overline{WR}$/$\overline{CASL}$
66		$P12_7$						
67		$P12_6$						
68		$P12_5$						
69		$P4_7$						$\overline{CS0}$/A_{23}
70		$P4_6$						$\overline{CS1}$/A_{22}
71		$P4_5$						$\overline{CS2}$/A_{21}
72		$P4_4$						$\overline{CS3}$/A_{20}(MA_{12})
73		$P4_3$						A_{19}(MA_{11})
74	V_{CC}							
75		$P4_2$						A_{18}(MA_{10})
76	V_{SS}							
77		$P4_1$						A_{17}(MA_9)
78		$P4_0$						A_{16}(MA_8)
79		$P3_7$						A_{15}(MA_7)(/D_{15})
80		$P3_6$						A_{14}(MA_6)(/D_{14})
81		$P3_5$						A_{13}(MA_5)(/D_{13})
82		$P3_4$						A_{12}(MA_4)(/D_{12})
83		$P3_3$						A_{11}(MA_3)(/D_{11})
84		$P3_2$						A_{10}(MA_2)(/D_{10})
85		$P3_1$						A_9(MA_1)(/D_9)
86		$P12_4$						
87		$P12_3$						
88		$P12_2$						
89		$P12_1$						
90		$P12_0$						
91	V_{CC}							
92		$P3_0$						A_8(MA_0)(/D_8)
93	V_{SS}							
94		$P2_7$					$AN2_7$	A_7(/D_7)
95		$P2_6$					$AN2_6$	A_6(/D_6)
96		$P2_5$					$AN2_5$	A_5(/D_5)

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
97		$P2_4$					$AN2_4$	A_4(/D_4)
98		$P2_3$					$AN2_3$	A_3(/D_3)
99		$P2_2$					$AN2_2$	A_2(/D_2)
100		$P2_1$					$AN2_1$	A_1(/D_1)
101		$P2_0$					$AN2_0$	A_0(/D_0)
102		$P1_7$	$\overline{INT5}$					D_{15}
103		$P1_6$	$\overline{INT4}$					D_{14}
104		$P1_5$	$\overline{INT3}$					D_{13}
105		$P1_4$						D_{12}
106		$P1_3$						D_{11}
107		$P1_2$						D_{10}
108		$P1_1$						D_9
109		$P1_0$						D_8
110		$P0_7$					$AN0_7$	D_7
111		$P0_6$					$AN0_6$	D_6
112		$P0_5$					$AN0_5$	D_5
113		$P0_4$					$AN0_4$	D_4
114		$P11_4$						
115		$P11_3$				$OUTC1_3$		
116		$P11_2$				$INPC1_2$/$OUTC1_2$/ISRxD1/$BE1_{IN}$		
117		$P11_1$				$INPC1_1$/$OUTC1_1$/ISCLK1		
118		$P11_0$				$OUTC1_0$/ISTxD1/$BE1_{OUT}$		
119		$P0_3$					$AN0_3$	D_3
120		$P0_2$					$AN0_2$	D_2
121		$P0_1$					$AN0_1$	D_1
122		$P0_0$					$AN0_0$	D_0
123		$P15_7$				$INPC0_7$	$AN15_7$	
124		$P15_6$				$INPC0_6$	$AN15_6$	
125		$P15_5$				$INPC0_5$/$OUTC0_5$	$AN15_5$	
126		$P15_4$				$INPC0_4$/$OUTC0_4$	$AN15_4$	
127		$P15_3$				$INPC0_3$	$AN15_3$	
128		$P15_2$				$INPC0_2$/ISRxD0/$BE0_{IN}$	$AN15_2$	
129		$P15_1$				$INPC0_1$/$OUTC0_1$/ISCLK0	$AN15_1$	
130	V_{SS}							
131		$P15_0$				$INPC0_0$/$OUTC0_0$/ISTxD0/$BE0_{OUT}$	$AN15_0$	
132	V_{CC}							
133		$P10_7$	$\overline{KI_3}$				AN_7	
134		$P10_6$	$\overline{KI_2}$				AN_6	
135		$P10_5$	$\overline{KI_1}$				AN_5	
136		$P10_4$	$\overline{KI_0}$				AN_4	
137		$P10_3$					AN_3	
138		$P10_2$					AN_2	
139		$P10_1$					AN_1	
140	AV_{SS}							
141		$P10_0$					AN_0	
142	V_{REF}							
143	AV_{CC}							
144		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

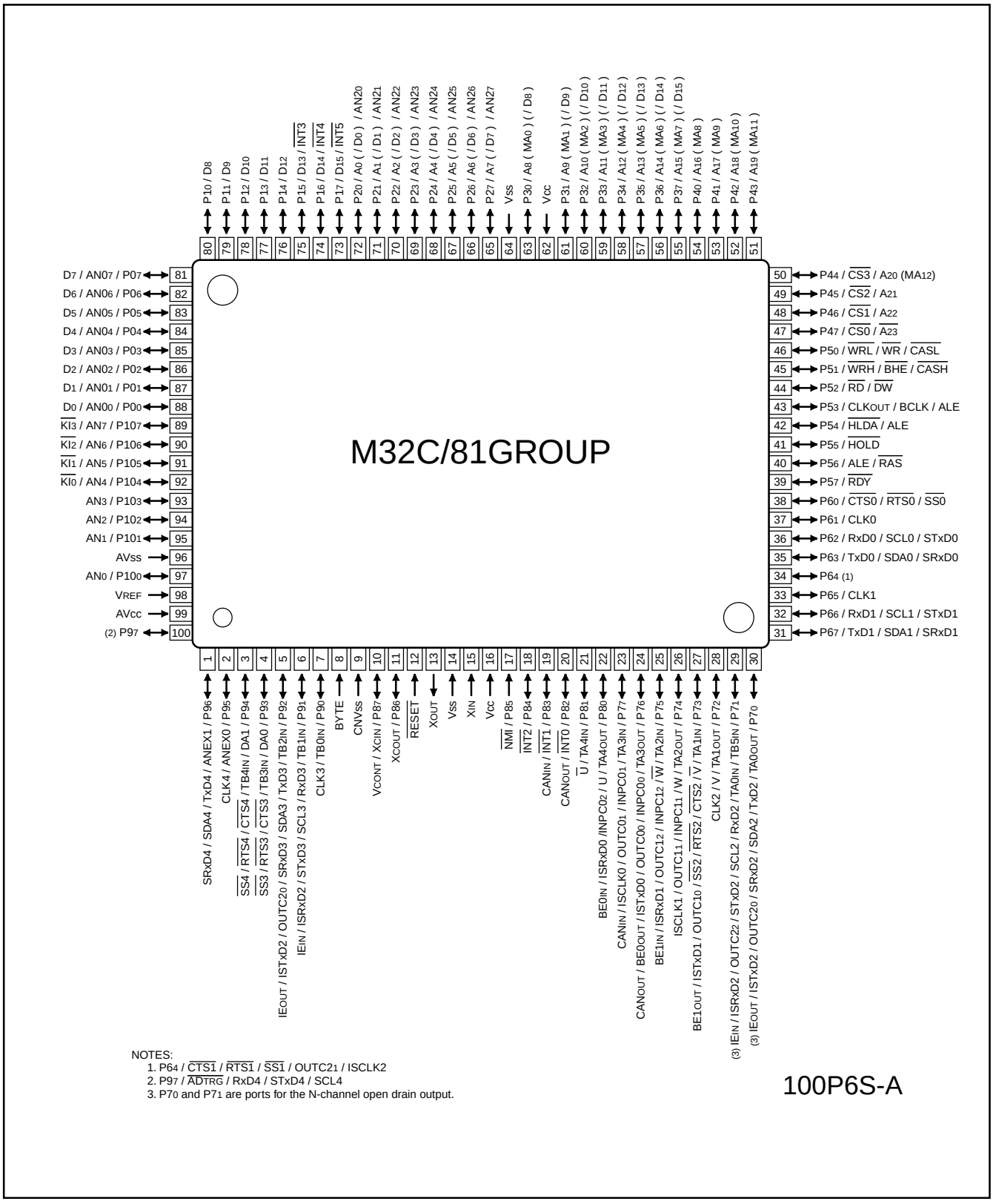


Figure 1.5 Pin assignment for 100-Pin Package

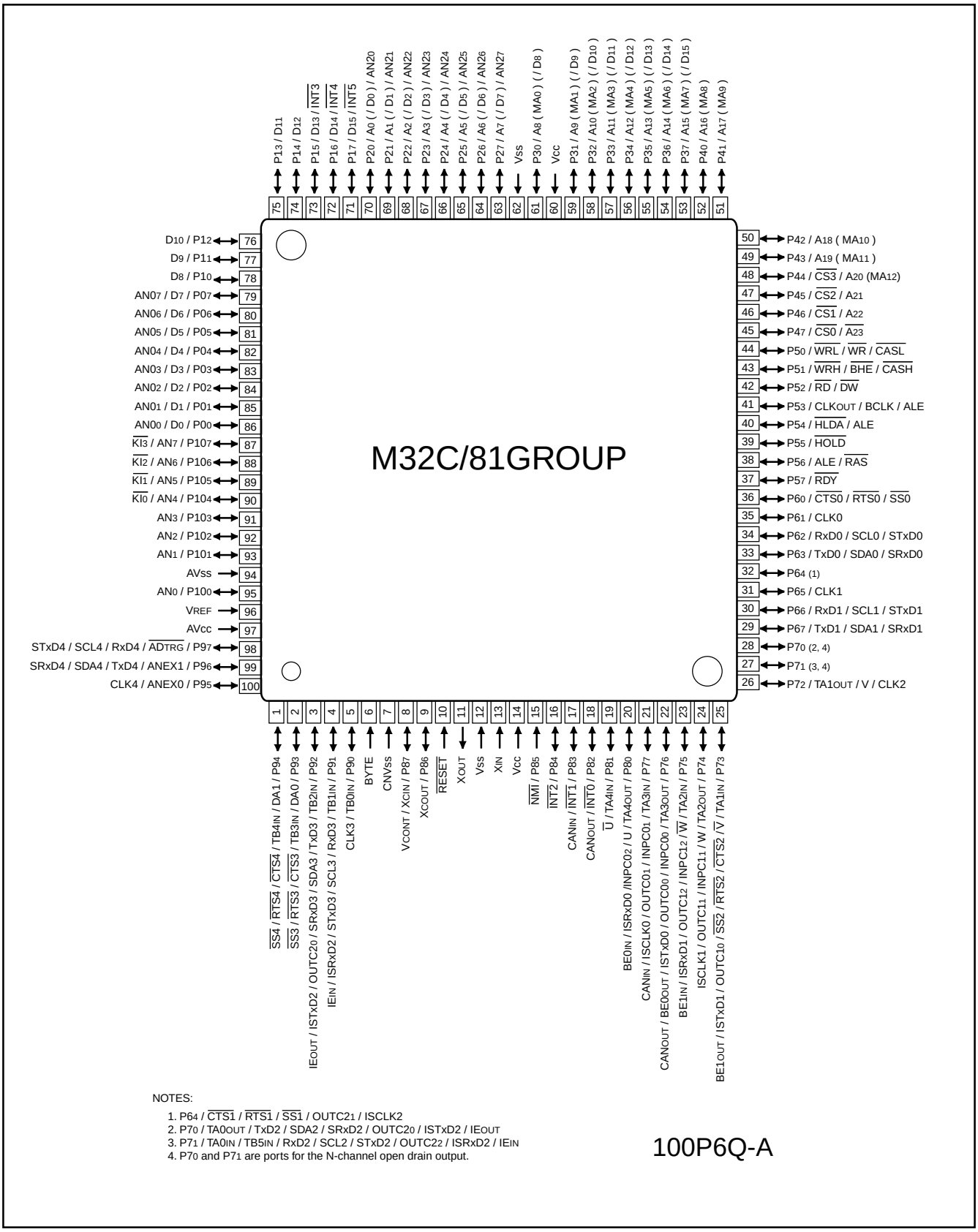


Figure 1.6 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No		Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
FP	GP								
1	99		P9$_6$			TxD4/SDA4/SRxD4		ANEX1	
2	100		P9$_5$			CLK4		ANEX0	
3	1		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1	
4	2		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0	
5	3		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3	OUTC2$_0$/IE$_{OUT}$/ISTxD2		
6	4		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3	IE$_{IN}$/ISRxD2		
7	5		P9$_0$		TB0$_{IN}$	CLK3			
8	6	BYTE							
9	7	CNV$_{SS}$							
10	8	X$_{CIN}$/V$_{CONT}$	P8$_7$						
11	9	X$_{COUT}$	P8$_6$						
12	10	$\overline{RESET}$							
13	11	X$_{OUT}$							
14	12	V$_{SS}$							
15	13	X$_{IN}$							
16	14	V$_{CC}$							
17	15		P8$_5$	$\overline{NMI}$					
18	16		P8$_4$	$\overline{INT2}$					
19	17		P8$_3$	$\overline{INT1}$		CAN$_{IN}$			
20	18		P8$_2$	$\overline{INT0}$		CAN$_{OUT}$			
21	19		P8$_1$		TA4$_{IN}$/$\overline{U}$				
22	20		P8$_0$		TA4$_{OUT}$/U		INPC0$_2$/ISRxD0/BE0$_{IN}$		
23	21		P7$_7$		TA3$_{IN}$	CAN$_{IN}$	INPC0$_1$/OUTC0$_1$/ISCLK0		
24	22		P7$_6$		TA3$_{OUT}$	CAN$_{OUT}$	INPC0$_0$/OUTC0$_0$/ISTxD0/BE0$_{OUT}$		
25	23		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$		
26	24		P7$_4$		TA2$_{OUT}$/W		INPC1$_1$/OUTC1$_1$/ISCLK1		
27	25		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	OUTC1$_0$/ISTxD1/BE1$_{OUT}$		
28	26		P7$_2$		TA1$_{OUT}$/V	CLK2			
29	27		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	OUTC2$_2$/ISRxD2/IE$_{IN}$		
30	28		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	OUTC2$_0$/ISTxD2/IE$_{OUT}$		
31	29		P6$_7$			TxD1/SDA1/SRxD1			
32	30		P6$_6$			RxD1/SCL1/STxD1			
33	31		P6$_5$			CLK1			
34	32		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$	OUTC2$_1$/ISCLK2		
35	33		P6$_3$			TxD0/SDA0/SRxD0			
36	34		P6$_2$			RxD0/SCL0/STxD0			
37	35		P6$_1$			CLK0			
38	36		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
39	37		P5$_7$						$\overline{RDY}$
40	38		P5$_6$						ALE/$\overline{RAS}$
41	39		P5$_5$						$\overline{HOLD}$
42	40		P5$_4$						$\overline{HLDA}$/ALE
43	41		P5$_3$						CLK$_{OUT}$/BCLK/ALE
44	42		P5$_2$						$\overline{RD}$/$\overline{DW}$
45	43		P5$_1$						$\overline{WRH}$/$\overline{BHE}$/$\overline{CASH}$
46	44		P5$_0$						$\overline{WRL}$/$\overline{WR}$/$\overline{CASL}$
47	45		P4$_7$						$\overline{CS0}$/A$_{23}$
48	46		P4$_6$						$\overline{CS1}$/A$_{22}$
49	47		P4$_5$						$\overline{CS2}$/A$_{21}$
50	48		P4$_4$						$\overline{CS3}$/A$_{20}$(MA$_{12}$)

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package pin No		Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
FP	GP								
51	49		$P4_3$						$A_{19}(MA_{11})$
52	50		$P4_2$						$A_{18}(MA_{10})$
53	51		$P4_1$						$A_{17}(MA_9)$
54	52		$P4_0$						$A_{16}(MA_8)$
55	53		$P3_7$						$A_{15}(MA_7)(/D_{15})$
56	54		$P3_6$						$A_{14}(MA_6)(/D_{14})$
57	55		$P3_5$						$A_{13}(MA_5)(/D_{13})$
58	56		$P3_4$						$A_{12}(MA_4)(/D_{12})$
59	57		$P3_3$						$A_{11}(MA_3)(/D_{11})$
60	58		$P3_2$						$A_{10}(MA_2)(/D_{10})$
61	59		$P3_1$						$A_9(MA_1)(/D_9)$
62	60	V_{CC}							
63	61		$P3_0$						$A_8(MA_0)(/D_8)$
64	62	V_{SS}							
65	63		$P2_7$					$AN2_7$	$A_7(/D_7)$
66	64		$P2_6$					$AN2_6$	$A_6(/D_6)$
67	65		$P2_5$					$AN2_5$	$A_5(/D_5)$
68	66		$P2_4$					$AN2_4$	$A_4(/D_4)$
69	67		$P2_3$					$AN2_3$	$A_3(/D_3)$
70	68		$P2_2$					$AN2_2$	$A_2(/D_2)$
71	69		$P2_1$					$AN2_1$	$A_1(/D_1)$
72	70		$P2_0$					$AN2_0$	$A_0(/D_0)$
73	71		$P1_7$	$\overline{INT5}$					D_{15}
74	72		$P1_6$	$\overline{INT4}$					D_{14}
75	73		$P1_5$	$\overline{INT3}$					D_{13}
76	74		$P1_4$						D_{12}
77	75		$P1_3$						D_{11}
78	76		$P1_2$						D_{10}
79	77		$P1_1$						D_9
80	78		$P1_0$						D_8
81	79		$P0_7$					$AN0_7$	D_7
82	80		$P0_6$					$AN0_6$	D_6
83	81		$P0_5$					$AN0_5$	D_5
84	82		$P0_4$					$AN0_4$	D_4
85	83		$P0_3$					$AN0_3$	D_3
86	84		$P0_2$					$AN0_2$	D_2
87	85		$P0_1$					$AN0_1$	D_1
88	86		$P0_0$					$AN0_0$	D_0
89	87		$P10_7$	$\overline{KI_3}$				AN_7	
90	88		$P10_6$	$\overline{KI_2}$				AN_6	
91	89		$P10_5$	$\overline{KI_1}$				AN_5	
92	90		$P10_4$	$\overline{KI_0}$				AN_4	
93	91		$P10_3$					AN_3	
94	92		$P10_2$					AN_2	
95	93		$P10_1$					AN_1	
96	94	AV_{SS}							
97	95		$P10_0$					AN_0	
98	96	V_{REF}							
99	97	AV_{CC}							
100	98		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

1.7 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Symbol	Function	I/O type	Description
V_{CC} V_{SS}	Power supply input	I I	Apply 3.0 to 5.5 V to the V_{CC} pins. Apply 0 V to the V_{SS} pin.
CNV$_{SS}$	CNV$_{SS}$	I	Switches processor mode. Connect this pin to V_{SS} to start up in single-chip mode (memory expansion mode). Connect this pin to V_{CC} to start up in microprocessor mode.
$\overline{RESET}$	Reset input	I	The microcomputer is in a reset state when applying "L" to the $\overline{RESET}$ pin.
X_{IN} X_{OUT}	Clock input Clock output	I O	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between X_{IN} and X_{OUT}. To use an external clock, input the clock to X_{IN} and leave X_{OUT} open.
BYTE	Input to switch external data bus width	I	Switches the data bus in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when the BYTE pin is held "H". Set to either. Connect this pin to V_{SS} when an external bus is not used.
AV$_{CC}$	Analog power supply input	I	Applies power supply for the A-D converter and D-A converter. Connect this pin to V_{CC}.
AV$_{SS}$	Analog power supply input	I	Applies power supply for the A-D converter and D-A converter. Connect this pin to V_{SS}.
V_{REF}	Reference voltage input	I	Applies reference voltage for the A-D converter.
P0$_0$ to P0$_7$	I/O port P0	I/O	8-bit I/O ports in CMOS having a direction register to select input or output. Each pin is set as an input port or output port. An input port in single-chip mode can be set for a pull-up or for no pull-up in 4-bit unit by program. When these pins are used as bus control pins in memory expansion mode and microprocessor mode, internal pull-up resistor cannot be selected. Ports used as input ports can be set for a pull-up or for no pull-up in the modes above.
D$_0$ to D$_7$	Data bus	I/O	Inputs and outputs data (D$_0$ to D$_7$) when these pins are set as the separate bus.
AN0$_0$ to AN0$_7$	Analog input pin	I	Analog input pins for the A-D converter
P1$_0$ to P1$_7$	I/O port P1	I/O	8-bit I/O ports having equivalent functions to P0
$\overline{INT}_3$ to $\overline{INT}_5$	$\overline{INT}$ interrupt input pin	I	Input pins for the $\overline{INT}$ interrupt
D$_8$ to D$_{15}$	Data bus	I/O	Inputs and outputs data (D$_8$ to D$_{15}$) when these pins are set as the separate bus.
P2$_0$ to P2$_7$	I/O port P2	I/O	8-bit I/O ports having equivalent functions to P0
A$_0$ to A$_7$	Address bus	O	Outputs 8 low-order address bits (A$_0$ to A$_7$).
A$_0$/D$_0$ to A$_7$/D$_7$	Address bus/data bus	I/O	Inputs and outputs data (D$_0$ to D$_7$) and outputs 8 low-order address bits (A$_0$ to A$_7$) by time-sharing when these pins are set as the multiplexed bus.
AN2$_0$ to AN2$_7$	Analog input pin	I	Analog input pins for A-D converter
P3$_0$ to P3$_7$	I/O port P3	I/O	8-bit I/O ports having equivalent functions to P0
A$_8$ to A$_{15}$	Address bus	O	Outputs 8 middle-order address bits (A$_8$ to A$_{15}$).
A$_8$/D$_8$ to A$_{15}$/D$_{15}$	Address bus/data bus	I/O	Inputs and outputs data (D$_8$ to D$_{15}$) and outputs 8 middle-order address bits (A$_8$ to A$_{15}$) by time-sharing when external 16-bit data bus is set as the multi-plexed bus.
MA$_0$ to MA$_7$	Address bus	O	Outputs row addresses and column addresses by time-sharing when accessing the DRAM area.

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
P4$_0$ to P4$_7$	I/O port P4	I/O	8-bit I/O ports having equivalent functions to P0
A$_{16}$ to A$_{22}$, $\overline{A_{23}}$	Address bus	O	Outputs 8 high-order address bits (A$_{16}$ to A$_{22}$, $\overline{A_{23}}$). The highest-order bit ($\overline{A_{23}}$) inversed is also output.
$\overline{CS_0}$ to $\overline{CS_3}$	Chip-select	O	Outputs $\overline{CS_0}$ to $\overline{CS_3}$ signals. $\overline{CS_0}$ to $\overline{CS_3}$ are chip-select signals specifying an external space.
MA$_8$ to MA$_{12}$	Address bus	O	Outputs row addresses and column addresses by time-sharing when accessing the DRAM area.
P5$_0$ to P5$_7$	I/O port P5	I/O	8-bit I/O ports having equivalent functions to P0
CLK$_{OUT}$	Clock output	O	Outputs the main clock divided by 8 or divided by 32 or the clock having the same frequency as the sub clock from P5$_3$.
$\overline{WRL}$ $\overline{WR}$ $\overline{WRH}$ $\overline{BHE}$ $\overline{RD}$ BCLK $\overline{HLDA}$ $\overline{HOLD}$ ALE $\overline{RDY}$	Bus control pin	O O O O O O O I O I	Outputs $\overline{WRL}$, $\overline{WRH}$, ($\overline{WR}$, $\overline{BHE}$), $\overline{RD}$, BCLK, $\overline{HLDA}$ and ALE signals. $\overline{WRL}$ and $\overline{WRH}$ or $\overline{BHE}$ and $\overline{WR}$ can be switched by program. ■ $\overline{WRL}$, $\overline{WRH}$ and $\overline{RD}$ are selected The $\overline{WRL}$ signal becomes "L" by writing data to an even address in an external memory space. The $\overline{WRH}$ signal becomes "L" by writing data to an odd address in an external memory space. The $\overline{RD}$ pin signal becomes "L" by reading data in an external memory space. ■ $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ are selected The $\overline{WR}$ signal becomes "L" by writing data to an external memory space. The $\overline{RD}$ signal becomes "L" by reading data in an external memory space. The $\overline{BHE}$ signal becomes "L" by accessing an odd address. Select $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ for an external 8-bit data bus. While the $\overline{HOLD}$ pin is held "L", the microcomputer is placed in a hold state. In a hold state, $\overline{HLDA}$ outputs a "L" signal. ALE is a signal latching the address. While the $\overline{RDY}$ pin is held "L", the microcomputer is placed in a wait state.
$\overline{DW}$ $\overline{CASL}$ $\overline{CASH}$ $\overline{RAS}$	DRAM bus control pin	O O O O	The $\overline{DW}$ signal becomes "L" by writing data to the DRAM area. $\overline{CASL}$ and $\overline{CASH}$ are signals indicating a timing to latch column addresses. The $\overline{CASL}$ signal becomes "L" by accessing an even address. The $\overline{CASH}$ signal becomes "L" by accessing an odd address. $\overline{RAS}$ is a signal latching row addresses.
P6$_0$ to P6$_7$	I/O port P6	I/O	8-bit I/O ports having equivalent functions to P0
$\overline{CTS0}$, $\overline{CTS1}$ $\overline{RTS0}$, $\overline{RTS1}$ $\overline{SS0}$, $\overline{SS1}$ CLK0, CLK1 RxD0, RxD1 SCL0, SCL1 STxD0, STxD1 TxD0, TxD1 SDA0, SDA1 SRxD0, SRxD1	UART pin	I O I I/O I I/O O O I/O I	I/O pins for UART0 (P6$_0$ to P6$_3$) and UART1 (P6$_4$ to P6$_7$)
ISCLK2 OUTC2$_1$	Intelligent I/O pin	I/O O	ISCKL2 inputs and outputs the clock for the intelligent I/O communication function. OUTC2$_1$ outputs the clock for the waveform generating function.

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
$P7_0$ to $P7_7$	I/O port P7	I/O	8-bit I/O ports having equivalent functions to P0 ($P7_0$ and $P7_1$ are ports for the N-channel open drain output.)
$TA0_{OUT}$ to $TA3_{OUT}$	Timer A pin	I/O	I/O pins for timers A0 to A3
$TA0_{IN}$ to $TA3_{IN}$		I	
$TB5_{IN}$	Timer B pin	I	Input pin for timer B5
V, $\overline{V}$	Three-phase motor	O	V-phase output pin
W, $\overline{W}$	control output pin	O	W-phase output pin
$\overline{CTS2}$	UART pin	I	I/O pins for UART2
$\overline{RTS2}$		O	
$\overline{SS2}$		I	
CLK2		I/O	
RxD2		I	
SCL2		I/O	
STxD2		O	
TxD2		O	
SDA2		I/O	
SRxD2		I	
$INPC0_0$, $INPC0_1$	Intelligent I/O pin	I	$INPC0_0$, $INPC0_1$, $INPC1_1$ and $INPC1_2$ are input pins for the time measurement function.
$INPC1_1$, $INPC1_2$			
$OUTC0_0$, $OUTC0_1$		O	$OUTC0_0$, $OUTC0_1$, $OUTC1_0$ to $OUTC1_2$, $OUTC2_0$ and $OUTC2_2$ are output pins for the waveform generating function.
$OUTC1_0$ to $OUTC1_2$			
$OUTC2_0$, $OUTC2_2$			ISCLK0 and ISCLK1 input and output the clock for the intelligent I/O communication function.
ISCLK0, ISCLK1		I/O	
ISTxD0 to ISTxD2		O	ISRxD1, ISRxD2, IE_{IN} and $BE1_{IN}$ input received data for the intelligent I/O communication function.
ISRxD1, ISRxD2		I	
IE_{OUT}		O	ISTxD0 to ISTxD2, IE_{OUT}, $BE0_{OUT}$, and $BE1_{OUT}$ output transmit data for the intelligent I/O communication function.
IE_{IN}		I	
$BE0_{OUT}$		O	
$BE1_{OUT}$		O	
$BE1_{IN}$		I	
$CAN0_{OUT}$	CAN pin	O	I/O pins for the CAN communication function
$CAN0_{IN}$		I	

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
P80 to P84, P86, P87	I/O port P8	I/O	I/O ports having equivalent functions to P0
XCIN	Sub clock	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT.
XCOUT		O	
VCONT	Low-pass filter connect pin for PLL frequency synthesizer pin		Connects the low-pass filter to the VCONT pin when using the PLL frequency synthesizer. Connect P86 to VSS to stabilize the PLL frequency.
TA4OUT	Timer A pin	I/O	I/O pins for timer A4
TA4IN		I	
U, $\overline{U}$	Three-phase motor control output pin	O	U-phase output pins
$\overline{INT0}$ to $\overline{INT2}$	$\overline{INT}$ interrupt input pin	I	Input pins for the $\overline{INT}$ interrupt
INPC02	Intelligent I/O pin	I	INPC02 is an input pin for the time measurement function.
ISRxD0		I	ISRxD0 and BE0IN input received data for the intelligent I/O communication function.
BE0IN		I	
CANOUT	CAN pin	O	I/O pins for the CAN communication function
CANIN		I	
P85/$\overline{NMI}$	$\overline{NMI}$ interrupt input pin	I	Input pin for the $\overline{NMI}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.
P90 to P97	I/O port P9	I/O	8-bit I/O ports having equivalent functions P0. The PRCR register prevents PD9 and PS3 registers from rewriting.
TB0IN to TB4IN	Timer B pin	I	Input pins for timers B0 to B4
$\overline{CTS3}$, $\overline{CTS4}$	UART pin	I	I/O pins for UART3 (P90 to P93) and UART4 (P94 to P97)
$\overline{RTS3}$, $\overline{RTS4}$		O	
$\overline{SS3}$, $\overline{SS4}$		I	
CLK3, CLK4		I/O	
RxD3, RxD4		I	
SCL3, SCL4		I/O	
STxD3, STxD4		O	
TxD3, TxD4		O	
SDA3, SDA4		I/O	
SRxD3, SRxD4		I	
DA0, DA1	D-A output pin	O	Output pins for the D-A converter
ANEX0,	A-D related pin	I/O	ANEX0 is an extended analog I/O pin for the A-D converter.
ANEX1,		I	ANEX1 is an extended analog input pin for the A-D converter.
$\overline{ADTRG}$		I	$\overline{ADTRG}$ is an A-D trigger input pin.
OUTC20	Intelligent I/O pin	O	OUTC20 is an output pin for the waveform generating function.
ISTxD2		O	ISTxD2 and IEOUT output transmit data for the intelligent I/O communication function.
IEOUT		O	
IEIN		I	ISRxD2 and IEIN input received data for the intelligent I/O communication function.
ISRxD2		I	
P100 to P107	I/O port P10	I/O	8-bit I/O ports having equivalent functions to P0
$\overline{KI0}$ to $\overline{KI3}$	Key input interrupt pin	I	Input pins for the key input interrupt
AN0 to AN7	Analog input pin	I	Analog input pins for the A-D converter

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (144-Pin Package only) (Continued)

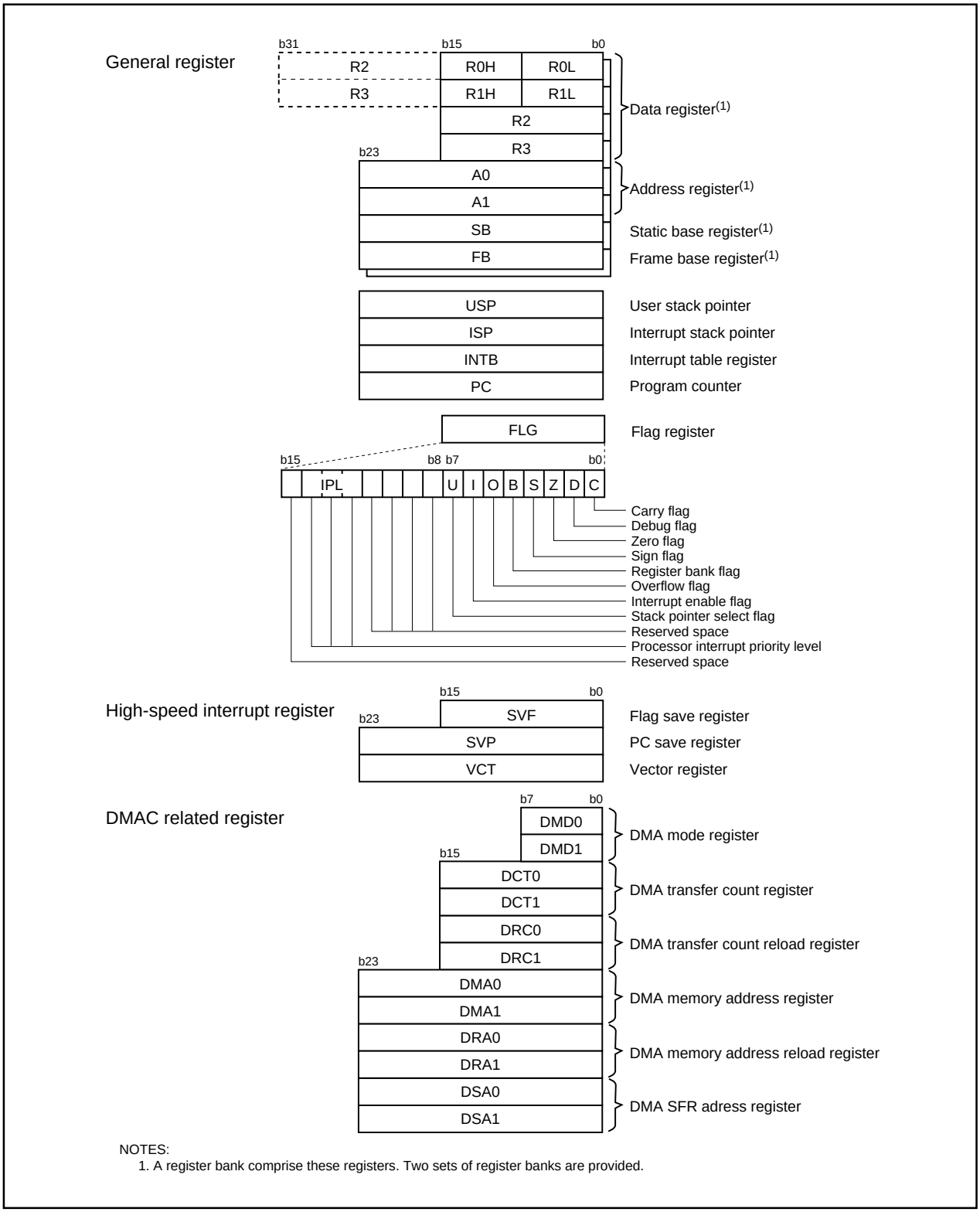
Symbol	Function	I/O type	Description
$P11_0$ to $P11_4$	I/O port P11	I/O	5-bit I/O ports having equivalent functions to P0.
$INPC11$, $INPC12$	Intelligent I/O pin	I	$INPC11$ and $INPC12$ are input pins for the time measurement function.
$OUTC10$ to $OUTC13$		O	$OUTC10$ to $OUTC13$ are output pins for the waveform generating function.
ISCLK1		I/O	ISCLK1 inputs and outputs the clock for the intelligent I/O communication
ISRxD1		I	function.
BE1IN		I	ISRxD1 and BE1IN input received data for the intelligent I/O communication
ISTxD1		O	function.
BE1OUT		O	ISTxD1 and BE1OUT output transmit data for the intelligent I/O communication function.
$P12_0$ to $P12_7$	I/O port P12	I/O	8-bit I/O ports having equivalent functions to P0
$P13_0$ to $P13_7$	I/O port P13	I/O	8-bit I/O ports having equivalent functions to P0
$OUTC20$ to $OUTC27$	Intelligent I/O pin	O	$OUTC20$ to $OUTC27$ are output pins for the waveform generating function.
ISCLK2		I/O	ISCLK2 inputs and outputs the clock for the intelligent I/O communication
ISRxD2		I	function.
IEIN		I	ISRxD2 and IEIN input received data for the intelligent I/O communication
ISTxD2		O	function.
IEOUT		O	ISTxD2 and IEOUT output transmit data for the intelligent I/O communication function.
$P14_0$ to $P14_6$	I/O port P14	I/O	7-bit I/O ports having equivalent functions to P0
$INPC16$,$INPC17$	Intelligent I/O pin	I	$INPC16$ and $INPC17$ are input pins for the time measurement function.
$OUTC14$ to $OUTC17$		O	$OUTC14$ to $OUTC17$ are output pins for the waveform generating function.
$P15_0$ to $P15_7$	I/O port P15	I/O	8-bit I/O ports having equivalent functions to P0
$INPC00$ to $INPC07$	Intelligent I/O pin	I	$INPC00$ to $INPC07$ are input pins for the time measurement function.
$OUTC00$, $OUTC01$		O	$OUTC00$, $OUTC01$, $OUTC04$ and $OUTC05$ are output pins for the waveform
$OUTC04$, $OUTC05$			generating function.
ISCLK0		I/O	ISCLK0 inputs and outputs the clock for the intelligent I/O communication
ISRxD0		I	function.
BE0IN		I	ISRxD0 and BE0IN input received data for the intelligent I/O communication
ISTxD0		O	function.
BE0OUT		O	ISTxD0 and BE0OUT output transmit data for the intelligent I/O communication function.
$AN150$ to$AN157$	Analog input port	I	Analog input pins for the A-D converter

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

A register bank comprises 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.



NOTES:
1. A register bank comprise these registers. Two sets of register banks are provided.

Figure 2.1 CPU Register

2.1 General Register

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R3R1.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC is 24 bits wide. It indicates an address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating a starting address of an interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

USP and ISP as the stack pointer are 24 bits wide. The U flag can switch USP to ISP and vice versa. Refer to "2.1.8 Flag Register (FLG)" about the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow occurs after an instruction is executed.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic calculation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic calculation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when a result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
An interrupt is disabled when the I flag is set to "0" and is enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".
The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide. It assigns an interrupt priority levels from level 0 to level 7.
If a requested interrupt has a greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to the reserved space, set to "0". When read, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows.

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-associated Registers

Registers associated with DMAC are as follows.

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/81 group.

The M32C/81 provides 16-Mbyte address space from addresses 000000$_{16}$ to FFFFFF$_{16}$.

The internal ROM is allocated in lower addresses beginning with address FFFFFF$_{16}$. For example, a 64-Kbyte internal ROM is allocated in addresses FF0000$_{16}$ to FFFFFF$_{16}$.

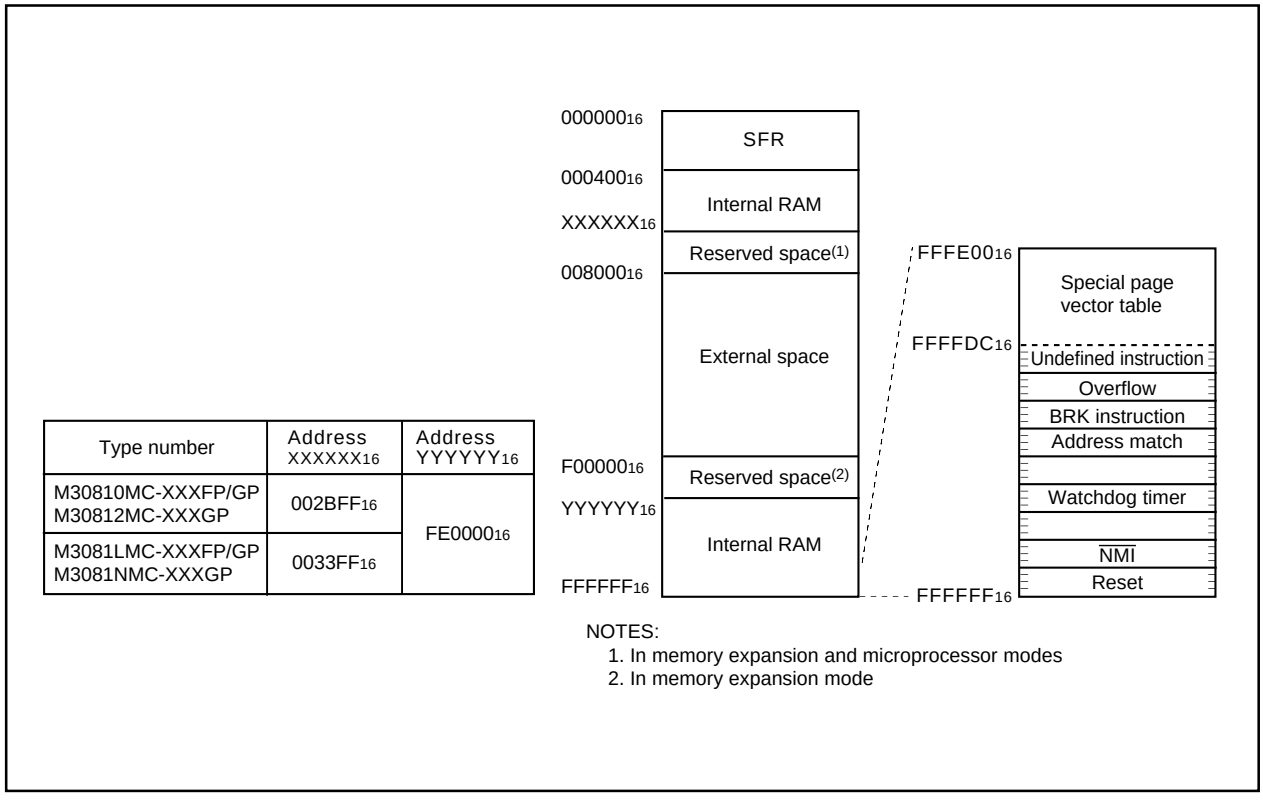
The fixed interrupt vectors are allocated in addresses FFFFDC$_{16}$ to FFFFFF$_{16}$. It stores the starting address of each interrupt routine.

The internal RAM is allocated in higher addresses beginning with address 000400$_{16}$. For example, a 10-Kbyte internal RAM is allocated in addresses 000400$_{16}$ to 002BFF$_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowleged.

The SFR is allocated in addresses 000000$_{16}$ to 0003FF$_{16}$. The control registers for peripheral functions such as I/O port, A-D conversion, serial I/O, timer are allocated here. All addresses, which have nothing allocated within the SFR, are reserved space and cannot be accessed by users.

The special page vectors are allocated in addresses FFFE00$_{16}$ to FFFFDB$_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **Software Manual** for details.

In memory expansion mode and microprocessor mode, some space are reserved and cannot be accessed by users.



Type number	Address XXXXXX$_{16}$	Address YYYYYY$_{16}$
M30810MC-XXXFP/GP M30812MC-XXXGP	002BFF$_{16}$	FE0000$_{16}$
M3081LMC-XXXFP/GP M3081NMC-XXXGP	0033FF$_{16}$	

Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
0000$_{16}$			
0001$_{16}$			
0002$_{16}$			
0003$_{16}$			
0004$_{16}$	Processor mode register 0	PM0	1000 0000$_2$(CNVss pin ="L") 0000 0011$_2$(CNVss pin ="H")
0005$_{16}$	Processor mode register 1	PM1	0X00 0000$_2$
0006$_{16}$	System clock control register 0	CM0	0000 X000$_2$
0007$_{16}$	System clock control register 1	CM1	0010 0000$_2$
0008$_{16}$	Wait control register	WCR	1111 1111$_2$
0009$_{16}$	Address match interrupt enable register	AIER	XXXX 0000$_2$
000A$_{16}$	Protect register	PRCR	XXXX 0000$_2$
000B$_{16}$	External data bus width control register	DS	XXXX 1000$_2$(BYTE pin ="L") XXXX 0000$_2$(BYTE pin ="H")
000C$_{16}$	Main clock division register	MCD	XXX0 1000$_2$
000D$_{16}$	Oscillation stop detect register	CM2	00$_{16}$
000E$_{16}$	Watchdog timer start register	WDTS	XX$_{16}$
000F$_{16}$	Watchdog timer control register	WDC	000X XXXX$_2$
0010$_{16}$ 0011$_{16}$ 0012$_{16}$	Address match interrupt register 0	RMAD0	000000$_{16}$
0013$_{16}$			
0014$_{16}$ 0015$_{16}$ 0016$_{16}$	Address match interrupt register 1	RMAD1	000000$_{16}$
0017$_{16}$	VDC control register for PLL	PLV	XXXX XX01$_2$
0018$_{16}$ 0019$_{16}$ 001A$_{16}$	Address match interrupt register 2	RMAD2	000000$_{16}$
001B$_{16}$	VDC control register 0	VDC0	00$_{16}$
001C$_{16}$ 001D$_{16}$ 001E$_{16}$	Address match interrupt register 3	RMAD3	000000$_{16}$
001F$_{16}$			
0020$_{16}$ 0021$_{16}$ 0022$_{16}$			
0023$_{16}$			
0024$_{16}$			
0025$_{16}$			
0026$_{16}$			
0027$_{16}$			
0028$_{16}$			
0029$_{16}$			
002A$_{16}$			
002B$_{16}$			
002C$_{16}$			
002D$_{16}$			
002E$_{16}$			
002F$_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0037₁₆			
0038₁₆			
0039₁₆			
003A₁₆			
003B₁₆			
003C₁₆			
003D₁₆			
003E₁₆			
003F₁₆			
0040₁₆	DRAM control register	DRAMCONT	XX₁₆
0041₁₆	DRAM refresh interval set register	REFCNT	XX₁₆
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆			
0049₁₆			
004A₁₆			
004B₁₆			
004C₁₆			
004D₁₆			
004E₁₆			
004F₁₆			
0050₁₆			
0051₁₆			
0052₁₆			
0053₁₆			
0054₁₆			
0055₁₆			
0056₁₆			
0057₁₆			
0058₁₆			
0059₁₆			
005A₁₆			
005B₁₆			
005C₁₆			
005D₁₆			
005E₁₆			
005F₁₆			

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Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
006016			
006116			
006216			
006316			
006416			
006516			
006616			
006716			
006816	DMA0 interrupt control register	DM0IC	XXXX X0002
006916	Timer B5 interrupt control register	TB5IC	XXXX X0002
006A16	DMA2 interrupt control register	DM2IC	XXXX X0002
006B16	UART2 receive /ACK interrupt control register	S2RIC	XXXX X0002
006C16	Timer A0 interrupt control register	TA0IC	XXXX X0002
006D16	UART3 receive /ACK interrupt control register	S3RIC	XXXX X0002
006E16	Timer A2 interrupt control register	TA2IC	XXXX X0002
006F16	UART4 receive /ACK interrupt control register	S4RIC	XXXX X0002
007016	Timer A4 interrupt control register	TA4IC	XXXX X0002
007116	UART0/UART3 bus conflict detect interrupt control register	BCN0IC/BCN3IC	XXXX X0002
007216	UART0 receive/ACK interrupt control register	S0RIC	XXXX X0002
007316	A-D0 conversion interrupt control register	AD0IC	XXXX X0002
007416	UART1 receive/ACK interrupt control register	S1RIC	XXXX X0002
007516	Intelligent I/O interrupt control register 0	IIO0IC	XXXX X0002
007616	Timer B1 interrupt control register	TB1IC	XXXX X0002
007716	Intelligent I/O interrupt control register 2	IIO2IC	XXXX X0002
007816	Timer B3 interrupt control register	TB3IC	XXXX X0002
007916	Intelligent I/O interrupt control register 4	IIO4IC	XXXX X0002
007A16	INT5 interrupt control register	INT5IC	XX00 X0002
007B16	Intelligent I/O interrupt control register 6	IIO6IC	XXXX X0002
007C16	INT3 interrupt control register	INT3IC	XX00 X0002
007D16	Intelligent I/O interrupt control register 8	IIO8IC	XXXX X0002
007E16	INT1 interrupt control register	INT1IC	XX00 X0002
007F16	Intelligent I/O interrupt control register 10/ CAN interrupt 1 control register	IIO10IC CAN1IC	XXXX X0002
008016			
008116	Intelligent I/O interrupt control register 11/ CAN interrupt 2 control register	IIO11IC CAN2IC	XXXX X0002
008216			
008316			
008416			
008516			
008616	A-D1 conversion interrupt control register	AD1IC	XXXX X0002
008716			
008816	DMA1 interrupt control register	DM1IC	XXXX X0002
008916	UART2 transmit /NACK interrupt control register	S2TIC	XXXX X0002
008A16	DMA3 interrupt control register	DM3IC	XXXX X0002
008B16	UART3 transmit /NACK interrupt control register	S3TIC	XXXX X0002
008C16	Timer A1 interrupt control register	TA1IC	XXXX X0002
008D16	UART4 transmit /NACK interrupt control register	S4TIC	XXXX X0002
008E16	Timer A3 interrupt control register	TA3IC	XXXX X0002
008F16	UART2 bus conflict detect interrupt control register	BCN2IC	XXXX X0002

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Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
009016	UART0 transmit /NACK interrupt control register	S0TIC	XXXX X0002
009116	UART1/UART4 bus conflict detect interrupt control register	BCN1IC/BCN4IC	XXXX X0002
009216	UART1 transmit/NACK interrupt control register	S1TIC	XXXX X0002
009316	Key input interrupt control register	KUPIC	XXXX X0002
009416	Timer B0 interrupt control register	TB0IC	XXXX X0002
009516	Intelligent I/O interrupt control register 1	IIO1IC	XXXX X0002
009616	Timer B2 interrupt control register	TB2IC	XXXX X0002
009716	Intelligent I/O interrupt control register 3	IIO3IC	XXXX X0002
009816	Timer B4 interrupt control register	TB4IC	XXXX X0002
009916	Intelligent I/O interrupt control register 5	IIO5IC	XXXX X0002
009A16	INT4 interrupt control register	INT4IC	XX00 X0002
009B16	Intelligent I/O interrupt control register 7	IIO7IC	XXXX X0002
009C16	INT2 interrupt control register	INT2IC	XX00 X0002
009D16	Intelligent I/O interrupt control register 9/ CAN interrupt 0 control register	IIO9IC CAN0IC	XXXX X0002
009E16	INT0 interrupt control register	INT0IC	XX00 X0002
009F16	Exit priority control register	RLVL	XXXX 00002
00A016	Interrupt request register 0	IIO0IR	0000 000X2
00A116	Interrupt request register 1	IIO1IR	0000 000X2
00A216	Interrupt request register 2	IIO2IR	0000 000X2
00A316	Interrupt request register 3	IIO3IR	0000 000X2
00A416	Interrupt request register 4	IIO4IR	0000 000X2
00A516	Interrupt request register 5	IIO5IR	0000 000X2
00A616	Interrupt request register 6	IIO6IR	0000 000X2
00A716	Interrupt request register 7	IIO7IR	0000 000X2
00A816	Interrupt request register 8	IIO8IR	0000 000X2
00A916	Interrupt request register 9	IIO9IR	0000 000X2
00AA16	Interrupt request register 10	IIO10IR	0000 000X2
00AB16	Interrupt request register 11	IIO11IR	0000 000X2
00AC16			
00AD16			
00AE16			
00AF16			
00B016	Interrupt enable register 0	IIO0IE	0016
00B116	Interrupt enable register 1	IIO1IE	0016
00B216	Interrupt enable register 2	IIO2IE	0016
00B316	Interrupt enable register 3	IIO3IE	0016
00B416	Interrupt enable register 4	IIO4IE	0016
00B516	Interrupt enable register 5	IIO5IE	0016
00B616	Interrupt enable register 6	IIO6IE	0016
00B716	Interrupt enable register 7	IIO7IE	0016
00B816	Interrupt enable register 8	IIO8IE	0016
00B916	Interrupt enable register 9	IIO9IE	0016
00BA16	Interrupt enable register 10	IIO10IE	0016
00BB16	Interrupt enable register 11	IIO11IE	0016
00BC16			
00BD16			
00BE16			
00BF16			

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Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0₁₆	Group 0 time measurement/waveform generating register 0	G0TM0/G0PO0	XX₁₆
00C1₁₆			XX₁₆
00C2₁₆	Group 0 time measurement/waveform generating register 1	G0TM1/G0PO1	XX₁₆
00C3₁₆			XX₁₆
00C4₁₆	Group 0 time measurement/waveform generating register 2	G0TM2/G0PO2	XX₁₆
00C5₁₆			XX₁₆
00C6₁₆	Group 0 time measurement/waveform generating register 3	G0TM3/G0PO3	XX₁₆
00C7₁₆			XX₁₆
00C8₁₆	Group 0 time measurement/waveform generating register 4	G0TM4/G0PO4	XX₁₆
00C9₁₆			XX₁₆
00CA₁₆	Group 0 time measurement/waveform generating register 5	G0TM5/G0PO5	XX₁₆
00CB₁₆			XX₁₆
00CC₁₆	Group 0 time measurement/waveform generating register 6	G0TM6/G0PO6	XX₁₆
00CD₁₆			XX₁₆
00CE₁₆	Group 0 time measurement/waveform generating register 7	G0TM7/G0PO7	XX₁₆
00CF₁₆			XX₁₆
00D0₁₆	Group 0 waveform generating control register 0	G0POCR0	0X00 X000₂
00D1₁₆	Group 0 waveform generating control register 1	G0POCR1	0X00 X000₂
00D2₁₆	Group 0 waveform generating control register 2	G0POCR2	0X00 X000₂
00D3₁₆	Group 0 waveform generating control register 3	G0POCR3	0X00 X000₂
00D4₁₆	Group 0 waveform generating control register 4	G0POCR4	0X00 X000₂
00D5₁₆	Group 0 waveform generating control register 5	G0POCR5	0X00 X000₂
00D6₁₆	Group 0 waveform generating control register 6	G0POCR6	0X00 X000₂
00D7₁₆	Group 0 waveform generating control register 7	G0POCR7	0X00 X000₂
00D8₁₆	Group 0 time measurement control register 0	G0TMCR0	00₁₆
00D9₁₆	Group 0 time measurement control register 1	G0TMCR1	00₁₆
00DA₁₆	Group 0 time measurement control register 2	G0TMCR2	00₁₆
00DB₁₆	Group 0 time measurement control register 3	G0TMCR3	00₁₆
00DC₁₆	Group 0 time measurement control register 4	G0TMCR4	00₁₆
00DD₁₆	Group 0 time measurement control register 5	G0TMCR5	00₁₆
00DE₁₆	Group 0 time measurement control register 6	G0TMCR6	00₁₆
00DF₁₆	Group 0 time measurement control register 7	G0TMCR7	00₁₆
00E0₁₆	Group 0 base timer register	G0BT	XX₁₆
00E1₁₆			XX₁₆
00E2₁₆	Group 0 base timer control register 0	G0BCR0	00₁₆
00E3₁₆	Group 0 base timer control register 1	G0BCR1	00₁₆
00E4₁₆	Group 0 time measurement prescaler register 6	G0TPR6	00₁₆
00E5₁₆	Group 0 time measurement prescaler register 7	G0TPR7	00₁₆
00E6₁₆	Group 0 function enable register	G0FE	00₁₆
00E7₁₆	Group 0 function select register	G0FS	00₁₆
00E8₁₆	Group 0 SI/O receive buffer register	G0RB	XXXX XXXX₂
00E9₁₆			XX00 XXXX₂
00EA₁₆	Group 0 transmit buffer/receive data register	G0TB/G0DR	XX₁₆
00EB₁₆			
00EC₁₆	Group 0 receive input register	G0RI	XX₁₆
00ED₁₆	Group 0 SI/O communication mode register	G0MR	00₁₆
00EE₁₆	Group 0 transmit output register	G0TO	XX₁₆
00EF₁₆	Group 0 SI/O communication control register	G0CR	0000 X000₂

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Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00F0$_{16}$	Group 0 data compare register 0	G0CMP0	XX$_{16}$
00F1$_{16}$	Group 0 data compare register 1	G0CMP1	XX$_{16}$
00F2$_{16}$	Group 0 data compare register 2	G0CMP2	XX$_{16}$
00F3$_{16}$	Group 0 data compare register 3	G0CMP3	XX$_{16}$
00F4$_{16}$	Group 0 data mask register 0	G0MSK0	XX$_{16}$
00F5$_{16}$	Group 0 data mask register 1	G0MSK1	XX$_{16}$
00F6$_{16}$			
00F7$_{16}$			
00F8$_{16}$ 00F9$_{16}$	Group 0 receive CRC code register	G0RCRC	XX$_{16}$ XX$_{16}$
00FA$_{16}$ 00FB$_{16}$	Group 0 transmit CRC code register	G0TCRC	00$_{16}$ 00$_{16}$
00FC$_{16}$	Group 0 SI/O extended mode register	G0EMR	00$_{16}$
00FD$_{16}$	Group 0 SI/O extended receive control register	G0ERC	00$_{16}$
00FE$_{16}$	Group 0 SI/O special communication interrupt detect register	G0IRF	0000 00XX$_2$
00FF$_{16}$	Group 0 SI/O extended transmit control register	G0ETC	0000 0XXX$_2$
0100$_{16}$ 0101$_{16}$	Group 1 time measurement/waveform generating register 0	G1TM0/G1PO0	XX$_{16}$ XX$_{16}$
0102$_{16}$ 0103$_{16}$	Group 1 time measurement/waveform generating register 1	G1TM1/G1PO1	XX$_{16}$ XX$_{16}$
0104$_{16}$ 0105$_{16}$	Group 1 time measurement/waveform generating register 2	G1TM2/G1PO2	XX$_{16}$ XX$_{16}$
0106$_{16}$ 0107$_{16}$	Group 1 time measurement/waveform generating register 3	G1TM3/G1PO3	XX$_{16}$ XX$_{16}$
0108$_{16}$ 0109$_{16}$	Group 1 time measurement/waveform generating register 4	G1TM4/G1PO4	XX$_{16}$ XX$_{16}$
010A$_{16}$ 010B$_{16}$	Group 1 time measurement/waveform generating register 5	G1TM5/G1PO5	XX$_{16}$ XX$_{16}$
010C$_{16}$ 010D$_{16}$	Group 1 time measurement/waveform generating register 6	G1TM6/G1PO6	XX$_{16}$ XX$_{16}$
010E$_{16}$ 010F$_{16}$	Group 1 time measurement/waveform generating register 7	G1TM7/G1PO7	XX$_{16}$ XX$_{16}$
0110$_{16}$	Group 1 waveform generating control register 0	G1POCR0	0X00 X000$_2$
0111$_{16}$	Group 1 waveform generating control register 1	G1POCR1	0X00 X000$_2$
0112$_{16}$	Group 1 waveform generating control register 2	G1POCR2	0X00 X000$_2$
0113$_{16}$	Group 1 waveform generating control register 3	G1POCR3	0X00 X000$_2$
0114$_{16}$	Group 1 waveform generating control register 4	G1POCR4	0X00 X000$_2$
0115$_{16}$	Group 1 waveform generating control register 5	G1POCR5	0X00 X000$_2$
0116$_{16}$	Group 1 waveform generating control register 6	G1POCR6	0X00 X000$_2$
0117$_{16}$	Group 1 waveform generating control register 7	G1POCR7	0X00 X000$_2$
0118$_{16}$	Group 1 time measurement control register 0	G1TMCR0	00$_{16}$
0119$_{16}$	Group 1 time measurement control register 1	G1TMCR1	00$_{16}$
011A$_{16}$	Group 1 time measurement control register 2	G1TMCR2	00$_{16}$
011B$_{16}$	Group 1 time measurement control register 3	G1TMCR3	00$_{16}$
011C$_{16}$	Group 1 time measurement control register 4	G1TMCR4	00$_{16}$
011D$_{16}$	Group 1 time measurement control register 5	G1TMCR5	00$_{16}$
011E$_{16}$	Group 1 time measurement control register 6	G1TMCR6	00$_{16}$
011F$_{16}$	Group 1 time measurement control register 7	G1TMCR7	00$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
012016 012116	Group 1 base timer register	G1BT	XX16 XX16
012216	Group 1 base timer control register 0	G1BCR0	0016
012316	Group 1 base timer control register 1	G1BCR1	0016
012416	Group 1 time measurement prescaler register 6	G1TPR6	0016
012516	Group 1 time measurement prescaler register 7	G1TPR7	0016
012616	Group 1 function enable register	G1FE	0016
012716	Group 1 function select register	G1FS	0016
012816 012916	Group 1 SI/O receive buffer register	G1RB	XXXX XXXX2 XX00 XXXX2
012A16	Group 1 transmit buffer/receive data register	G1TB/G1DR	XX16
012B16			
012C16	Group 1 receive input register	G1RI	XX16
012D16	Group 1 SI/O communication mode register	G1MR	0016
012E16	Group 1 transmit output register	G1TO	XX16
012F16	Group 1 SI/O communication control register	G1CR	0000 X0002
013016	Group 1 data compare register 0	G1CMP0	XX16
013116	Group 1 data compare register 1	G1CMP1	XX16
013216	Group 1 data compare register 2	G1CMP2	XX16
013316	Group 1 data compare register 3	G1CMP3	XX16
013416	Group 1 data mask register 0	G1MSK0	XX16
013516	Group 1 data mask register 1	G1MSK1	XX16
013616			
013716			
013816 013916	Group 1 receive CRC code register	G1RCRC	XX16 XX16
013A16 013B16	Group 1 transmit CRC code register	G1TCRC	0016 0016
013C16	Group 1 SI/O extended mode register	G1EMR	0016
013D16	Group 1 SI/O extended receive control register	G1ERC	0016
013E16	Group 1 SI/O special communication interrupt detect register	G1IRF	0000 00XX2
013F16	Group 1 SI/O extended transmit control register	G1ETC	0000 0XXX2
014016 014116	Group 2 waveform generating register 0	G2PO0	XX16 XX16
014216 014316	Group 2 waveform generating register 1	G2PO1	XX16 XX16
014416 014516	Group 2 waveform generating register 2	G2PO2	XX16 XX16
014616 014716	Group 2 waveform generating register 3	G2PO3	XX16 XX16
014816 014916	Group 2 waveform generating register 4	G2PO4	XX16 XX16
014A16 014B16	Group 2 waveform generating register 5	G2PO5	XX16 XX16
014C16 014D16	Group 2 waveform generating register 6	G2PO6	XX16 XX16
014E16 014F16	Group 2 waveform generating register 7	G2PO7	XX16 XX16

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0150$_{16}$	Group 2 waveform generating control register 0	G2POCR0	00$_{16}$
0151$_{16}$	Group 2 waveform generating control register 1	G2POCR1	00$_{16}$
0152$_{16}$	Group 2 waveform generating control register 2	G2POCR2	00$_{16}$
0153$_{16}$	Group 2 waveform generating control register 3	G2POCR3	00$_{16}$
0154$_{16}$	Group 2 waveform generating control register 4	G2POCR4	00$_{16}$
0155$_{16}$	Group 2 waveform generating control register 5	G2POCR5	00$_{16}$
0156$_{16}$	Group 2 waveform generating control register 6	G2POCR6	00$_{16}$
0157$_{16}$	Group 2 waveform generating control register 7	G2POCR7	00$_{16}$
0158$_{16}$			
0159$_{16}$			
015A$_{16}$			
015B$_{16}$			
015C$_{16}$			
015D$_{16}$			
015E$_{16}$			
015F$_{16}$			
0160$_{16}$ 0161$_{16}$	Group 2 base timer register	G2BT	XX$_{16}$ XX$_{16}$
0162$_{16}$	Group 2 base timer control register 0	G2BCR0	00$_{16}$
0163$_{16}$	Group 2 base timer control register 1	G2BCR1	00$_{16}$
0164$_{16}$	Base timer start register	BTSR	XXXX 0000$_2$
0165$_{16}$			
0166$_{16}$	Group 2 function enable register	G2FE	00$_{16}$
0167$_{16}$	Group 2 RTP output buffer register	G2RTP	00$_{16}$
0168$_{16}$			
0169$_{16}$			
016A$_{16}$	Group 2 SI/O communication mode register	G2MR	00XX X000$_2$
016B$_{16}$	Group 2 SI/O communication control register	G2CR	0000 X000$_2$
016C$_{16}$ 016D$_{16}$	Group 2 SI/O transmit buffer register	G2TB	XX$_{16}$ XX$_{16}$
016E$_{16}$ 016F$_{16}$	Group 2 SI/O receive buffer register	G2RB	XX$_{16}$ XX$_{16}$
0170$_{16}$ 0171$_{16}$	Group 2 IEBus address register	IEAR	XX$_{16}$ XX$_{16}$
0172$_{16}$	Group 2 IEBus control register	IECR	00XX X000$_2$
0173$_{16}$	Group 2 IEBus transmit interrupt cause detect register	IETIF	XXX0 0000$_2$
0174$_{16}$	Group 2 IEBus receive interrupt cause detect register	IERIF	XXX0 0000$_2$
0175$_{16}$			
0176$_{16}$			
0177$_{16}$			
0178$_{16}$	Input function select register	IPS	00$_{16}$
0179$_{16}$			
017A$_{16}$			
017B$_{16}$			
017C$_{16}$			
017D$_{16}$			
017E$_{16}$			
017F$_{16}$ to 01AF$_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
01B0$_{16}$			
01B1$_{16}$			
01B2$_{16}$			
01B3$_{16}$			
01B4$_{16}$			
01B5$_{16}$			
01B6$_{16}$			
01B7$_{16}$			
01B8$_{16}$			
01B9$_{16}$			
01BA$_{16}$			
01BB$_{16}$			
01BC$_{16}$			
01BD$_{16}$			
01BE$_{16}$			
01BF$_{16}$			
01C0$_{16}$ 01C1$_{16}$	A-D1 register 0	AD10	XX$_{16}$ XX$_{16}$
01C2$_{16}$ 01C3$_{16}$	A-D1 register 1	AD11	XX$_{16}$ XX$_{16}$
01C4$_{16}$ 01C5$_{16}$	A-D1 register 2	AD12	XX$_{16}$ XX$_{16}$
01C6$_{16}$ 01C7$_{16}$	A-D1 register 3	AD13	XX$_{16}$ XX$_{16}$
01C8$_{16}$ 01C9$_{16}$	A-D1 register 4	AD14	XX$_{16}$ XX$_{16}$
01CA$_{16}$ 01CB$_{16}$	A-D1 register 5	AD15	XX$_{16}$ XX$_{16}$
01CC$_{16}$ 01CD$_{16}$	A-D1 register 6	AD16	XX$_{16}$ XX$_{16}$
01CE$_{16}$ 01CF$_{16}$	A-D1 register 7	AD17	XX$_{16}$ XX$_{16}$
01D0$_{16}$			
01D1$_{16}$			
01D2$_{16}$			
01D3$_{16}$			
01D4$_{16}$	A-D1 control register 2	AD1CON2	X00X X000$_2$
01D5$_{16}$			
01D6$_{16}$	A-D1 control register 0	AD1CON0	00$_{16}$
01D7$_{16}$	A-D1 control register 1	AD1CON1	XX00 0000$_2$
01D8$_{16}$			
01D9$_{16}$			
01DA$_{16}$			
01DB$_{16}$			
01DC$_{16}$			
01DD$_{16}$			
01DE$_{16}$			
01DF$_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
01E0₁₆	CAN0 message slot buffer 0 standard ID0	C0SLOT0_0	XX₁₆
01E1₁₆	CAN0 message slot buffer 0 standard ID1	C0SLOT0_1	XX₁₆
01E2₁₆	CAN0 message slot buffer 0 extended ID0	C0SLOT0_2	XX₁₆
01E3₁₆	CAN0 message slot buffer 0 extended ID1	C0SLOT0_3	XX₁₆
01E4₁₆	CAN0 message slot buffer 0 extended ID2	C0SLOT0_4	XX₁₆
01E5₁₆	CAN0 message slot buffer 0 data length code	C0SLOT0_5	XX₁₆
01E6₁₆	CAN0 message slot buffer 0 data 0	C0SLOT0_6	XX₁₆
01E7₁₆	CAN0 message slot buffer 0 data 1	C0SLOT0_7	XX₁₆
01E8₁₆	CAN0 message slot buffer 0 data 2	C0SLOT0_8	XX₁₆
01E9₁₆	CAN0 message slot buffer 0 data 3	C0SLOT0_9	XX₁₆
01EA₁₆	CAN0 message slot buffer 0 data 4	C0SLOT0_10	XX₁₆
01EB₁₆	CAN0 message slot buffer 0 data 5	C0SLOT0_11	XX₁₆
01EC₁₆	CAN0 message slot buffer 0 data 6	C0SLOT0_12	XX₁₆
01ED₁₆	CAN0 message slot buffer 0 data 7	C0SLOT0_13	XX₁₆
01EE₁₆	CAN0 message slot buffer 0 time stamp high-order	C0SLOT0_14	XX₁₆
01EF₁₆	CAN0 message slot buffer 0 time stamp low-order	C0SLOT0_15	XX₁₆
01F0₁₆	CAN0 message slot buffer 1 standard ID0	C0SLOT1_0	XX₁₆
01F1₁₆	CAN0 message slot buffer 1 standard ID1	C0SLOT1_1	XX₁₆
01F2₁₆	CAN0 message slot buffer 1 extended ID0	C0SLOT1_2	XX₁₆
01F3₁₆	CAN0 message slot buffer 1 extended ID1	C0SLOT1_3	XX₁₆
01F4₁₆	CAN0 message slot buffer 1 extended ID2	C0SLOT1_4	XX₁₆
01F5₁₆	CAN0 message slot buffer 1 data length code	C0SLOT1_5	XX₁₆
01F6₁₆	CAN0 message slot buffer 1 data 0	C0SLOT1_6	XX₁₆
01F7₁₆	CAN0 message slot buffer 1 data 1	C0SLOT1_7	XX₁₆
01F8₁₆	CAN0 message slot buffer 1 data 2	C0SLOT1_8	XX₁₆
01F9₁₆	CAN0 message slot buffer 1 data 3	C0SLOT1_9	XX₁₆
01FA₁₆	CAN0 message slot buffer 1 data 4	C0SLOT1_10	XX₁₆
01FB₁₆	CAN0 message slot buffer 1 data 5	C0SLOT1_11	XX₁₆
01FC₁₆	CAN0 message slot buffer 1 data 6	C0SLOT1_12	XX₁₆
01FD₁₆	CAN0 message slot buffer 1 data 7	C0SLOT1_13	XX₁₆
01FE₁₆	CAN0 message slot buffer 1 time stamp high-order	C0SLOT1_14	XX₁₆
01FF₁₆	CAN0 message slot buffer 1 time stamp low-order	C0SLOT1_15	XX₁₆
0200₁₆ 0201₁₆	CAN0 control register 0	C0CTLR0	XX01 0X01₂(1) XXXX 0000₂(1)
0202₁₆ 0203₁₆	CAN0 status register	C0STR	0000 0000₂(1) X000 0X01₂(1)
0204₁₆ 0205₁₆	CAN0 extended ID register	C0IDR	00₁₆(1) 00₁₆(1)
0206₁₆ 0207₁₆	CAN0 configuration register	C0CONR	0000 XXXX₂(1) 0000 0000₂(1)
0208₁₆ 0209₁₆	CAN0 time stamp register	C0TSR	00₁₆(1) 00₁₆(1)
020A₁₆	CAN0 transmit error count register	C0TEC	00₁₆(1)
020B₁₆	CAN0 receive error count register	C0REC	00₁₆(1)
020C₁₆ 020D₁₆	CAN0 slot interrupt status register	C0SISTR	00₁₆(1) 00₁₆(1)
020E₁₆			
020F₁₆			

X: Indeterminate

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NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
021016	CAN0 slot interrupt mask register	C0SIMKR	0016(2)
021116			0016(2)
021216			
021316			
021416	CAN0 error interrupt mask register	C0EIMKR	XXXX X0002(2)
021516	CAN0 error interrupt status register	C0EISTR	XXXX X0002(2)
021616			
021716	CAN0 baud rate prescaler	C0BRP	0000 00012(2)
021816			
021916			
021A16			
021B16			
021C16			
021D16			
021E16			
021F16			
022016			
022116			
022216			
022316			
022416			
022516			
022616			
022716			
022816	CAN0 global mask register standard ID0	C0GMR0	XXX0 00002(2)
022916	CAN0 global mask register standard ID1	C0GMR1	XX00 00002(2)
022A16	CAN0 global mask register extended ID0	C0GMR2	XXXX 00002(2)
022B16	CAN0 global mask register extended ID1	C0GMR3	0016(2)
022C16	CAN0 global mask register extended ID2	C0GMR4	XX00 00002(2)
022D16			
022E16			
022F16			
023016	CAN0 message slot 0 control register /	C0MCTL0/	0000 00002(2)
	CAN0 local mask register A standard ID0	C0LMAR0	XXX0 00002(2)
023116	CAN0 message slot 1 control register /	C0MCTL1/	0000 00002(2)
	CAN0 local mask register A standard ID1	C0LMAR1	XX00 00002(2)
023216	CAN0 message slot 2 control register /	C0MCTL2/	0000 00002(2)
	CAN0 local mask register A extended ID0	C0LMAR2	XXXX 00002(2)
023316	CAN0 message slot 3 control register /	C0MCTL3/	0016(2)
	CAN0 local mask register A extended ID1	C0LMAR3	0016(2)
023416	CAN0 message slot 4 control register /	C0MCTL4/	0000 00002(2)
	CAN0 local mask register A extended ID2	C0LMAR4	XX00 00002(2)
023516	CAN0 message slot 5 control register	C0MCTL5	0016(2)
023616	CAN0 message slot 6 control register	C0MCTL6	0016(2)
023716	CAN0 message slot 7 control register	C0MCTL7	0016(2)
023816	CAN0 message slot 8 control register /	C0MCTL8/	0000 00002(2)
	CAN0 local mask register B standard ID0	C0LMBR0	XXX0 00002(2)

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
023916	CAN0 message slot 9 control register / CAN0 local mask register B standard ID1	C0MCTL9/ C0LMBR1	0000 00002(2) XX00 00002(2)
023A16	CAN0 message slot 10 control register / CAN0 local mask register B extended ID0	C0MCTL10/ C0LMBR2	0000 00002(2) XXXX 00002(2)
023B16	CAN0 message slot 11 control register / CAN0 local mask register B extended ID1	C0MCTL11/ C0LMBR3	0016(2) 0016(2)
023C16	CAN0 message slot 12 control register / CAN0 local mask register B extended ID2	C0MCTL12/ C0LMBR4	0000 00002(2) XX00 00002(2)
023D16	CAN0 message slot 13 control register	C0MCTL13	0016(2)
023E16	CAN0 message slot 14 control register	C0MCTL14	0016(2)
023F16	CAN0 message slot 15 control register	C0MCTL15	0016(2)
024016	CAN0 slot buffer select register	C0SBS	0016(2)
024116	CAN0 control register 1	C0CTLR1	XX00 00XX2(2)
024216	CAN0 sleep control register	C0SLPR	XXXX XXX02
024316			
024416	CAN0 acceptance filter support register	C0AFS	0016(2)
024516			0116(2)
024616			
024716			
024816			
024916			
024A16			
024B16			
024C16			
024D16			
024E16			
024F16			
025016			
025116			
025216			
025316			
025416			
025516			
025616			
025716			
025816			
025916			
025A16			
025B16			
025C16			
025D16			
025E16			
025F16			
026016			
026116 to 02BF16			

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02C0$_{16}$	X0 register Y0 register	X0R,Y0R	XX$_{16}$
02C1$_{16}$			XX$_{16}$
02C2$_{16}$	X1 register Y1 register	X1R,Y1R	XX$_{16}$
02C3$_{16}$			XX$_{16}$
02C4$_{16}$	X2 register Y2 register	X2R,Y2R	XX$_{16}$
02C5$_{16}$			XX$_{16}$
02C6$_{16}$	X3 register Y3 register	X3R,Y3R	XX$_{16}$
02C7$_{16}$			XX$_{16}$
02C8$_{16}$	X4 register Y4 register	X4R,Y4R	XX$_{16}$
02C9$_{16}$			XX$_{16}$
02CA$_{16}$	X5 register Y5 register	X5R,Y5R	XX$_{16}$
02CB$_{16}$			XX$_{16}$
02CC$_{16}$	X6 register Y6 register	X6R,Y6R	XX$_{16}$
02CD$_{16}$			XX$_{16}$
02CE$_{16}$	X7 register Y7 register	X7R,Y7R	XX$_{16}$
02CF$_{16}$			XX$_{16}$
02D0$_{16}$	X8 register Y8 register	X8R,Y8R	XX$_{16}$
02D1$_{16}$			XX$_{16}$
02D2$_{16}$	X9 register Y9 register	X9R,Y9R	XX$_{16}$
02D3$_{16}$			XX$_{16}$
02D4$_{16}$	X10 register Y10 register	X10R,Y10R	XX$_{16}$
02D5$_{16}$			XX$_{16}$
02D6$_{16}$	X11 register Y11 register	X11R,Y11R	XX$_{16}$
02D7$_{16}$			XX$_{16}$
02D8$_{16}$	X12 register Y12 register	X12R,Y12R	XX$_{16}$
02D9$_{16}$			XX$_{16}$
02DA$_{16}$	X13 register Y13 register	X13R,Y13R	XX$_{16}$
02DB$_{16}$			XX$_{16}$
02DC$_{16}$	X14 register Y14 register	X14R,Y14R	XX$_{16}$
02DD$_{16}$			XX$_{16}$
02DE$_{16}$	X15 register Y15 register	X15R,Y15R	XX$_{16}$
02DF$_{16}$			XX$_{16}$
02E0$_{16}$	XY control register	XYC	XXXX XX00$_2$
02E1$_{16}$			
02E2$_{16}$			
02E3$_{16}$			
02E4$_{16}$	UART1 special mode register 4	U1SMR4	00$_{16}$
02E5$_{16}$	UART1 special mode register 3	U1SMR3	00$_{16}$
02E6$_{16}$	UART1 special mode register 2	U1SMR2	00$_{16}$
02E7$_{16}$	UART1 special mode register	U1SMR	00$_{16}$
02E8$_{16}$	UART1 transmit/receive mode register	U1MR	00$_{16}$
02E9$_{16}$	UART1 baud rate register	U1BRG	XX$_{16}$
02EA$_{16}$	UART1 transmit buffer register	U1TB	XX$_{16}$
02EB$_{16}$			XX$_{16}$
02EC$_{16}$	UART1 transmit/receive control register 0	U1C0	0000 1000$_2$
02ED$_{16}$	UART1 transmit/receive control register 1	U1C1	0000 0010$_2$
02EE$_{16}$	UART1 receive buffer register	U1RB	XX$_{16}$
02EF$_{16}$			XX$_{16}$

X: Indeterminate

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Address	Register	Symbol	Value after RESET
02F0$_{16}$			
02F1$_{16}$			
02F2$_{16}$			
02F3$_{16}$			
02F4$_{16}$	UART4 special mode register 4	U4SMR4	00$_{16}$
02F5$_{16}$	UART4 special mode register 3	U4SMR3	00$_{16}$
02F6$_{16}$	UART4 special mode register 2	U4SMR2	00$_{16}$
02F7$_{16}$	UART4 special mode register	U4SMR	00$_{16}$
02F8$_{16}$	UART4 transmit/receive mode register	U4MR	00$_{16}$
02F9$_{16}$	UART4 baud rate register	U4BRG	XX$_{16}$
02FA$_{16}$ 02FB$_{16}$	UART4 transmit buffer register	U4TB	XX$_{16}$ XX$_{16}$
02FC$_{16}$	UART4 transmit/receive control register 0	U4C0	0000 1000$_2$
02FD$_{16}$	UART4 transmit/receive control register 1	U4C1	0000 0010$_2$
02FE$_{16}$ 02FF$_{16}$	UART4 receive buffer register	U4RB	XX$_{16}$ XX$_{16}$
0300$_{16}$	Timer B3,B4,B5 count start flag	TBSR	000X XXXX$_2$
0301$_{16}$			
0302$_{16}$ 0303$_{16}$	Timer A1-1 register	TA11	XX$_{16}$ XX$_{16}$
0304$_{16}$ 0305$_{16}$	Timer A2-1 register	TA21	XX$_{16}$ XX$_{16}$
0306$_{16}$ 0307$_{16}$	Timer A4-1 register	TA41	XX$_{16}$ XX$_{16}$
0308$_{16}$	Three-phase PWM control register 0	INVC0	00$_{16}$
0309$_{16}$	Three-phase PWM control register 1	INVC1	00$_{16}$
030A$_{16}$	Three-phase output buffer register 0	IDB0	XX11 1111$_2$
030B$_{16}$	Three-phase output buffer register 1	IDB1	XX11 1111$_2$
030C$_{16}$	Dead time timer	DTT	XX$_{16}$
030D$_{16}$	Timer B2 interrupt generating frequency set counter	ICTB2	XX$_{16}$
030E$_{16}$			
030F$_{16}$			
0310$_{16}$ 0311$_{16}$	Timer B3 register	TB3	XX$_{16}$ XX$_{16}$
0312$_{16}$ 0313$_{16}$	Timer B4 register	TB4	XX$_{16}$ XX$_{16}$
0314$_{16}$ 0315$_{16}$	Timer B5 register	TB5	XX$_{16}$ XX$_{16}$
0316$_{16}$			
0317$_{16}$			
0318$_{16}$			
0319$_{16}$			
031A$_{16}$			
031B$_{16}$	Timer B3 mode register	TB3MR	00XX 0000$_2$
031C$_{16}$	Timer B4 mode register	TB4MR	00XX 0000$_2$
031D$_{16}$	Timer B5 mode register	TB5MR	00XX 0000$_2$
031E$_{16}$			
031F$_{16}$	External interrupt cause select register	IFSR	00$_{16}$

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Address	Register	Symbol	Value after RESET
0320₁₆			
0321₁₆			
0322₁₆			
0323₁₆			
0324₁₆	UART3 special mode register 4	U3SMR4	00₁₆
0325₁₆	UART3 special mode register 3	U3SMR3	00₁₆
0326₁₆	UART3 special mode register 2	U3SMR2	00₁₆
0327₁₆	UART3 special mode register	U3SMR	00₁₆
0328₁₆	UART3 transmit/receive mode register	U3MR	00₁₆
0329₁₆	UART3 baud rate register	U3BRG	XX₁₆
032A₁₆ 032B₁₆	UART3 transmit buffer register	U3TB	XX₁₆ XX₁₆
032C₁₆	UART3 transmit/receive control register 0	U3C0	0000 1000₂
032D₁₆	UART3 transmit/receive control register 1	U3C1	0000 0010₂
032E₁₆ 032F₁₆	UART3 receive buffer register	U3RB	XX₁₆ XX₁₆
0330₁₆			
0331₁₆			
0332₁₆			
0333₁₆			
0334₁₆	UART2 special mode register 4	U2SMR4	00₁₆
0335₁₆	UART2 special mode register 3	U2SMR3	00₁₆
0336₁₆	UART2 special mode register 2	U2SMR2	00₁₆
0337₁₆	UART2 special mode register	U2SMR	00₁₆
0338₁₆	UART2 transmit/receive mode register	U2MR	00₁₆
0339₁₆	UART2 baud rate register	U2BRG	XX₁₆
033A₁₆ 033B₁₆	UART2 transmit buffer register	U2TB	XX₁₆ XX₁₆
033C₁₆	UART2 transmit/receive control register 0	U2C0	0000 1000₂
033D₁₆	UART2 transmit/receive control register 1	U2C1	0000 0010₂
033E₁₆ 033F₁₆	UART2 receive buffer register	U2RB	XX₁₆ XX₁₆
0340₁₆	Count start flag	TABSR	00₁₆
0341₁₆	Clock prescaler reset flag	CPSRF	0XXX XXXX₂
0342₁₆	One-shot start flag	ONSF	00₁₆
0343₁₆	Trigger select register	TRGSR	00₁₆
0344₁₆	Up-down flag	UDF	00₁₆
0345₁₆			
0346₁₆ 0347₁₆	Timer A0 register	TA0	XX₁₆ XX₁₆
0348₁₆ 0349₁₆	Timer A1 register	TA1	XX₁₆ XX₁₆
034A₁₆ 034B₁₆	Timer A2 register	TA2	XX₁₆ XX₁₆
034C₁₆ 034D₁₆	Timer A3 register	TA3	XX₁₆ XX₁₆
034E₁₆ 034F₁₆	Timer A4 register	TA4	XX₁₆ XX₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0350₁₆	Timer B0 register	TB0	XX₁₆
0351₁₆			XX₁₆
0352₁₆	Timer B1 register	TB1	XX₁₆
0353₁₆			XX₁₆
0354₁₆	Timer B2 register	TB2	XX₁₆
0355₁₆			XX₁₆
0356₁₆	Timer A0 mode register	TA0MR	0000 0X00₂
0357₁₆	Timer A1 mode register	TA1MR	0000 0X00₂
0358₁₆	Timer A2 mode register	TA2MR	0000 0X00₂
0359₁₆	Timer A3 mode register	TA3MR	0000 0X00₂
035A₁₆	Timer A4 mode register	TA4MR	0000 0X00₂
035B₁₆	Timer B0 mode register	TB0MR	00XX 0000₂
035C₁₆	Timer B1 mode register	TB1MR	00XX 0000₂
035D₁₆	Timer B2 mode register	TB2MR	00XX 0000₂
035E₁₆	Timer B2 special mode register	TB2SC	XXXX XXX0₂
035F₁₆	Count source prescaler register	TCSPR	0XXX 0000₂
0360₁₆			
0361₁₆			
0362₁₆			
0363₁₆			
0364₁₆	UART0 special mode register 4	U0SMR4	00₁₆
0365₁₆	UART0 special mode register 3	U0SMR3	00₁₆
0366₁₆	UART0 special mode register 2	U0SMR2	00₁₆
0367₁₆	UART0 special mode register	U0SMR	00₁₆
0368₁₆	UART0 transmit/receive mode register	U0MR	00₁₆
0369₁₆	UART0 baud rate register	U0BRG	XX₁₆
036A₁₆	UART0 transmit buffer register	U0TB	XX₁₆
036B₁₆			XX₁₆
036C₁₆	UART0 transmit/receive control register 0	U0C0	0000 1000₂
036D₁₆	UART0 transmit/receive control register 1	U0C1	0000 0010₂
036E₁₆	UART0 receive buffer register	U0RB	XX₁₆
036F₁₆			XX₁₆
0370₁₆			
0371₁₆			
0372₁₆			
0373₁₆			
0374₁₆			
0375₁₆			
0376₁₆	PLL control register 0	PLC0	0011 X100₂
0377₁₆	PLL control register 1	PLC1	XXXX 0000₂
0378₁₆	DMA0 cause select register	DM0SL	0X00 0000₂
0379₁₆	DMA1 cause select register	DM1SL	0X00 0000₂
037A₁₆	DMA2 cause select register	DM2SL	0X00 0000₂
037B₁₆	DMA3 cause select register	DM3SL	0X00 0000₂
037C₁₆	CRC data register	CRCD	XX₁₆
037D₁₆			XX₁₆
037E₁₆	CRC input register	CRCIN	XX₁₆
037F₁₆			

X: Indeterminate

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Address	Register	Symbol	Value after RESET
038016	A-D0 register 0	AD00	XX16
038116			XX16
038216	A-D0 register 1	AD01	XX16
038316			XX16
038416	A-D0 register 2	AD02	XX16
038516			XX16
038616	A-D0 register 3	AD03	XX16
038716			XX16
038816	A-D0 register 4	AD04	XX16
038916			XX16
038A16	A-D0 register 5	AD05	XX16
038B16			XX16
038C16	A-D0 register 6	AD06	XX16
038D16			XX16
038E16	A-D0 register 7	AD07	XX16
038F16			XX16
039016			
039116			
039216			
039316			
039416	A-D0 control register 2	AD0CON2	X000 00002
039516			
039616	A-D0 control register 0	AD0CON0	0016
039716	A-D0 control register 1	AD0CON1	0016
039816	D-A register 0	DA0	XX16
039916			
039A16	D-A register 1	DA1	XX16
039B16			
039C16	D-A control register	DACON	XXXX XX002
039D16			
039E16			
039F16			

X: Indeterminate

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<144-pin package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$	Function select register A8	PS8	X000 0000$_2$
03A1$_{16}$	Function select register A9	PS9	00$_{16}$
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$			
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$			
03AD$_{16}$			
03AE$_{16}$			
03AF$_{16}$	Function select register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function select register A0	PS0	00$_{16}$
03B1$_{16}$	Function select register A1	PS1	00$_{16}$
03B2$_{16}$	Function select register B0	PSL0	00$_{16}$
03B3$_{16}$	Function select register B1	PSL1	00$_{16}$
03B4$_{16}$	Function select register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function select register A3	PS3	00$_{16}$
03B6$_{16}$	Function select register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function select register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$	Function select register A5	PS5	XXX0 0000$_2$
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$	Function select register A7	PS7	00$_{16}$
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 register	P6	XX$_{16}$
03C1$_{16}$	Port P7 register	P7	XX$_{16}$
03C2$_{16}$	Port P6 direction register	PD6	00$_{16}$
03C3$_{16}$	Port P7 direction register	PD7	00$_{16}$
03C4$_{16}$	Port P8 register	P8	XX$_{16}$
03C5$_{16}$	Port P9 register	P9	XX$_{16}$
03C6$_{16}$	Port P8 direction register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 direction register	PD9	00$_{16}$
03C8$_{16}$	Port P10 register	P10	XX$_{16}$
03C9$_{16}$	Port P11 register	P11	XX$_{16}$
03CA$_{16}$	Port P10 direction register	PD10	00$_{16}$
03CB$_{16}$	Port P11 direction register	PD11	XXX0 0000$_2$
03CC$_{16}$	Port P12 register	P12	XX$_{16}$
03CD$_{16}$	Port P13 register	P13	XX$_{16}$
03CE$_{16}$	Port P12 direction register	PD12	00$_{16}$
03CF$_{16}$	Port P13 direction register	PD13	00$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03D0$_{16}$	Port P14 register	P14	XX$_{16}$
03D1$_{16}$	Port P15 register	P15	XX$_{16}$
03D2$_{16}$	Port P14 direction register	PD14	X000 0000$_2$
03D3$_{16}$	Port P15 direction register	PD15	00$_{16}$
03D4$_{16}$			
03D5$_{16}$			
03D6$_{16}$			
03D7$_{16}$			
03D8$_{16}$			
03D9$_{16}$			
03DA$_{16}$	Pull-up control register 2	PUR2	00$_{16}$
03DB$_{16}$	Pull-up control register 3	PUR3	00$_{16}$
03DC$_{16}$	Pull-up control register 4	PUR4	XXXX 0000$_2$
03DD$_{16}$			
03DE$_{16}$			
03DF$_{16}$			
03E0$_{16}$	Port P0 register	P0	XX$_{16}$
03E1$_{16}$	Port P1 register	P1	XX$_{16}$
03E2$_{16}$	Port P0 direction register	PD0	00$_{16}$
03E3$_{16}$	Port P1 direction register	PD1	00$_{16}$
03E4$_{16}$	Port P2 register	P2	XX$_{16}$
03E5$_{16}$	Port P3 register	P3	XX$_{16}$
03E6$_{16}$	Port P2 direction register	PD2	00$_{16}$
03E7$_{16}$	Port P3 direction register	PD3	00$_{16}$
03E8$_{16}$	Port P4 register	P4	XX$_{16}$
03E9$_{16}$	Port P5 register	P5	XX$_{16}$
03EA$_{16}$	Port P4 direction register	PD4	00$_{16}$
03EB$_{16}$	Port P5 direction register	PD5	00$_{16}$
03EC$_{16}$			
03ED$_{16}$			
03EE$_{16}$			
03EF$_{16}$			
03F0$_{16}$	Pull-up control register 0	PUR0	00$_{16}$
03F1$_{16}$	Pull-up control register 1	PUR1	XXXX 0000$_2$
03F2$_{16}$			
03F3$_{16}$			
03F4$_{16}$			
03F5$_{16}$			
03F6$_{16}$			
03F7$_{16}$			
03F8$_{16}$			
03F9$_{16}$			
03FA$_{16}$			
03FB$_{16}$			
03FC$_{16}$			
03FD$_{16}$			
03FE$_{16}$			
03FF$_{16}$	Port control register	PCR	XXXX XXX0$_2$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin package>

Address	Register	Symbol	Value after RESET	
03A0$_{16}$				(Note 2)
03A1$_{16}$				
03A2$_{16}$				
03A3$_{16}$				
03A4$_{16}$				
03A5$_{16}$				
03A6$_{16}$				
03A7$_{16}$				
03A8$_{16}$				
03A9$_{16}$				
03AA$_{16}$				
03AB$_{16}$				
03AC$_{16}$				
03AD$_{16}$				
03AE$_{16}$				
03AF$_{16}$	Function select register C	PSC	0X00 0000$_2$	
03B0$_{16}$	Function select register A0	PS0	00$_{16}$	
03B1$_{16}$	Function select register A1	PS1	00$_{16}$	
03B2$_{16}$	Function select register B0	PSL0	00$_{16}$	
03B3$_{16}$	Function select register B1	PSL1	00$_{16}$	
03B4$_{16}$	Function select register A2	PS2	00X0 0000$_2$	
03B5$_{16}$	Function select register A3	PS3	00$_{16}$	
03B6$_{16}$	Function select register B2	PSL2	00X0 0000$_2$	
03B7$_{16}$	Function select register B3	PSL3	00$_{16}$	
03B8$_{16}$				
03B9$_{16}$				(Note 2)
03BA$_{16}$				
03BB$_{16}$				
03BC$_{16}$				(Note 2)
03BD$_{16}$				
03BE$_{16}$				
03BF$_{16}$				
03C0$_{16}$	Port P6 register	P6	XX$_{16}$	
03C1$_{16}$	Port P7 register	P7	XX$_{16}$	
03C2$_{16}$	Port P6 direction register	PD6	00$_{16}$	
03C3$_{16}$	Port P7 direction register	PD7	00$_{16}$	
03C4$_{16}$	Port P8 register	P8	XX$_{16}$	
03C5$_{16}$	Port P9 register	P9	XX$_{16}$	
03C6$_{16}$	Port P8 direction register	PD8	00X0 0000$_2$	
03C7$_{16}$	Port P9 direction register	PD9	00$_{16}$	
03C8$_{16}$	Port P10 register	P10	XX$_{16}$	
03C9$_{16}$				(Note 2)
03CA$_{16}$	Port P10 direction register	PD10	00$_{16}$	
03CB$_{16}$				(Note 1)
03CC$_{16}$				(Note 2)
03CD$_{16}$				
03CE$_{16}$				(Note 1)
03CF$_{16}$				

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Set address spaces 03CB$_{16}$, 03CE$_{16}$ and 03CF$_{16}$ to "FF$_{16}$" in the 100-pin package.
2. Address spaces 03A0$_{16}$, 03A1$_{16}$, 03B9$_{16}$, 03BC$_{16}$, 03BD$_{16}$, 03C9$_{16}$, 03CC$_{16}$ and 03CD$_{16}$ are not provided in the 100-pin package.

<100-pin package>

Address	Register	Symbol	Value after RESET	
03D0$_{16}$				(Note 3)
03D1$_{16}$				
03D2$_{16}$				(Note 1)
03D3$_{16}$				
03D4$_{16}$				
03D5$_{16}$				
03D6$_{16}$				
03D7$_{16}$				
03D8$_{16}$				
03D9$_{16}$				
03DA$_{16}$	Pull-up control register 2	PUR2	00$_{16}$	
03DB$_{16}$	Pull-up control register 3	PUR3	00$_{16}$	
03DC$_{16}$				(Note 2)
03DD$_{16}$				
03DE$_{16}$				
03DF$_{16}$				
03E0$_{16}$	Port P0 register	P0	XX$_{16}$	
03E1$_{16}$	Port P1 register	P1	XX$_{16}$	
03E2$_{16}$	Port P0 direction register	PD0	00$_{16}$	
03E3$_{16}$	Port P1 direction register	PD1	00$_{16}$	
03E4$_{16}$	Port P2 register	P2	XX$_{16}$	
03E5$_{16}$	Port P3 register	P3	XX$_{16}$	
03E6$_{16}$	Port P2 direction register	PD2	00$_{16}$	
03E7$_{16}$	Port P3 direction register	PD3	00$_{16}$	
03E8$_{16}$	Port P4 register	P4	XX$_{16}$	
03E9$_{16}$	Port P5 register	P5	XX$_{16}$	
03EA$_{16}$	Port P4 direction register	PD4	00$_{16}$	
03EB$_{16}$	Port P5 direction register	PD5	00$_{16}$	
03EC$_{16}$				
03ED$_{16}$				
03EE$_{16}$				
03EF$_{16}$				
03F0$_{16}$	Pull-up control register 0	PUR0	00$_{16}$	
03F1$_{16}$	Pull-up control register 1	PUR1	XXXX 0000$_2$	
03F2$_{16}$				
03F3$_{16}$				
03F4$_{16}$				
03F5$_{16}$				
03F6$_{16}$				
03F7$_{16}$				
03F8$_{16}$				
03F9$_{16}$				
03FA$_{16}$				
03FB$_{16}$				
03FC$_{16}$				
03FD$_{16}$				
03FE$_{16}$				
03FF$_{16}$	Port control register	PCR	XXXX XXX0$_2$	

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Set address spaces 03D2$_{16}$ and 03D3$_{16}$ to "FF$_{16}$" in the 100-pin package.
2. Set address spaces 03DC$_{16}$ to "00$_{16}$" in the 100-pin package.
3. Address space 03D0$_{16}$ and 03D1$_{16}$ are not provided in the 100-pin package.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V_{CC}	Supply voltage		V_{CC}=AV_{CC}	-0.3 to 6.0	V
AV_{CC}	Analog supply voltage		V_{CC}=AV_{CC}	-0.3 to 6.0	V
V_I	Input voltage	$\overline{RESET}$, CNV_{SS}, BYTE, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), V_{REF}, X_{IN}		-0.3 to V_{CC}+0.3	V
		$P7_0$, $P7_1$		-0.3 to 6.0	
V_O	Output voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{OUT}		-0.3 to V_{CC}+0.3	V
		$P7_0$, $P7_1$		-0.3 to 6.0	V
Pd	Power Dissipation		Topr=25° C	500	mW
Topr	Operating ambient temperature			-20 to 85/-40 to 85(2)	° C
Tstg	Storage temperature			-65 to 150	° C

NOTES:
1. P11 to P15 are provided in the 144-pin package.
2. This is an option that is on request basis.

Table 5.2 Recommended Operating Conditions (V_{CC} = 3.0V to 5.5V at Topr = – 20 to 85°C/– 40 to 85°C(3))

Symbol	Parameter			Standard			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage (Through VDC)			3.0	5.0	5.5	V
	Supply voltage (Not through VDC)			3.0	3.3	3.6	V
AV_{CC}	Analog supply voltage				V_{CC}		V
V_{SS}	Supply voltage				0		V
AV_{SS}	Analog supply voltage				0		V
V_{IH}	Input high ("H") voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(4), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(5), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		0.8V_{CC}		V_{CC}	V
		$P7_0$, $P7_1$		0.8V_{CC}		6.0	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (In single-chip mode)		0.8V_{CC}		V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (In memory expansion mode and microprocesor mode)		0.5V_{CC}		V_{CC}	V
V_{IL}	Input low ("L") voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(4), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(5), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		0		0.2V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (In single-chip mode)		0		0.2V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (In memory expansion mode and microprocesor mode)		0		0.16V_{CC}	V
$I_{OH(peak)}$	Peak output high ("H") current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(5)				-10.0	mA
$I_{OH(avg)}$	Average output high ("H") current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(5)				-5.0	mA
$I_{OL(peak)}$	Peak output low ("L") current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(5)				10.0	mA
$I_{OL(avg)}$	Average output low ("L") current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(5)				5.0	mA
$f(X_{IN})$	Main clock input frequency	Through VDC	V_{CC}=4.2 to 5.5V	0		32	MHz
			V_{CC}=3.0 to 5.5V	0		20	MHz
		Not through VDC	V_{CC}=3.0 to 3.6V	0		20	MHz
$f(X_{CIN})$	Sub clock oscillation frequency				32.768	50	kHz

NOTES:

1. Output current is averaged with 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be less than or equal to 80mA.
   Total $I_{OH(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be less than or equal to -80mA.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be less than or equal to 80mA.
   Total $I_{OH(peak)}$ for P3, P4, P5, P6, $P7_2$ to $P7_7$, $P8_0$ to $P8_4$, P12 and P13 must be less than or equal to -80mA.
3. This is an option that is on request basis.
4. V_{IH} and V_{IL} reference for $P8_7$ applies to $P8_7$ used as a programmable input ports. It does not apply to $P8_7$ used as X_{CIN}.
5. P11 to P15 are provided in the 144-pin package only.

VCC = 5V

Table 5.3 Electrical Characteristics (VCC=4.2 to 5.5V, VSS=0V at Topr= –20 to 85°C, unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V_{OH}	Output high ("H") voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_{CC}=5V I_{OH}=-5mA	3.0			V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_{CC}=5V I_{OH}=-200µA	4.7			V
		X_{OUT}	V_{CC}=5V I_{OH}=-1mA	3.0			V
		X_{COUT}	No load applied		3.3		V
V_{OL}	Output low ("L") voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=5mA			2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=200µA			0.45	V
		X_{OUT}	I_{OL}=1mA			2.0	V
		X_{COUT}	No load applied		0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	Input high ("H") current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=V_{CC}			5.0	µA
I_{IL}	Input low ("L") current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_I=0V	30	50	167	kΩ
Rf_{XIN}	Feedback resistance	X_{IN}			1.5		MΩ
Rf_{XCIN}	Feedback resistance	X_{CIN}			10		MΩ
V_{RAM}	RAM standby voltage	Through VDC		2.5			V
I_{CC}	Power supply current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	$f(X_{IN})$=32 MHz, square wave, no division		28	54	mA
			$f(X_{CIN})$=32 kHz, with a wait state, Topr=25° C		470		µA
			Topr=25° C when the clock stops		0.4	20	µA

NOTES:
1. P11 to P15 are provided in the 144-pin package only.

VCC = 5V

Table 5.4 A-D Conversion Characteristics (VCC = AVCC = VREF = 4.2 to 5.5V, Vss = AVSS = 0V at Topr = –20 to 85°C, nless otherwise specified)

Symbol	Parameter	Measurement condition		Standard			Unit
				Min	Typ	Max	
-	Resolution	VREF=VCC				10	Bits
INL	Integral nonlinearity error	VREF=VCC=5V	AN0 to AN7 ANEX0, ANEX1			±3	LSB LSB
			External op-amp connection mode			±7	LSB LSB
DNL	Differential nonlinearity error					±1	LSB
-	Offset error					±3	LSB
-	Gain error					±3	LSB
RLADDER	Resistor ladder	VREF=VCC		8		40	kΩ
tCONV	10-bit conversion time			2.1			µs
tCONV	8-bit conversion time			1.8			µs
tSAMP	Sample time			0.3			µs
VREF	Reference voltage			2		VCC	V
VIA	Analog input voltage			0		VREF	V

NOTES:
1. Divide f(XIN), if exceeding 10 MHz, to keep ϕAD frequency less than or equal to 10 MHz.

Table 5.5 D-A Conversion Characteristics (VCC = VREF = 4.2 to 5.5V, VSS = AVSS = 0V at Topr = –20 to 85°C, unless otherwise specified)

Symbol	Parameter	Measurement condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute accuracy				1.0	%
tSU	Setup time				3	µs
RO	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(Note 1)			1.5	mA

NOTES:
1. Mesurement condition is that one of two D-A converters is used and the DAi register (i=0, 1) for the unused D-A converter to "00$_{16}$". The resistor ladder in the A-D converter is exclued. IVREF flows even if the ADiCON1 register is set to "0" (no VREF connection).

VCC = 5V

Timing Requirements (VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.6 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc	External clock input cycle time	31.3		ns
tw(H)	External clock input high ("H") pulse width	13		ns
tw(L)	External clock input low ("L") pulse width	13		ns
tr	External clock rising edge time		5	ns
tf	External clock falling edge time		5	ns

Table 5.7 Memory Expansion and Microprocessor Modes

Symbol	Parameter	Standard		Unit
		Min	Max	
tac1(RD-DB)	Data input access time (RD standard, with no wait state)		(Note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard, with no wait state)		(Note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, with a wait state)		(Note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, CS standard, with a wait state)		(Note 1)	ns
tac3(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac3(AD-DB)	Data input access time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac4(RAS-DB)	Data input access time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAS-DB)	Data input access time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAD-DB)	Data input access time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
tsu(DB-BCLK)	Data input setup time	26		ns
tsu(RDY-BCLK)	$\overline{RDY}$ input setup time	26		ns
tsu(HOLD-BCLK)	$\overline{HOLD}$ input setup time	30		ns
th(RD-DB)	Data input hold time	0		ns
th(CAS-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{RDY}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{HOLD}$ input hold time	0		ns
td(BCLK-HLDA)	$\overline{HLDA}$ output delay time		25	ns

NOTES:
1. A value can be obtained from the following expressions according to the BCLK frequecncy. Insert a wait state or use lower f(BCLK) as an operation frequency if a calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9}{f(BCLK) \times 2} - 35 \quad [ns]$$

$$t_{ac1(AD-DB)} = \frac{10^9}{f(BCLK)} - 35 \quad [ns]$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]\ (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times n}{f(BCLK)} - 35 \quad [ns]\ (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$t_{ac3(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]\ (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3(AD-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns]\ (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$t_{ac4(RAS-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]\ (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$t_{ac4(CAS-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns]\ (n=1 \text{ with 1 wait state and } n=3 \text{ when 2 wait states})$$

$$t_{ac4(CAD-DB)} = \frac{10^9 \times l}{f(BCLK)} - 35 \quad [ns]\ (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

VCC = 5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.8 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAiIN input cycle time	100		ns
tw(TAH)	TAiIN input high ("H") pulse width	40		ns
tw(TAL)	TAiIN input low ("L") pulse width	40		ns

Table 5.9 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAiIN input cycle time	400		ns
tw(TAH)	TAiIN input high ("H") pulse width	200		ns
tw(TAL)	TAiIN input low ("L") pulse width	200		ns

Table 5.10 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAiIN input cycle time	200		ns
tw(TAH)	TAiIN input high ("H") pulse width	100		ns
tw(TAL)	TAiIN input low ("L") pulse width	100		ns

Table 5.11 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(TAH)	TAiIN input high ("H") pulse width	100		ns
tw(TAL)	TAiIN input low ("L") pulse width	100		ns

Table 5.12 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high ("H") pulse width	1000		ns
tw(UPL)	TAiOUT input low ("L") pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

VCC = 5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.13 Timer B Input (Count Source Input in eEvent Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input high ("H") pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input low ("L") pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input high ("H") pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input low ("L") pulse width (counted on both edges)	80		ns

Table 5.14 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high ("H") pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low ("L") pulse width	200		ns

Table 5.15 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high ("H") pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low ("L") pulse width	200		ns

Table 5.16 A-D trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ input high ("H") pulse width (trigger available at minimum)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input low ("L") pulse width	125		ns

Table 5.17 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high ("H") pulse width	100		ns
$t_{w(CKL)}$	CLKi input low ("L") pulse width	100		ns
$t_{d(C-Q)}$	TxDi output delay time		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input hold time	30		ns
$t_{h(C-Q)}$	RxDi input hold time	90		ns

Table 5.18 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(INH)}$	$\overline{INTi}$ input high ("H") pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input low ("L") pulse width	250		ns

VCC = 5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.19 Memory Expansion Mode and Microprocessor Mode (with No Wait State)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address output hold time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address output hold time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select signal output delay time			18	ns
$t_{h(BCLK-CS)}$	Chip-select signal output hold time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-select signal output hold time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-select signal output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			18	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-2		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			18	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		-5		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			18	ns
$t_{d(BCLK-WR)}$	WR signal outpu hold time		-3		ns
$t_{d(DB-WR)}$	Data output delay time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data outpu hold time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	Write pulse width		(Note 1)		ns

NOTES:
1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{w(WR)} = \frac{10^9}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$

VCC = 5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.20 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address output hold time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address output hold time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select signal output delay time			18	ns
$t_{h(BCLK-CS)}$	Chip-select signal output hold time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-select signal output hold time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-select signal output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			18	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-2		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			18	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		-5		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			18	ns
$t_{d(BCLK-WR)}$	WR signal outpu hold time		-3		ns
$t_{d(DB-WR)}$	Data output delay time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data outpu hold time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	Write pulse width		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9 \times n}{f_{(BCLK)}} - 20 \quad [ns]$$ (n=1 with 1 wait state, n=2 with 2 wait states and n=3 with 3 wait states)

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$ (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

VCC = 5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.21 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)		(Note 1)		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-AD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
td(BCLK-WR)	WR signal output hold time		-3		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(DB-WR)	Data output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		-2		ns
td(AD-ALE)	ALE signal output delay time (address standard)		(Note 1)		ns
th(ALE-AD)	ALE signal output hold time (address standard)		(Note 1)		ns
tdz(RD-AD)	Address output high-impedance time			8	ns

NOTES:
1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{h(RD-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(RD-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{d(AD-ALE)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(ALE-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

VCC = 5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.22 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory and Selecting the DRAM Area)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
$td_{(BCLK-AD)}$	Row address output delay time	See Figure 5.1		18	ns
$th_{(BCLK-AD)}$	Row address output hold time (BCLK standard)		-3		ns
$th_{(BCLK-CAD)}$	Column address output delay time			18	ns
$td_{(BCLK-CAD)}$	Column address output hold time (BCLK standard)		-3		ns
$th_{(RAS-RAD)}$	Row address output hold time after RAS output		(Note 1)		ns
$td_{(BCLK-RAS)}$	RAS output delay time (BCLK standard)			18	ns
$th_{(BCLK-RAS)}$	RAS output hold time (BCLK standard)		-3		ns
t_{RP}	RAS high ("H") hold time		(Note 1)		ns
$td_{(BCLK-CAS)}$	CAS output delay time (BCLK standard)			18	ns
$th_{(BCLK-CAS)}$	CAS output hold time (BCLK standard)		-3		ns
$td_{(BCLK-DW)}$	DW output delay time (BCLK standard)			18	ns
$th_{(BCLK-DW)}$	DW output hold time (BCLK standard)		-5		ns
$tsu_{(DB-CAS)}$	CAS output setup time after DB output		(Note 1)		ns
$th_{(BCLK-DB}$	DB signal output hold time (BCLK standard)		-7		ns
$tsu_{(CAS-RAS)}$	CAS output setup time before RAS output (refresh)		(Note 1)		ns

NOTES:

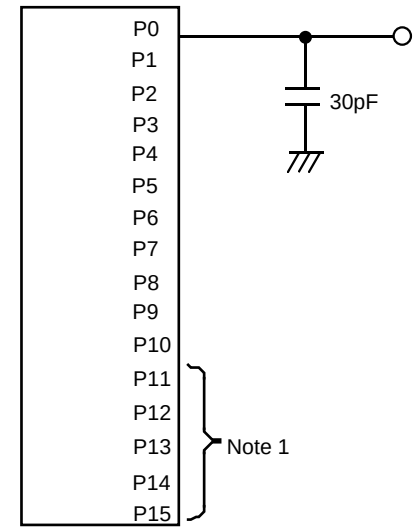
1. A value can be obtained from the following expressions according to the BCLK frequency.

$$th_{(RAS-RAD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

$$t_{RP} = \frac{10^9}{f_{(BCLK)} \times 2} \times 3 - 20 \quad [ns]$$

$$tsu_{(DB-CAS)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$tsu_{(CAS-RAS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$



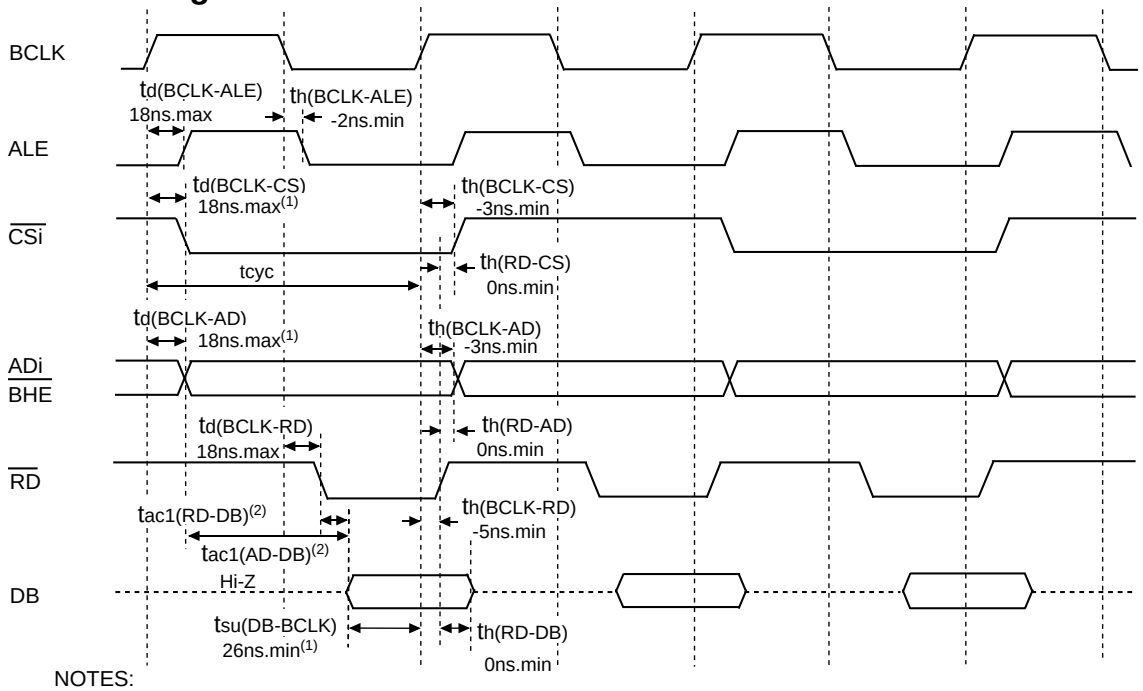
NOTES:
1. P11 to P15 are provided in the 144-pin package only.

Figure 5.1 P0 to P15 Measurement Circuit

Vcc=5V

Memory expansion mode and microprocessor mode (with no wait state)

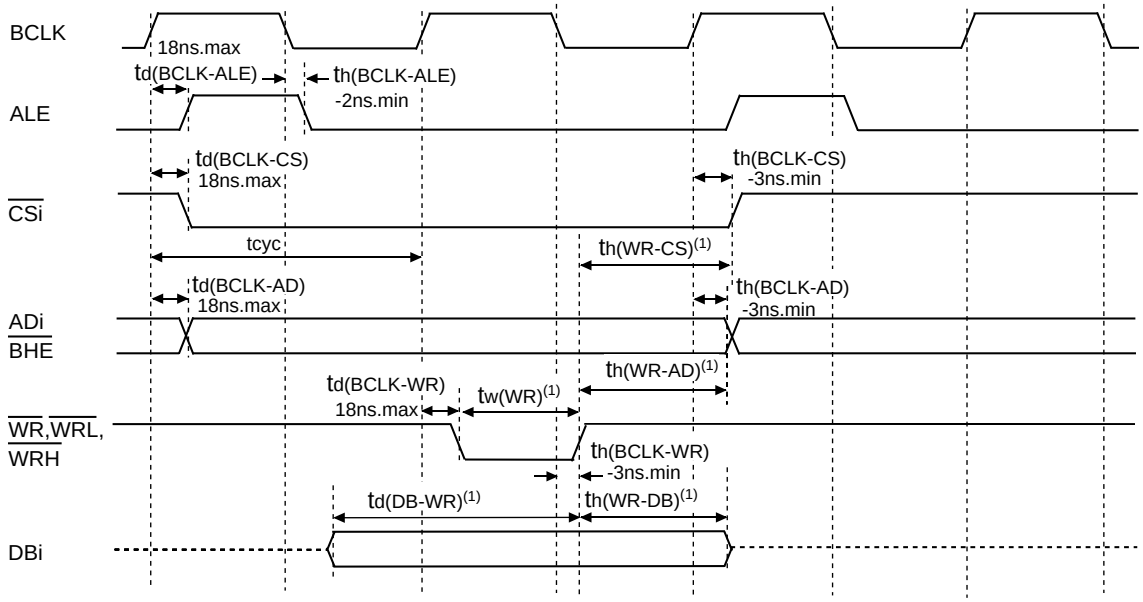
Read timing



NOTES:

1. A value is guaranteed with no external factor. Maximum 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. It varies with the operation frequency.
   $t_{ac1(RD-DB)}$=(tcyc/2-35)ns.max
   $t_{ac1(AD-DB)}$=(tcyc-35)ns.max

Write timing (written in 2 cycles with no wait state)



NOTES:

1. It varies with the operation frequency.
   $t_{d(DB-WR)}$=(tcyc-20)ns.min
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2-15)ns.min

Measurement conditions

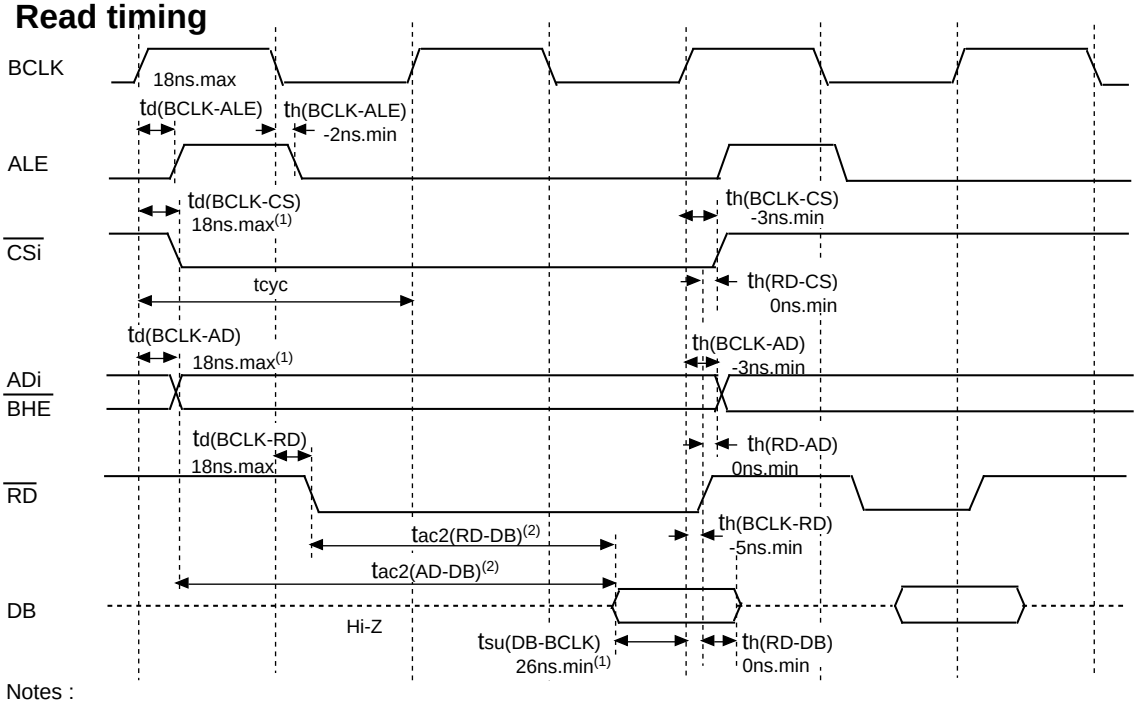
- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 5.2 Vcc=5V Timing Diagram (1)

Vcc=5V

Memory expansion mode and microprocessor mode (with a wait state)

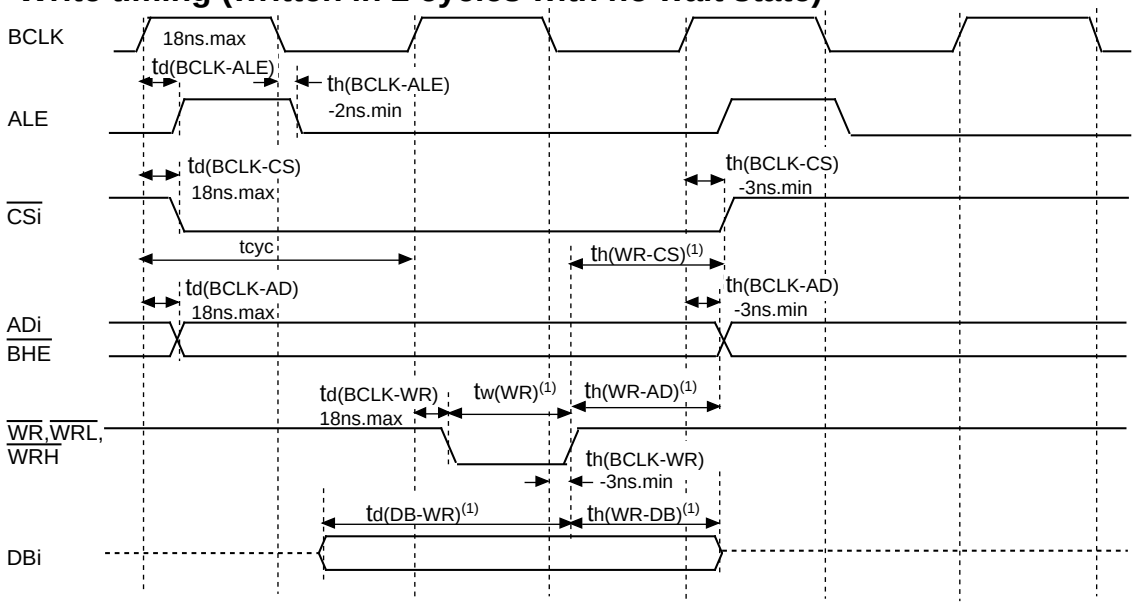
Read timing



Notes :

1. A value is guaranteed with no external factor. Maximum 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. It varies with the operation frequency.
   $t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state, m=5 with 2 wait states and m=7 with 3 wait states.)
   $t_{ac2(AD-DB)}$=(tcyc x n-35)ns.max (n=2 with 1 wait state, n=3 with 2 wait states and n=4 with 3 wait states.)

Write timing (written in 2 cycles with no wait state)



NOTES:

1. It varies with the operation frequency.
   $t_{d(DB-WR)}$=(tcyc x n-20)ns.min
   (n=1 with 1 wait state, n=2 with 2 wait states and n=3 with 3 wait states)
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2 x n-15)ns.min
   (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

Measurement conditions
- V_{CC}=4.2 to 5.5V
- Input high and low voltage:
  V_{IH}=2.5V, V_{IL}=0
- Output high and low voltage:
  V_{OH}=2.0V, V_{OL}=0.8V

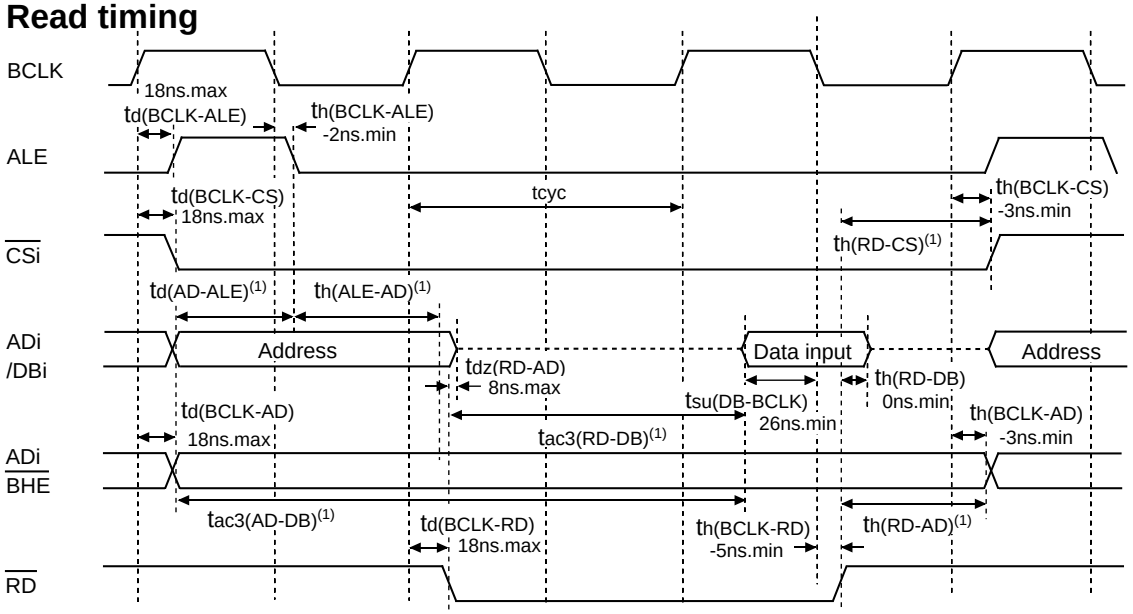
Figure 5.3 Vcc=5V Timing Diagram (2)

Memory expansion mode and microprocessor mode

Vcc=5V

(with a wait state, when accessing an external memory and using the multiplexed bus)

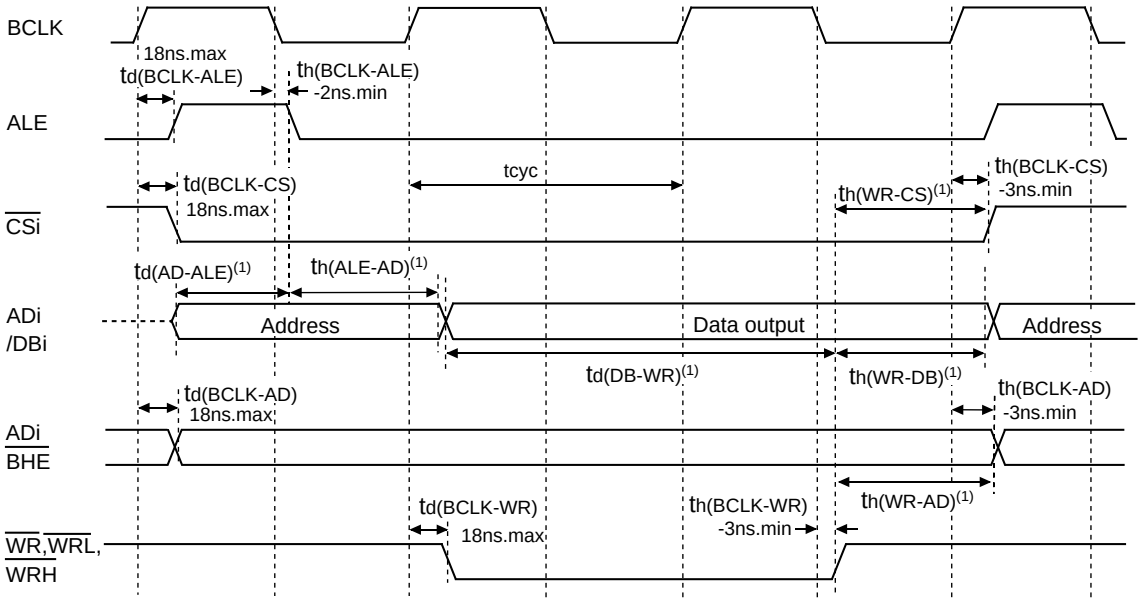
Read timing



NOTES:

1. It varies with the operation frequency.
   td(AD-ALE)=(tcyc/2-20)ns.min
   th(ALE-AD)=(tcyc/2-10)ns.min, th(RD-AD)=(tcyc/2-10)ns.min, th(RD-CS)=(tcyc/2-10)ns.min
   tac3(RD-DB)=(tcyc/2 x m-35)ns.max (m=3 with 2 wait states and m=5 with 3 wait states)
   tac3(AD-DB)=(tcyc/2 x n-35)ns.max (n=5 with 2 wait states and n=7 with 3 wait states)

Write timing (written in 2 cycles with no wait state)



NOTES:

1. It varies with the operation frequency.
   td(AD-ALE)=(tcyc/2-20)ns.min
   th(ALE-AD)=(tcyc/2-10)ns.min, th(WR-AD)=(tcyc/2-10)ns.min
   th(WR-CS)=(tcyc/2-10)ns.min, th(WR-DB)=(tcyc/2-10)ns.min
   td(DB-WR)=(tcyc/2 x m-25)ns.min

Measurement conditions

- Vcc=4.2 to 5.5V
- Input high and low voltage:
  VIH=2.5V, VIL=0.8V
- Output high and low voltage:
  VOH=2.0V, VOL=0.8V

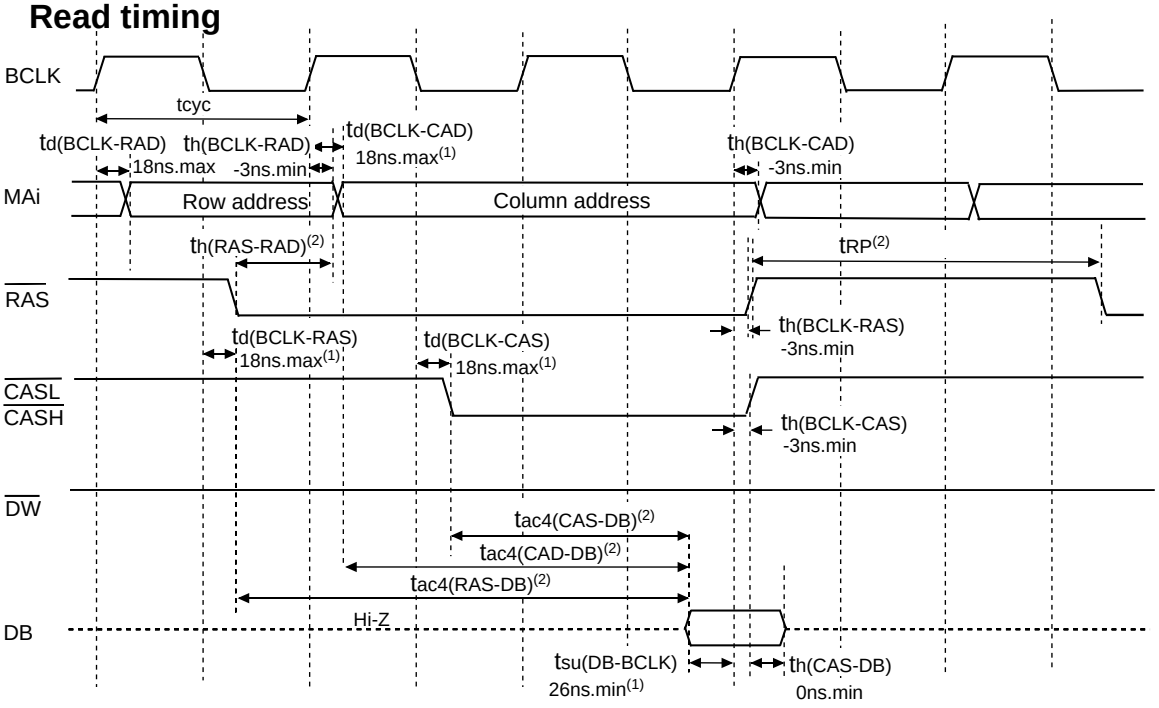
Figure 5.4 Vcc=5V Timing Diagram (3)

Memory expansion mode and microprocessor mode

Vcc=5V

(When accessing the DRAM area)

Read timing



NOTES:

1. A value is guaranteed with no external factor. Maximum 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
   - $t_{d(BCLK-RAS)} + t_{su(DB-BCLK)}$
   - $t_{d(BCLK-CAS)} + t_{su(DB-BCLK)}$
   - $t_{d(BCLK-CAD)} + t_{su(DB-BCLK)}$
2. It varies with the operation frequency.
   - $t_{ac4(RAS-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state and m=5 with 2 wait states)
   - $t_{ac4(CAS-DB)}$=(tcyc/2 x n-35)ns.max (n=1 with 1 wait state and n=3 with 2 wait states)
   - $t_{ac4(CAD-DB)}$=(tcyc x l-35)ns.max (l=1 with 1 wait state and l=2 with 2 wait states)
   - $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   - t_{RP}=(tcyc/2 x 3-20)ns.min

Measurement conditions

- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

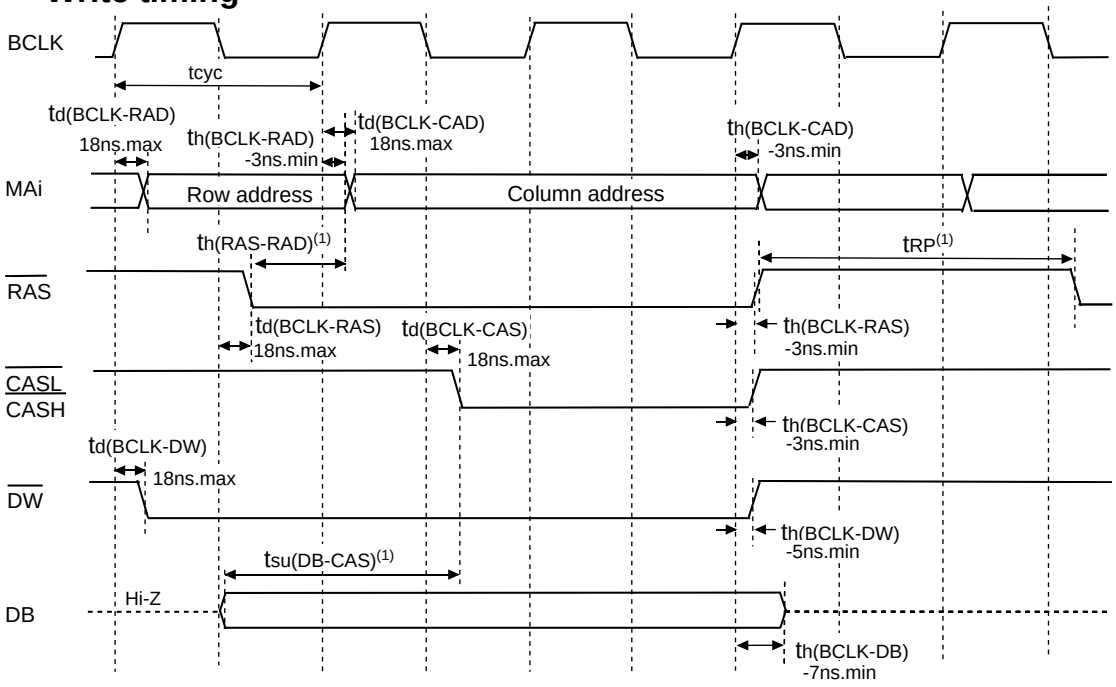
Figure 5.5 V_{CC}=5V Timing Diagram (4)

Memory expansion mode and microprocessor mode

Vcc=5V

(When accessing the DRAM area)

Write timing



NOTES:

1. It varies with the operation frequency.
   $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   t_{RP}=(tcyc/2 x 3-20)ns.min
   $t_{su(DB-CAS)}$=(tcyc-20)ns.min

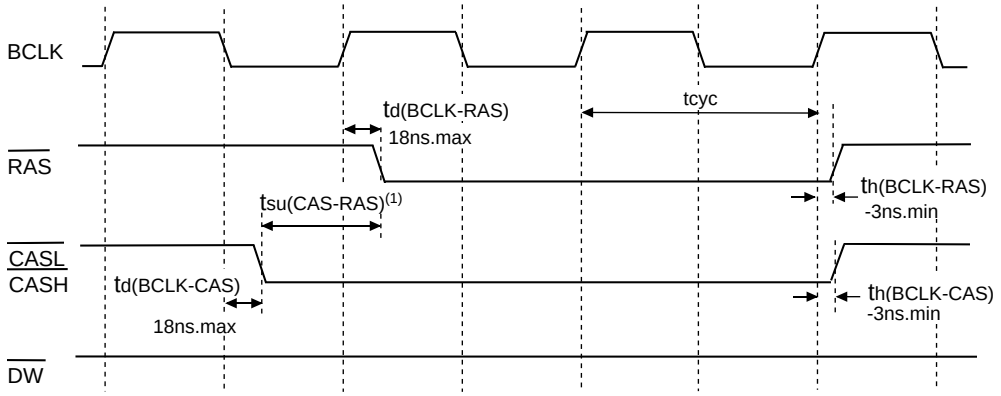
Measurement conditions

- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 5.6 V_{CC}=5V Timing Diagram (5)

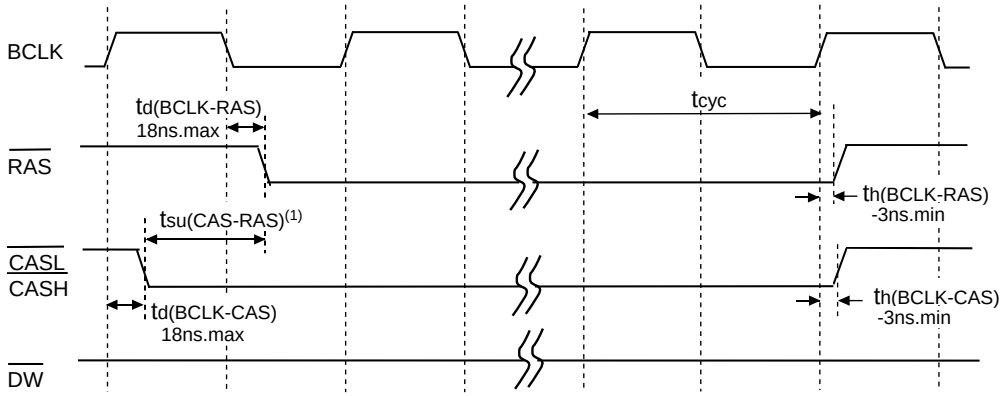
Memory expansion mode and microprocessor mode Vcc=5V

Refresh timing (CAS-before-RAS refresh)



NOTES :
1. It varies with the operation frequency.
$t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Refresh timing (Self-refresh)



NOTES:
1. It varies with the operation frequency.
$t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Measurement conditions
- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 5.7 Vcc=5V Timing Diagram (6)

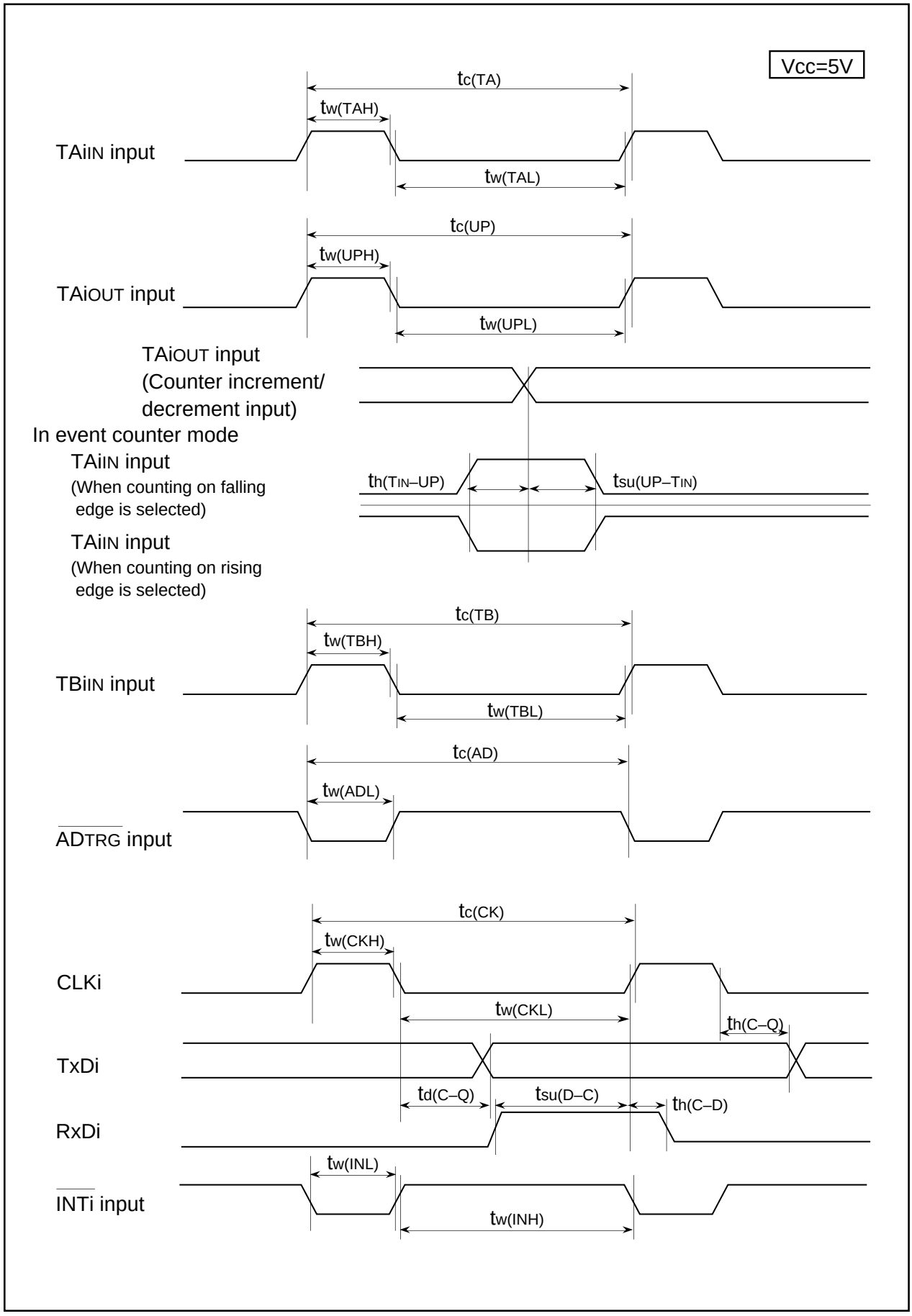
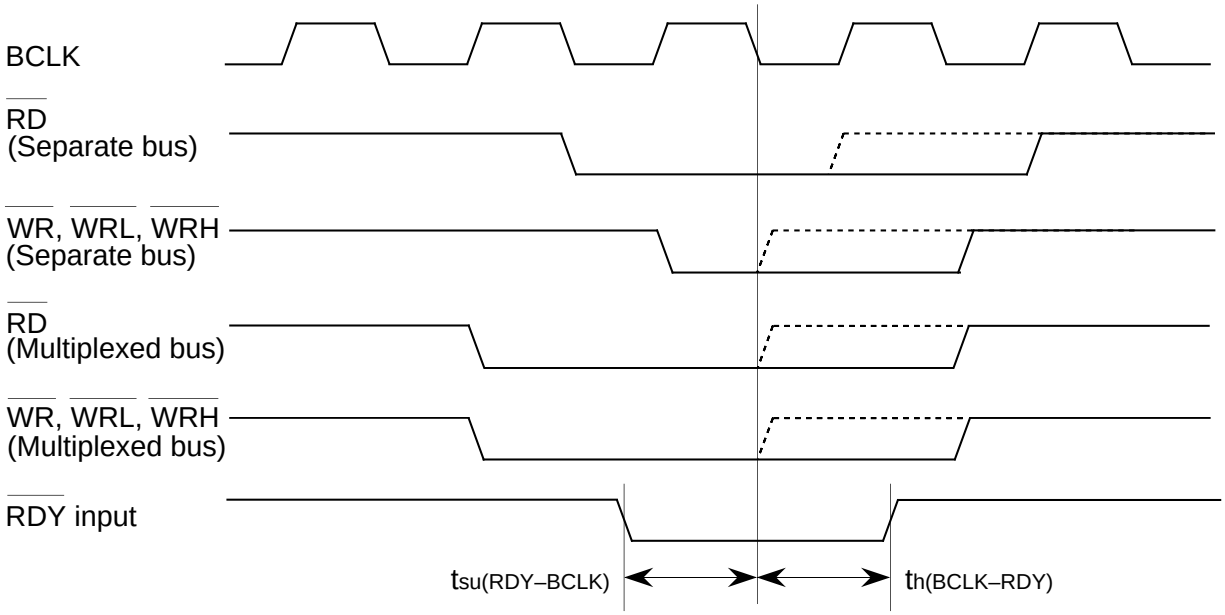


Figure 5.8 Vcc=5V Timing Diagram (7)

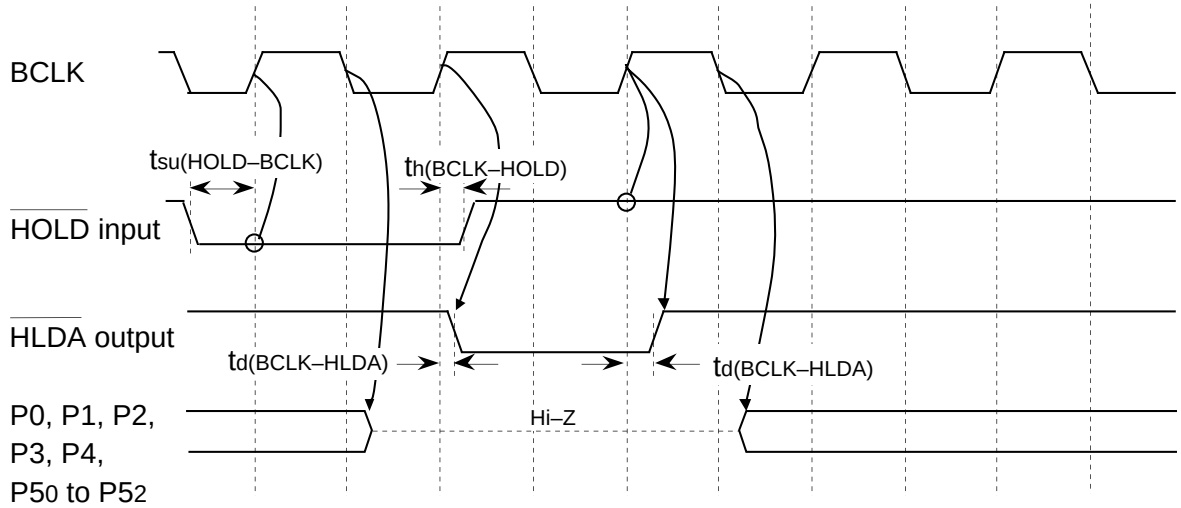
Vcc=5V

Memory expansion mode and microprocessor mode

(Valid only with a wait state)



(Valid with a wait state or with no wait state)



Measurement conditions
- VCC=4.2 to 5.5V
- Input high and low voltage: VIH=4.0V, VIL=1.0V
- Output high and low voltage: VOH=2.5V, VOL=2.5V

Figure 5.9 Vcc=5V Timing Diagram (8)

V_{CC} = 3.3V

Table 5.23 Electrical Characteristics (V_{CC}=3.0 to 3.6V, V_{SS}=0V at Topr = –20 to 85°C, unless otherwise specified)

Symbol	Parameter			Condition	Standard			Unit
					Min	Typ	Max	
V_{OH}	Output high ("H") voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OH}=-1mA	2.7			V
		X_{OUT}		I_{OH}=-0.1mA	2.7			V
		X_{COUT}		No load applied		3.3		V
V_{OL}	Output low ("L") voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OL}=1mA			0.5	V
		X_{OUT}		I_{OL}=0.1mA			0.5	V
		X_{COUT}		No load applied		0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4			0.2		1.0	V
		$\overline{RESET}$			0.2		1.8	V
I_{IH}	Input high ("H") current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		V_I=V_{CC}			4.0	µA
I_{IL}	Input low ("L") current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		V_I=0V			-4.0	µA
R_{PULLUP}	Pull-up resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		V_I=0V	66	120	500	kΩ
Rf_{XIN}	Feedback resistance	X_{IN}				3.0		MΩ
Rf_{XCIN}	Feedback resistance	X_{CIN}				20.0		MΩ
V_{RAM}	RAM standby voltage	Through VDC			2.5			V
		Not through VDC			2.0			
I_{CC}	Power supply current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(X_{IN})=20 MHz, square wave, no division			17	38	mA
			f(X_{CIN})=32 kHz, with a wait state, not through VDC, Topr=25° C			5.0		µA
			f(X_{CIN})=32 kHz, with a wait state, through VDC, Topr=25° C			340		µA
			Topr=25° C when the clock stops			0.4	20	µA

NOTES:
1. P11 to P15 are provided in the 144-pin package only.

V_{CC} = 3.3V

Table 5.24 A-D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 3.0 to 3.6V, V_{SS} = AV_{SS} = 0V at Topr = –20 to 85°C, unless otherwise specified)

Symbol	Parameter		Measurement condition	Standard			Unit
				Min	Typ	Max	
-	Resolution		V_{REF}=V_{CC}			10	Bits
INL	Integral nonlinearity error	No S&H function (8-bit)	V_{CC}=V_{REF}=3.3V			±2	LSB
DNL	Differential nonlinearity error	No S&H function (8-bit)				±1	LSB
-	Offset error	No S&H function (8-bit)				±2	LSB
-	Gain error	No S&H function (8-bit)				±2	LSB
R_{LADDER}	Resistor ladder		V_{REF}=V_{CC}	8		40	kΩ
t_{CONV}	8-bit conversion time			4.9			µs
V_{REF}	Reference voltage			3.0		V_{CC}	V
V_{IA}	Analog input voltage			0		V_{REF}	V

S&H: Sample and hold

NOTES:
1. Divide f(X_{IN}), if exceeding 10 MHz, to keep ϕAD frequency less than or equal to 10 MHz.

Table 5.25 D-A Conversion Characteristics (V_{CC} = V_{REF} = 3.0 to 3.6V, V_{SS} = AV_{SS} = 0V at Topr = –20 to 85°C, unless otherwise specified)

Symbol	Parameter	Measurement condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute accuracy				1.0	%
t_{SU}	Setup time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference power supply input current	(Note 1)			1.0	mA

NOTES:
1. Mesurement condition is that one of two D-A converters is used and the DAi register (i=0, 1) for the unused D-A converter to "00_{16}". The resistor ladder in the A-D converter is exclued. I_{VREF} flows even if the ADiCON1 register is set to "0" (no V_{REF} connection).

VCC = 3.3V

Timing Requirements (Vcc = 3.0 to 3.6V, Vss = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.26 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc	External clock input cycle time	50		ns
tw(H)	External clock input high ("H") pulse width	22		ns
tw(L)	External clock input low ("L") pulse width	22		ns
tr	External clock rising-edge time		5	ns
tf	External clock falling-edge time		5	ns

Table 5.27 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min	Max	
tac1(RD-DB)	Data input access time (RD standard, with no wait state)		(Note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard, with no wait state)		(Note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, with a wait state)		(Note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, CS standard, with a wait state)		(Note 1)	ns
tac3(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac3(AD-DB)	Data input access time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac4(RAS-DB)	Data input access time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAS-DB)	Data input access time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAD-DB)	Data input access time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
tsu(DB-BCLK)	Data input setup time	30		ns
tsu(RDY-BCLK)	$\overline{RDY}$ input setup time	40		ns
tsu(HOLD-BCLK)	$\overline{HOLD}$ input setup time	60		ns
th(RD-DB)	Data input hold time	0		ns
th(CAS-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{RDY}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{HOLD}$ input hold time	0		ns
td(BCLK-HLDA)	$\overline{HLDA}$ output delay time		25	ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequecncy. Insert a wait state or use lower f(BCLK) as an operation frequency if a calculated value is negative.

$$tac1(RD-DB) = \frac{10^9}{f(BCLK) \times 2} - 35 \quad [ns]$$

$$tac1(AD-DB) = \frac{10^9}{f(BCLK)} - 35 \quad [ns]$$

$$tac2(RD-DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35$$ [ns] (m=3 with 1 wait state, m=5 with 2 wait states and m=7 with 3 wait states)

$$tac2(AD-DB) = \frac{10^9 \times n}{f(BCLK)} - 35$$ [ns] (n=2 with 1 wait state, n=3 with 2 wait states and n=4 with 3 wait states)

$$tac3(RD-DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35$$ [ns] (m=3 with 2 wait states and m=5 with 3 wait states)

$$tac3(AD-DB) = \frac{10^9 \times n}{f(BCLK) \times 2} - 35$$ [ns] (n=5 with 2 wait states and n=7 with 3 wait states)

$$tac4(RAS-DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35$$ [ns] (m=3 with 1 wait state and m=5 with 2 wait states)

$$tac4(CAS-DB) = \frac{10^9 \times n}{f(BCLK) \times 2} - 35$$ [ns] (n=1 with 1 wait state and n=3 when 2 wait states)

$$tac4(CAD-DB) = \frac{10^9 \times l}{f(BCLK)} - 35$$ [ns] (l=1 with 1 wait state and l=2 with 2 wait states)

VCC = 3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.28 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} input cycle time	100		ns
$t_{w(TAH)}$	TAi_{IN} input high ("H") pulse width	40		ns
$t_{w(TAL)}$	TAi_{IN} input low ("L") pulse width	40		ns

Table 5.29 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} input cycle time	400		ns
$t_{w(TAH)}$	TAi_{IN} input high ("H") pulse width	200		ns
$t_{w(TAL)}$	TAi_{IN} input low ("L") pulse width	200		ns

Table 5.30 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} input cycle time	200		ns
$t_{w(TAH)}$	TAi_{IN} input high ("H") pulse width	100		ns
$t_{w(TAL)}$	TAi_{IN} input low ("L") pulse width	100		ns

Table 5.31 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(TAH)}$	TAi_{IN} input high ("H") pulse width	100		ns
$t_{w(TAL)}$	TAi_{IN} input low ("L") pulse width	100		ns

Table 5.32 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(UP)}$	TAi_{OUT} input cycle time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} input high ("H") pulse width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} input low ("L") pulse width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} input setup time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} input hold time	400		ns

VCC = 3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.33 Timer B input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} input high ("H") pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} input low ("L") pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} input high ("H") pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} input low ("L") pulse width (counted on both edges)	80		ns

Table 5.34 Timer B input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} input cycle time	400		ns
$t_{w(TBH)}$	TBi_{IN} input high ("H") pulse width	200		ns
$t_{w(TBL)}$	TBi_{IN} input low ("L") pulse width	200		ns

Table 5.35 Timer B input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} input cycle time	400		ns
$t_{w(TBH)}$	TBi_{IN} input high ("H") pulse width	200		ns
$t_{w(TBL)}$	TBi_{IN} input low ("L") pulse width	200		ns

Table 5.36 A-D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ input high ("H") pulse width (trigger available at minimum)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input low ("L") pulse width	125		ns

Table 5.37 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high ("H") pulse width	100		ns
$t_{w(CKL)}$	CLKi input low ("L") pulse width	100		ns
$t_{d(C-Q)}$	TxDi output delay time		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input hold time	30		ns
$t_{h(C-Q)}$	RxDi input hold time	90		ns

Table 5.38 External Interrupt $\overline{INTi}$ input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(INH)}$	$\overline{INTi}$ input high ("H") pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input low ("L") pulse width	250		ns

VCC = 3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C, unless otherwise specified)

Table 5.39 Memory Expansion Mode and Microprocessor Mode (with No Wait State)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address output hold time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address output hold time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select signal output delay time			18	ns
$t_{h(BCLK-CS)}$	Chip-select signal output hold time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-select signal output hold time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-select signal output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			18	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-2		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			18	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		-3		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			18	ns
$t_{d(BCLK-WR)}$	WR signal outpu hold time		0		ns
$t_{d(DB-WR)}$	Data output delay time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data outpu hold time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR output width		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9}{f(BCLK)} - 20 \quad [ns]$$

$$t_{h(WR-DB)} = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$t_{w(WR)} = \frac{10^9}{f(BCLK) \times 2} - 15 \quad [ns]$$

VCC = 3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.40 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address output hold time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address output hold time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select signal output delay time			18	ns
$t_{h(BCLK-CS)}$	Chip-select signal output hold time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-select signal output hold time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-select signal output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			18	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-2		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			18	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		-3		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			18	ns
$t_{d(BCLK-WR)}$	WR signal outpu hold time		0		ns
$t_{d(DB-WR)}$	Data output delay time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data outpu hold time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR output width		(Note 1)		ns

NOTES:
1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9 \times n}{f_{(BCLK)}} - 20 \quad [ns]$$ (n=1 with 1 wait state, n=2 with 2 wait states and n=3 with 3 wait states)

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$ (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

VCC = 3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.41 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		0		ns
th(RD-AD)	Address output hold time (RD standard)		(Note 1)		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		0		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-AD)	RD signal output hold time		-3		ns
td(BCLK-WR)	WR signal output delay time			18	ns
td(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(DB-WR)	Data output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		-2		ns
td(AD-ALE)	ALE signal output delay time (address standard)		(Note 1)		ns
th(ALE-AD)	ALE signal output hold time (address standard)		(Note 1)		ns
tdz(RD-AD)	Address output high-impedance time			8	ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$th(RD-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(AD-ALE) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

$$th(ALE-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

VCC = 3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.42 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory and Selecting the DRAM Area)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Row address output delay time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Row address output hold time (BCLK standard)		0		ns
$t_{h(BCLK-CAD)}$	Column address output delay time			18	ns
$t_{d(BCLK-CAD)}$	Column address output hold time (BCLK standard)		0		ns
$t_{h(RAS-RAD)}$	Row address output hold time after RAS output		(Note 1)		ns
$t_{d(BCLK-RAS)}$	RAS output delay time (BCLK standard)			18	ns
$t_{h(BCLK-RAS)}$	RAS output hold time (BCLK standard)		0		ns
t_{RP}	RAS high ("H") hold time		(Note 1)		ns
$t_{d(BCLK-CAS)}$	CAS output delay time (BCLK standard)			18	ns
$t_{h(BCLK-CAS)}$	CAS output hold time (BCLK standard)		0		ns
$t_{d(BCLK-DW)}$	DW output delay time (BCLK standard)			18	ns
$t_{h(BCLK-DW)}$	DW output hold time (BCLK standard)		-3		ns
$t_{su(DB-CAS)}$	CAS output setup time after DB output		(Note 1)		ns
$t_{h(BCLK-DB}$	DB signal output hold time (BCLK standard)		-7		ns
$t_{su(CAS-RAS)}$	CAS output setup time before RAS output (refresh)		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{h(RAS-RAD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

$$t_{RP} = \frac{10^9 \times 3}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

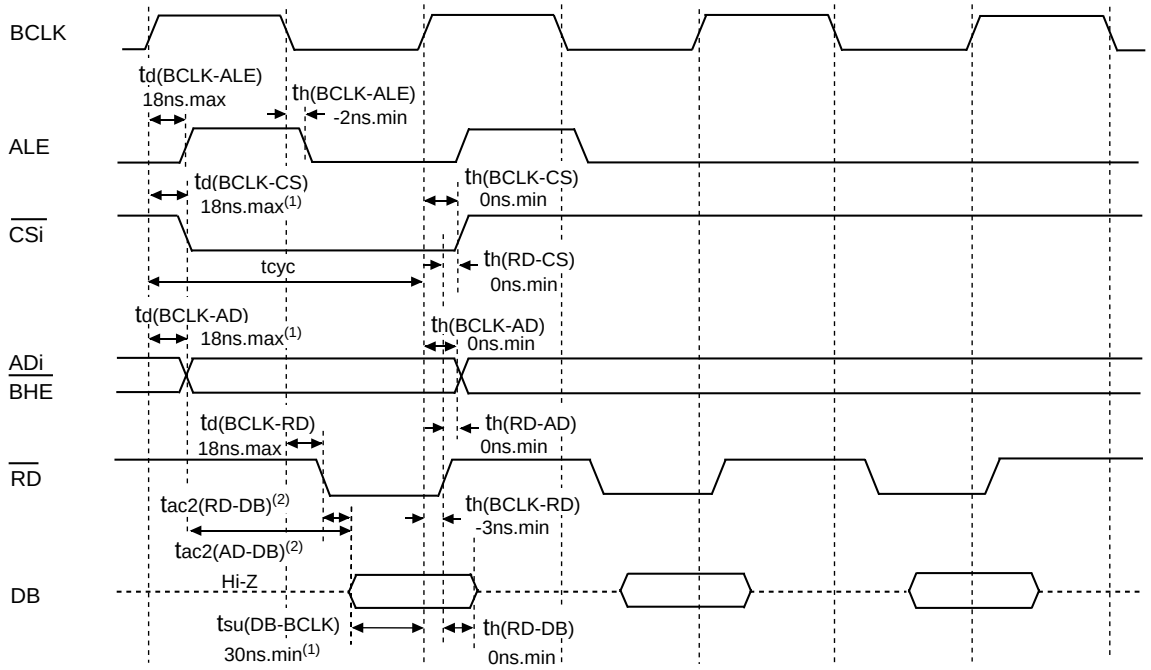
$$t_{su(DB-CAS)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{su(CAS-RAS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

Vcc=3.3V

Memory expansion mode and microprocessor mode (with no wait state)

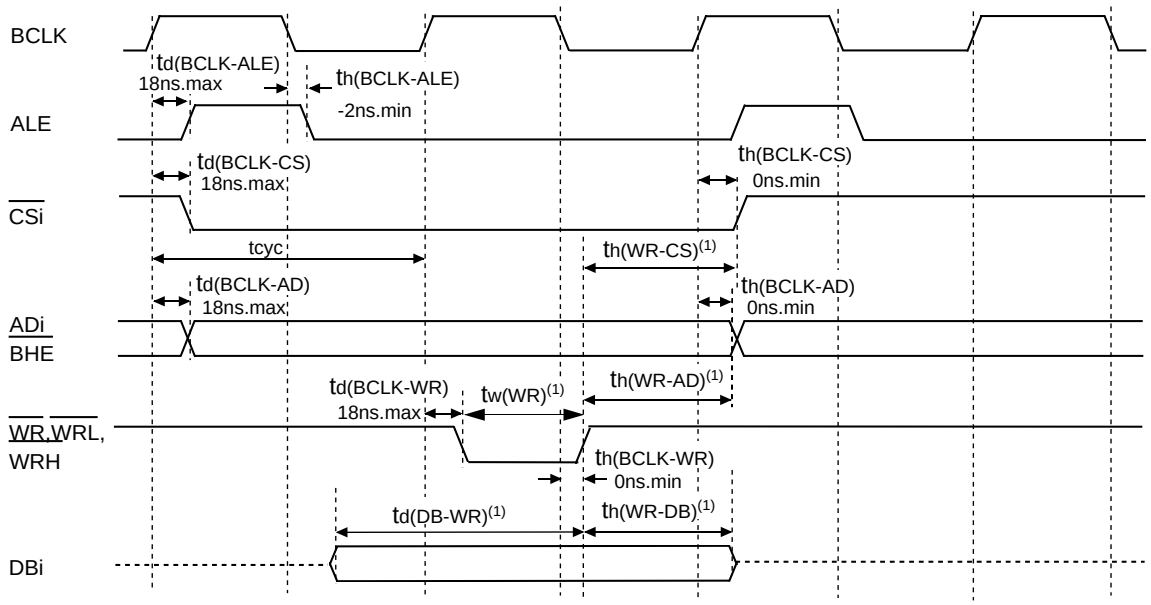
Read timing



NOTES:

1. A value is guarantee with no external factor. Maximum 35ns is garanteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. It varies with the operation frequency.
   $t_{ac2(RD-DB)}$=(tcyc/2-35)ns.max
   $t_{ac2(AD-DB)}$=(tcyc-35)ns.max

Write timing



NOTES:

1. It varies with the operation frequency.
   $t_{d(DB-WR)}$=(tcyc-20)ns.min
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2-15)ns.min

Measurement conditions

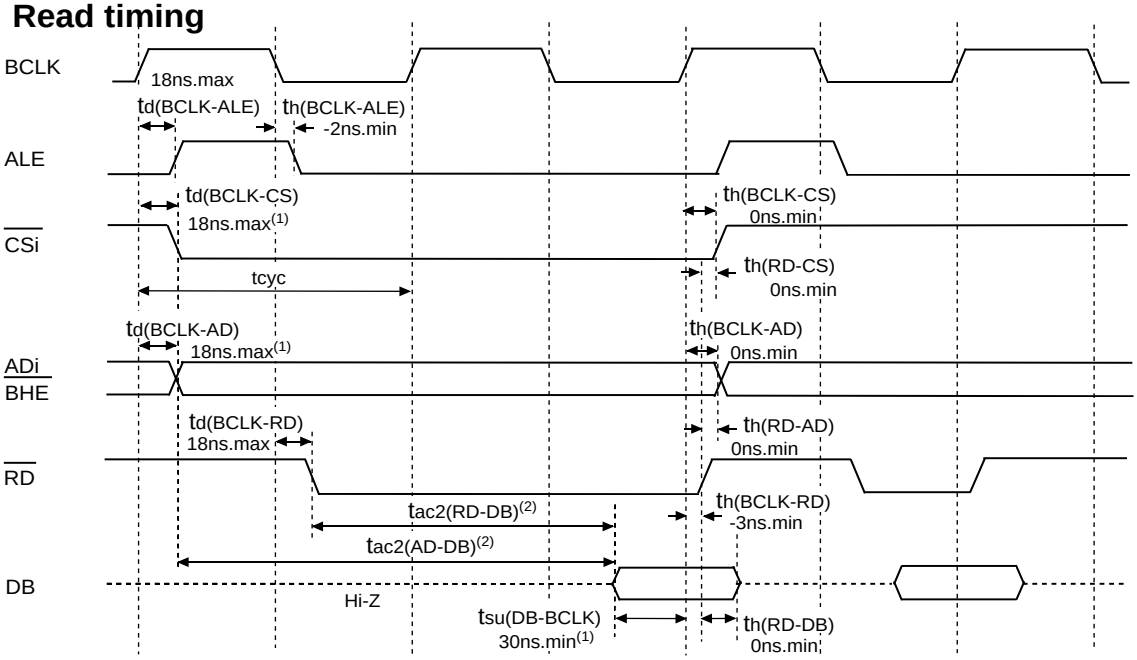
- VCC=3.0 to 3.6V
- Input high and low voltage: VIH=1.5V, VIL=0.5V
- Output high and low voltage: VOH=1.5V, VOL=1.5V

Figure 5.10 VCC=3.3V Timing Diagram (1)

Vcc=3.3V

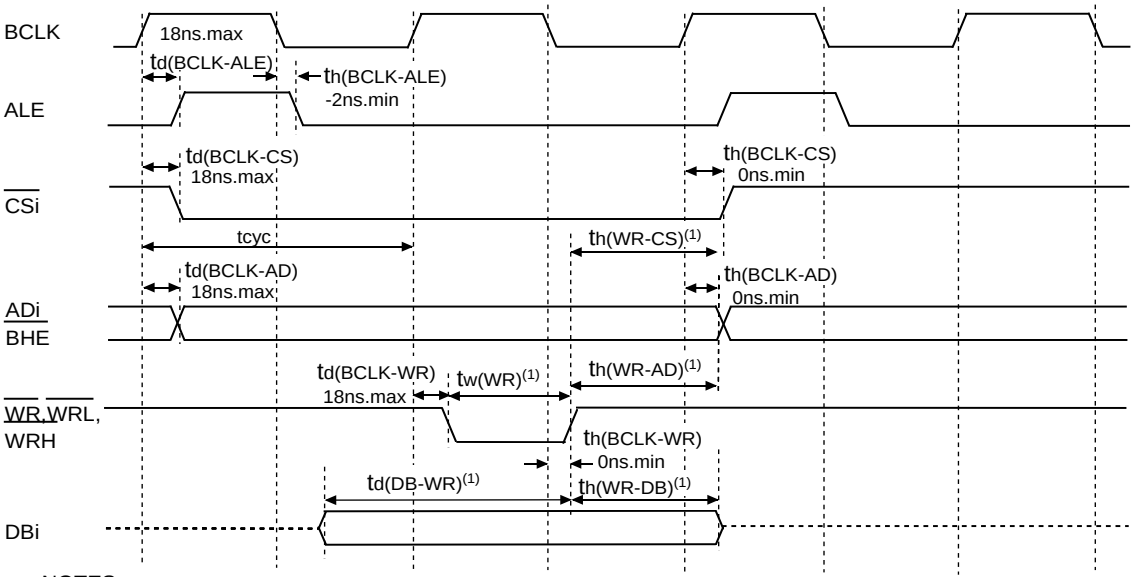
Memory expansion mode and microprocessor mode (with a wait state)

Read timing



NOTES:
1. A value is guarantee with no external factor. Maximum 35ns is garanteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. It varies with the operation frequency.
   $t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state, m=5 with 2 wait states and m=7 with 3 wait states)
   $t_{ac2(AD-DB)}$=(tcyc x n-35)ns.max (n=2 with 1 wait state, n=3 with 2 wait states and n=4 with 3 wait states)

Write timing



NOTES:
1. It varies with the operation frequency.
   $t_{d(DB-WR)}$=(tcyc x n-20)ns.min
   (n=1 when 1 wait, n=2 with 2 wait states and n=3 with 3 wait states)
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2 x n-15)ns.min
   (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

Measurement conditions
- V_{CC}=3.0 to 3.6V
- Input high and low voltage:
  V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
  V_{OH}=1.5V, V_{OL}=1.5V

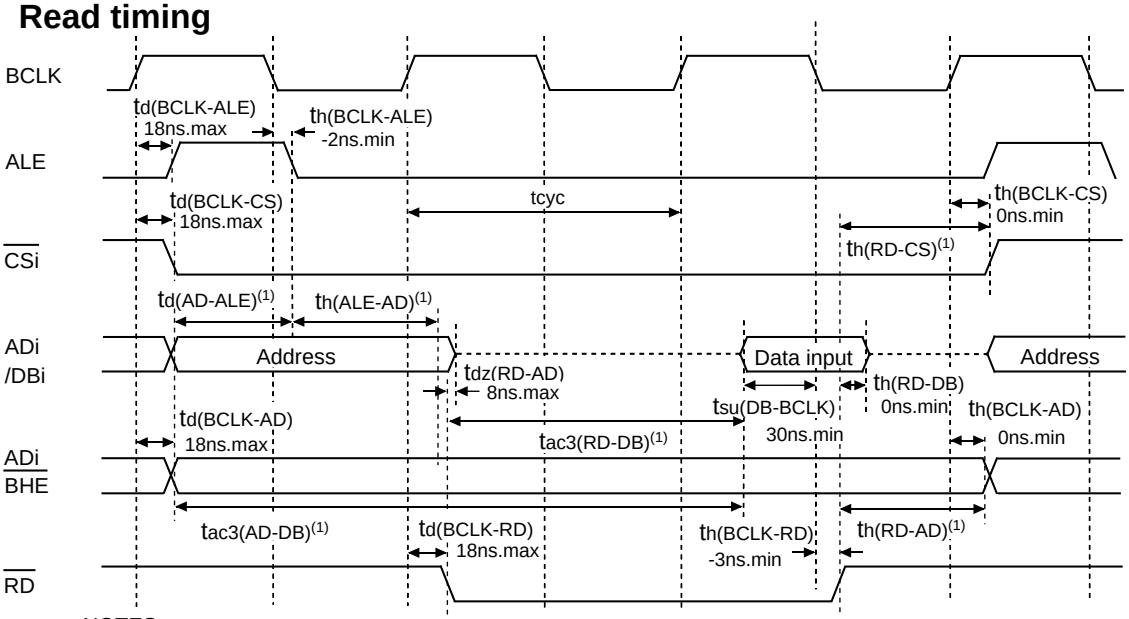
Figure 5.11 V_{CC}=3.3V Timing Diagram (2)

Memory expansion mode and microprocessor mode

Vcc=3.3V

(with a wait state, when accessing an external memory and using the multiplexed bus)

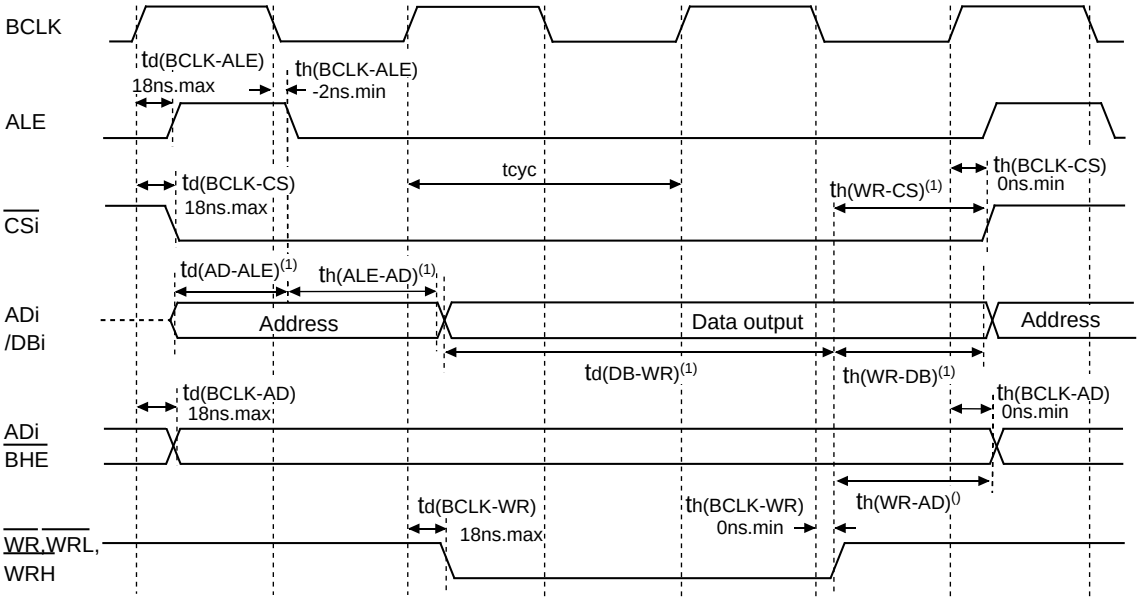
Read timing



NOTES:

1. It varies with the operation frequency.
   $t_{d(AD-ALE)}$=(tcyc/2-20)ns.min
   $t_{h(ALE-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min
   $t_{ac3(RD-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 2 wait states and m=5 with 3 wait states)
   $t_{ac3(AD-DB)}$=(tcyc/2 x n-35)ns.max (n=5 with 2 wait states and n=7 with 3 wait states)

Write Timing



NOTES:

1. It varies with the operation frequency.
   $t_{d(AD-ALE)}$=(tcyc/2-20)ns.min
   $t_{h(ALE-AD)}$=(tcyc/2-10)ns.min, $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min
   (m=3 with 2 wait states and m=5 with 3 wait states)

Measurement conditions

- Vcc=3.0 to 3.6V
- Input high and low voltage:
  VIH=1.5V, VIL=0.5V
- Output high and low voltage:
  VOH=1.5V, VOL=1.5V

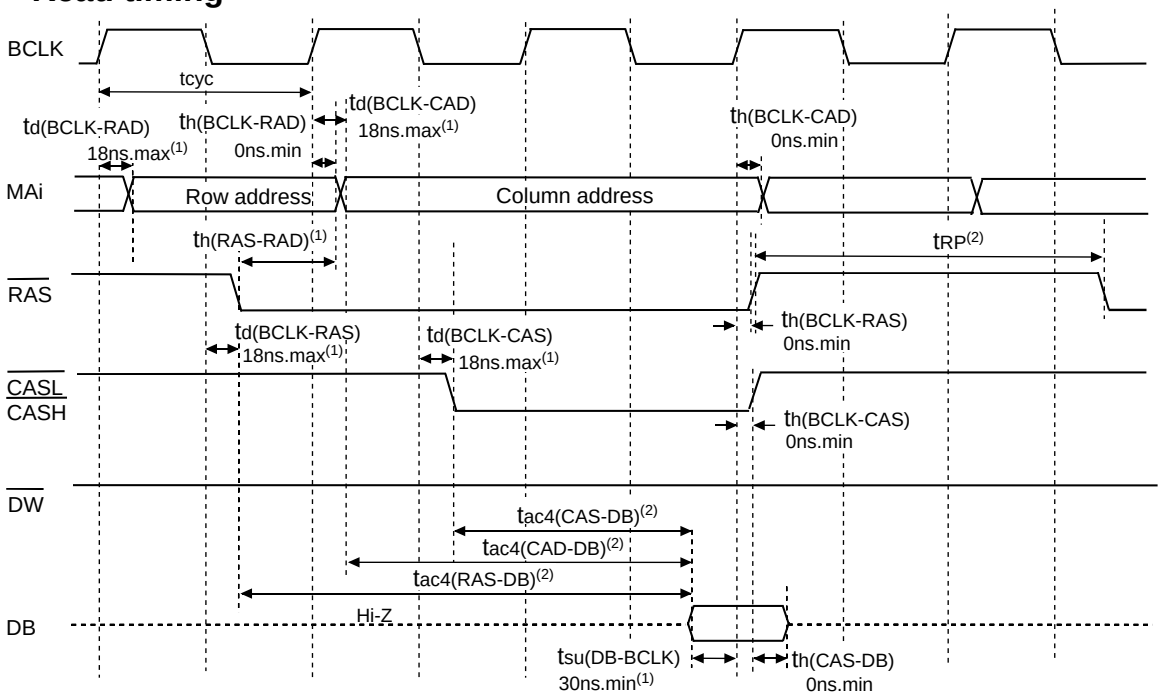
Figure 5.12 Vcc=3.3V Timing Diagram (3)

Memory expansion mode and microprocessor mode

Vcc=3.3V

(With 2 wait states, when accessing the DRAM area)

Read timing



NOTES:

1. A value is guaranteed with no external factor. Maximum 35ns is garanteed for the followings:
   - $t_{d(BCLK-RAS)} + t_{su(DB-BCLK)}$
   - $t_{d(BCLK-CAS)} + t_{su(DB-BCLK)}$
   - $t_{d(BCLK-CAD)} + t_{su(DB-BCLK)}$
2. It varies with the operation frequency.
   - $t_{ac4(RAS-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state and m=5 with 2 wait states)
   - $t_{ac4(CAS-DB)}$=(tcyc/2 x n-35)ns.max (n=1 with 1 wait state and n=3 with 2 wait states)
   - $t_{ac4(CAD-DB)}$=(tcyc x l-35)ns.max (l=1 with 1 wait state and l=2 with 2 wait states)
   - $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   - t_{RP}=(tcyc/2 x 3-20)ns.min

Measurement conditions

- VCC=3.0 to 3.6V
- Input high and low voltage: VIH=1.5V, VIL=0.5V
- Output high and low voltage: VOH=1.5V, VOL=1.5V

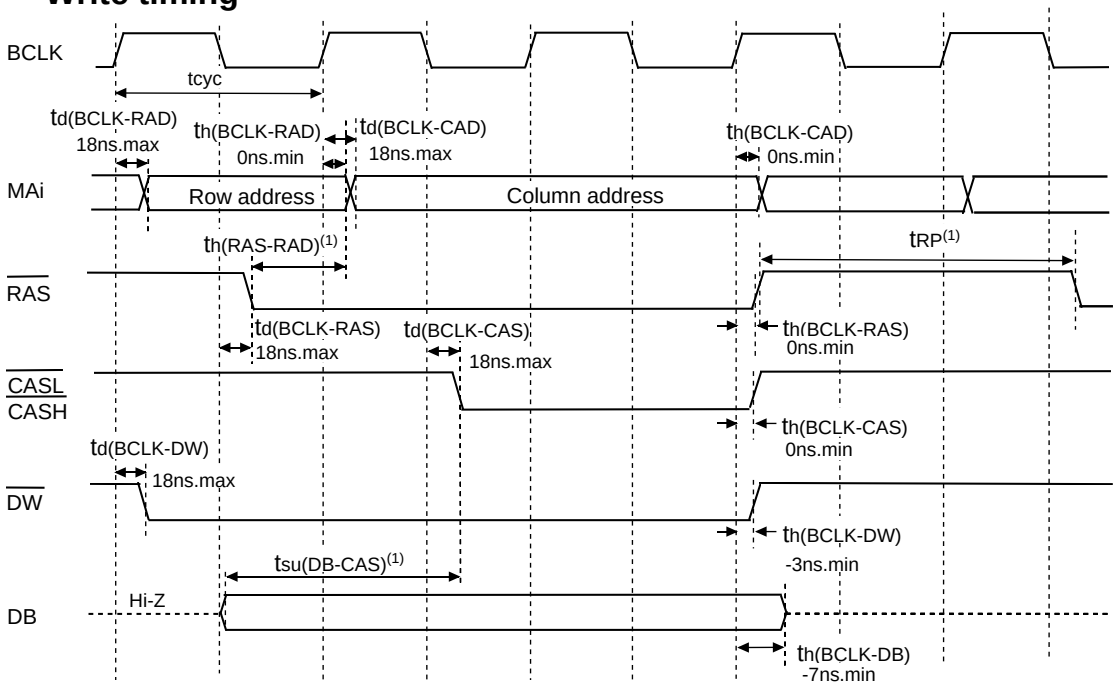
Figure 5.13 VCC=3.3V Timing Diagram (4)

Memory expansion mode and microprocessor mode

Vcc=3.3V

(With 2 wait states, when accessing the DRAM area)

Write timing



NOTES:

1. It varies with the operation frequency.
   $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   t_{RP}=(tcyc/2 x 3-20)ns.min
   $t_{su(DB-CAS)}$=(tcyc-20)ns.min

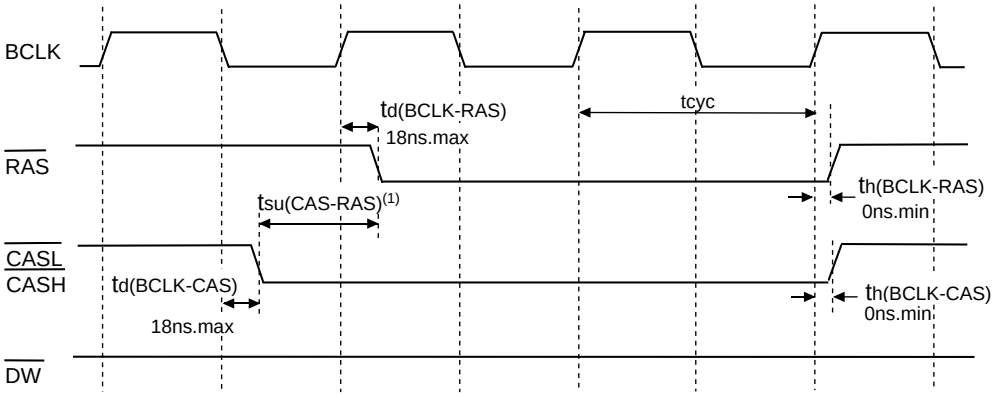
Measurement conditions

- V_{CC}=3.0 to 3.6V
- Input high and low voltage:
  V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
  V_{OH}=1.5V, V_{OL}=1.5V

Figure 5.14 V_{CC}=3.3V Timing Diagram (5)

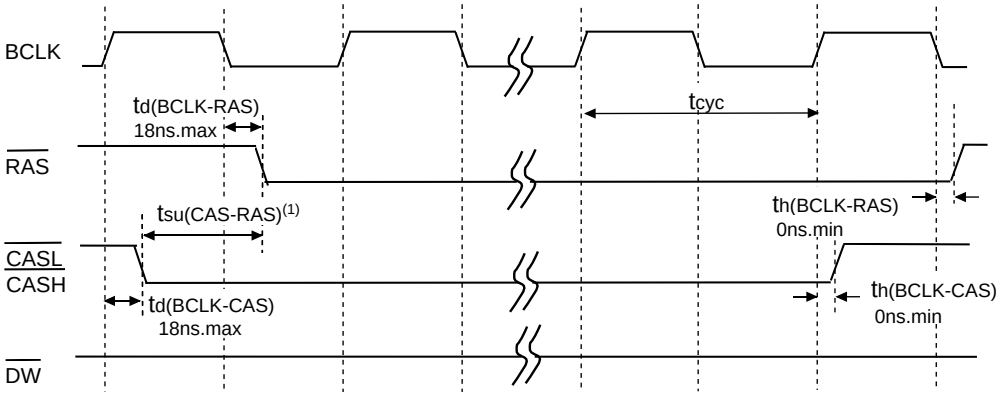
Memory expansion mode and microprocessor mode Vcc=3.3V

Refresh timing (CAS-before-RAS refresh)



NOTES:
1. It varies with the operation frequency.
$t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Refresh timing (Self-refresh)



NOTES:
1. It varies with the operation frequency.
$t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Measurement conditions
- VCC=3.0 to 3.6V
- Input high and low voltage: VIH=1.5V, VIL=0.5V
- Output high and low voltage: VOH=1.5V, VOL=1.5V

Figure 5.15 VCC=3.3V Timing Diagram (6)

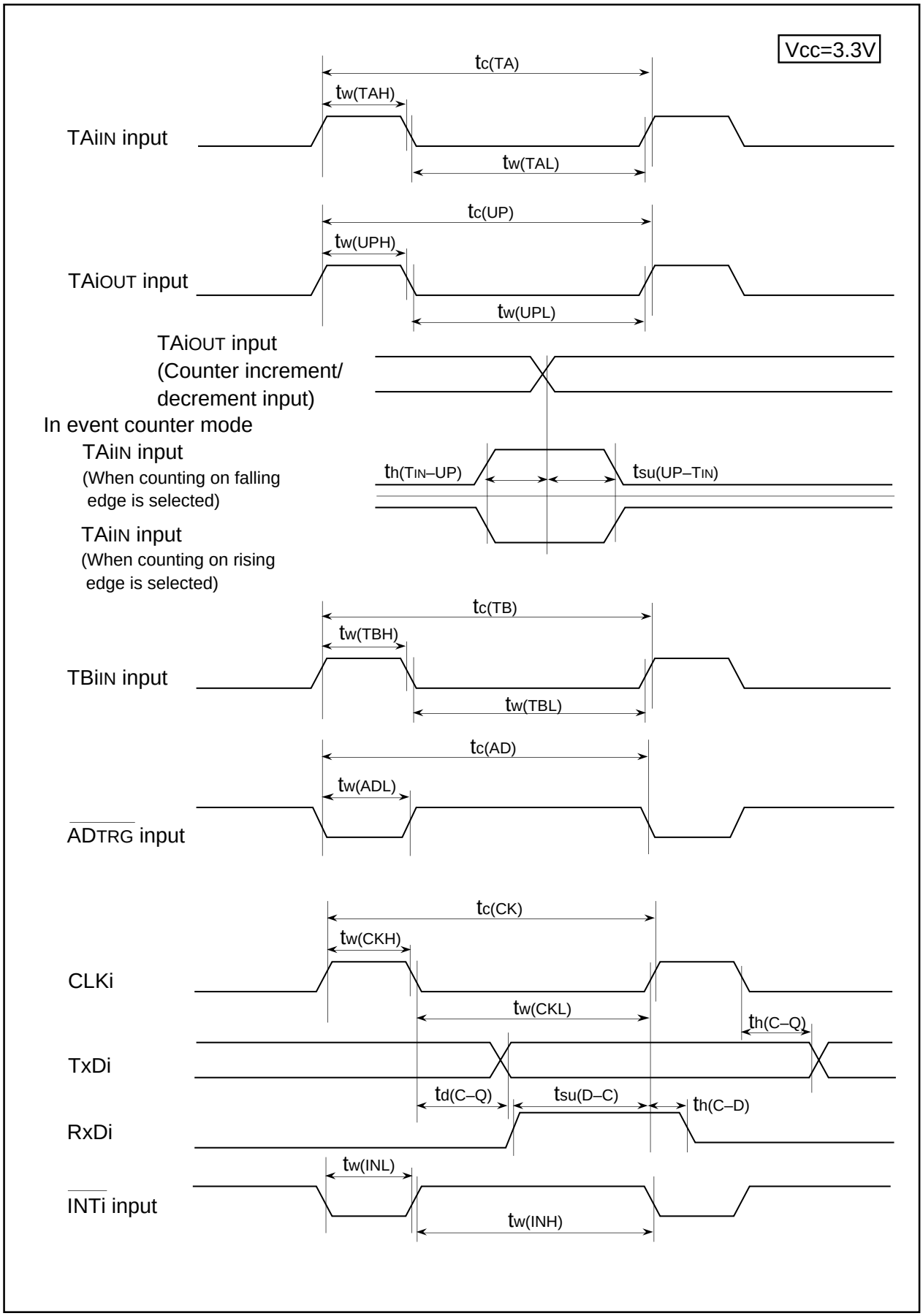
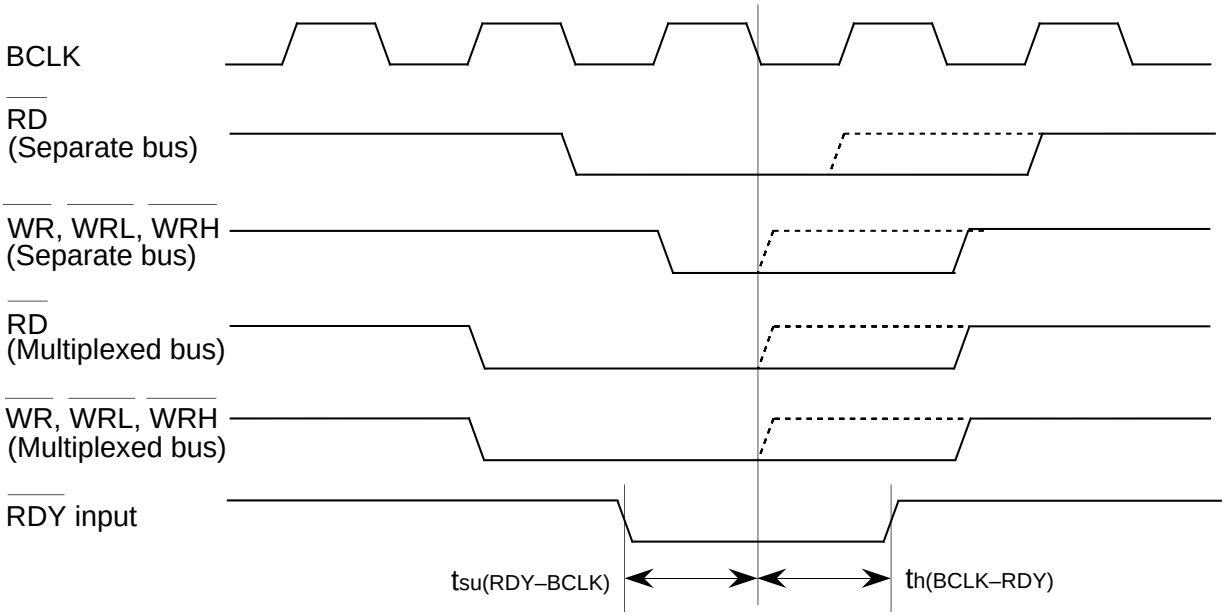


Figure 5.16 Vcc=3.3V Timing Diagram (7)

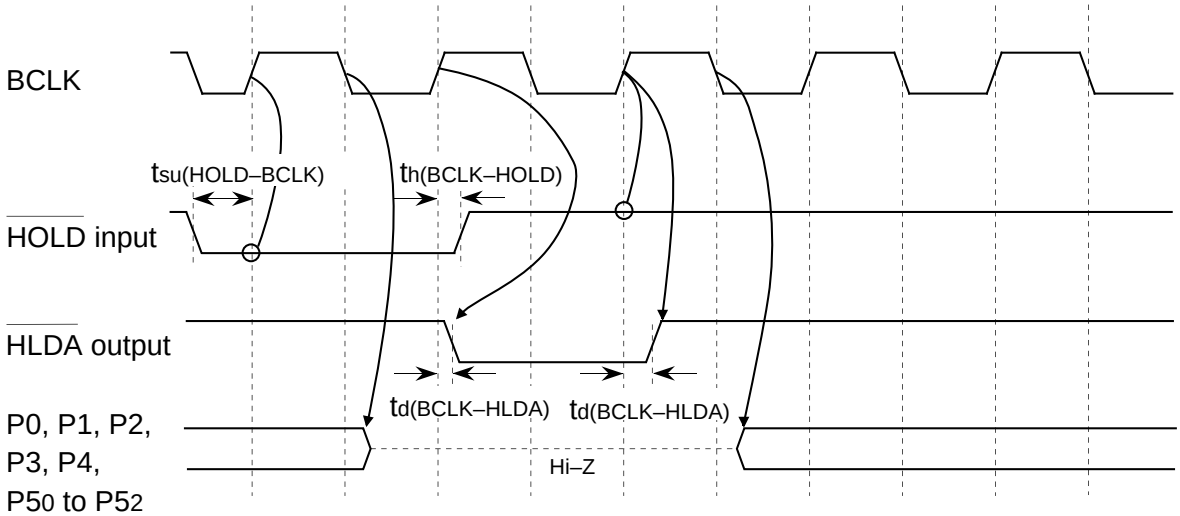
Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode

(Valid only with a wait state)



(Valid with a wait state and no wait state)



Measurement conditions
- VCC=3.0 to 3.6V
- Input high or low voltage: VIH=2.4V, VIL=0.6V
- Output high or low voltage: VOH=1.5V, VOL=1.5V

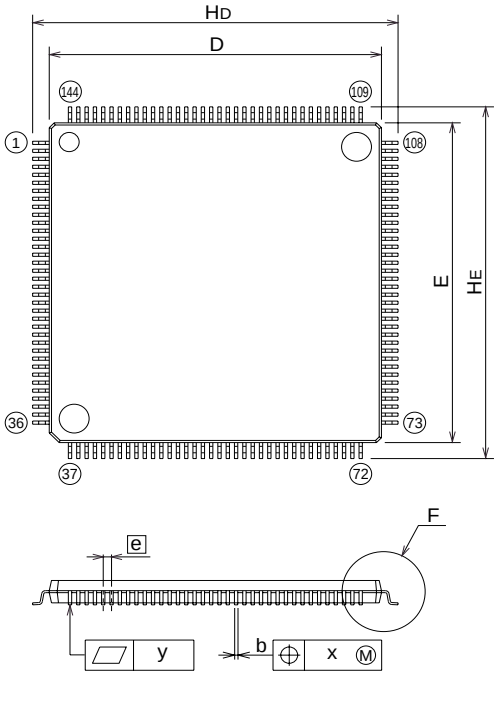
Figure 5.17 VCC=3.3V Timing Diagram (8)

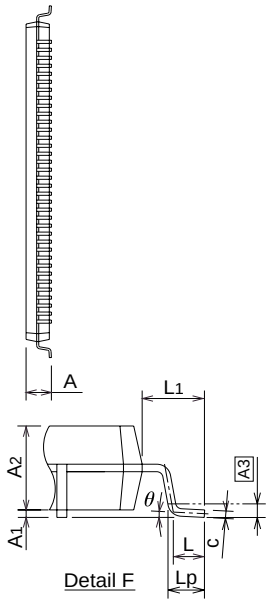
Package Dimensions

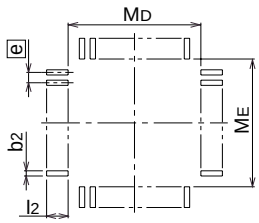
144P6Q-A

Plastic 144pin 20×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP144-P-2020-0.50	–	1.23	Cu Alloy







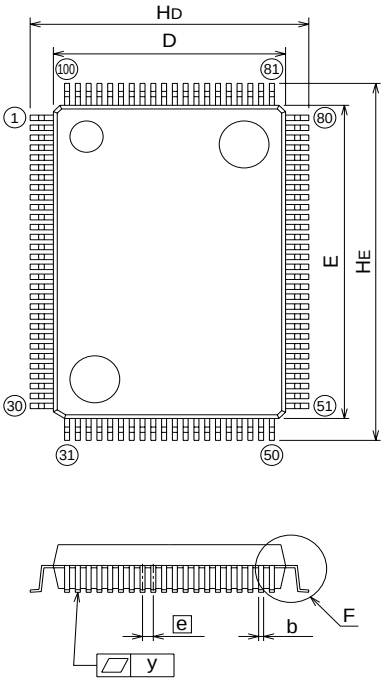
Recommended Mount Pad

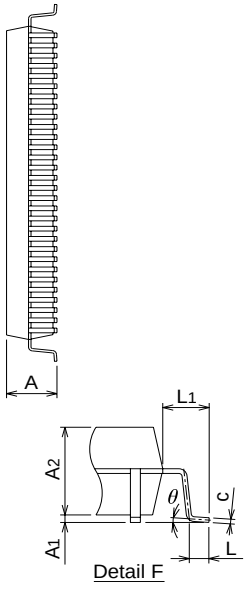
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0.05	0.125	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	–	0.5	–
HD	21.8	22.0	22.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
I2	0.95	–	–
MD	–	20.4	–
ME	–	20.4	–

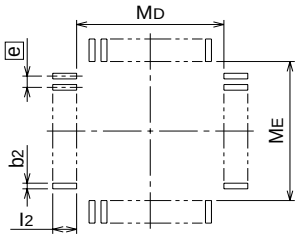
100P6S-A

Plastic 100pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	–	1.58	Alloy 42







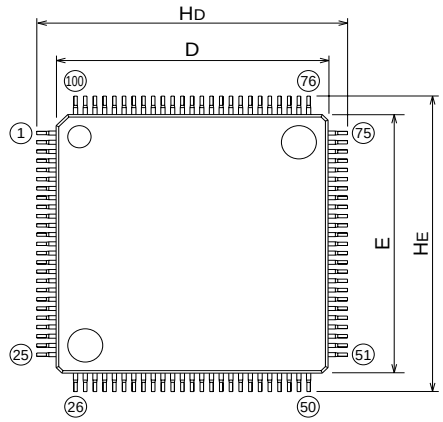
Recommended Mount Pad

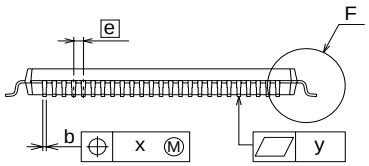
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	–	1.4	–
y	–	–	0.1
θ	0°	–	10°
b2	–	0.35	–
I2	1.3	–	–
MD	–	14.6	–
ME	–	20.6	–

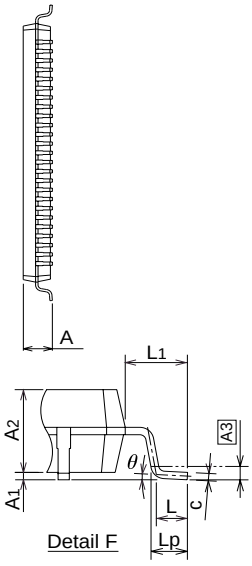
100P6Q-A (MMP)

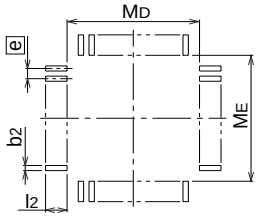
Plastic 100pin 14×14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	–	0.63	Cu Alloy









Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	14.4	–
ME	–	14.4	–

REVISION HISTORY	M32C/81 Group Short Sheet/Data Sheet

Rev.	Date	Description	
		Page	Summary
0.20	01/06/2003		New Document
0.30	30/09/2003		Overview
		2	- "1.2 Difference between the M32C/81 Group and the M32C/83 Group" has been modified.
		3 to 4	- "DRAMC" and "Oscillator stop detect function" have been added to Tables 1.1 and 1.2
		10,14	- V_{REF} pin has been changed from analog input pin to control pin.
		16 to 18	- SDA0 to SDA4 pins have been changed from output pins to I/O pins.
		17	- Description of intelligent I/O has been modified.
		18	- $OUTC3_0$, $OUTC3_2$, ISTxD3 and ISRxD3 have been deleted from port P8.
		19	- Intelligent I/O pin has been deleted from port P12.
		19	- BE_{IN} and BE_{OUT} pins have been modified to IE_{IN} and IE_{OUT} pins in port P13.
			SFR
		25 to 34	- Details of addresses not modifiable by the user has been deleted.
		24,25	- $001F_{16}$ to 0025_{16} and 0030_{16} to 0035_{16} have been deleted.
		27	- Value after RLVL register reset has been modified.
		41	- Function select register A6 has been deleted.
			Electrical Characteristics
		46	- Maximum value of sub clock oscillation frequency has been added in Table 5.2.
		66	- Value of 8-bit conversion time has been modified in Table 5.24

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