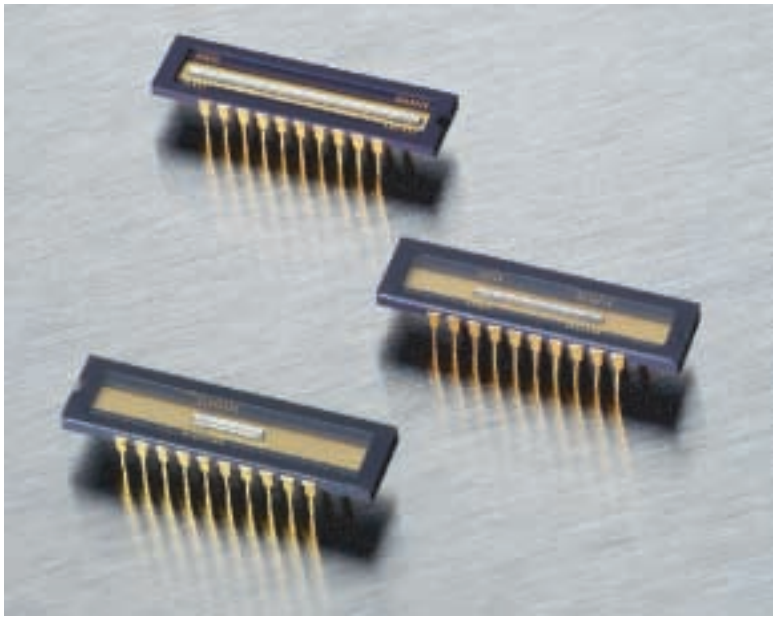
DATASHEET

RETICON

P-Series Linear Photodiode Array Imagers

14µm, single output, 512, 1024, 2048 elements



Description

In the P-series linear imagers, PerkinElmer has combined the best features of high-sensitivity photodiode array detection and high-speed charge-coupled scanning to offer an uncompromising solution to the increasing demands of advanced imaging applications.

These high-performance imagers feature low noise, high sensitivity, impressive charge storage capacity, and lag-free dynamic imaging in a convenient single-output architecture. The 14 µm square contiguous pixels in these imagers reproduce images with minimum information loss and artifact generation, while their unique photodiode structure provides excellent blue response extending below 250 nm in the ultraviolet.

The two-phase CCD readout register requires only five volts for clocking yet achieves excellent charge transfer efficiency. Additional electrodes provide independent control of exposure and antiblooming. Finally, the high-sensitivity readout amplifier provides a large output signal to relax the noise requirements on the camera electronics that follow.

Available in array lengths of 512, 1024 and 2048 elements with either low-cost glass or UV-enhanced fused silica windows, these versatile imagers are widely used in high-speed document reading, web inspection, mail sorting, production measurement and gauging position sensing, spectroscopy and many other industrial and scientific applications requiring peak imager performance.

Note: While the P-Series imagers have been designed to resist electrostatic discharge (ESD), they can be damaged from such discharges. Always observe proper ESD precautions when handling and storing this imager.

Features

- Extended spectral range—250 to 1000 nm
- 40 MHz pixel readout rate
- 2500:1 dynamic range
- 5-volt clocking
- Line rates to 70 kHz
- Ultra low image lag
- Electronic exposure control
- Antiblooming control
- Square pixels with 100% fill factor

PerkinElmer optoelectronics

Description (cont.)

P-series imagers combine high-performance photodiodes with high-speed CCD readout registers and a high-sensitivity readout amplifier. Refer to Figure 1 for construction details.

Light Detection Area

The light detection area in P-series imagers is a linear array of contiguous pinned photodiodes on 14 µm centers. These photodiodes are constructed using PerkinElmer's advanced photodiode design that extends short-wavelength sensitivity into the deep UV below 250 nm, while preserving 100% fill factor and delivering extremely low image lag. This unique design also avoids polysilicon layers in the light detection area that reduces the quantum efficiency of most CCD imagers. The P-series imagers are supplied with glass windows for general visible use, and fused silica windows for use in the ultraviolet below 350 nm. See Figure 2 for the sensitivity and window transmission curves.

For lowest lag, all P-series imagers feature pinned photodiodes. Pinning, which requires a special semiconductor process step, provides a uniform internal voltage reference for the charge stored in every photodiode. This stable reference assures that every photodiode is fully discharged after every scan.

Figure 2a: Spectral Sensitivity Curve

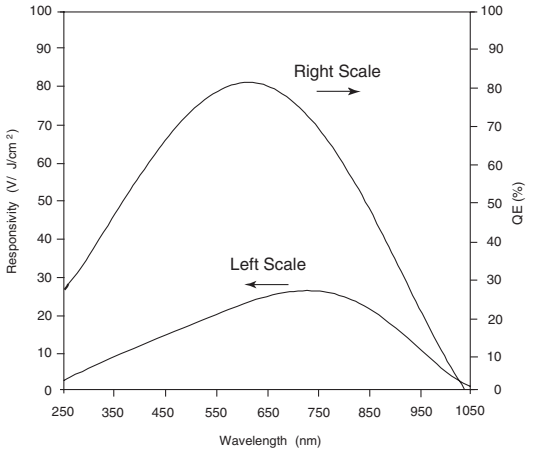
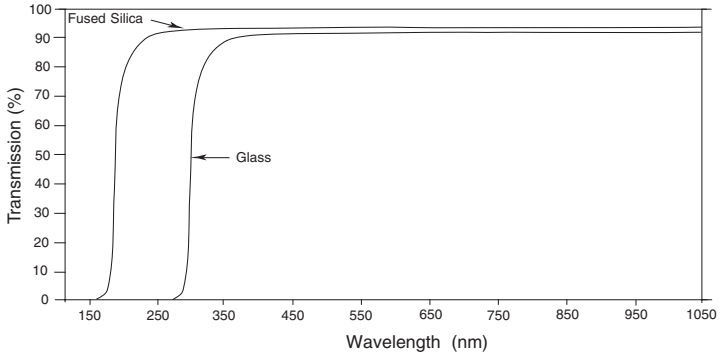


Figure 2b: Window Transmission Curve

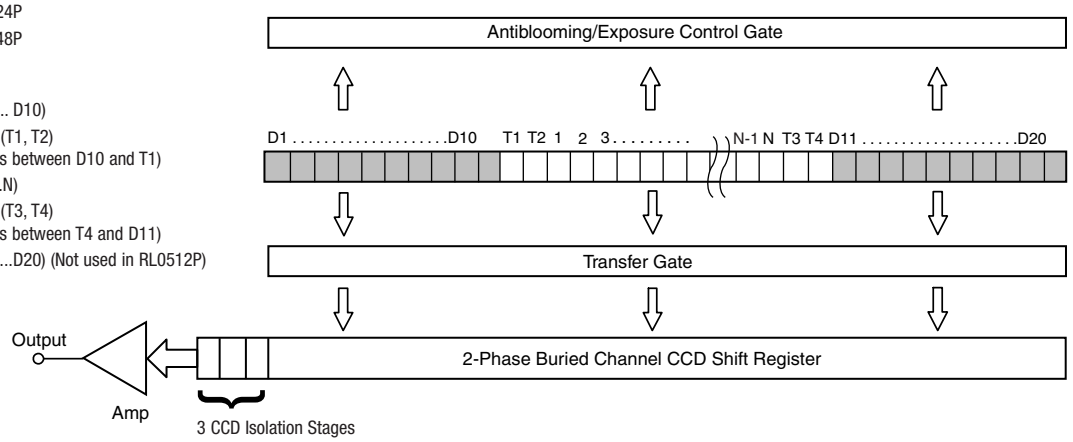


Photodiodes covered with light shields included at one or both ends of the imager provide a dark current reference for clamping. These are separated from the active photodiodes by two unshielded transition pixels that assure uniform response out to the last active photodiode. Due to the potential for light leakage, the two dark pixels nearest the transition pixels should not be used as a dark reference.

Figure 1: Imager Functional Diagram

N = 512 for the RL0512P
N = 1024 for the RL1024P
N = 2048 for the RL2048P

3	Isolation stages
10	Dark pixels (D1 ... D10)
2	Transition pixels (T1, T2) (Light shield ends between D10 and T1)
N	Active pixels (1...N)
2	Transition pixels (T3, T4) (Light shield ends between T4 and D11)
10	Dark pixels (D11...D20) (Not used in RL0512P)



Horizontal Shift Registers

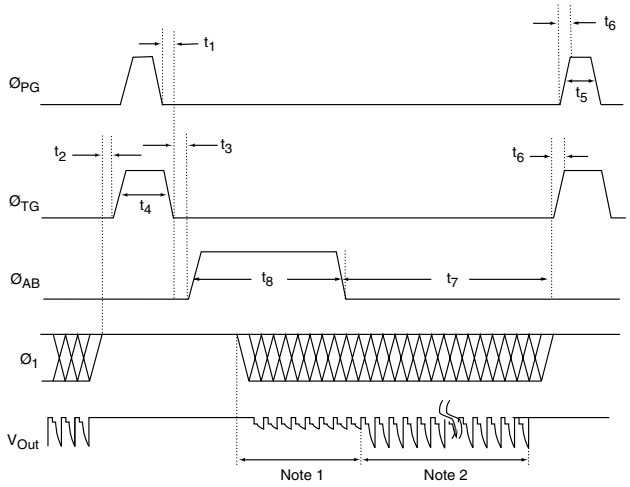
Charge packets collected in the photodiodes as light is received are converted to a serialized output stream through a buried-channel, two-phase CCD shift register that provides high charge transfer efficiency at shift frequencies up to 40 MHz. The PerkinElmer 5-volt CCD process used in this design enables low-power, high-speed operation with inexpensive, readily available driver devices.

The transfer gate ($Ø_{TG}$) controls the movement of charge packets from the photodiodes to the CCD shift register. During charge integration, the voltage controlling the transfer gate is held in its low state to isolate the photodiodes from the shift register. When transfer of charge to the shift register is desired, $Ø_{TG}$ is switched to its high state to create a transfer channel between the photodiodes and the shift register. The charge transfer sequence, detailed in Figure 4, proceeds as follows:

After readout of a particular image line (n), the shift register is empty of charge and ready to accept new charge packets from the photodiodes representing image line (n+1). To begin the transfer sequence, the horizontal clock pulses ($Ø_1$ and $Ø_2$) are stopped with $Ø_1$ held in its high state, and $Ø_2$ in its low state. The transfer gate voltage phase ($Ø_{TG}$) is then switched high to start the transfer of charge to the shift register. Once the transfer gate reaches its high state, the photo gate voltage ($Ø_{PG}$) is set high to complete the transfer. It is recommended that the photo gate voltage be held in the high state for at least 0.1 µs to ensure complete transfer. After this interval, the photo gate voltage is returned to its low state, and when that is completed, the transfer gate voltage is also returned to the low state. The details of the transfer timing are shown in Figure 3 with ranges and tolerances in Table 1.

After transfer, the charge is transported along the shift register by the alternate action of two horizontal phase voltages

Figure 3: Transfer Timing Diagram



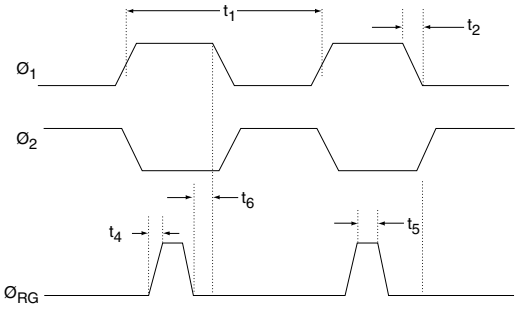
Notes:
1. Transition and dark pixels
2. Active pixels

Table 1. Transfer Timing Requirements

Item	Sym	Min	Typ	Max
Delay of $Ø_{TG}$ falling edge from $Ø_{PG}$ falling edge	t_1	5 ns	20 ns	-
Delay of $Ø_{TG}$ rising edge from end of $Ø_1$ and $Ø_2$ clocks	t_2	0 ns	10 ns	-
Delay of $Ø_{AB}$ rising edge from $Ø_{PG}$ falling edge	t_3	5 ns	5 ns	-
$Ø_{TG}$ pulse width	t_4	100 ns	500 ns	-
$Ø_{PG}$ pulse width	t_5	100 ns	400 ns	-
Rise/fall time	t_6	10 ns	20 ns	-
Integration time	t_7	0 ns	-	-
$Ø_{AB}$ pulse width	t_8	-	750 ns[1]	-

Note 1: 750ns is the typical time to fully reset the photodiode.

Figure 4: Readout Timing Waveforms



Horizontal Shift Registers (cont.)

$Ø_1$ and $Ø_2$. While the two-phase CCD shift register architecture allows relaxed timing tolerances over those required in three- or four-phase designs, optimum charge transfer efficiency and lowest power dissipation is obtained when the overlap of the two-phase CCD clocks occurs around the 50% transition level. Additionally, the phase difference between signals $Ø_1$ and $Ø_2$ should be maintained near 180° and the duty cycle of both signals should be set near 50% to prevent loss of full-well charge storage capacity and charge transfer efficiency. Readout timing details are shown in Figure 4 with ranges and tolerances in Table 2.

Timing Requirements

In high-speed applications, fast waveform transitions allow maximum settling time of the output signal. However, it is generally advisable to use the slowest rise and fall times consistent with required video performance because fast edges tend to introduce more transition noise into the video waveform. When the highest speeds are required, careful smoothing of the waveform transitions may improve the balance between speed and video quality.

Output Amplifier

Charge emerging from the last stage of the shift register is converted to a voltage signal by a charge integrator and video amplifier. The integrator, a capacitor created by a floating diffusion, is initially set to a DC reference voltage (V_{RD}), by setting the reset transistor voltage ($Ø_{RG}$) to its high state. To read out the charge, $Ø_{RG}$ is pulsed low turning the reset transistor off and isolating the integrator from V_{RD}. The next time $Ø_1$ goes low, the charge packet is transferred to the integrator where it generates a voltage proportional to the packet size. The reset transistor voltage, $Ø_{RG}$, must reach its low state prior to the high-to-low transition of $Ø_1$. An apparent clipping of the video signal will result if this

Table 2. Readout Timing Requirements

Item	Sym	Min	Typ	Max
$Ø_1$, $Ø_2$ clock period	t_1	25 ns	-	-
$Ø_1$, $Ø_2$ rise/fall time	t_2	-	5 ns	-
$Ø_{RG}$ rise/fall time	t_4	-	5 ns	-
$Ø_{RG}$ clock - high duration	t_5	5 ns	-	-
Delay of $Ø_1$ high - low transition from $Ø_{RG}$ low*	t_6	0 ns	-	-

Note: The cross over point for $Ø_1$ and $Ø_2$ clock transitions should occur within the 10 - 90% level of the clock amplitude.

Table 3. Imager Performance (Typical)

Pixel count	512 elements (RL0512P)
	1024 elements (RL1024P)
	2048 elements (RL2048P)
Pixel size	14 µm x 14 µm
Exposure control	yes
Horizontal clocking	2Ø (5V clock amplitude)
Number of outputs	1
Dynamic range[1]	2500:1
Readout noise (rms)	
amplifier	25 electrons
reset transistor	55 electrons
total noise without CDS	60 electrons
Saturation exposure[2]	24 nJ/cm^2
Noise equivalent exposure[2]	9.6 pJ/cm^2
Amplifier sensitivity	4 µV/electrons
Saturation output voltage	600 mv
Saturation charge capacity	150,000 electrons
Charge transfer efficiency	0.99995
Peak responsivity	25V/µJ/cm^2
PRNU match across array	±10%
Dead pixels	0
Lag	< 1%
Spectral response range	250 nm - 1000 nm
Data rate (per output)	40 MHz

Notes:
1. Defined as Q_{sat}/rms noise (total).
2. For illumination at 750 nm.

Output Amplifier (cont.)

condition is not satisfied. Figure 4 details the clock waveform requirements and overlap tolerances.

The video amplifier buffers the signal from the integrator for output from the imager. Care must be taken to keep the load on this amplifier within its ability to drive highly reactive or low impedance loads. The half power bandwidth into an external load of 10 pF is 150 MHz. It is recommended that the output video signal be buffered with a wide bandwidth emitter follower or other appropriate amplifier to provide a large Z_{IN} to the output amplifier. Keep the external amplifier close to the output pins to minimize stray inductive and capacitive coupling of the output signal that can harm signal quality.

Exposure Control and Antiblooming

An exposure control feature in the P-series imagers supports variable charge accumulation time in the photodiode. When the antiblooming gate voltage ($Ø_{AB}$) is set to its high state, charge is drained from the pixel storage gate to the exposure control drain. During normal charge collection in the photodiode, $Ø_{AB}$ is set to its low state. Due to the timing requirements of the exposure control mode, charge is always accumulated at the end of the period just before the charge is transferred to the readout register. Figure 3 includes the timing requirements for exposure control with the antiblooming gate. The exposure control timing shown will act on the charge packets that emerge as video data on the next readout cycle.

Table 4. Operating Voltages

Signal	Function	State	Voltage	Tolerance
$Ø_1$, $Ø_2$	Horizontal Clocks	High Low	5 0	±5%
$Ø_{TG}$	Transfer Gate	High Low	8 0	±10%
$Ø_{PG}$	Photo Gate	High Low	8 -4	±5%
$Ø_{AB}$	Antiblooming Gate	High Low	4 -4	±5%
V_{OG}	Output Gate		3	±5%
$Ø_{RG}$	Reset Gate	High Low	8 0	±10%
V_{DD}	Amplifier Voltage Supply		12	±5%
V_{RD}	Amplifier Reset Drain		9.5	±5%
V_{RD}/LS	Amplifier Return / Light Shield		0	

Table 5. Absolute Maximum Rating Above Which Useful Life May Be Impaired

	Min	Max	Units
Temperature			
Storage	-25	+85	°C
Operating	-25	+55	°C
Voltage (with respect to GND)			
Pins 3, 4, 17 - 19	-0.3	+18	V
Pins 2, 10, 20	-0.3	+18	V
Pins 1, 11	-0.3	+ 0	V
Pins 15, 16	-4.3	+18	V

Precautionary Note: The CCD output pin (Pin #2) must never be shorted to either V_{SS} or V_{DD} while power is applied to the device. Catastrophic device failure will result!

Imager Performance

In P-series images each element performs its own function admirably while integrating smoothly with the other elements on the team. The photodiodes efficiently transform light to charge, the readout registers accurately transport the charge to the amplifier, and the amplifier delivers a clean, robust signal for use in image processing electronics. While the actual performance of these imagers depends strongly on the details of the electronics and timing the camera provides, their straightforward implementation requirements facilitate optimum designs.

Operating Conditions

For optimum performance and longest life, carefully follow the operational requirements of these imagers. Provide stable voltage sources free of noise and variation and clean waveforms with controlled edges. Protect the imager from electrostatic discharge and excessive voltages and temperature. Do not violate the limits on output register speed or reduce timing margins below the minimums.

Imager Configuration

All P-series imagers are constructed using ceramic packages and optically-flat windows. Imager die are secured to precision leadframes by thermal silver-filled epoxy. Packages are baked before sealing to elminate moisture, and tested for seal integrity.

Table 6. Pinout Description and Capacitance Values of Clocked Phases

Pin	Sym	Function	Capacitance (pF) (Typ) Pixels	2048	1024	512
1	V_{SS}	Amplifier return		50	30	20
2	V_{Out}	Signal output		75	45	30
3	$Ø_2$	CCD horizontal phase 2		270	140	70
4	$Ø_1$	CCD horizontal phase 1		350	180	90
5	N/C	No connection				
6	N/C	No connection				
7	N/C	No connection				
8	N/C	No connection				
9	N/C	No connection				
10	V_{DD}	Amplifier drain supply				
11	LS	Light shield/die attach				
12	N/C	No connection				
13	N/C	No connection				
14	N/C	No connection				
15	$Ø_{AB}$	Antiblooming gate		70	35	20
16	$Ø_{PG}$	Photo gate		100	50	25
17	$Ø_{TG}$	Transfer gate		90	50	25
18	V_{OG}	Output gate		8	8	8
19	$Ø_{RG}$	Reset gate		7	2	2
20	V_{RD}	Reset drain				

Figure 5. Pinout Configuration

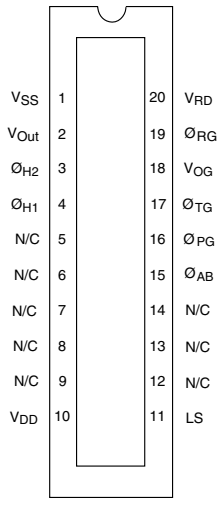
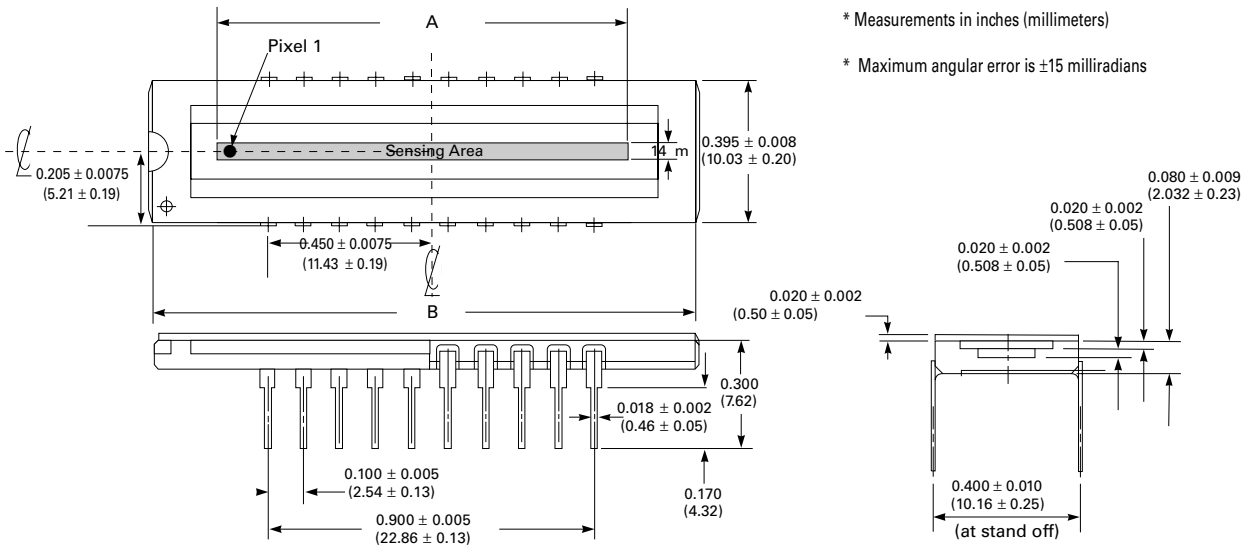


Figure 6: Outline Drawings



Ordering Information

The RL0512, RL1024 and RL2048 P-series imagers are available with either glass or fused silica windows. On special orders, PerkinElmer can supply anti-reflectance coated windows or windowless packages. Imagers are individually packed in electrostatic-resistant boxes and identified by lot number for tracking.

Table 7. Package Dimensions and Tolerances

	A		B	
Device	**Inches**	**mm**	**Inches**	**mm**
RL0512P	0.284	7.224	1.500 ± 0.15	38.1 ± 0.381
RL1024P	0.566	14.392	1.500 ± 0.15	38.1 ± 0.381
RL2048P	1.131	28.728	1.500 ± 0.15	38.1 ± 0.381

Notes:
1. Includes active and transition pixels.

Table 8. Stock Part Numbers

	Active Pixels		
Window	**512**	**1024**	**2048**
Glass	RL0512PAG-712	RL1024PAG-712	RL2048PAG-712
Fused Silica	RL0512PAQ-712	RL1024PAQ-712	RL2048PAQ-712

For more information e-mail us at opto@perkinelmer.com or visit our web site at **www.perkinelmer.com/opto**. All values are nominal; specifications subject to change without notice.

Table 9. Sales Offices

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