The Measurement of DC Voltage Signal Using the UTI

1. INTRODUCTION

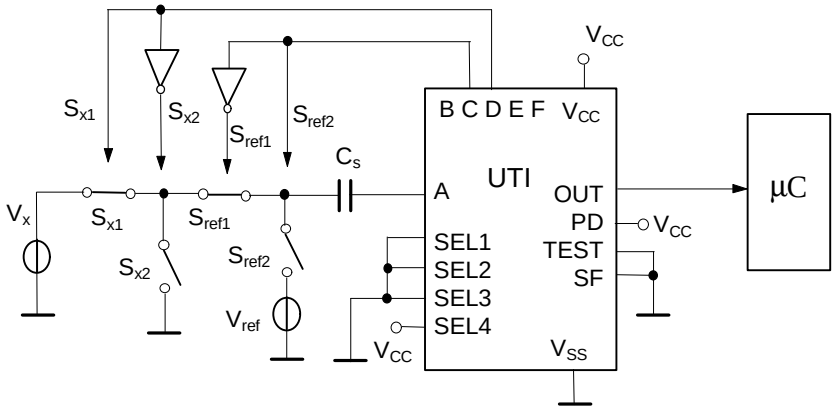
UTI can offer an interface for many passive sensing elements, such as, capacitors, resistors, resistive bridges and resistive potentiometers. By using some external components, UTI can offer an interface for the measurement of DC voltage signals also. This is very useful for the application of the thermocouple signal measurement.

In this section, we present a measurement concept for the DC voltage signal using the UTI.

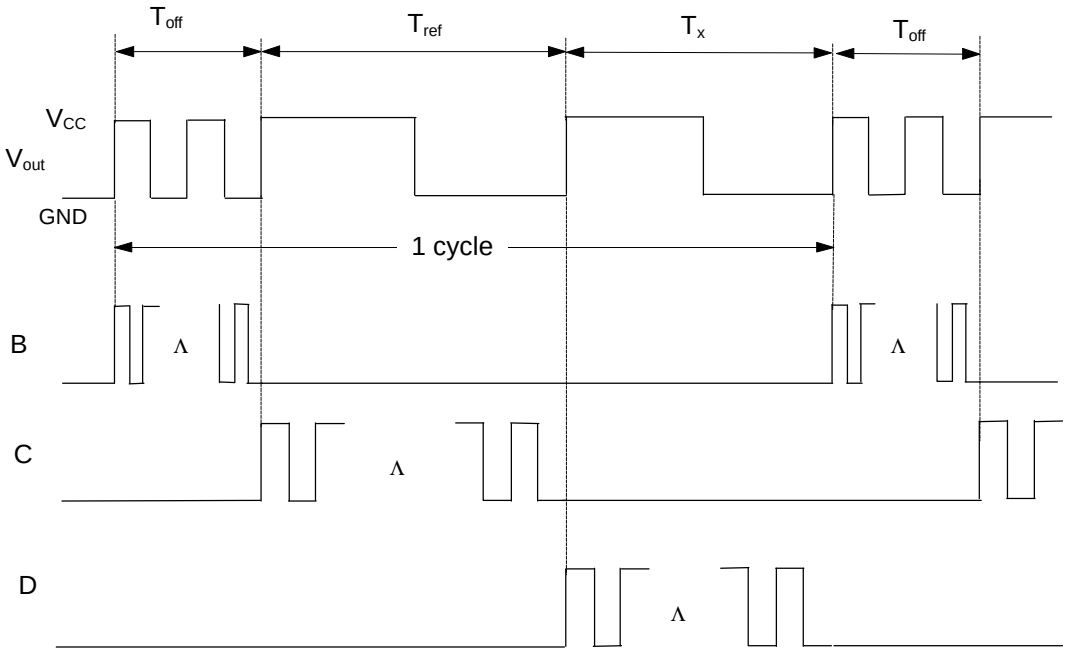
2. MEASUREMENT CONCEPT

The capacitance measurement functions of the UTI can be employed to measure voltage signals . As an example, Figure 1(a) shows a schematic diagram circuit for the measurement of voltage signals using the mode C23 of the UTI. In this circuit, V_x denotes an unknown voltage (measurand), V_{ref} is a known reference voltage. The capacitor C_s and switches S_{x1}, S_{x2}, S_{ref1}, S_{ref2} sample the voltage signals V_x and V_{ref} alternatively and convert the voltage signals into charges alternatively. The UTI will convert the charges into the periods of the output of the UTI.

The three-signal technique [3] is applied to ensure the accuracy and reliability of the circuit by eliminating the gain and offset parameters of the interface system. To perform this three-signal technique, a reference signal (V_{ref}) and a constant part (including offset voltages) are measured in exactly the same way as the sensor signal (V_x) during two additional phases. Figure 1(b) shows one complete cycle, consisting of three phases T_{off}, T_x and T_{ref}.



(a)



(b)

Figure 1 (a) The schematic diagram of the measurement system. (b) Output signal V_{out} of the UTI.

In the following, we explain the measurement principle:

When UTI works at mode C23, pin A is the input of the charge amplifier in UTI, pins E and F are grounded internally, and pins B, C and D of the UTI output square-wave signals (see figure 1(b)). The periods of these square-wave signals are modulated by the charges in the capacitor C_s. These square-wave signals also control the states of the sampling switches.

During pin B output the square-wave signal the initial offset of the UTI is measured. During pin C output the square-wave signal the reference voltage is measured. And during pin D output the square-wave signal the measurand (a voltage signal) is measured. The duration of each phase is proportional to the signal which is measured during that phase. They are given by:

$$T_{off} = KC_{off} , \tag{1}$$

$$T_x = K\frac{V_x}{V_{CC}}C_s + T_{off} . \tag{2}$$

$$T_{ref} = K\frac{V_{ref}}{V_{CC}}C_s + T_{off} . \tag{3}$$

where V_{CC} is the power supply voltage. K is the linear transfer coefficient of the UTI. C_{off} is a initial constant part (including offset capacitance).

With equations (1), (2) and (3), the measurand V_x is found from

$$V_x = \frac{T_x - T_{off}}{T_{ref} - T_{off}}V_{ref} . \tag{4}$$

Formula (4) shows that the values and inaccuracies of the capacitances C_s and voltage power supply V_{CC} and the error of the linear transfer coefficient K do not affect the measured result because of the applied three-signal technique.

The measurement principle described above is also suitable for the mode of C25, C12, CMUX and C300.

3. NONIDEALITIES

Many nonidealities are eliminated by using the three-signal technique. However, some effects cannot eliminated by this technique, as discussed below.

A. The Effect of the Parasitic Capacitors

Figure 2 shows some critical parasitic capacitances C_{px}, C_{pref}, C_{p1} and C_{pin} in the voltage measurement system.

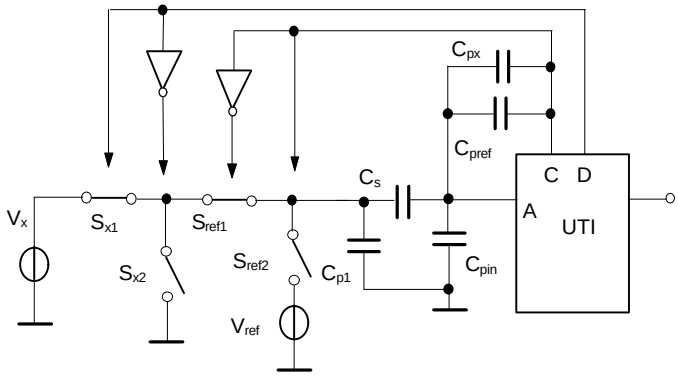


Figure 2 The parasitic capacitances in the voltage measurement system.

1) The parasitic capacitance C_{pin}

As described in ref. [2], the parasitic capacitance C_{pin} will cause a nonlinearity of the conversion of the input signal to the output period. For a nonlinearity of 300 ppm, the parasitic capacitance C_{pin} of up to 250 pF is allowed.

2) The parasitic capacitances C_{px} and C_{pref}

The influence of the parasitic capacitances C_{px} and C_{pref} on the results can be expressed by the following equation:

$$\frac{T_x - T_{off}}{T_{ref} - T_{off}} \cong \frac{V_x}{V_{ref}}\left(1 - \frac{V_{cc}}{V_{ref}} \cdot \frac{C_{pref}}{C_s}\right) + \frac{V_{cc}}{V_{ref}} \cdot \frac{C_{px}}{C_s}. \tag{5}$$

Equation (5) shows that even after applying the three-signal technique the parasitic capacitors C_{pref} and C_{px} cause a gain error and an offset on the result. These systematic errors can be eliminated after calibration while using a compensation algorithm in the microcontroller. For such a compensation, it is necessary that the parasitics do not change after calibration.

B. Output impedances R_{oref}, R_{ox} of reference voltage source and V_x

The output impedance R_{ox} or R_{oref} of the reference source or measurand V_x and capacitances associated with resistors R_{ox} and R_{oref} form an RC circuit with a time constant of

$$t_i \cong (2R_{ON} + R_{oi})(C_s + C_{p1}), \tag{6}$$

where R_{oi} represents the output impedances R_{ox} or R_{oref}. Further, R_{ON} is the switch-ON resistance of switches S_x and S_{ref}. This effect results in a relative error for the result,

$$e_{NL} \cong \exp\left(-\frac{T_p}{2}\frac{1}{t_i}\right), \tag{7}$$

Example: for a relative error of, for instance smaller than 10^{-5}, with R_{ON} = 200 Ω, T_p = 10 μs and C_s+C_{p1} = 10 pF, R_{oi} must be smaller than 43 kΩ.

C. Switch clock feedthrough

It is common practice to reduce the effect of switch clock feedthrough by compensation. Because switches S_{x1} and S_{x2}, S_{ref1} and S_{ref2} are controlled by opposing clock signals, the effect of the clock feedthrough is canceled partly. Moreover, it is possible to obtain a further reduction of the clock feedthrough by using CMOS switches.

D. Noise

In the voltage measurement, by using the system shown in Figure 1(a), the noise originates mainly from two parts: the oscillator noise and the quatization noise caused by sampling in the microcontroller. The standard deviations of the relative errors caused by these two noise sources can be expressed by, respectively:

$$e_{no} = \sqrt{\frac{C_{pin}}{C_s^2}\frac{2 f_T C_{int} u_{eq}^2}{V_{cc}^2 N}}, \tag{8}$$

$$e_{nqt} = \frac{1}{\sqrt{3}}\frac{1}{NT_p f_c}, \tag{9}$$

where f_T is the bandwidth of the OTA, u_{eq} is the RMS value of the equivalent input noise (V/√Hz) of the OTA, f_c is the sampling frequency of the microcontroller and N is the measured period number.

4. Optimization of the Measurement Range

In order to guarantee that the UTI works in its optimum linear measurement range, the measurement range for the voltage signal $V_{x,range}$ and the value of the sampling capacitor C_s are determined by the following relationship:

$$V_{x,range} C_s \le V_{cc} C_{x,range}, \tag{10}$$

where $C_{x,range}$ is the capacitance measurement range of the UTI. For instance, for the mode C23 of UTI, $C_{x,range}$ = 2 pF.

When the sampling switches are supplied by a power supply V_{DD} which is larger than the power supply V_{CC} of the UTI, the measurement system described by Figure 1(a) can measure a voltage signal larger than V_{CC}.

5. The Measurement of Voltage Signal Using Modes C12 and C25

The voltage signal can also be measured by using modes C12 and C25 of the UTI. Figure 3 shows the schematic diagram circuit for the measurement of voltage signals using modes C12 and C25 of the UTI.

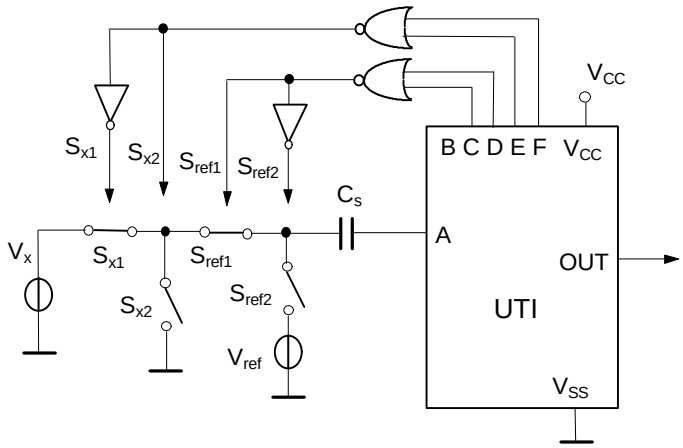


Figure 3 A schematic diagram circuit for the measurement of voltage signals using modes C12 and C25.

Figure 4 shows the output signal of the UTI at modes C12 and C25.

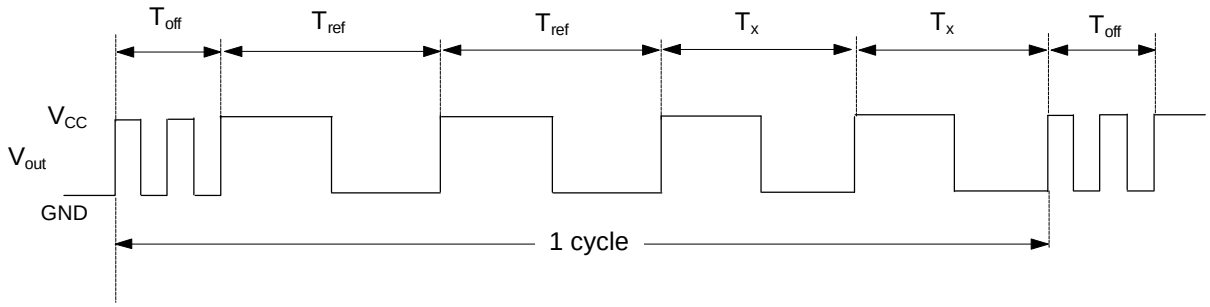


Figure 4 Output signal of the UTI.

6. THE MEASUREMENT OF VOLTAGE SIGNAL USING MODE CMUX

Figure 5 shows the schematic diagram circuit for the measurement of voltage signals using mode CMUX of the UTI.

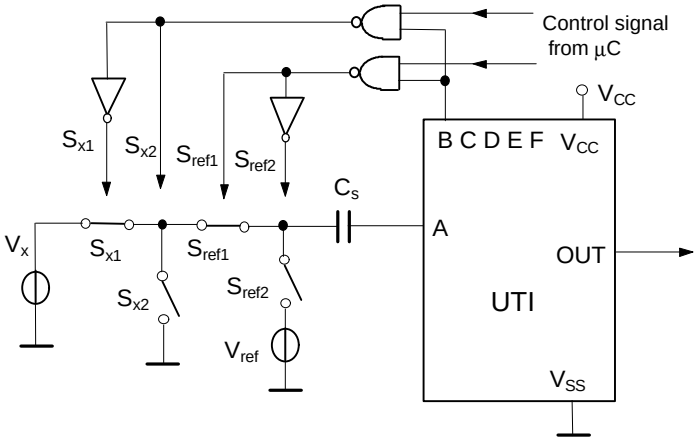


Figure 5 A schematic diagram circuit for the measurement of voltage signals using mode CMUX.