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OKI

ML63295A
User's Manual

CMOS 4-bit microcontroller

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Preface

This manual describes the hardware of Oki's original CMOS 4-bit microcontroller ML63295A.

Refer to the "nX-4/250, 300 Core Instruction Manual" for details of the 4-bit CPU core nX-4/250 which is built in the ML63295A.

The manuals related to the ML63295A are shown below.

- nX-4/250, 300 Core Instruction Manual:
  Describes the base architecture and instruction set of nX-4/250 core and nX-4/300 core.

- SASM63K User's Manual:
  Describes the structured assembler operation and assembler language specification.

- Dr.63295 User's Manual:
  Describes the hardware of the emulator.

- DT63K Debugger/DTS63K Simulator User's Manual:
  Describes the debugger commands and the hardware of the simulator.

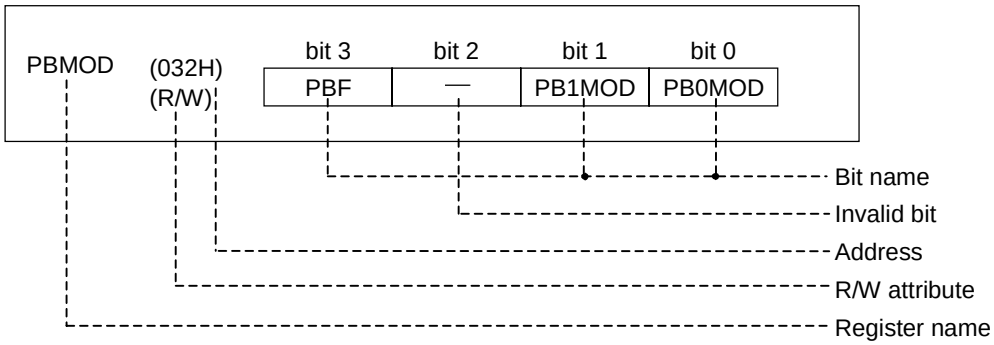
This document is subject to change without notice.

Notation

Classification	Notation	Description
■ Numeric value	xxh, xxH	Represents a hexadecimal number.
	xxb	Represents a binary number.
■ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 2 nibbles = 8 bits
	nibble, N	1 nibble = 4 bits
	mega-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, µ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
	KB	1 KB = 1 kilobyte = 1024 bytes
	MB	1 MB = 1 megabyte = 2^{20} bytes = 1,048,576 bytes
■ Symbol	⚠ Note:	Gives more information about mistakable items.
■ Terminology	"H" level	Indicates high side voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level	Indicates low side voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

■ Register description

Invalid bit : When read, a value of "1" is always obtained. Write operations are invalid.
R/W attribute : "R" indicates data can be read and "W" indicates data can be written.



Contents

Chapter 1

Overview

1. Overview

1.1 Overview

The ML63295A is a CMOS 4-bit microcontroller that employs Oki's original CPU core nX-4/250.

The ML63295A operates on a power supply voltage of 6 V.

With built-in 3072-dot matrix LCD drivers (96 SEG. × 32 COM.), the ML63295A is suited for applications such as electronic dictionaries with an LCD.

1.2 Features

The ML63295A has the following features.

a. Extensive instruction set
- 439 instructions
  Transfer, rotate, increment/decrement, arithmetic operations, compare, logic operations, mask operations, bit operations, ROM table reference, external memory transfer, stack operations, flag operations, jump, conditional branch, call/return, control

b. Wide variety of addressing modes
- Indirect addressing mode for 4 types of data memory with current bank register, extra bank register, HL register and XY register
- Data memory bank internal direct addressing mode

c. Processing speed
- 2 clocks per machine cycle, with most instructions executed in 1 machine cycle
- Minimum instruction execution time: 61 µs (@ 32.768 kHz system clock)
  1 µs (@ 2 MHz system clock)

d. Clock generation circuit
- Low-speed clock:
  Crystal oscillation or RC oscillation selected with mask option (30 kHz to 80 kHz)
- High-speed clock:
  Ceramic oscillation or RC oscillation selected with software (2 MHz max.)

e. Program memory space
- 32K words
- The basic instruction length is 16 bits per word.

f. Data memory space
- 2048 nibbles

g. External data memory space
- 64 Kbytes (expandable furthermore by using the I/O ports)

h. Stack level
- Call stack level: 16 levels
- Register stack level: 16 levels

i. Ports

- Input ports:
  Selectable as input with pull-up resistor/input with pull-down resistor/high impedance input.
- Output ports:
  Selectable as P-channel open drain output/N-channel open drain output/high-impedance output/CMOS output.
- I/O ports:
  Selectable as input with pull-up resistor/input with pull-down resistor/high impedance input.
  Selectable as P-channel open drain output/N-channel open drain output/high impedance output/CMOS output.
- Can be interfaced with external peripherals that use a different power supply than this device uses (provided with V_{DDI} as the port-dedicated power supply pin and V_{DDE} as the power supply for the MD and MDB pins).
- Number of ports:
  Input port: 2 ports × 4 bits
  Output port: 6 ports × 4 bits
  Input-output port: 6 ports × 4 bits

j. Melody output

- Melody frequency: 529 Hz to 2979 Hz
- Tone length: 63 varieties
- Tempo: 15 varieties
- Melody data: Stored in program memory
- Buzzer driver signal output: 4 kHz

k. LCD driver

- Number of segments: 3072 Max. (96 SEG. × 32 COM.)
- Duty: Selectable as 1/2, 1/4, 1/6, 1/8, 1/10, 1/12, 1/14, 1/16, 1/18, 1/20, 1/22, 1/24, 1/26, 1/28, 1/30, or 1/32 duty
- Bias: Selectable as 1/5 or 1/6 bias (regulator built-in)
- Frame frequency: ex. 64 Hz (at 1/32 duty), 128 Hz (at 1/16 duty), 256 Hz (at 1/8 duty), 512 Hz (at 1/4 duty), 1024 Hz (at 1/2 duty)
- Contrast: 16 levels adjustable
- Display modes: Selectable as all-ON mode/all-OFF mode/power down mode/normal display mode

l. Multiplication/division circuit

- Multiplication: (8 bits) × (8 bits) → Product (16 bits)
- Division: (16 bits)/(8 bits) → Quotient (16 bits), Remainder (8 bits)

m. System reset function

- System reset through RESET pin
- System reset by power-on detection
- System reset by low-speed oscillation halt

n. Battery check

- Low-voltage supply check
- The value of the judgment voltage is selected by the software (by setting the LD1 and LD0 bits of BLDCON)

LD1	LD0	Judgment voltage (V)	Remarks
1	0	4.5 ±0.1	Ta = 25°C
1	1	5.1 ±0.1	Ta = 25°C

o. Timers and counter

- 8-bit timer: 2
  Selectable as auto-reload mode/clock frequency measurement mode
- Watchdog timer: 1
- 100 Hz timer: 1
  Measurable in steps of 1/100 sec.
- 15-bit time-base counter: 1
  1, 2, 4, 8, 16, 32, 64, and 128 Hz signals can be read

p. Serial port

- Mode: Selectable as UART mode, synchronous mode
- UART communication speed: 1200 bps, 2400 bps, 4800 bps, 9600 bps
- Clock frequency in synchronous mode: Internal clock mode (32.768 kHz), external clock frequency
- Data length: 5 to 8 bits

q. Shift register

- Shift clock: 1 × or 1/2 × System clock, external clock
- Data length: 8 bits

r. Interrupt factors

- External interrupt: 5
- Internal interrupt: 12

s. Operating temperature: –20 to +70°C

t. Power supply voltage: 3.5 to 7.2 V

u. Package:

- Chip (212 pads): (Product name: ML63295A-xxxWA)
- 240-pin plastic QFP (QFP240-P-3232-0.50-BK4): (Product name: ML63295A-xxxGA) … under consideration
  xxx indicates the code number.

1.3 Function List

Table 1-1 lists the ML63295A functions. The solid black circles within the chart indicate that the product has the particular function.

Table 1-1 Function List

Function		Symbol	ML63295A	Reference page
ROM (× 16 bits)		ROM	3276	→2-7
RAM (× 4 bits)		RAM	2048	→2-8
STACK RAM	Call	STACK	16 levels	→2-5
	Register		16 levels	→2-6
System reset generation circuit		RST	●	→3-2
Interrupt		INT	●	→4-1
Clock generator circuit		OSC	●	→5-1
Time base counter		TBC	●	→6-1
Timers		TIMER	● (2ch)	→7-1
100 Hz timer counter		100HzTC	●	→8-1
Watchdog timer		WDT	●	→9-1
Input port		INPUT PORT	2 ports × 4 bits	—
	Port 0	P0	●	→10-2
	Port 1	P1	●	→10-2
Output port		OUTPUT PORT	6 ports × 4 bits	—
	Port 2	P2	●	→10-9
	Port 3	P3	●	
	Port 4	P4	●	→10-13
	Port 5	P5	●	
	Port 6	P6	●	
	Port 7	P7	●	
I/O port		I/O PORT	6 ports × 4 bits	—
	Port 8	P8	●	→10-21
	Port 9	P9	●	
	Port A	PA	●	
	Port B	PB	●	→10-30
	Port C	PC	●	→10-37
	Port E	PE	●	→10-45
External memory interface		EXTMEM	●	→11-1
Melody driver		MELODY	●	→12-1
Serial port		SIO	●	→13-1
Shift register		SFT	●	→14-1
LCD driver	COM	LCD	32 lines	→15-1
	SEG		96 lines	
Display register (× 4 bits)		DSPR	768	→15-4
Bias generator		BIAS	●	→15-6
Multiplication/division circuit		MULDIV	●	→16-1
Battery low detect circuit		BLD	●	→17-1
Power supply circuit		POWER	●	→18-1

1.4 Block Diagram

Asterisks (*) indicate port secondary functions. Signal names enclosed by chain lines (·····) indicate interface signals of the V_{DDI} power supply system. Signal names enclosed by ▭ indicate signals of the V_{DDE} power supply system.

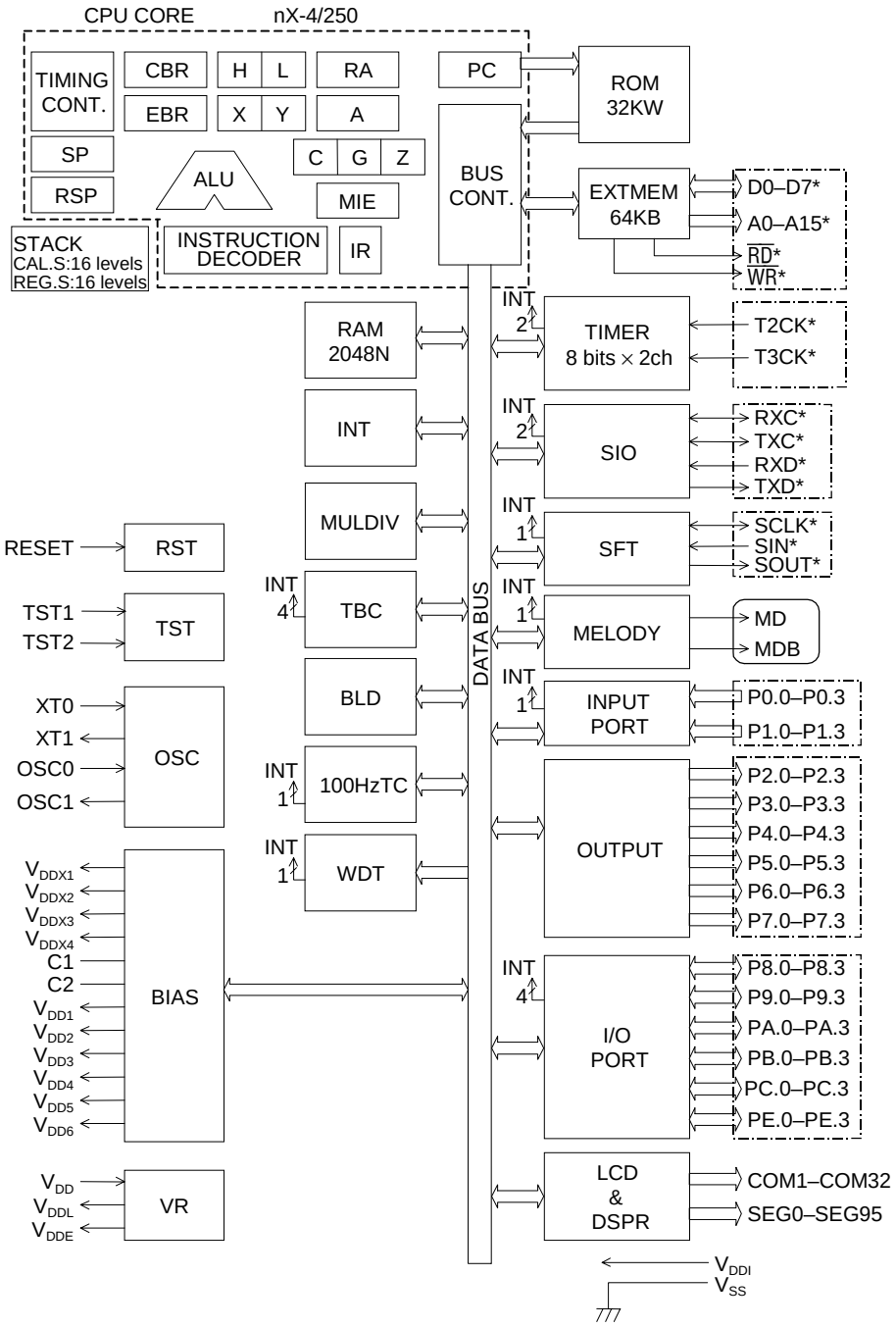


Figure 1-1 ML63295A Block Diagram

1.5 Pin Configuration

1.5.1 Pin Configuration

The ML63295A pin configuration, chip pin configuration, and pad coordinates are shown in Figures 1-2, 1-3, and Table 1-2, respectively.

NC (not connected) indicates an unused pin that is left unconnected (open).

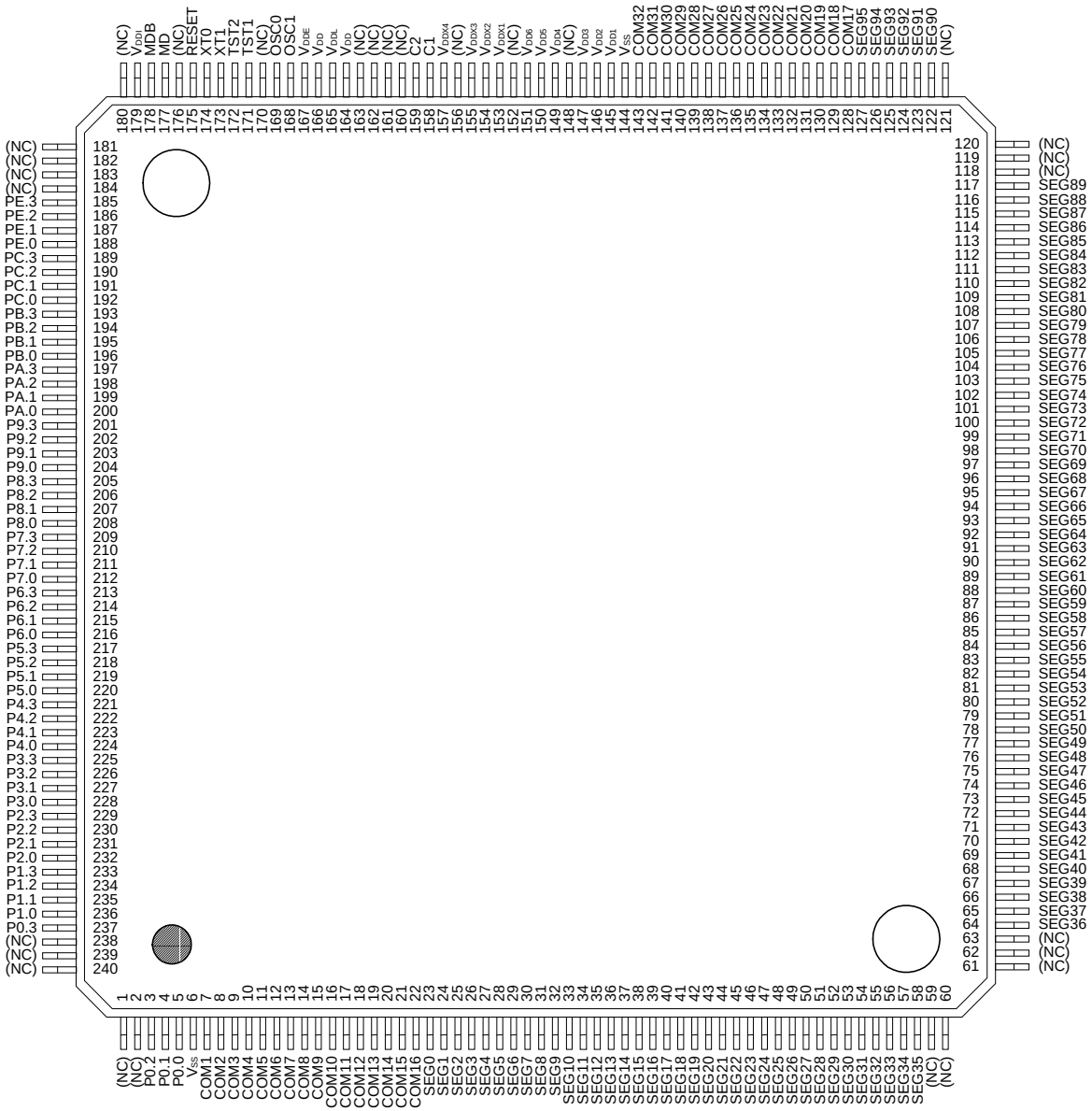
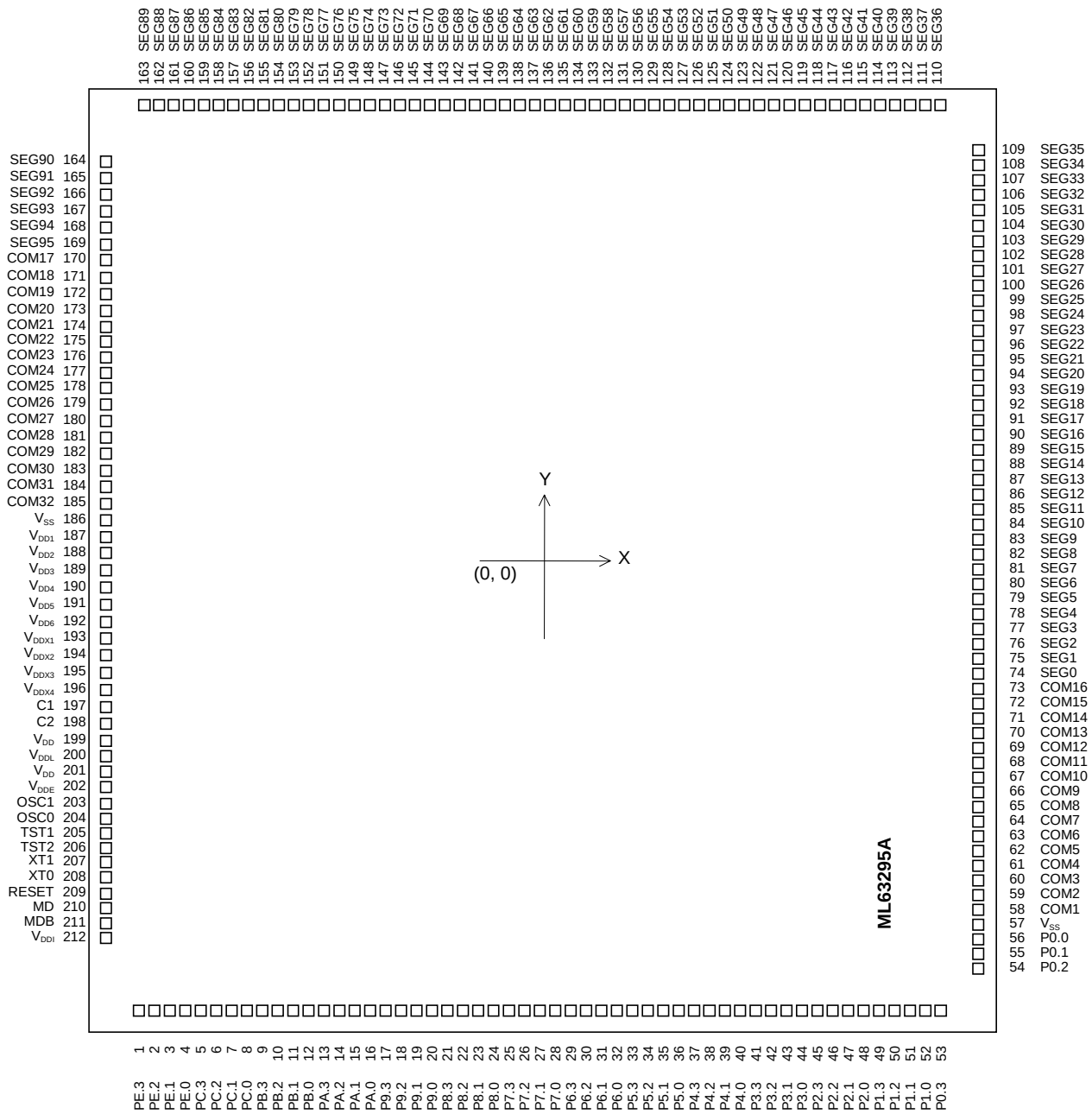


Figure 1-2 ML63295A 240-Pin QFP Pin Configuration (Top View)
(GA: QFP240-P-3232-0.50-BK4)



- Chip size : 8.25 mm × 8.20 mm
- Chip thickness : 350 μm (280 μm: available as required)
- Coordinate origin : center of chip
- Pad hole size : 100 μm × 100 μm
- Pad size : 110 μm × 110 μm
- Minimum pad pitch : 120 μm

Note: The chip substrate voltage is V_{SS}.

Figure 1-3 ML63295A Chip Pin Configuration (Top View)

Table 1-2 ML63295A Pad Coordinates

Center of chip: X = 0, Y = 0

Pad No.	Pad Name	X (µm)	Y (µm)
1	PE.3	–3138	–3905
2	PE.2	–3018	–3905
3	PE.1	–2898	–3905
4	PE.0	–2778	–3905
5	PC.3	–2658	–3905
6	PC.2	–2538	–3905
7	PC.1	–2418	–3905
8	PC.0	–2298	–3905
9	PB.3	–2178	–3905
10	PB.2	–2058	–3905
11	PB.1	–1938	–3905
12	PB.0	–1818	–3905
13	PA.3	–1698	–3905
14	PA.2	–1578	–3905
15	PA.1	–1458	–3905
16	PA.0	–1338	–3905
17	P9.3	–1218	–3905
18	P9.2	–1098	–3905
19	P9.1	–978	–3905
20	P9.0	–858	–3905
21	P8.3	–738	–3905
22	P8.2	–618	–3905
23	P8.1	–498	–3905
24	P8.0	–378	–3905
25	P7.3	–258	–3905
26	P7.2	–138	–3905
27	P7.1	–18	–3905
28	P7.0	102	–3905
29	P6.3	222	–3905
30	P6.2	342	–3905
31	P6.1	462	–3905
32	P6.0	582	–3905
33	P5.3	702	–3905
34	P5.2	822	–3905
35	P5.1	942	–3905
36	P5.0	1062	–3905
37	P4.3	1182	–3905
38	P4.2	1302	–3905
39	P4.1	1422	–3905
40	P4.0	1542	–3905
41	P3.3	1662	–3905
42	P3.2	1782	–3905
43	P3.1	1902	–3905
44	P3.0	2022	–3905
45	P2.3	2142	–3905
46	P2.2	2262	–3905
47	P2.1	2382	–3905
48	P2.0	2502	–3905
49	P1.3	2622	–3905
50	P1.2	2742	–3905
51	P1.1	2862	–3905
52	P1.0	2982	–3905
53	P0.3	3102	–3905
54	P0.2	3965	–3281
55	P0.1	3965	–3161
56	P0.0	3965	–3041
57	V_{SS}	3965	–2907
58	COM1	3965	–2766
59	COM2	3965	–2646
60	COM3	3965	–2526
61	COM4	3965	–2406
62	COM5	3965	–2286
63	COM6	3965	–2166
64	COM7	3965	–2046
65	COM8	3965	–1926
66	COM9	3965	–1806
67	COM10	3965	–1686
68	COM11	3965	–1566
69	COM12	3965	–1446
70	COM13	3965	–1326
71	COM14	3965	–1206
72	COM15	3965	–1086
73	COM16	3965	–966
74	SEG0	3965	–846
75	SEG1	3965	–726
76	SEG2	3965	–606
77	SEG3	3965	–486
78	SEG4	3965	–366
79	SEG5	3965	–246
80	SEG6	3965	–126
81	SEG7	3965	–6
82	SEG8	3965	114
83	SEG9	3965	234
84	SEG10	3965	354
85	SEG11	3965	474
86	SEG12	3965	594

Table 1-2 ML63295A Pad Coordinates (continued)

Center of chip: X = 0, Y = 0

Pad No.	Pad Name	X (μm)	Y (μm)
87	SEG13	3965	714
88	SEG14	3965	834
89	SEG15	3965	954
90	SEG16	3965	1074
91	SEG17	3965	1194
92	SEG18	3965	1314
93	SEG19	3965	1434
94	SEG20	3965	1554
95	SEG21	3965	1674
96	SEG22	3965	1794
97	SEG23	3965	1914
98	SEG24	3965	2034
99	SEG25	3965	2154
100	SEG26	3965	2274
101	SEG27	3965	2394
102	SEG28	3965	2514
103	SEG29	3965	2634
104	SEG30	3965	2754
105	SEG31	3965	2874
106	SEG32	3965	2994
107	SEG33	3965	3114
108	SEG34	3965	3234
109	SEG35	3965	3354
110	SEG36	3185	3905
111	SEG37	3065	3905
112	SEG38	2945	3905
113	SEG39	2825	3905
114	SEG40	2705	3905
115	SEG41	2585	3905
116	SEG42	2465	3905
117	SEG43	2345	3905
118	SEG44	2225	3905
119	SEG45	2105	3905
120	SEG46	1985	3905
121	SEG47	1865	3905
122	SEG48	1745	3905
123	SEG49	1625	3905
124	SEG50	1505	3905
125	SEG51	1385	3905
126	SEG52	1265	3905
127	SEG53	1145	3905
128	SEG54	1025	3905
129	SEG55	905	3905
130	SEG56	785	3905
131	SEG57	665	3905
132	SEG58	545	3905
133	SEG59	425	3905
134	SEG60	305	3905
135	SEG61	185	3905
136	SEG62	65	3905
137	SEG63	–55	3905
138	SEG64	–175	3905
139	SEG65	–295	3905
140	SEG66	–415	3905
141	SEG67	–535	3905
142	SEG68	–655	3905
143	SEG69	–775	3905
144	SEG70	–895	3905
145	SEG71	–1015	3905
146	SEG72	–1135	3905
147	SEG73	–1255	3905
148	SEG74	–1375	3905
149	SEG75	–1495	3905
150	SEG76	–1615	3905
151	SEG77	–1735	3905
152	SEG78	–1855	3905
153	SEG79	–1975	3905
154	SEG80	–2095	3905
155	SEG81	–2215	3905
156	SEG82	–2335	3905
157	SEG83	–2455	3905
158	SEG84	–2575	3905
159	SEG85	–2695	3905
160	SEG86	–2815	3905
161	SEG87	–2935	3905
162	SEG88	–3055	3905
163	SEG89	–3175	3905
164	SEG90	–3965	3432
165	SEG91	–3965	3312
166	SEG92	–3965	3192
167	SEG93	–3965	3072
168	SEG94	–3965	2952
169	SEG95	–3965	2832
170	COM17	–3965	2712
171	COM18	–3965	2592
172	COM19	–3965	2472
173	COM20	–3965	2352
174	COM21	–3965	2232

Table 1-2 ML63295A Pad Coordinates (continued)

Center of chip: X = 0, Y = 0

Pad No.	Pad Name	X (μm)	Y (μm)
175	COM22	–3965	2112
176	COM23	–3965	1992
177	COM24	–3965	1872
178	COM25	–3965	1752
179	COM26	–3965	1632
180	COM27	–3965	1512
181	COM28	–3965	1392
182	COM29	–3965	1272
183	COM30	–3965	1152
184	COM31	–3965	1032
185	COM32	–3965	912
186	V_{SS}	–3965	730
187	V_{DD1}	–3965	580
188	V_{DD2}	–3965	430
189	V_{DD3}	–3965	280
190	V_{DD4}	–3965	130
191	V_{DD5}	–3965	–20
192	V_{DD6}	–3965	–170
193	V_{DDX1}	–3965	–320
194	V_{DDX2}	–3965	–470
195	V_{DDX3}	–3965	–620
196	V_{DDX4}	–3965	–770
197	C1	–3965	–920
198	C2	–3965	–1070
199	V_{DD}	–3965	–1220
200	V_{DDL}	–3965	–1370
201	V_{DD}	–3965	–1520
202	V_{DDE}	–3965	–1670
203	OSC1	–3965	–1924
204	OSC0	–3965	–2074
205	TST1	–3965	–2268
206	TST2	–3965	–2388
207	XT1	–3965	–2593
208	XT0	–3965	–2743
209	RESET	–3965	–2912
210	MD	–3965	–3120
211	MDB	–3965	–3240
212	V_{DDI}	–3965	–3392

1.6 Pin Descriptions

1.6.1 Descriptions of the Basic Functions of Each Pin

The basic functions of each pin of the ML63295A are listed in Table 1-3. Use of a slash ("/") in a pin name indicates that the pin has a secondary function. Refer to section 1.6.2, "Descriptions of the Secondary Functions of Each Pin."

In the I/O column, "—" indicates a power supply pin, "I" indicates an input pin, "O" indicates an output pin, and "I/O" indicates an input/output pin.

Table 1-3 Pin Description (Basic Functions)

Classification	Pin name	Pin No.	Pad No.	I/O	Function
Power supply	V_{DD}	164, 166	199, 201	—	Positive power supply pin
	V_{SS}	6, 144	57, 186	—	Negative power supply pin
	V_{DD1}	145	187	—	Power supply pins for LCD bias voltage (internally generated): Capacitors (1.0 μF) should be connected between these pins and V_{SS}.
	V_{DD2}	146	188		
	V_{DD4}	149	190		
	V_{DD5}	150	191		
	V_{DD6}	151	192		
	V_{DDX1}	153	193	—	Positive power supply for low-speed oscillation.
	V_{DD3}	147	189	—	Power supply pins for LCD bias voltage generation: Capacitors (1.0 μF) should be connected between these pins and V_{SS}.
	V_{DDX4}	157	196		
	C1	158	197	—	Capacitor connection pins for LCD bias voltage generation: A capacitor (1.0 μF) should be connected between C1 and C2, and between V_{DDX2} and V_{DDX3}.
	C2	159	198		
	V_{DDX2}	154	194	—	
	V_{DDX3}	155	195		
	V_{DDI}	179	212	—	Positive power supply pin for external interface (Power supply for input, output, and input-output ports)
	V_{DDL}	165	200	—	Positive power supply pin for internal logic (internally generated): A capacitor (0.1 μF) should be connected between this pin and V_{SS}.
	V_{DDE}	167	202	—	Constant voltage output pin: A capacitor (1.0 μF) should be connected between this pin and V_{SS}.
Oscillator	XT0	174	208	I	Low-speed clock oscillation pins: An option for using crystal oscillation or RC oscillation is chosen by the mask option. If the crystal oscillation is chosen, a crystal should be connected between XT0 and XT1, and capacitor (C_G) should be connected between XT0 and V_{SS}. If the RC oscillation is chosen, external oscillation resistor (R_{OSL}) should be connected between XT0 and XT1.
	XT1	173	207	O	
	OSC0	169	204	I	High-speed clock oscillation pins: Either a ceramic resonator and capacitors (C_{L0}, C_{L1}) or an external oscillation resistor (R_{OSH}) should be connected to these pins.
	OSC1	168	203	O	

Table 1-3 Pin Description (Basic Functions) (continued)

Classification	Pin name	Pin No.	Pad No.	I/O	Function
Test	TST1	171	205	I	Input pins for testing: A pull-down resistor is internally connected to these pins.
	TST2	172	206	I	
Reset	RESET	175	209	I	System reset input pin: Setting this pin to "H" level puts this device into a reset state. Then, setting this pin to "L" level starts executing an instruction from address 0000H. A pull-down resistor is internally connected to this pin.
Melody	MD	177	210	O	Melody output pin (non-inverted output)
	MDB	178	211	O	Melody output pin (inverted output)
Port	P0.0/INT5	5	56	I	4-bit input ports: Each bit can be selected as the following. • Input with pull-up resistor • Input with pull-down resistor • High-impedance input
	P0.1/INT5	4	55		
	P0.2/INT5	3	54		
	P0.3/INT5	237	53		
	P1.0/INT5	236	52	I	
	P1.1/INT5	235	51		
	P1.2/INT5	234	50		
	P1.3/INT5	233	49		
	P2.0	232	48	O	4-bit output ports: P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	P2.1	231	47		
	P2.2	230	46		
	P2.3	229	45		
	P3.0	228	44	O	
	P3.1	227	43		
	P3.2	226	42		
	P3.3	225	41		
	P4.0/A0	224	40	O	
	P4.1/A1	223	39		
	P4.2/A2	222	38		
	P4.3/A3	221	37		
	P5.0/A4	220	36	O	
	P5.1/A5	219	35		
	P5.2/A6	218	34		
	P5.3/A7	217	33		
	P6.0/A8	216	32	O	
	P6.1/A9	215	31		
	P6.2/A10	214	30		
	P6.3/A11	213	29		
	P7.0/A12	212	28	O	
	P7.1/A13	211	27		
	P7.2/A14	210	26		
	P7.3/A15	209	25		

Table 1-3 Pin Description (Basic Functions) (continued)

Classification	Pin name	Pin No.	Pad No.	I/O	Function
Port	P8.0/$\overline{RD}$	208	24	I/O	4-bit I/O ports: During the input mode, each bit can be selected as the following. • Input with pull-up resistor • Input with pull-down resistor • High-impedance input During the output mode, each bit can be selected as the following. • P-channel open drain output • N-channel open drain output • CMOS output • High-impedance output
	P8.1/$\overline{WR}$	207	23		
	P8.2	206	22		
	P8.3/INT4	205	21		
	P9.0/D0	204	20	I/O	
	P9.1/D1	203	19		
	P9.2/D2	202	18		
	P9.3/D3	201	17		
	PA.0/D4	200	16	I/O	
	PA.1/D5	199	15		
	PA.2/D6	198	14		
	PA.3/D7	197	13		
	PB.0/INT0	196	12	I/O	
	PB.1/INT0	195	11		
	PB.2/INT0/ T2CK	194	10		
	PB.3/INT0/ T3CK	193	9		
	PC.0/INT1/ RXD	192	8	I/O	
	PC.1/INT1/ TXC	191	7		
	PC.2/INT1/ RXC	190	6		
	PC.3/INT1/ TXD	189	5		
	PE.0/SIN	188	4	I/O	
	PE.1/SOUT	187	3		
	PE.2/SCLK	186	2		
	PE.3/INT2	185	1		

Table 1-5 Pin Description (Basic Functions) (continued)

Classification	Pin name	Pin No.	Pad No.	I/O	Function
LCD	COM1	7	58	O	LCD common signal output pins (COM1 to COM32)
	COM2	8	59		
	COM3	9	60		
	COM4	10	61		
	COM5	11	62		
	COM6	12	63		
	COM7	13	64		
	COM8	14	65		
	COM9	15	66		
	COM10	16	67		
	COM11	17	68		
	COM12	18	69		
	COM13	19	70		
	COM14	20	71		
	COM15	21	72		
	COM16	22	73		
	COM17	128	170		
	COM18	129	171		
	COM19	130	172		
	COM20	131	173		
	COM21	132	174		
	COM22	133	175		
	COM23	134	176		
	COM24	135	177		
	COM25	136	178		
	COM26	137	179		
	COM27	138	180		
	COM28	139	181		
	COM29	140	182		
	COM30	141	183		
	COM31	142	184		
	COM32	143	185		

Table 1-3 Pin Description (Basic Functions) (continued)

Classification	Pin name	Pin No.	Pad No.	I/O	Function
LCD	SEG0	23	74	O	LCD segment signal output pins (SEG0 to SEG47)
	SEG1	24	75		
	SEG2	25	76		
	SEG3	26	77		
	SEG4	27	78		
	SEG5	28	79		
	SEG6	29	80		
	SEG7	30	81		
	SEG8	31	82		
	SEG9	32	83		
	SEG10	33	84		
	SEG11	34	85		
	SEG12	35	86		
	SEG13	36	87		
	SEG14	37	88		
	SEG15	38	89		
	SEG16	39	90		
	SEG17	40	91		
	SEG18	41	92		
	SEG19	42	93		
	SEG20	43	94		
	SEG21	44	95		
	SEG22	45	96		
	SEG23	46	97		
	SEG24	47	98		
	SEG25	48	99		
	SEG26	49	100		
	SEG27	50	101		
	SEG28	51	102		
	SEG29	52	103		
	SEG30	53	104		
	SEG31	54	105		
	SEG32	55	106		
	SEG33	56	107		
	SEG34	57	108		
	SEG35	58	109		
	SEG36	64	110		
	SEG37	65	111		
	SEG38	66	112		
	SEG39	67	113		
	SEG40	68	114		
	SEG41	69	115		
	SEG42	70	116		
	SEG43	71	117		
	SEG44	72	118		
	SEG45	73	119		
	SEG46	74	120		
	SEG47	75	121		

Table 1-5 Pin Description (Basic Functions) (continued)

Classification	Pin name	Pin No.	Pad No.	I/O	Function
LCD	SEG48	76	122	O	LCD segment signal output pins (SEG48 to SEG95)
	SEG49	77	123		
	SEG50	78	124		
	SEG51	79	125		
	SEG52	80	126		
	SEG53	81	127		
	SEG54	82	128		
	SEG55	83	129		
	SEG56	84	130		
	SEG57	85	131		
	SEG58	86	132		
	SEG59	87	133		
	SEG60	88	134		
	SEG61	89	135		
	SEG62	90	136		
	SEG63	91	137		
	SEG64	92	138		
	SEG65	93	139		
	SEG66	94	140		
	SEG67	95	141		
	SEG68	96	142		
	SEG69	97	143		
	SEG70	98	144		
	SEG71	99	145		
	SEG72	100	146		
	SEG73	101	147		
	SEG74	102	148		
	SEG75	103	149		
	SEG76	104	150		
	SEG77	105	151		
	SEG78	106	152		
	SEG79	107	153		
	SEG80	108	154		
	SEG81	109	155		
	SEG82	110	156		
	SEG83	111	157		
	SEG84	112	158		
	SEG85	113	159		
	SEG86	114	160		
	SEG87	115	161		
	SEG88	116	162		
	SEG89	117	163		
	SEG90	122	164		
	SEG91	123	165		
	SEG92	124	166		
	SEG93	125	167		
	SEG94	126	168		
	SEG95	127	169		

1.6.2 Descriptions of the Secondary Functions of Each Pin

The secondary functions of each pin of the ML63295A are listed in Table 1-4.

Table 1-4 Pin Description (Secondary Functions)

Classification	Pin name	Pin No.	Pad No.	I/O	Function
External interrupt	PB.0/INT0	196	12	I	External interrupt 0 input pins: The change of input signal level causes an interrupt to occur. The Port B Interrupt Enable register (PBIE) enables or disables an interrupt for each bit.
	PB.1/INT0	195	11		
	PB.2/INT0	194	10		
	PB.3/INT0	193	9		
	PC.0/INT1	192	8	I	External interrupt 1 input pins: The change of input signal level causes an interrupt to occur. The Port C Interrupt Enable register (PCIE) enables or disables an interrupt for each bit.
	PC.1/INT1	191	7		
	PC.2/INT1	190	6		
	PC.3/INT1	189	5		
	PE.3/INT2	185	1	I	External interrupt 2 input pin: The change of input signal level causes an interrupt to occur.
	P8.3/INT4	205	21	I	External interrupt 4 input pin: The change of input signal level causes an interrupt to occur.
	P0.0/INT5	5	56	I	External interrupt 5 input pins: The change of input signal level causes an interrupt to occur. The Port 0 Interrupt Enable register (P0IE) and Port 1 Interrupt Enable register (P1IE) enable or disable an interrupt for each bit.
	P0.1/INT5	4	55		
	P0.2/INT5	3	54		
	P0.3/INT5	237	53		
	P1.0/INT5	236	52		
	P1.1/INT5	235	51		
	P1.2/INT5	234	50		
	P1.3/INT5	233	49		
Timer	PB.2/T2CK	194	10	I	External clock input pin for timer 2
	PB.3/T3CK	193	9	I	External clock input pin for timer 3

Table 1-4 Pin Description (Secondary Functions) (continued)

Classification	Pin name	Pin No.	Pad No.	I/O	Function
Serial port	PC.0/RXD	192	8	I	Serial port receive data input pin
	PC.1/TXC	191	7	I/O	Sync serial port clock input-output pin: Transmit clock output when this device is used as a master processor. Transmit clock input when this device is used as a slave processor.
	PC.2/RXC	190	6	I/O	Sync serial port clock input-output pin: Receive clock output when this device is used as a master processor. Receive clock input when this device is used as a slave processor.
	PC.3/TXD	189	5	O	Serial port transmit data output pin
Shift register	PE.0/SIN	188	4	I	Shift register receive data input pin
	PE.1/SOUT	187	3	O	Shift register transmit data output pin
	PE.2/SCLK	186	2	I/O	Shift register clock input-output pin: Clock output when this device is used as a master processor. Clock input when this device is used as a slave processor.
External memory	P4.0/A0	224	40	O	Address output bus for external memory
	P4.1/A1	223	39		
	P4.2/A2	222	38		
	P4.3/A3	221	37		
	P5.0/A4	220	36		
	P5.1/A5	219	35		
	P5.2/A6	218	34		
	P5.3/A7	217	33		
	P6.0/A8	216	32		
	P6.1/A9	215	31		
	P6.2/A10	214	30		
	P6.3/A11	213	29		
	P7.0/A12	212	28		
	P7.1/A12	211	27		
	P7.2/A14	210	26		
	P7.3/A15	209	25		
	P9.0/D0	204	20	I/O	Data bus for external memory
	P9.1/D1	203	19		
	P9.2/D2	202	18		
	P9.3/D3	201	17		
	PA.0/D4	200	16		
	PA.1/D5	199	15		
	PA.2/D6	198	14		
	PA.3/D7	197	13		
	P8.0/$\overline{RD}$	208	24	O	Read signal output pin for external memory (negative logic)
	P8.1/$\overline{WR}$	207	23	O	Write signal output pin for external memory (negative logic)

1.6.3 Handling of Unused Pins

Table 1-5 shows how unused pins should be handled.

Table 1-5 Handling of Unused Pins

Pin	Recommended pin handling
OSC0, OSC1	Open
C1, C2	Open
V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DD5}, V_{DD6}	Open
V_{DDX2}, V_{DDX3}, V_{DDX4}	Open
TST1, TST2	Open or connect to V_{SS}
P0.0–P0.3	Open
P1.0–P1.3	Open
P2.0–P2.3	Open
P3.0–P3.3	Open
P4.0–P4.3	Open
P5.0–P5.3	Open
P6.0–P6.3	Open
P7.0–P7.3	Open
P8.0–P8.3	Open
P9.0–P9.3	Open
PA.0–PA.3	Open
PB.0–PB.3	Open
PC.0–PC.3	Open
PE.0–PE.3	Open
MD, MDB	Open
COM1–COM32	Open
SEG0–SEG95	Open

Notes:

1. If a pin set as a high impedance input is left unconnected, the supply current may become excessive. Therefore, it is recommended that unused input ports and input/output ports be set as inputs with either a pull-down or pull-up resistor.
2. When test pins TST1 and TST2 are left unconnected, malfunction may result if there is a large amount of external noise. Therefore, it is recommended to permanently connect TST1 and TST2 to V_{SS}.
3. Connect a capacitor (0.1 µF) between the V_{DDX1} pin and the V_{SS} pin when the LCD drivers are not used.

1.7 Basic Timing

1.7.1 Basic Timing of CPU Operation

The low-speed oscillation clock from the XT0/XT1 pins or the high-speed oscillation clock from the OSC0/OSC1 pins are used without frequency division as the system clock (CLK). The system clock signal is in phase with the signal from the XT1 pin or the OSC1 pin.

As shown in Figure 1-4, a single machine cycle is composed of two states, S1 and S2. One state is the interval from a falling edge of CLK to the falling edge of the next CLK.

Instructions are processed in machine cycle units and each instruction is executed in 1 to 3 machine cycles. Instructions are classified according to the number of machine cycles: 1-machine-cycle instructions (M1), 2-machine-cycle instructions (M1 + M2), and 3-machine-cycle instructions (M1 + M2 + M3).

Most instructions are executed in 1 machine cycle.

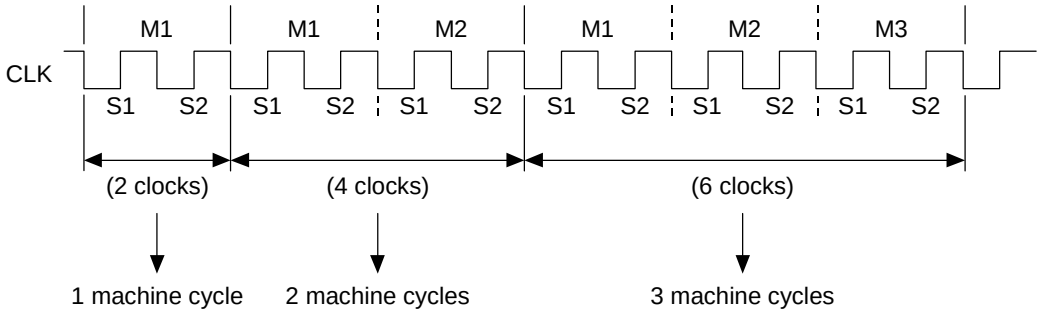


Figure 1-4 Clock Configuration of Each Machine Cycle

1.7.2 Port I/O Basic Timing

Figure 1-5 shows the basic I/O timing.

During the execution of an instruction that outputs data to a port, setting data (data A) is output at the rising edge of the clock in the S2 state during the machine cycle of that instruction.

During the execution of an instruction that inputs data from a port, data at the input pin (data B) is captured internally while the clock is at a "H" level in the S1 state during the machine cycle of that instruction. That data is transferred to the accumulator at the start of the next machine cycle.

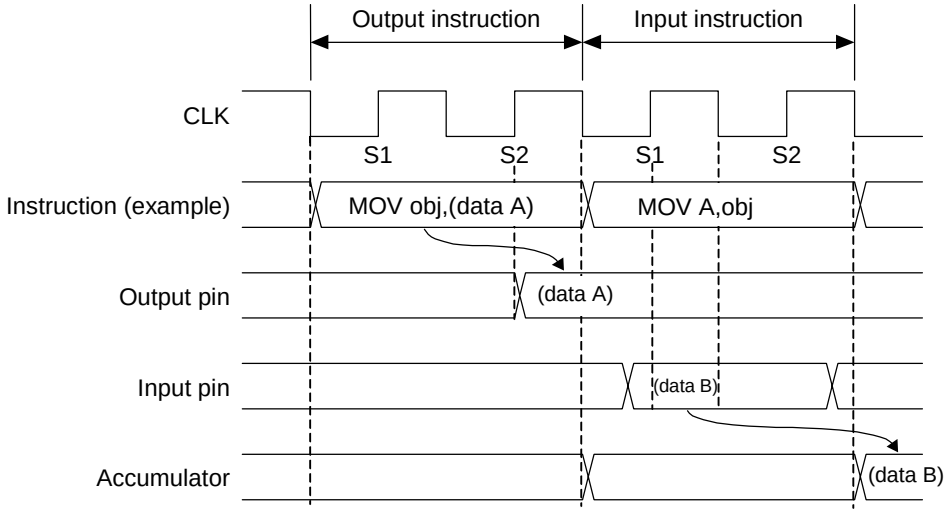


Figure 1-5 Port I/O Basic Timing

Note:

Regarding input signals

"0" will be captured in the internal register if a "L" level is input to the input pin even once (① of Figure 1-6) during the data capture interval.

"1" will be captured in the internal register only if a "H" level is maintained (② of Figure 1-6) throughout the data capture interval.

Therefore, if noise occurs in the input data, implement noise reduction measures with the program and peripheral devices.

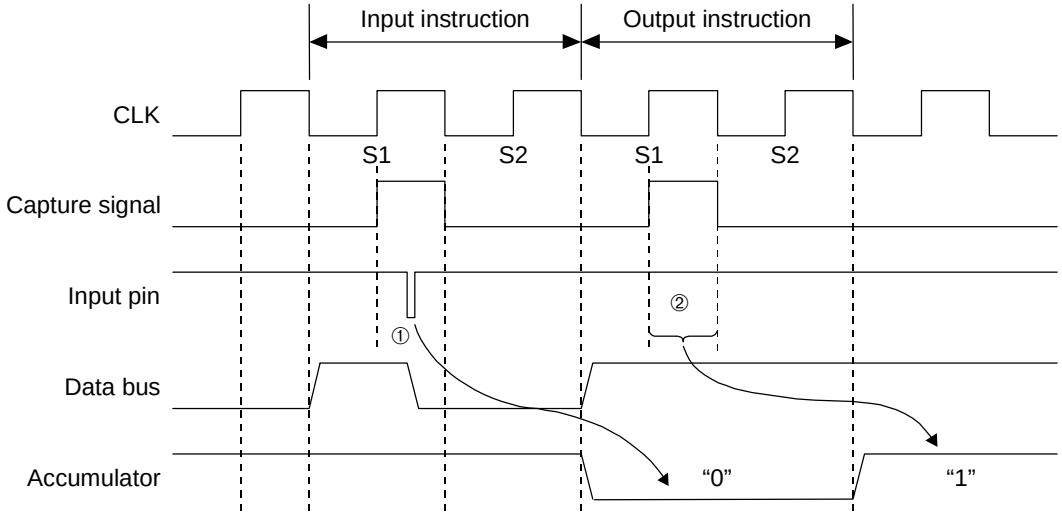


Figure 1-6 Input Data Example

1.7.3 Interrupt Basic Timing

Figure 1-7 shows the basic interrupt timing.

As shown in the figure, when an interrupt factor is generated, the interrupt factor is sampled at the falling edge of CLK and an interrupt request (IRQ) is set at the first half of S1.

When an interrupt condition is established and the CPU receives an interrupt, the interrupt routine will start beginning from the next machine cycle.

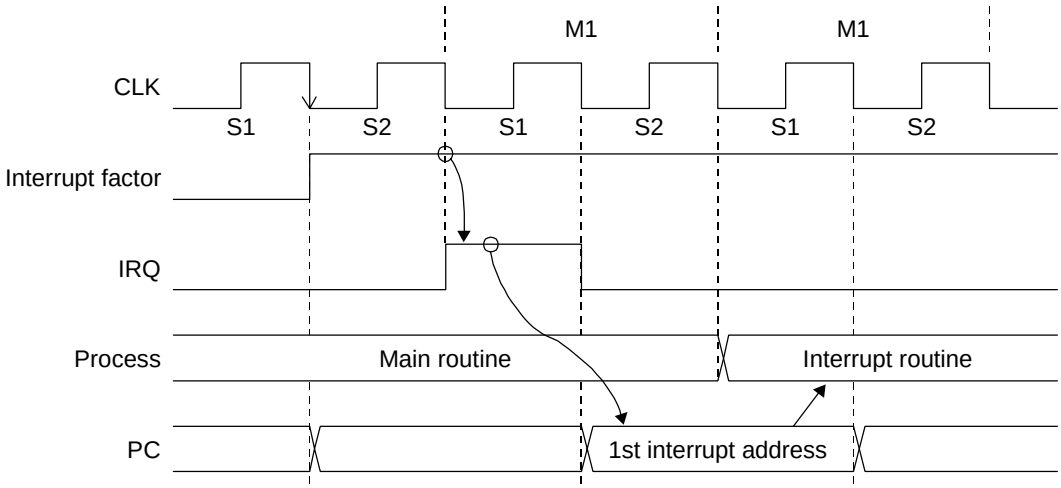


Figure 1-7 Interrupt Basic Timing

Chapter 2

CPU and Memory Spaces

2. CPU and Memory Spaces

2.1 Overview

The ML63295A is equipped with Oki's original CPU core nX-4/250.

The instruction set of the nX-4/250 core consists of 439 types of instructions.

The memory space consists of a 16-bit wide program memory space and a 4-bit wide data memory space. A stack for saving the program counter during a subroutine call or interrupt (call stack) and a stack for saving registers during a PUSH instruction (register stack) are provided separately from the memory space.

The program memory space is used for program data, ROM table data and melody note data.

In the data memory space, special function registers (SFRs) are located in BANK 0, the LCD display register (DSPR) in BANKS 1 to 3, and data RAM in BANKS 4 to 11.

2.2 Registers

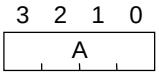
The nX-4/250 core processes data mainly with the accumulator and register set.

The register set is a programming model consisting of the HL and XY registers that store data memory addresses, the current bank register (CBR), the extra bank register (EBR), the RA register that stores program memory addresses, registers that control program flow, and registers that control flags and memory.

2.2.1 Accumulator (A)

The accumulator (A) is the central register for various arithmetic operations.

At system reset, the accumulator is initialized to "0". When an interrupt occurs, a "PUSH HL" instruction can be used if necessary to save the accumulator on the register stack. The accumulator can be restored with a "POP HL" instruction.



Accumulator

2.2.2 Flag Register

The flag register consists of 3 flags: the carry flag (C), the zero flag (Z) and the G flag (G). When an interrupt occurs, a "PUSH HL" instruction can be used if necessary to save the flag register on the register stack. The flag register can be restored with a "POP HL" instruction.

Flag register

2.2.2.1 Carry Flag (C)

The carry flag (C) is a 1-bit flag that is loaded with a carry during addition or a borrow during subtraction. At system reset, the carry flag is initialized to "0".

2.2.2.2 Zero Flag (Z)

The zero flag (Z) is a 1-bit flag that is set to "1" when the contents of the accumulator (A) are loaded with "0H". The zero flag is set to "0" when the contents of the accumulator (A) are loaded with a value other than "0H". However, the XCH instruction does not change the zero flag. At system reset, the zero flag is initialized to "0".

2.2.2.3 G Flag (G)

The G flag (G) changes to "1" when the HL, XY or RA registers overflow as the result of execution of a post-increment register indirect addressing instruction or as the result of an increment instruction for the HL, XY or RA registers. At system reset, the G flag is initialized to "0".

2.2.3 Master Interrupt Enable Flag (MIE)

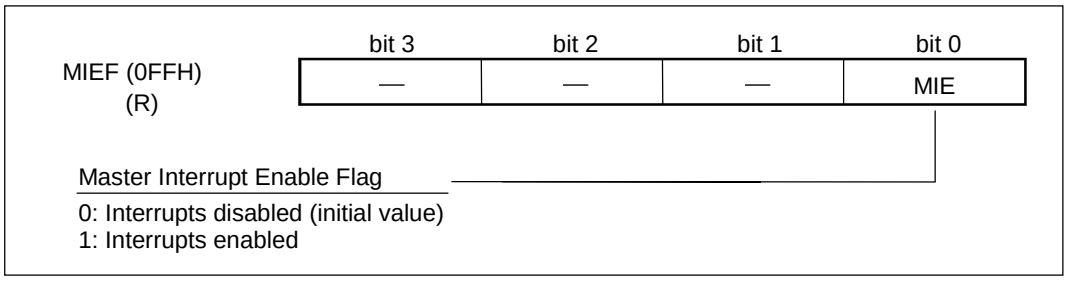
MIE (bit 0 of MIEF) is a flag that disables or enables all interrupts except for the watchdog timer interrupt. MIEF is a 4-bit register in which bit 0 is the master interrupt enable flag (MIE).

If MIE is "0", all interrupts are disabled. If MIE is "1", all interrupts are enabled (with the exception of the watchdog timer).

When any interrupt is received, MIE is cleared to "0". MIE is set to "1" by execution of a return from interrupt instruction (RTI instruction).

If multi-level interrupt processing is to be performed, execute a RTI instruction (MIE←"1") during the interrupt processing routines.

At system reset, MIE is initialized to "0". MIEF only supports data reference (R) of data memory through addressing instructions.



Note:

When setting MIE, use "EI" instructions (MIE← "1") and "DI" instructions (MIE← "0").

2.2.4 Current Bank Register (CBR), Extra Bank Register (EBR), HL Register (HL), XY Register (XY)

The CBR, EBR, HL, and XY registers are used for indirect addressing of data memory.

The CBR and EBR registers indicate the data memory bank. The HL and XY registers indicate addresses in the bank. CBR is also used in combination with 8-bit data in the instruction code for direct addressing within the current bank.

Figure 2-1 shows the various register combinations.

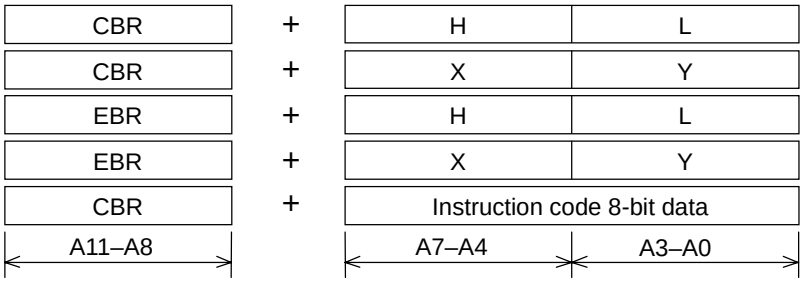


Figure 2-1 Various Register Combinations

A11 to A0 in Figure 2-1 indicate data memory addresses (4K nibbles max.).

At system reset, the CBR, EBR, HL, and XY registers are initialized to "0".

When an interrupt occurs, a "PUSH HL" or "PUSH XY" instruction can be used if necessary to save the CBR, EBR, HL, and XY registers on the register stack. These registers can be restored with a "POP HL" or "POP XY" instruction.

The CBR, EBR, HL, and XY registers are assigned to special function register (SFR) addresses 0F9H to 0FEH.

		bit 3	bit 2	bit 1	bit 0
EBR	(0FEH) (R/W)	e_3	e_2	e_1	e_0
CBR	(0FDH) (R/W)	c_3	c_2	c_1	c_0
H	(0FCH) (R/W)	h_3	h_2	h_1	h_0
L	(0FBH) (R/W)	l_3	l_2	l_1	l_0
X	(0FAH) (R/W)	x_3	x_2	x_1	x_0
Y	(0F9H) (R/W)	y_3	y_2	y_1	y_0

2.2.5 Program Counter (PC)

The program counter (PC) is a counter with 16 valid bits that specifies the program memory space.

2.2.6 RA Registers (RA3, RA2, RA1, RA0)

The RA registers are used for indirect program memory addressing (ROM table reference instructions).

Figure 2-2 shows the address configuration of the RA registers.

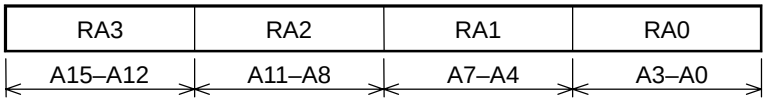
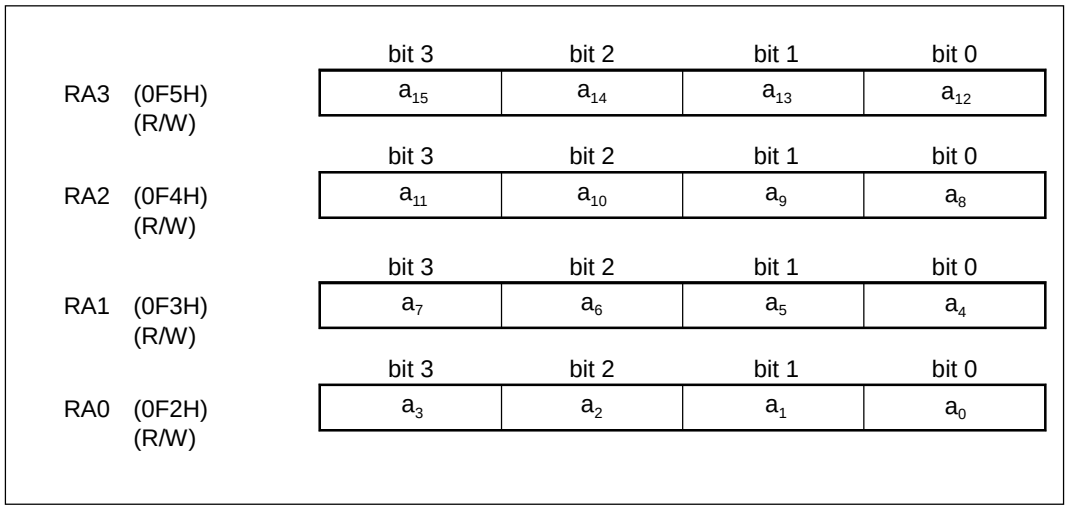


Figure 2-2 Address Configuration of RA3 to RA0 Registers

Within the A15 to A0 of Figure 2-2, A14 to A0 indicate program memory addresses (32K words max.).

RA3 to RA0 are assigned to special function register (SFR) addresses 0F2H to 0F5H.



At system reset, RA3 to RA0 are initialized to "0".

Note:

When executing a ROM table reference instruction that uses RA registers, do not use addresses located in the SFR area to transfer ROM table data to RA registers, otherwise indirect addressing of program memory will not operate properly.

2.2.7 Stack Pointer (SP) and Call Stack

The stack pointer (SP) is a pointer that indicates the call stack address where the program counter is saved when a subroutine call or interrupt occurs.

The SP is a 4-bit up/down counter that is incremented during stack saves and is decremented during stack restores.

The call stack has 16 levels from address 0H to address 0FH. Because the hardware requires 1 level of the call stack during program execution, only 15 levels can be used for stack saves. The contents of the call stack cannot be read or written by the program.

Figure 2-3 shows the relation between SP and the call stack.

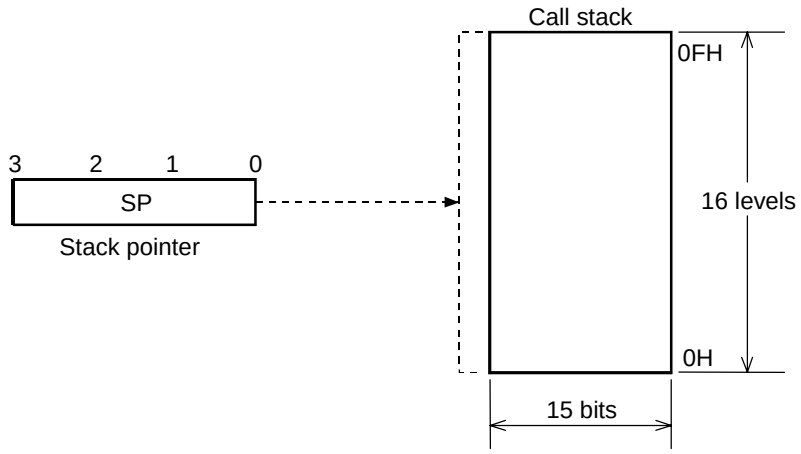


Figure 2-3 Relation between SP and Call Stack

SP is assigned to special function register (SFR) address 0F7H.

	bit 3	bit 2	bit 1	bit 0
SP (0F7H) (R)	SP3	SP2	SP1	SP0

At system reset, SP is initialized to "0" and points to address "0H" of the call stack. SP is a read-only register and writes are invalid.

2.2.8 Register Stack Pointer (RSP) and Register Stack

The register stack pointer (RSP) is a pointer that indicates the register stack address for saving various registers.

RSP is a 4-bit up/down counter that is incremented during stack saves (execution of PUSH instructions) and is decremented during stack restores (execution of POP instructions).

The register stack has 16 levels from address 0H to address 0FH. The contents of the register stack cannot be read or written by the program.

Figure 2-4 shows the relation between RSP and the register stack.

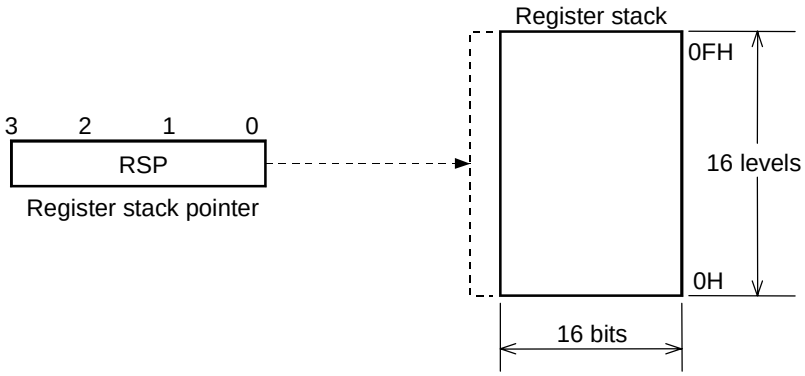


Figure 2-4 Relation between RSP and Register Stack

The various registers shown in Figure 2-5 are saved onto and restored from the register stack by PUSH and POP instructions.

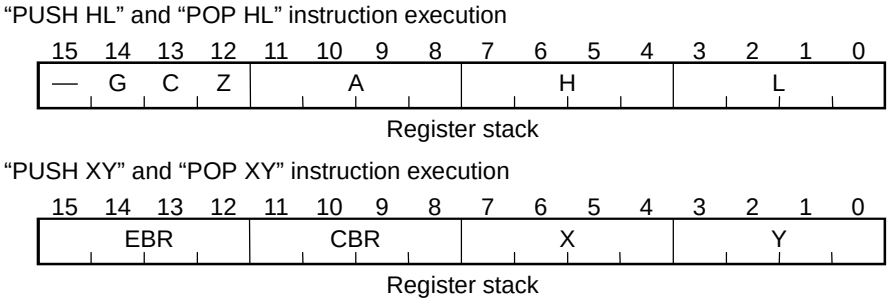


Figure 2-5 Register Save/Restore by Execution of PUSH/POP Instructions

RSP is assigned to special function register (SFR) address 0F6H.

	bit 3	bit 2	bit 1	bit 0
RSP (0F6H) (R/W)	rsp3	rsp2	rsp1	rsp0

At system reset, RSP is initialized to "0" and points to address "0H" of the register stack.

2.3 Memory Spaces

2.3.1 Program Memory Space

The program memory space is the read-only memory that stores program data.

The program memory space has a data length of 16 bits and extends from address 0000H to address 7FFFH.

In addition to program data, the program memory can also store ROM table data and the melody data. Figure 2-6 shows the configuration of the program memory space.

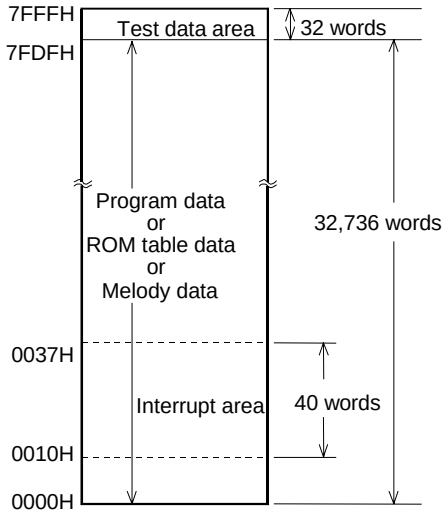


Figure 2-6 Program Memory Space Configuration

After system reset, instruction execution begins at address 0000H. The interrupt area from address 0010H to address 0037H contains starting addresses of the interrupt processing routines that are executed when interrupts are generated. (Refer to Chapter 4, "Interrupt".)

ROM table data is transferred to data memory by ROM table reference instructions.

The melody data defines the tone, tone length, and end tone used in the melody circuit of the ML63295A. After an MSA instruction specifies the starting address, the melody data is automatically transferred to the melody circuit when a melody data interrupt occurs. (Refer to Chapter 12, "Melody Driver".)

Because the test data area contains program data for testing, it cannot be used as a program data area.

2.3.2 Data Memory Space

The data memory space contains data RAM and special function registers (SFRs).

The data memory consists of 10 banks. One bank unit is 256 nibbles. BANK 0 is allocated as a SFR area, BANKS 1 to 3 as the LCD display register, and BANK 4 and the following BANKS are data RAM.

Figure 2-7 shows the configuration of the data memory space.

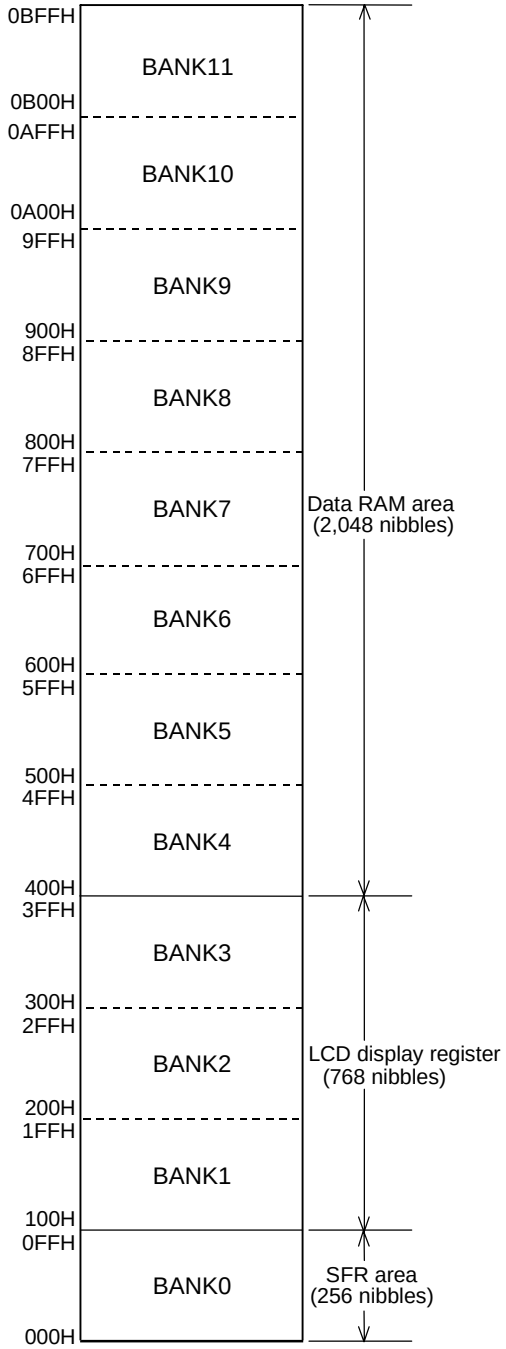


Figure 2-7 Data Memory Space Configuration

2.3.3 External Memory Space

The external memory space has an 8-bit data length, allocated from address 0 to address 0FFFFH.

See Chapter 11 "External Memory Interface".

It is configured as indicated in Figure 2-8.

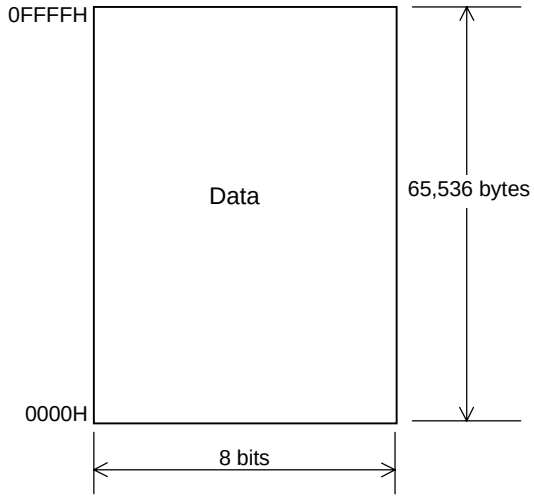


Figure 2-8 External Memory Space Configuration

Chapter 3

CPU Control Functions

3. CPU Control Functions

3.1 Overview

Operating states, including system reset, are classified as follows.

- Normal operation mode
- System reset mode
- Halt mode

Figure 3-1 shows the CPU operating state transition diagram.

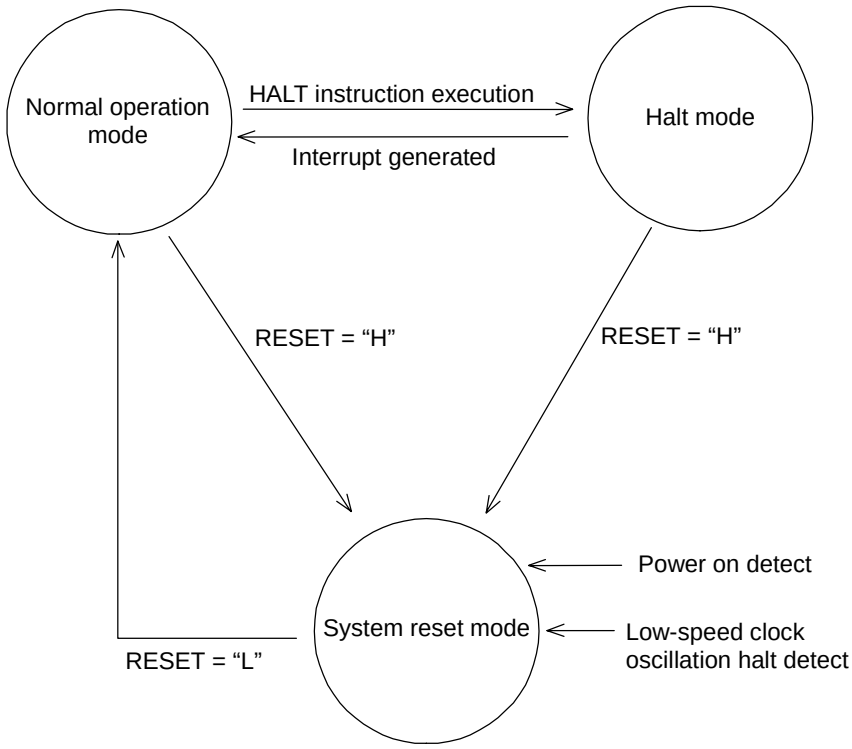


Figure 3-1 Operating State Transition Diagram

The normal operation mode is the state in which the CPU executes instructions sequentially.

The system reset mode begins when a reset input causes the CPU to begin system reset processing where registers and pins are initialized. The CPU remains in this state until instruction execution begins. After system reset processing, instruction execution begins from address 0000H.

The halt mode is the state in which the CPU is halted (instruction execution suspended) but internal peripheral functions continue to operate. During the halt mode, the PC is not incremented. Even upon entering the halt mode, port and peripheral functions will not change. Transfer to the halt mode is accomplished by executing a "HALT" instruction.

3.2 System Reset Mode (RST)

3.2.1 Transfer to and State of System Reset Mode

The following three factors cause a transfer to the system reset mode.

- Setting the RESET pin to a "H" level
- Detection of power on
- Detection of a low-speed clock oscillation halt

The following operations are performed in the system reset mode.

(1) CPU is initialized.
(2) Backup flag changes to "1" and backup circuit changes to ON state.
(3) Bias reference voltage supply (VR) is energized.
(4) All LCD driver outputs are turned OFF and the outputs change to the V_{SS} level.
(5) All special function registers (SFRs) are initialized. However, data RAM and display registers are not initialized.

After system reset processing, instruction execution begins from address 0000H.

Figure 3-2 shows the system reset generator circuit and Figure 3-3 shows the signals when a system reset is generated.

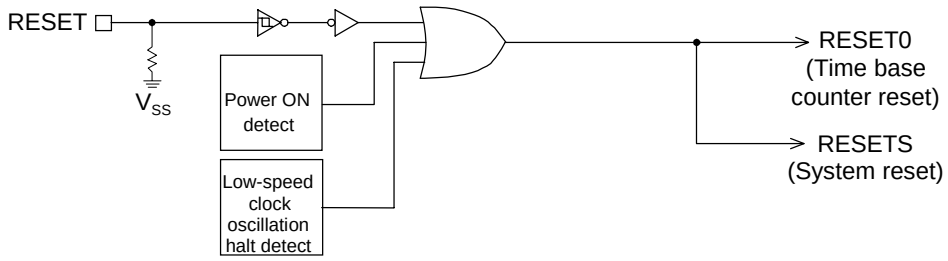


Figure 3-2 System Reset Generator Circuit

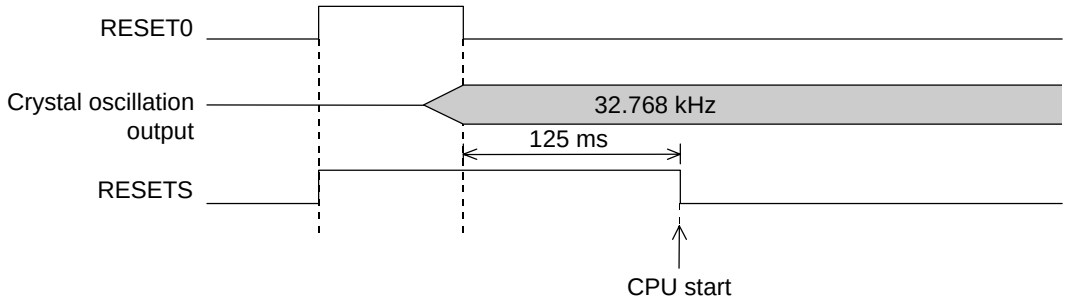


Figure 3-3 Signals When System Reset is Generated

Note:

System reset takes priority over all other processing and terminates all processing up to that point in time. Therefore, the contents of RAM and display registers, which are not initialized, cannot be guaranteed after a system reset.

3.3 Halt Mode

3.3.1 Transfer to and State of Halt Mode

Transfer to the halt mode is performed by the software when a HALT instruction is executed.

When a HALT instruction is executed, the CPU enters the HALT mode at the S2 state of the HALT instruction.

Oscillation and time base counter operation continue while in the halt mode.

If an interrupt request occurs at the same time as execution of a HALT instruction, interrupt processing has priority and the HALT instruction will not be executed. After the HALT instruction performs the equivalent operation of a NOP instruction, the interrupt routine is entered. When an RTI instruction is used to complete the interrupt routine, the main routine is resumed beginning from the instruction immediately following the HALT instruction.

Figure 3-4 shows the timing when a HALT instruction and interrupt request occur simultaneously.

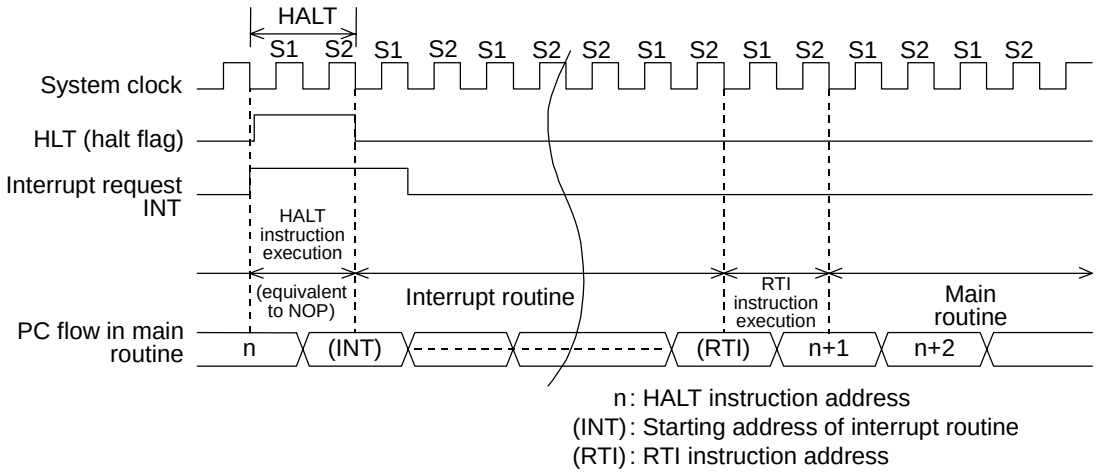


Figure 3-4 Timing of Simultaneous HALT Instruction and Interrupt Request

Note:

While an interrupt request is generated, execution of a HALT instruction will not transfer operation to the halt mode.

3.3.2 Halt Mode Release

The following two methods are available to release the halt mode.

- Release by interrupt generation (transfer to normal operation mode)
- Release by RESET pin (transfer to system reset mode)

3.3.2.1 Release of Halt Mode by Interrupt

If the halt mode is to be released by an interrupt, the enable flag of the interrupt used for release must be set to "1" prior to entering the halt mode. When the halt mode is released by an interrupt, operation transfers to the normal operation mode.

Figure 3-5 shows the timing of transferring to the halt mode by execution of a HALT instruction and of releasing the halt mode by an interrupt.

When the halt mode is released by an interrupt request, the first instruction immediately following the HALT instruction is executed and then the interrupt routine is entered. When an RTI instruction is used to complete the interrupt routine, the main routine is resumed beginning from the second instruction after the HALT instruction.

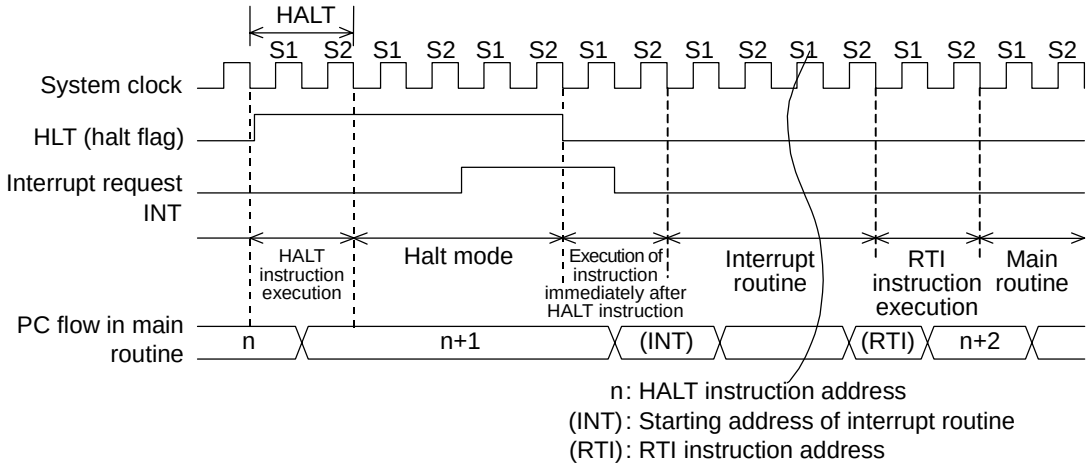


Figure 3-5 Timing of Transfer to Halt Mode and Release of Halt Mode by Interrupt

Note:

If the halt mode is to be released, set individual interrupt enable flags to "1". If an individual interrupt enable flag is "0", the corresponding interrupt request signal cannot reset the HLT flag, regardless of whether the master interrupt enable flag (MIE) is "0" or "1".

3.3.2.2 Release of Halt Mode by RESET Pin

If a high-level is input to the RESET pin, the CPU is released from the halt mode and transfers to the system reset mode.

3.3.3 Melody Data Interrupt and Halt Mode Release

The halt mode is not released by a melody data interrupt.

The melody data interrupt is different from a conventional interrupt in that the melody data interrupt is a hardware processing interrupt used for transfer of melody data to the melody circuit. It is not dependent on the program.

When this interrupt is generated, the instruction immediately after the HALT instruction is executed, then the melody data is transferred to the melody circuit, and the HALT instruction is executed again. This sequence is indicated in Figure 3-6.

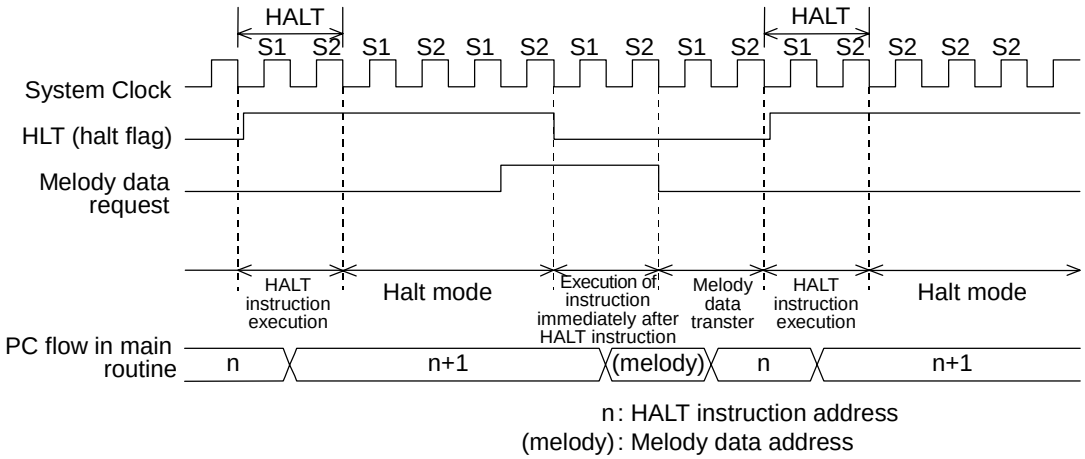


Figure 3-6 Melody Data Request Interrupt Operation

3.3.4 Note Concerning HALT Instruction

As described above, the instruction immediately after the HALT instruction may be executed any number of times. For this reason, always place an NOP instruction immediately after the HALT instruction.

(Example)

•
•
•
HALT
NOP
•
•
•

Chapter 4

Interrupt (INT)

4. Interrupt (INT)

4.1 Overview

The ML63295A supports 17 interrupt factors: 5 external interrupts and 12 internal interrupts.

With the exception of the watchdog timer interrupt, interrupt enable/disable is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE0 to IE4). Watchdog timer interrupt is a non-maskable interrupt.

When interrupt conditions are met, the interrupt routine is executed from the interrupt start address.

Table 4-1 indicates a list of interrupt factors, and Figure 4-1 shows the interrupt control equivalent circuit.

Table 4-1 Interrupt Factors

Priority	Interrupt factor	Symbol	Interrupt start address
1	Watchdog timer interrupt	WDTINT	0010H
2	Melody end interrupt	MDINT	0012H
3	External interrupt 0 (PB 4-bit OR input)	XI0INT	0014H
4	External interrupt 1 (PC 4-bit OR input)	XI1INT	0016H
5	External interrupt 2 (PE.3)	XI2INT	0018H
6	External interrupt 4 (P8.3)	XI4INT	001CH
7	External interrupt 5 (P0 4-bit OR input)	XI5INT	001EH
8	Timer 2 interrupt	TM2INT	0024H
9	Timer 3 interrupt	TM3INT	0026H
10	Serial port receive interrupt	SRINT	0028H
11	Serial port transmit interrupt	STINT	002AH
12	Shift register interrupt	SFTINT	002CH
13	T10 Hz interrupt	T10HzINT	002EH
14	32 Hz interrupt	32HzINT	0030H
15	16 Hz interrupt	16HzINT	0032H
16	4 Hz interrupt	4HzINT	0034H
17	2 Hz interrupt	2HzINT	0036H

If multiple interrupts are detected simultaneously, the lowest interrupt start address is given priority.

For details on interrupt operation, refer to Chapter 6 (Time Base Counter), Chapter 7 (Timers), Chapter 8 (100 Hz Timer Counter), Chapter 9 (Watchdog Timer), Chapter 10 (Ports), Chapter 12 (Melody Driver), Chapter 13 (Serial Port), and Chapter 14 (Shift Register).

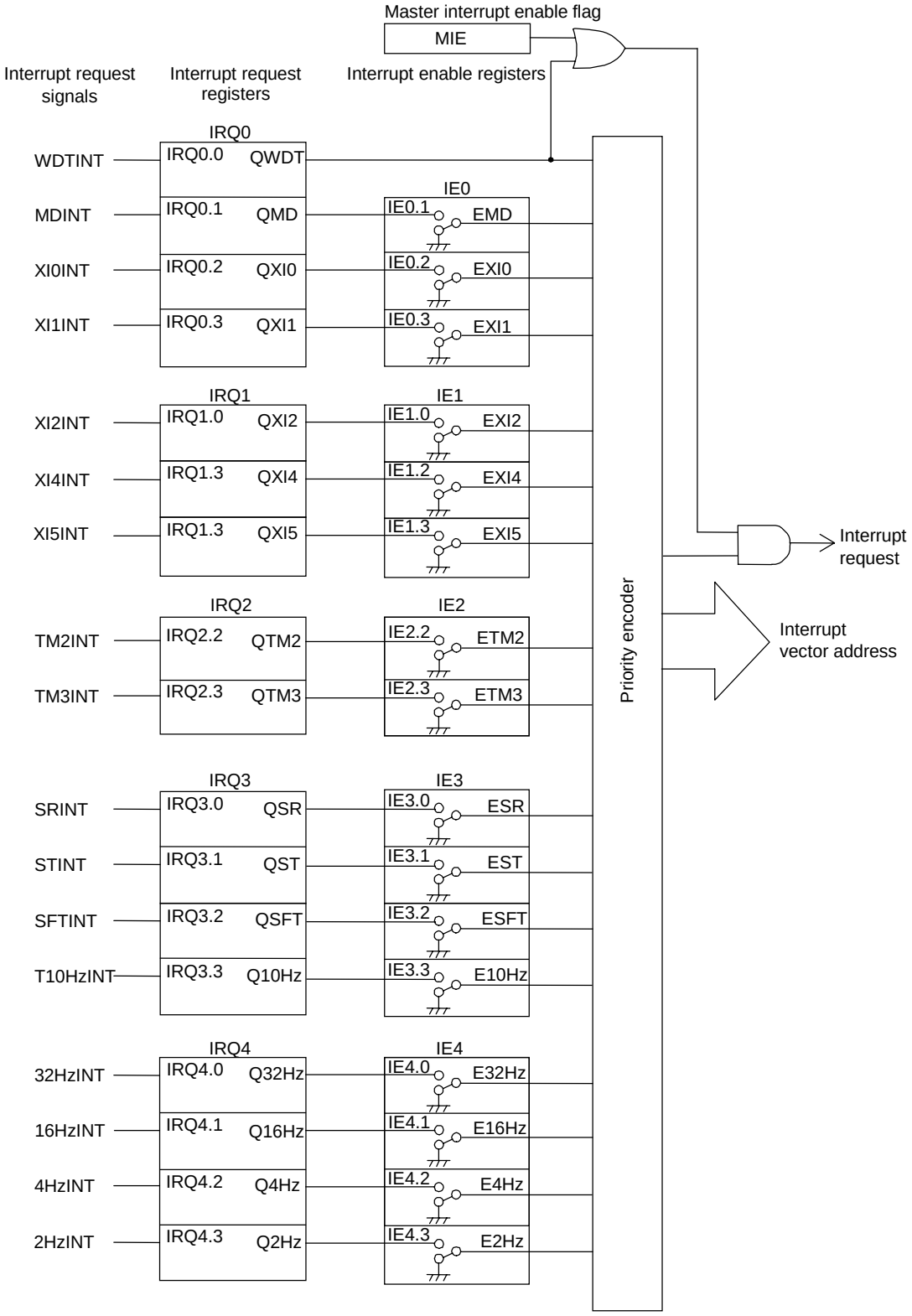


Figure 4-1 Interrupt Control Equivalent Circuit

4.2 Interrupt Registers

The following three types of registers are used to control interrupts.

(1) Master interrupt enable register (MIEF)
(2) Interrupt enable registers (IE0 to IE4)
(3) Interrupt request registers (IRQ0 to IRQ4)

These registers are described below.

(1) Master interrupt enable register (MIEF)

MIEF is a 4-bit register in which bit 0 is the master interrupt enable flag (MIE).

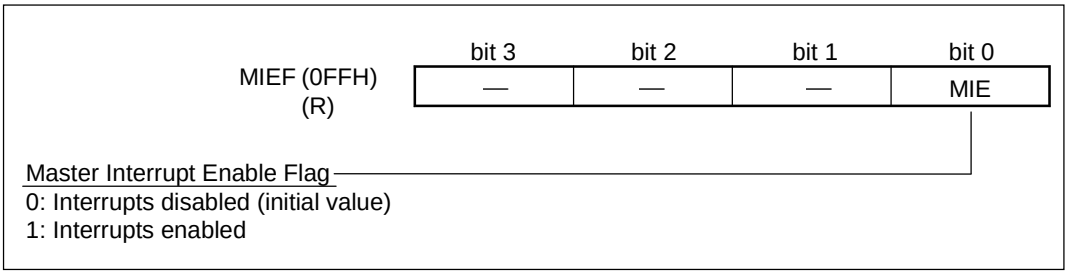
MIE (bit 0 of MIEF) is a flag that disables or enables all interrupts except for the watchdog timer interrupt.

If MIE is "0", all interrupts are disabled. If MIE is "1", all interrupts are enabled (with the exception of the watchdog timer).

When any interrupt is received, MIE is cleared to "0". MIE is set to "1" by execution of a return from interrupt instruction (RTI instruction).

If multi-level interrupt processing is to be performed, execute an RTI instruction (MIE←"1") during the interrupt processing routines.

At system reset, MIE is initialized to "0". MIEF only supports data reference (R) of data memory through addressing instructions.



Note:

When setting MIE, use "EI" instructions (MIE←"1") and "DI" instructions (MIE←"0").

(2) Interrupt enable registers (IE0 to IE4)

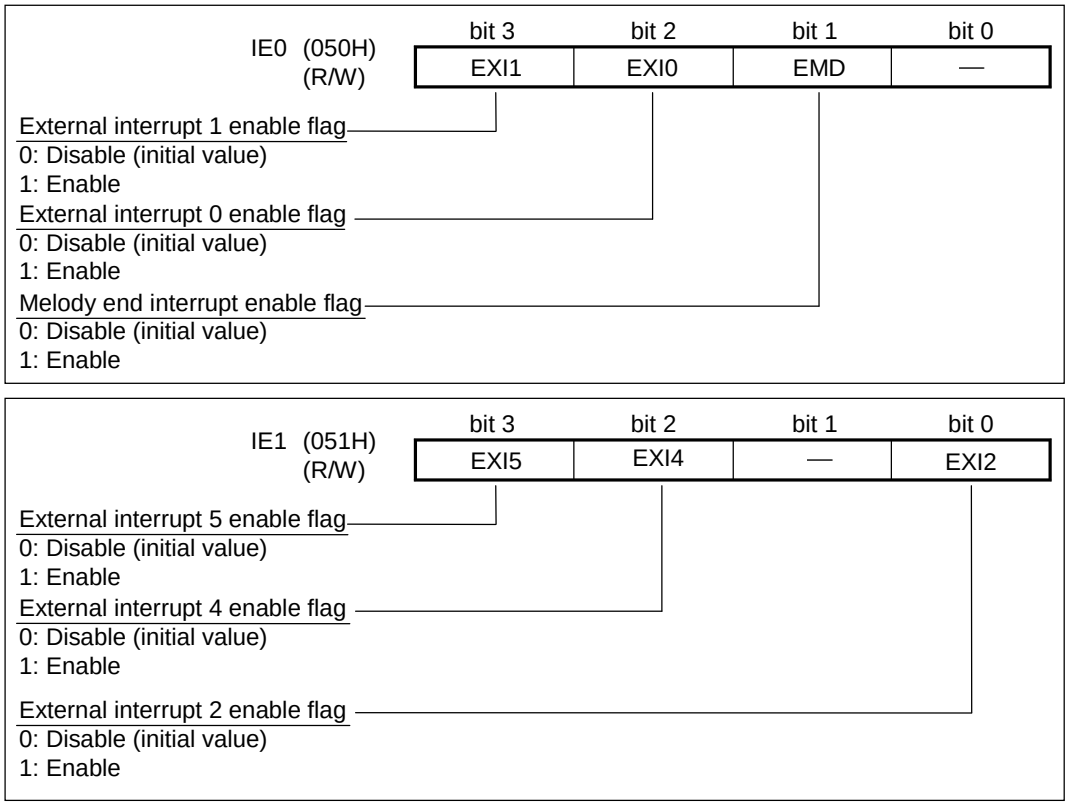
IE0, IE1, IE2, IE3, and IE4 are registers that consist of 4 bits each.

A logical AND of the corresponding bits of an interrupt enable register (IE0 to IE4) and an interrupt request register (IRQ0 to IRQ4) determines whether or not each interrupt request is issued to the CPU. The watchdog timer interrupt is non-maskable, and is therefore not dependent upon the interrupt enable registers (IE0 to IE4) and the master interrupt enable register (MIEF).

If multiple interrupts request the CPU at the same time, the interrupts are accepted in order of highest priority and low priority interrupts are placed on hold (see Table 4-1 for the order of priority).

When an interrupt is received, the master interrupt enable flag (MIE) is cleared to "0". The corresponding bits in the interrupt enable registers (IE0 to IE4) do not change.

At system reset, each bit of IE0 through IE4 is initialized to "0".



IE2 (052H) (R/W)

bit 3	bit 2	bit 1	bit 0
ETM3	ETM2	—	—

Timer 3 interrupt enable flag
0: Disable (initial value)
1: Enable

Timer 2 interrupt enable flag
0: Disable (initial value)
1: Enable

IE3 (053H) (R/W)

bit 3	bit 2	bit 1	bit 0
E10Hz	ESFT	EST	ESR

10 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

Shift register interrupt enable flag
0: Disable (initial value)
1: Enable

Serial port transmit interrupt enable flag
0: Disable (initial value)
1: Enable

Serial port receive interrupt enable flag
0: Disable (initial value)
1: Enable

IE4 (054H) (R/W)

bit 3	bit 2	bit 1	bit 0
E2Hz	E4Hz	E16Hz	E32Hz

2 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

4 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

16 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

32 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

(3) Interrupt request registers (IRQ0 to IRQ4)

IRQ0, IRQ1, IRQ2, IRQ3 and IRQ4 are registers that consist of 4 bits each.

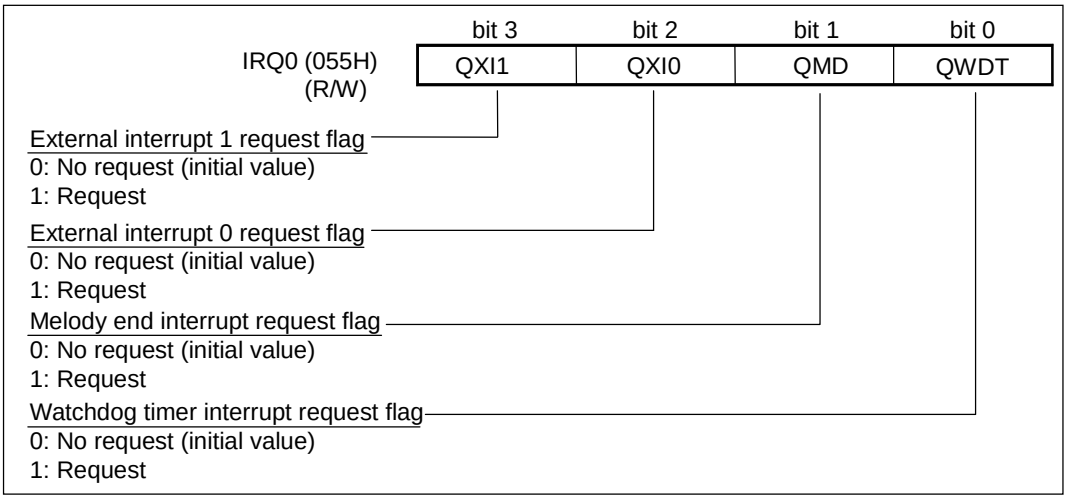
When an interrupt request is generated, the corresponding bit of the interrupt request register is set to "1" in the first half of the S1 state of the next instruction. So that the CPU can receive interrupt requests, set the master interrupt enable flag (MIE) to "1" and set the appropriate flag of the corresponding interrupt enable register (IE0 to IE4) to "1".

The watchdog timer interrupt is non-maskable and does not depend upon the interrupt enable register or the master interrupt enable register (MIEF).

Setting the appropriate bits of an interrupt request register to "1" allows software interrupts to be generated.

When an interrupt request is received, the corresponding bits of IRQ0 to IRQ4 are cleared to "0".

At system reset, each bit of IRQ0 through IRQ4 is initialized to "0".



bit 3: QXI1 (reQuest eXternal Interrupt 1)

The external interrupt 1 request flag.
The external interrupt 1 is assigned as the secondary function of each bit of port C (PC.0 to PC.3).
External interrupt 1 requests are generated by a 4-bit ORed input.

bit 2: QXI0 (reQuest eXternal Interrupt 0)

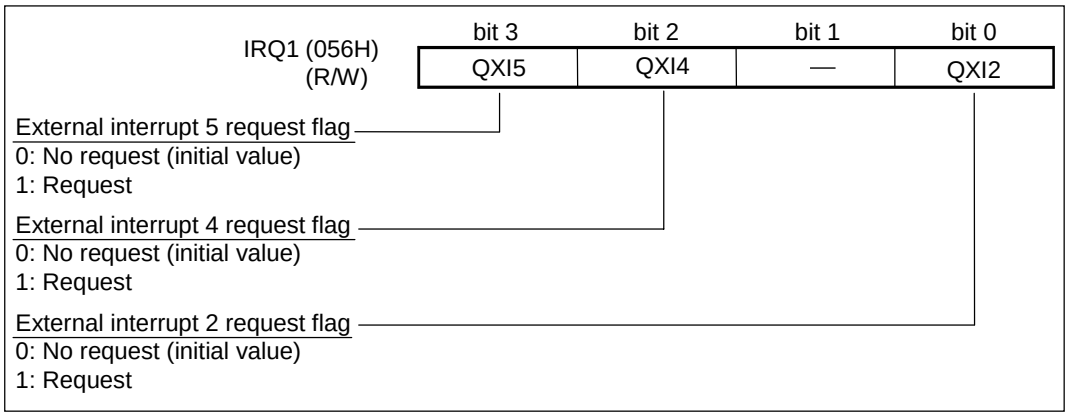
The external interrupt 0 request flag.
The external interrupt 0 is assigned as the secondary function of each bit of port B (PB.0 to PB.3).
External interrupt 0 requests are generated by a 4-bit ORed input.

bit 1: QMD (reQuest Melody Driver)

Melody end interrupt request flag.
Melody end interrupts are generated when the melody driver outputs the end note data (END bit = "1").

bit 0: QWDT (reQuest WatchDog Timer)

Watchdog timer interrupt request flag.
When the watchdog timer is started and then overflow occurs, an interrupt is requested. The watchdog timer interrupt is non-maskable and does not depend upon the interrupt enable registers or the master interrupt enable register (MIE).



bit 3: QXI5 (reQuest eXternal Interrupt 5)

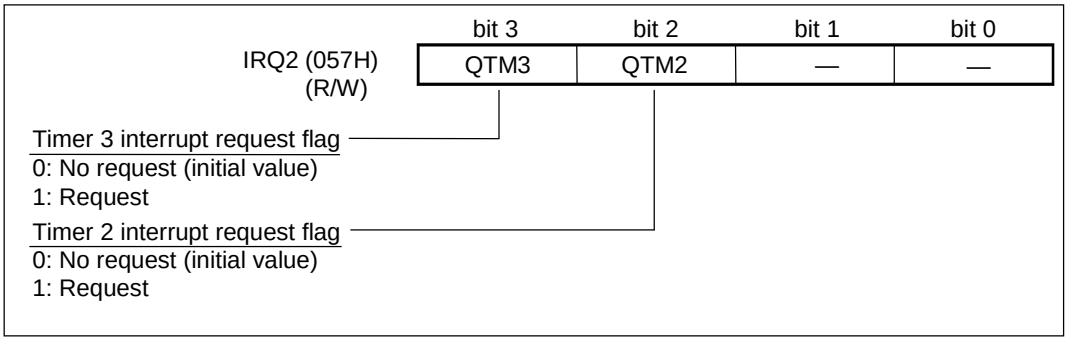
External interrupt 5 request flag.
The external interrupt 5 is assigned as a secondary function to each bit (P0.0 to P0.3) of port 0 and each bit (P1.0 to P1.3) of port 1.
An external interrupt request is generated through the 4-bit ORed input.

bit 2: QXI4 (reQuest eXternal Interrupt 4)

External interrupt 4 request flag.
The external interrupt 4 is assigned as a secondary function of port 8.3 (P8.3). Generation of the external interrupt 4 is triggered by the falling edge of the 128 Hz or 4 kHz output of the time base counter.

bit 0: QXI2 (reQuest eXternal Interrupt 2)

External interrupt 2 request flag.
The external interrupt 2 is assigned as a secondary function of port E.3 (PE.3). Generation of the external interrupt 2 is triggered by the falling edge of the 128 Hz or 4 kHz output of the time base counter.

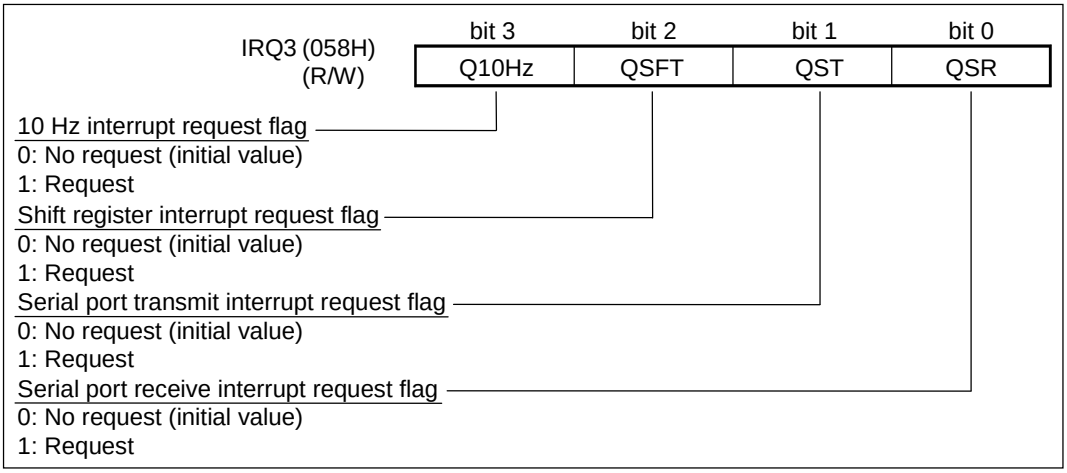


bit 3: QTM3 (reQuest TiMer 3)

Timer 3 interrupt request flag.
A timer 3 interrupt request is generated whenever timer 3 overflows.

bit 2: QTM2 (reQuest TiMer 2)

Timer 2 interrupt request flag.
A timer 2 interrupt request is generated whenever timer 2 overflows.



bit 3: Q10Hz (reQuest 10 Hz)

10 Hz interrupt request flag.
A 10 Hz interrupt request is generated whenever the 10 Hz carry generated by the 100 Hz timer counter is output.

bit 2: QSFT (reQuest ShiFT register)

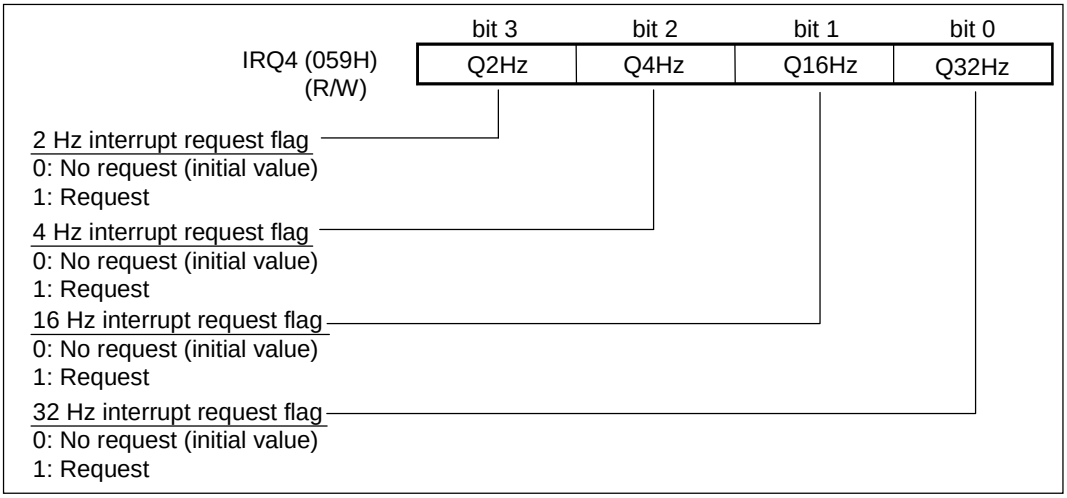
Shift register interrupt request flag.
A shift register interrupt is generated when the 8-bit data transfer for the shift register is completed.

bit 1: QST

Serial port transmit interrupt request flag.
A serial port transmit interrupt request is generated when a serial port transmit operation is completed.

bit 0: QSR

Serial port receive interrupt request flag.
A serial port receive interrupt is generated when a serial port receive operation is completed.



bit 3: Q2Hz (reQuest 2 Hz)

2 Hz interrupt request flag.
A 2 Hz interrupt request is generated at every falling edge of the 2 Hz output of the time base counter.

bit 2: Q4Hz (reQuest 4 Hz)

4 Hz interrupt request flag.
A 4 Hz interrupt request is generated at every falling edge of the 4 Hz output of the time base counter.

bit1: Q16Hz (reQuest 16 Hz)

16 Hz interrupt request flag.
A 16 Hz interrupt request is generated at every falling edge of the 16 Hz output of the time base counter.

bit 0: Q32Hz (reQuest 32 Hz)

32 Hz interrupt request flag.
A 32 Hz interrupt request is generated at every falling edge of the 32 Hz output of the time base counter.

4.3 Interrupt Sequence

4.3.1 Interrupt Processing

While MIE is "1", operation transfers to interrupt processing when individual interrupt factors are generated.

The watchdog timer interrupt is non-maskable and regardless of the MIE flag status, operation will shift to interrupt processing when the watchdog timer interrupt factor is generated.

The following processes are performed when an interrupt is generated.

(1) MIE and the corresponding interrupt request flag are cleared to "0".
(2) The program counter (PC) is saved on the call stack.
(3) The call stack pointer (SP) is incremented by 1. (SP←SP+1)
(4) The starting address of the interrupt routine is loaded into the program counter (PC).

Interrupt processing is performed in 0 machine cycles.

Figure 4-2 shows the stack contents after an interrupt is generated.

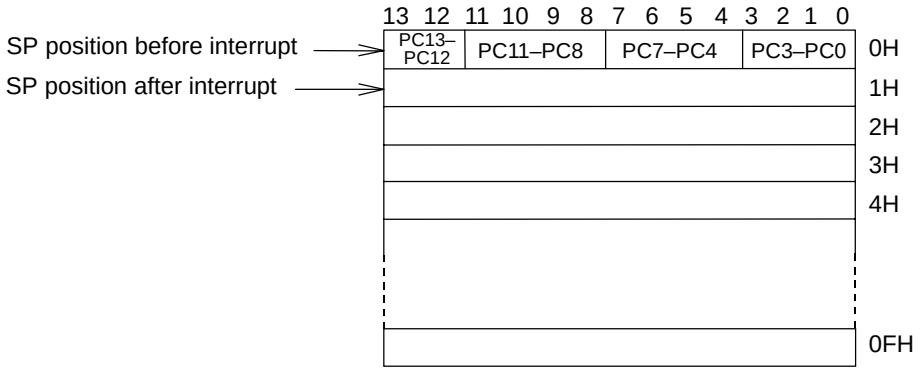


Figure 4-2 Call Stack Contents after Interrupt Generation

4.3.2 Return from an Interrupt Routine

Return from a watchdog timer interrupt routine is performed with an "RTNMI" instruction.

Return from all other interrupt routines is performed with an "RTI" instruction.

Execution of "RTI" and "RTNMI" instructions both require 1 machine cycle.

When returning from an interrupt routine, the CPU performs the following processes.

(1) The call stack pointer (SP) is decremented by 1. (SP←SP–1)
(2) MIE is set to "1" (when an "RTNMI" instruction is used, MIE is restored to its state prior to the interrupt).
(3) 1 is added to the call stack contents and that value is loaded into the program counter (PC).

 Note:

- While the MIE flag is "0" (interrupt disabled state), if a watchdog timer interrupt is processed and an "RTI" instruction is executed, the MIE flag will be set to "1" and interrupts enabled.
- Use "RTNMI" instructions to return from watchdog timer interrupts only. Use "RTI" instructions for normal interrupts.

4.3.3 Interrupt Hold Instructions

Interrupt requests are not received during execution of the following instructions. These instructions are processed with priority, and interrupt processing is delayed until completion of the instruction.

- ROM table reference instructions
- External memory transfer instructions
- Stack operation instructions
- Jump instructions
- Conditional branch instructions
- Call/return instructions
- "EI" (set MIE flag) instructions, "DI" (clear MIE flag) instructions and "MSA cadr15" (start melody output) instructions within control instructions

 Note:

If interrupt hold instructions are to be used consecutively, consider that an interrupt, when generated, will be put on hold for a certain amount of time before the interrupt routine begins.

Chapter 5

Clock Generator Circuit (OSC)

5. Clock Generator Circuit (OSC)

5.1 Overview

The clock generator circuit (OSC) consists of a low-speed clock generator circuit, a high-speed clock generator circuit and a clock controller unit. The clock generator circuit generates the system clock (CLK), time base clock (TBCCLK) and the high-speed clock (HSCLK).

The following modes can be selected for the low-speed clock generator circuit and the high-speed clock generator circuit.

- Low-speed clock generator circuit: crystal oscillation mode or RC oscillation mode (mask option selection)
- High-speed clock generator circuit: ceramic oscillation mode or RC oscillation mode (software selection)

The system clock is the basic operation clock for the CPU. The time base clock is the basic operation clock for the time base counter.

Depending on the contents of the frequency control register (FCON), the system clock frequency is switched to either the output of the low-speed clock generator circuit (TBCCLK) or the output of the high-speed clock generator circuit (HSCLK).

The frequency control register (FCON) also controls modes of the high-speed clock generator circuit.

5.2 Clock Generator Circuit Configuration

Figure 5-1 shows a block diagram of the clock generator circuit.

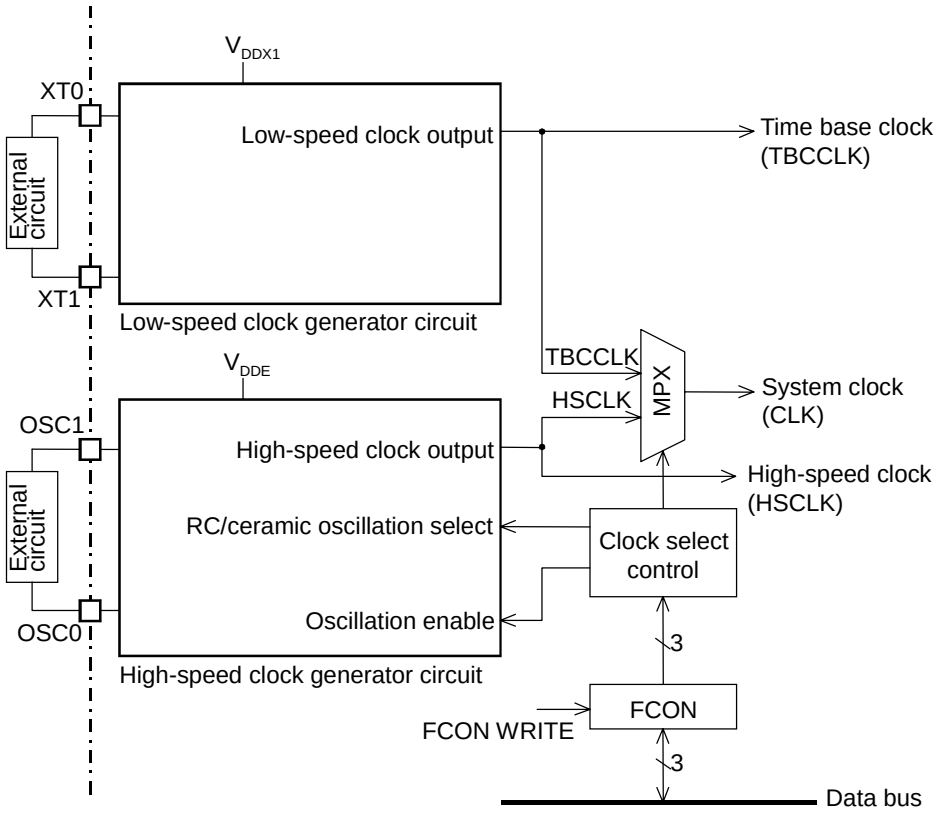


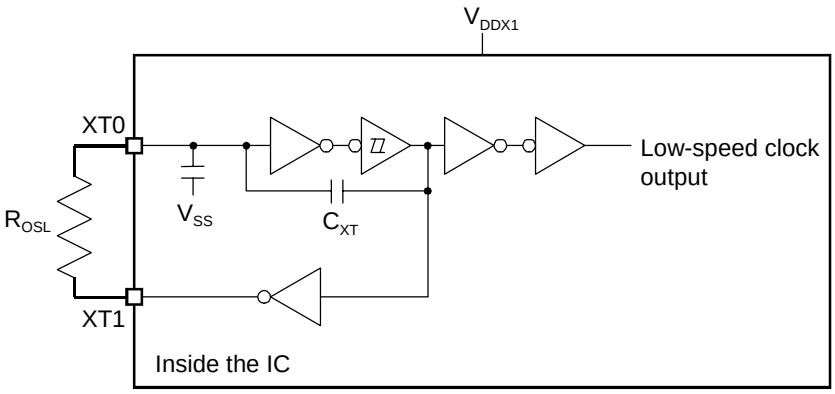
Figure 5-1 Clock Generator Circuit Configuration

5.3 Low-Speed Clock Generator Circuit

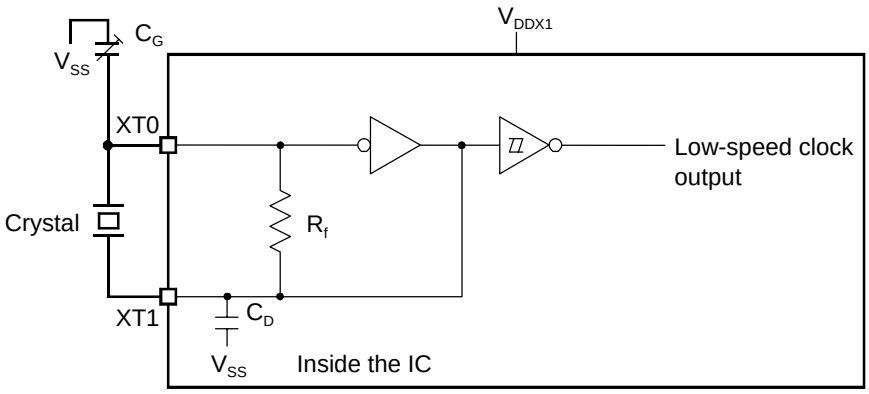
The low-speed clock generator circuit has two modes that are selected by the mask option, the RC oscillation mode and crystal oscillation mode. The oscillation frequency is 30 to 80 kHz.

For the RC oscillation mode, attach an external resistor, R_{OSL}, as shown in Figure 5-2(a).

For the crystal oscillation mode, attach an external crystal unit and capacitor, C_G, as shown in Figure 5-2(b).



(a) External Circuit for RC Oscillation Mode



(b) External Circuit for Crystal Oscillation Mode

Figure 5-2 External Circuits for Low-Speed Clock Oscillation

Note:

For convenience, the descriptions of this manual assume that a 32.768 kHz crystal unit is used in the low-speed clock oscillation circuit.

For the method of specifying mask options for the low-speed clock oscillation circuit, see "Appendix G: Mask Option."

Table 5-1 lists typical values of oscillation frequency when the low-speed side RC oscillation mode is selected. Table 5-2 shows an example external component to be attached when the low-speed side crystal oscillation mode is selected.

Table 5-1 Typical Oscillation Frequencies for the Low-Speed Side RC Oscillation Mode

R_{OSL}	f_{ROSL}
1.5 MΩ	32 kHz ±30%
700 kΩ	60 kHz ±30%
500 kΩ	80 kHz ±30%

Table 5-2 Example External Component for the Low-Speed Side Crystal Oscillation Mode

C_G	f_{XT}
12 pF	32.768 kHz

5.4 High-Speed Clock Generator Circuit

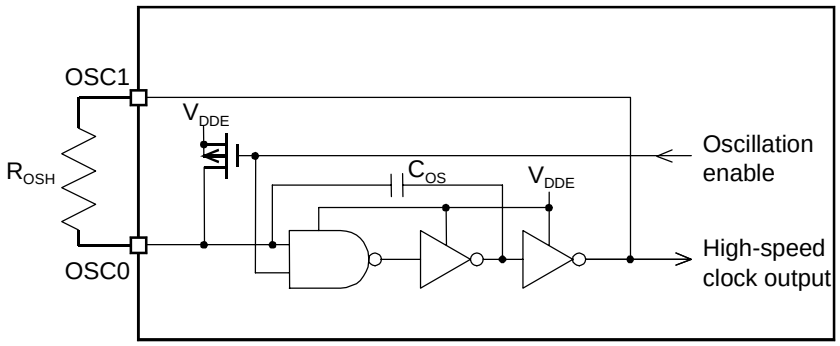
The high-speed clock generator circuit has two modes, the RC oscillation mode and ceramic oscillation mode. Oscillation modes are set by OSCSEL (bit 2 of FCON). The maximum oscillation frequency is 2 MHz.

- OSCSEL = "0" : RC oscillation mode
- OSCSEL = "1" : ceramic oscillation mode

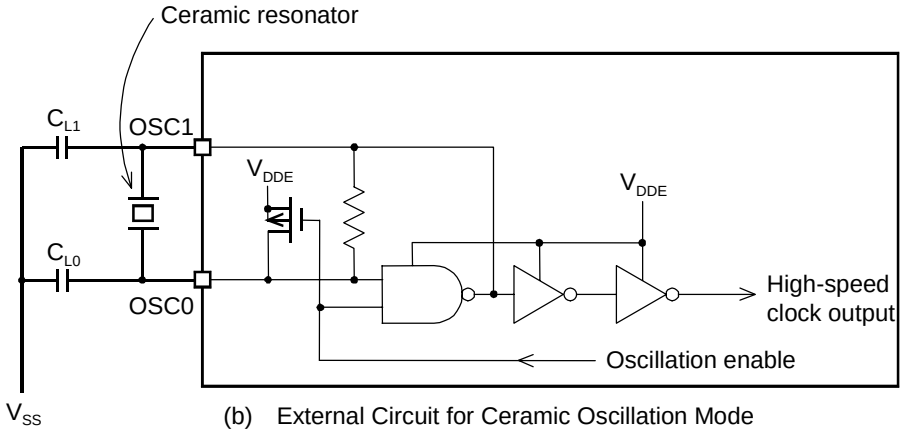
If the high-speed clock is not to be used, leave the OSC0 and OSC1 pins open (unconnected).

For the RC oscillation mode, attach an external resistor, R_{OSH}, as shown in Figure 5-3(a).

For the ceramic oscillation mode, attach an external ceramic unit and capacitors as shown in Figure 5-3(b).



(a) External Circuit for RC Oscillation Mode



(b) External Circuit for Ceramic Oscillation Mode

Figure 5-3 External Circuits for High-Speed Clock Oscillation

Table 5-3 lists typical values of oscillation frequency when the high-speed side RC oscillation mode is selected. Table 5-4 lists example external components to be attached when the high-speed side ceramic oscillation mode is selected.

Table 5-3 Typical Oscillation Frequencies for the High-Speed Side RC Oscillation Mode

R_{OSH} (kΩ)	V_{DD} (V)	f_{ROSH}
100	3.5 to 7.2	700 kHz ±30%
75		1 MHz ±30%
51		1.35 MHz ±30%
30		2 MHz ±30%

Table 5-4 Example External Components for the High-Speed Side Ceramic Oscillation Mode

C_{L0} (pF)	C_{L1} (pF)	Ceramic unit
330	330	CSB200D (200 kHz)*
220	220	CSB300D (300 kHz)*
150	150	CSB500E (500 kHz)*
68	68	CSB1000J (1 MHz)*
30	30	CSA2.00MG (2 MHz)*

* Ceramic unit manufactured by Murata MFG. Co., Ltd.

5.5 System Clock Control

The system clock is the basic operation clock of the CPU.

The clock can be selected as follows with the CPUCLK (bit 0 of FCON) setting.

- CPUCLK = "0" (initial value)
  The output of the low-speed clock generator circuit (TBCCLK) is the system clock.
- CPUCLK = "1"
  The output of the high-speed clock generator circuit (HSCLK) is the system clock.

When HSCLK is selected as the system clock, the high-speed clock must be in the oscillating state (ENOSC = "1"). The crystal generator circuit will continue to oscillate even when the high-speed generator circuit is selected.

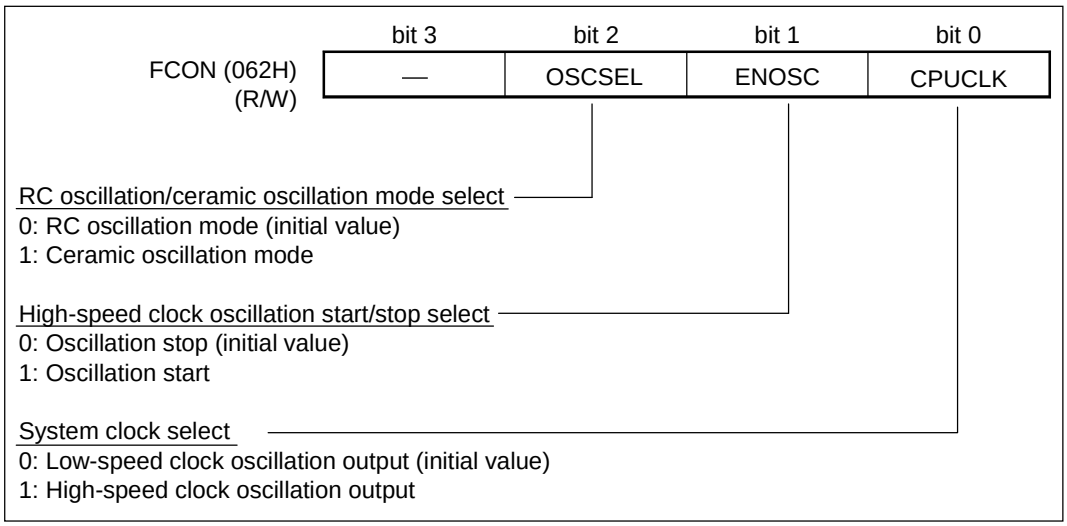
To reduce the total power consumption in applications that use the high-speed clock generator circuit, the following clock controls are generally implemented in software.

- During normal operation, the output of the low-speed clock generator circuit (CPUCLK = "0") should be the system clock.
- Only when high-speed operation is necessary should the high-speed clock oscillate (ENOSC = "1") and output of the high-speed clock generator circuit (CPUCLK = "1") should be selected.

For details of the system clock select timing, refer to section 5.7, "System Clock Select Timing".

5.6 Frequency Control Register (FCON)

FCON is a special function register (SFR) that selects the system clock.



bit 2: OSCSEL

This bit selects the RC oscillation mode or the ceramic oscillation mode of the high-speed clock generator circuit. At system reset, this bit is cleared to "0", selecting the RC oscillation mode.

bit 1: ENOSC

This bit starts and stops oscillation of the high-speed clock generator circuit. At system reset, this bit is cleared to "0", stopping oscillation of the high-speed clock generator circuit.

bit 0: CPUCLK

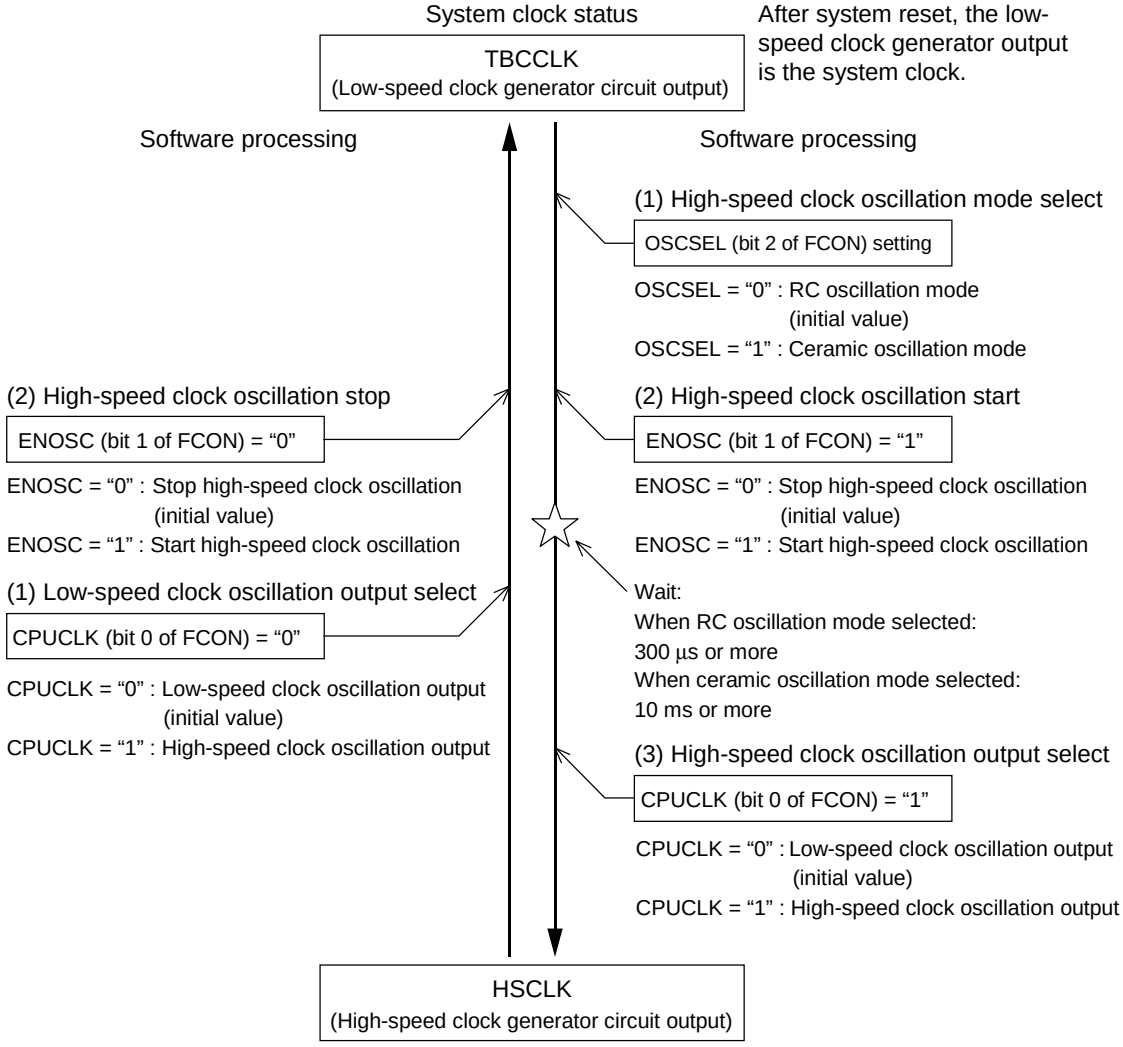
This bit selects the system clock, the basic operation clock of the CPU. At system reset, this bit is cleared to "0", selecting output of the low-speed clock generator circuit (TBCCLK).

5.7 System Clock Select Timing

After system reset, the system clock is TBCCLK.

When high-speed operation is necessary, switch the system clock to HSCLK.

A flowchart of system clock operation is shown below.



When ENOSC (bit 1 of FCON) is set to "1", oscillation starts in the mode selected by OSCSEL. At the same time, the internal logic power supply (V_{DDL}) switches from the constant voltage circuit output level (approx. 1.5 V) to the V_{DDE} level. Next, if CPUCLK is set to "1", the system clock switches from crystal oscillation output (TBCCLK) to high-speed clock output (HSCLK).

Figure 5-4 shows the system clock select timing and status of the internal logic power supply (V_{DDL}).

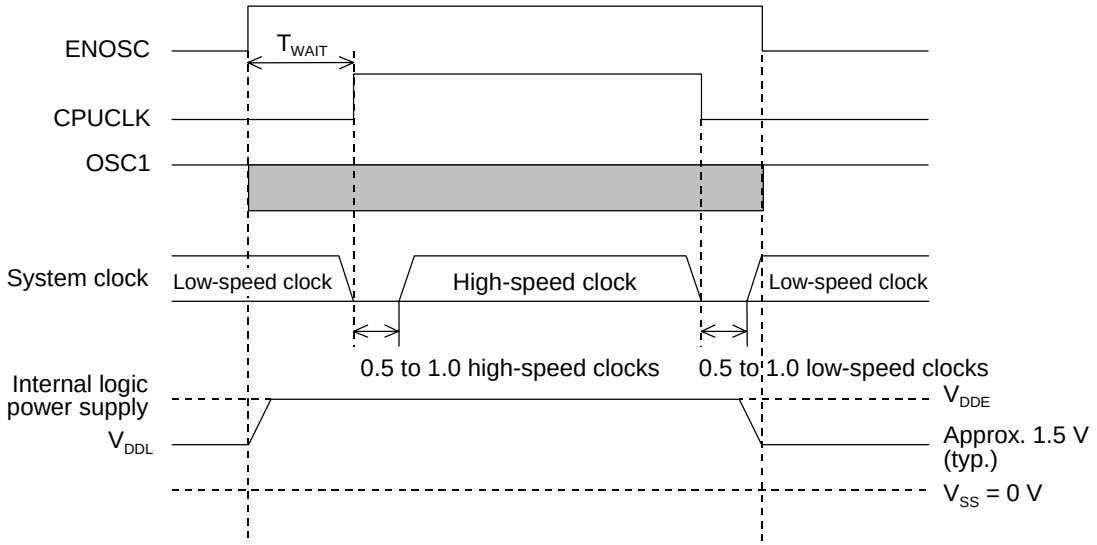


Figure 5-4 System Clock Select Timing

In the ceramic oscillation mode, 10 ms are required from the time when ENOSC is set to "1" until the high-speed clock generator circuit enters the oscillating state. Therefore, in this mode, when switching CPUCLK to a high-speed setting, wait for an interval of at least T_{WAIT} = 10 ms after the rising edge of ENOSC.

In the RC oscillation mode, oscillation begins soon after setting ENOSC to "1". When switching CPUCLK to a high-speed setting, wait for an interval of at least T_{WAIT} = 300 µs after the rising edge of ENOSC.

When switching from the high-speed mode to the low-speed mode, set the CPUCLK bit to "0", and sometime after the next instruction, set the ENOSC bit to "0".

Chapter 6

Time Base Counter (TBC)

6. Time Base Counter (TBC)

6.1 Overview

The time base counter (TBC) is a 15-bit internal counter, which generates the clock supplied to internal peripheral functions.

The TBC clock is a time base clock (TBCCLK).

TBC outputs are used for functions such as time base interrupts and various other circuits.
TBC8–11 and TBC12–15 can be read/reset by software.

The TBC generates an interrupt request at the falling edge of 32 Hz/16 Hz/4 Hz/2 Hz output.

The TBC is initialized to 0000H at system reset.

6.2 Time Base Counter Configuration

The configuration of the time base counter (TBC) is shown in Figure 6-1.

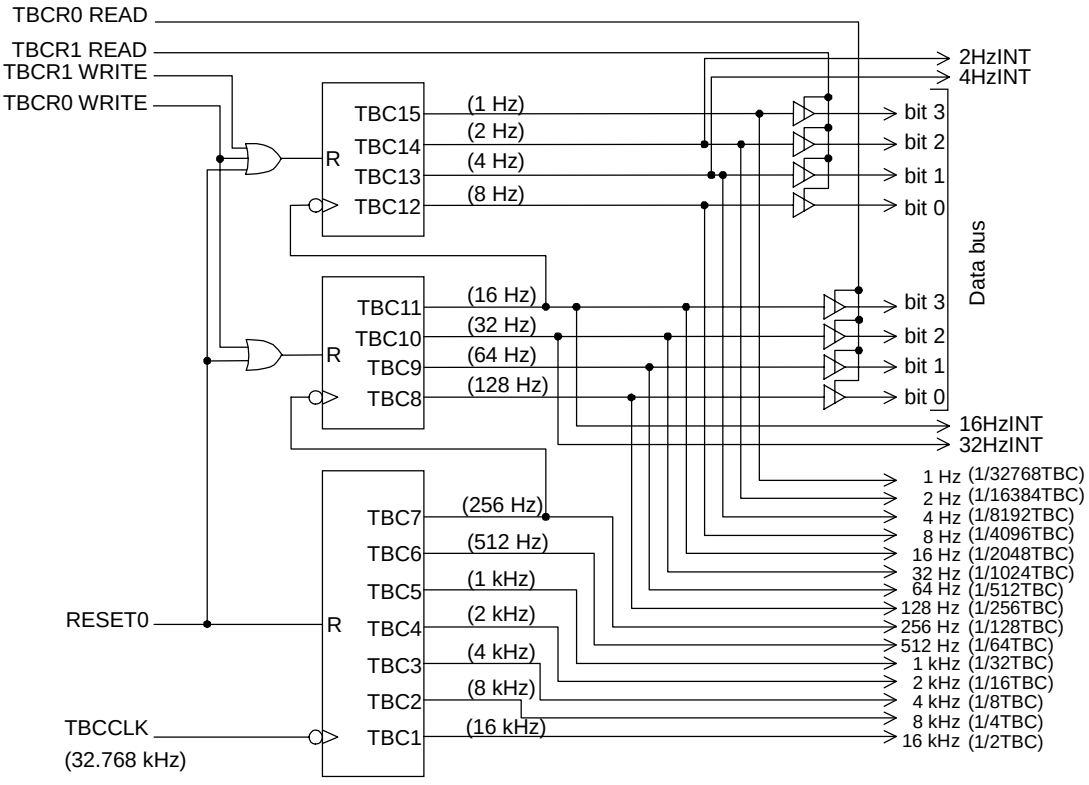


Figure 6-1 Time Base Counter (TBC) Configuration

(when a 32.768 kHz crystal is used for low-speed clock oscillation)

6.3 Time Base Counter Registers

Time base counter register 0 (TBCR0), time base counter register 1 (TBCR1)

These 4-bit special function registers (SFRs) are used to read the 1 to 8 Hz and 16 to 128 Hz outputs of the time base counter.

A write operation to TBCR0 sets both the 1 to 8 Hz and 16 to 128 Hz outputs to "0", and a write operation to TBCR1 sets the 1 to 8 Hz outputs to "0".

	bit 3	bit 2	bit 1	bit 0
TBCR0 (060H) (R/W)	16 Hz	32 Hz	64 Hz	128 Hz
	bit 3	bit 2	bit 1	bit 0
TBCR1 (061H) (R/W)	1 Hz	2 Hz	4 Hz	8 Hz

6.4 Time Base Counter Operation

After system reset the time base counter (TBC) begins to count up from 0000H. The count is incremented at the falling edge of the TBCCLK.

TBC 32 Hz/16 Hz/4 Hz/2 Hz outputs are used as time base interrupts. At their respective output falling edges, the four bits of interrupt request register 4 (IRQ4) are set to "1", namely bit 3 (Q32Hz), bit 2 (Q16Hz), bit 1 (Q4Hz) and bit 0 (Q2Hz), requesting an interrupt to the CPU. TBC outputs are also used as clocks for various circuits.

TBC 1 to 8 Hz outputs and 16 to 128 Hz outputs can be read through the time base counter registers 0/1 (TBCR0/TBCR1).

A write operation to TBCR1 sets the 1 to 8 Hz output counter to "0", and a write operation to TBCR0 sets both the 1 to 8 Hz and 16 to 128 Hz output counters to "0". The write data in these write operations has no significance. For example, the "MOV TBCR0, A" instruction can be used to write, but is not dependent on accumulator content in any way. When write is executed to TBCR0 and TBCR1 and the 1 to 8 Hz and 16 to 128 Hz counters reset, interrupt requests are generated if 32 Hz/16 Hz/4 Hz/2 Hz outputs have been set to "1". To disable these interrupts, first set the master interrupt enable flag (MIE) or interrupt enable register 4 (IE4) to "0", execute the write operation to TBCR0/1, and set the interrupt request flag 4 (IRQ4) to "0".

Figure 6-2 shows interrupt generation timing and time base counter output reset timing by writing "1" to TBCR0 and TBCR1.

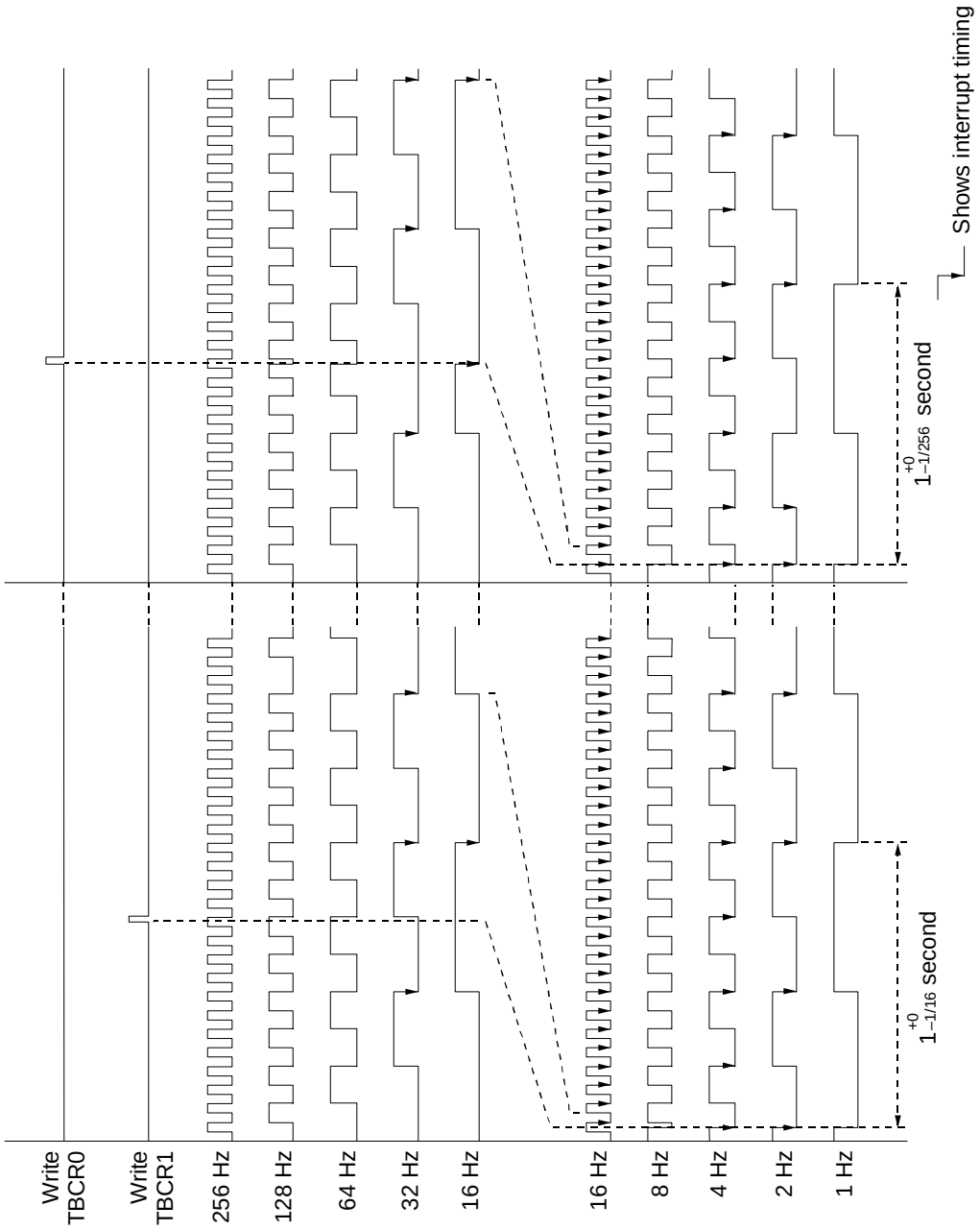


Figure 6-2 Interrupt Timing and Reset Timing by Writing "1" to TBCR0, TBCR1

Chapter 7

Timers (TIMER)

7. Timers (TIMER)

7.1 Overview

The ML63295A has two internal 8-bit timers (timers 2 and 3). Timers 2 and 3 can be used in tandem as a 16-bit timer.

Timers 2 and 3 have two modes: auto-reload and frequency measurement. Timer clock may be set to the time base clock (TBCCLK: 32.768 kHz), the high-speed clock (HSCLK), or an external clock. When using the timers as a 16-bit timer, the overflow signals of timer 2 is used as the clocks for timer 3.

Timers can be used not only for pulse generation and time measurement, but as baud rate generators for serial communication.

	Timer 2	Timer 3
8-bit timer	●	●
16-bit timer	● (Timer 2 overflow signal is used as clock for timer 3)	
Clock	TBCCLK/HSCLK/External clock (T2CK, T3CK)	
Auto-reload mode	●	●
Frequency measurement mode	●	●

7.2 Timer Configuration

Figures 7-1 and 7-2 show the configuration of timers 2 and 3 respectively.

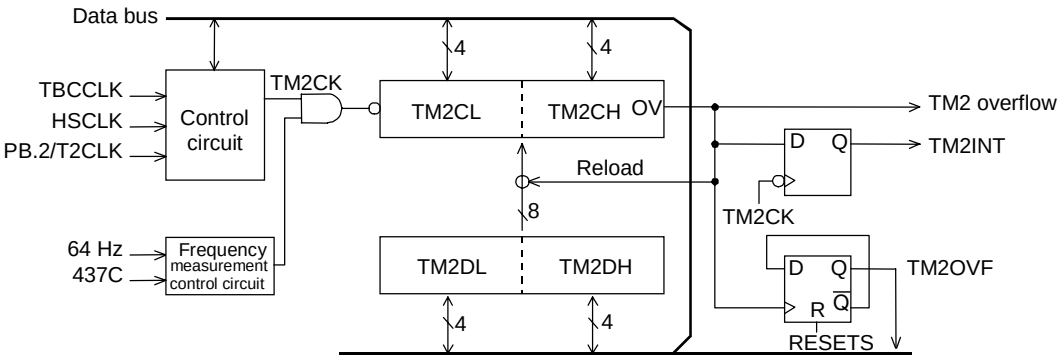


Figure 7-1 Timer 2 Configuration

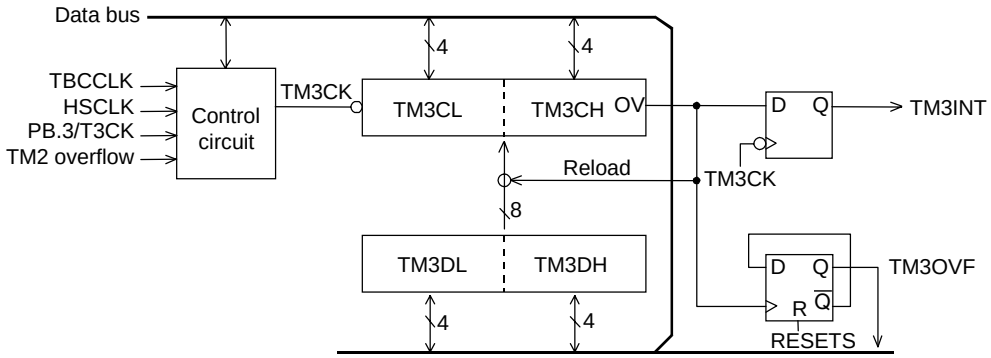


Figure 7-2 Timer 3 Configuration

7.3 Timer Registers

The following four types of registers are used for timer control:

(1) Timer data registers
(TM2DL, TM2DH, TM3DL, TM3DH)
(2) Timer counter registers
(TM2CL, TM2CH, TM3CL, TM3CH)
(3) Timer control registers
(TM2CON0, TM2CON1, TM3CON0, TM3CON1)
(4) Timer status registers
(TM2STAT, TM3STAT)

These registers are described below for each type.

(1) Timer data registers
(TM2DL, TM2DH, TM3DL, TM3DH)

- During the auto-reload mode, timer data registers store the reload values.
- At system reset, all valid bits are cleared to "0".
- Note regarding register values:
  When a value is written to any timer counter register, the same value is also written to the corresponding timer data register. However, when writing to a timer data register, the same value is not written to the corresponding timer counter register.

Timer 2 Registers

		bit 3	bit 2	bit 1	bit 0
TM2DL (Timer 2 lower)	(076H) (R/W)	T2D3	T2D2	T2D1	T2D0

		bit 3	bit 2	bit 1	bit 0
TM2DH (Timer 2 upper)	(077H) (R/W)	T2D7	T2D6	T2D5	T2D4

Timer 3 Registers

		bit 3	bit 2	bit 1	bit 0
TM3DL (Timer 3 lower)	(078H) (R/W)	T3D3	T3D2	T3D1	T3D0

		bit 3	bit 2	bit 1	bit 0
TM3DH (Timer 3 upper)	(079H) (R/W)	T3D7	T3D6	T3D5	T3D4

(2) Timer counter registers
(TM2CL, TM2CH, TM3CL, TM3CH)

- 8-bit binary counter operation
- At system reset, all valid bits are cleared to "0".
- Note regarding register values:
  When a value is written to any timer counter register, the same value is also written to the corresponding timer data register. However, when writing to a timer data register, the same value is not written to the corresponding timer counter register.

Timer 2 Registers

		bit 3	bit 2	bit 1	bit 0
TM2CL (Timer 2 lower)	(07AH) (R/W)	T2C3	T2C2	T2C1	T2C0
TM2CH (Timer 2 upper)	(07BH) (R/W)	T2C7	T2C6	T2C5	T2C4

Timer 3 Registers

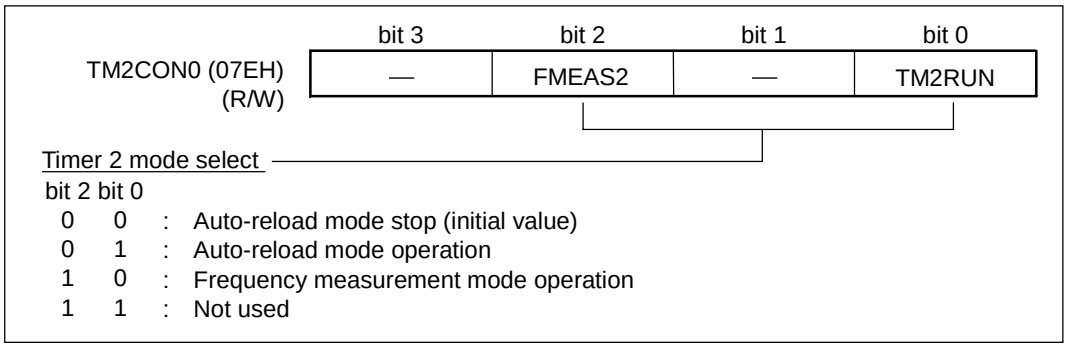
		bit 3	bit 2	bit 1	bit 0
TM3CL (Timer 3 lower)	(07CH) (R/W)	T3C3	T3C2	T3C1	T3C0
TM3CH (Timer 3 upper)	(07DH) (R/W)	T3C7	T3C6	T3C5	T3C4

(3) Timer control registers
(TM2CON0, TM2CON1, TM3CON0, TM3CON1)

- Timer control registers select the operation mode and clock for each timer.
- At system reset, all valid bits are cleared to "0".
- Note regarding register values:
  When a value is written to any timer counter register, the same value is also written to the corresponding timer data register. However, when writing to a timer data register, the same value is not written to the corresponding timer counter register.

Timer 2 Registers

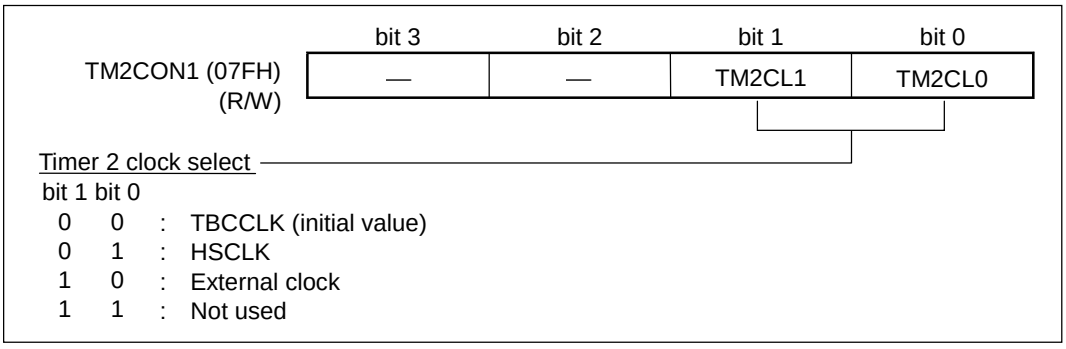
To use timer 3 in combination as a 16-bit timer, set timer 3 control registers TM3CON0 and TM3CON1.



bit 2, 0: FMEAS2, TM2RUN

These bits select the timer 2 operation mode.

The timer 2 operation mode can be selected as auto-reload mode or frequency measurement mode.



bit 1, 0: TM2CL1, TM2CL0

These bits select the timer 2 clock.

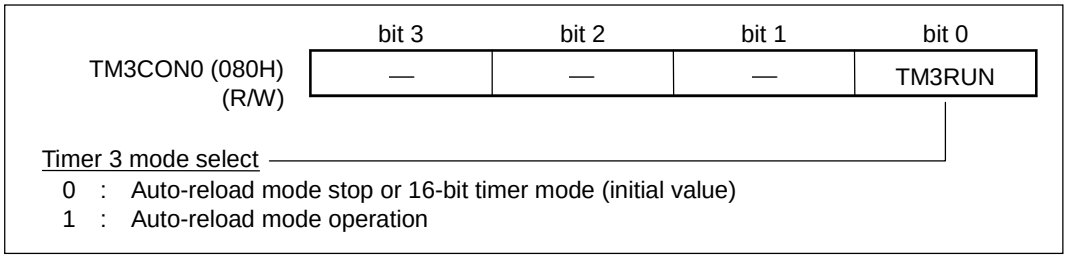
The timer 2 clock can be selected as TBCCLK (low-speed clock), HSCLK (high-speed clock), or external clock (T2CK: secondary function of PB.2).

Note:

If HSCLK is used as the clock, after ENOSC (bit 1 of FCON) is set to "1", wait for the following time interval before starting timer operation.

- Wait at least 10 ms when using ceramic oscillation.
- Wait at least 300 μs when using RC oscillation.

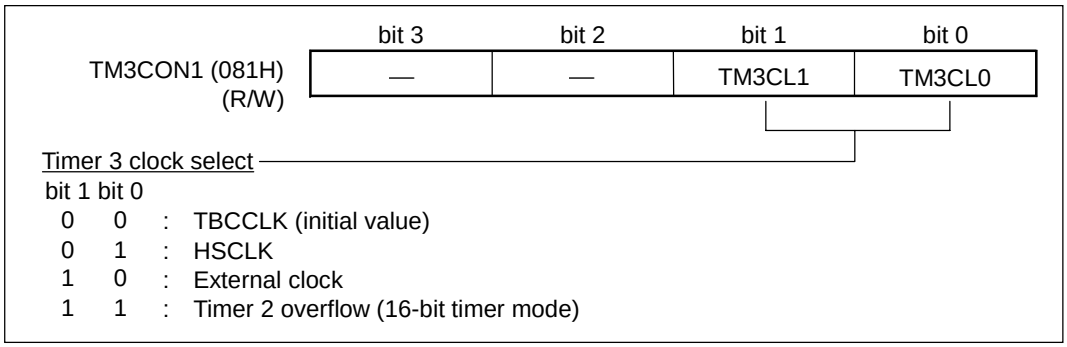
Timer 3 Registers



bit 0: TM3RUN

This bit selects the timer 3 operation mode.

The timer 3 operation mode can be selected as auto-reload mode or 16-bit timer mode.



bit 1, 0: TM3CL1, TM3CL0

These bits select the timer 3 clock.

The timer 3 clock can be selected as TBCCLK (low-speed clock), HSCLK (high-speed clock), external clock (T3CK: secondary function of PB.3), or the timer 2 overflow flag.

When using as a 16-bit timer, select timer 2 overflow for the clock.

Note:

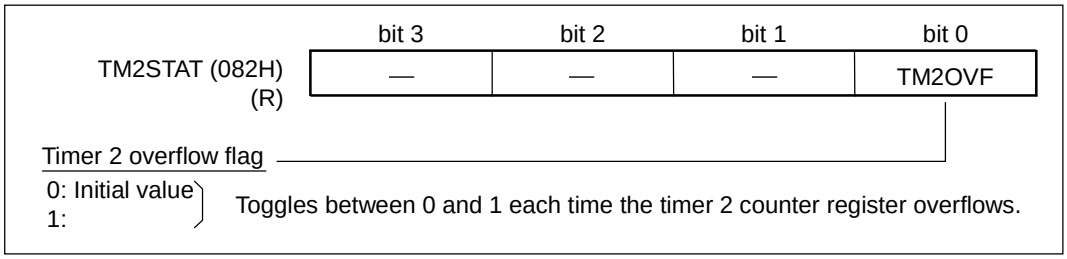
If HSCLK is used as the clock, after ENOSC (bit 1 of FCON) is set to "1", wait for the following time interval before starting timer operation.

- Wait at least 10 ms when using ceramic oscillation.
- Wait at least 300 μs when using RC oscillation.

(4) Timer status registers (TM2STAT, TM3STAT)

- Timer status registers read the status of each timer.
- At system reset, all valid bits are cleared to "0".

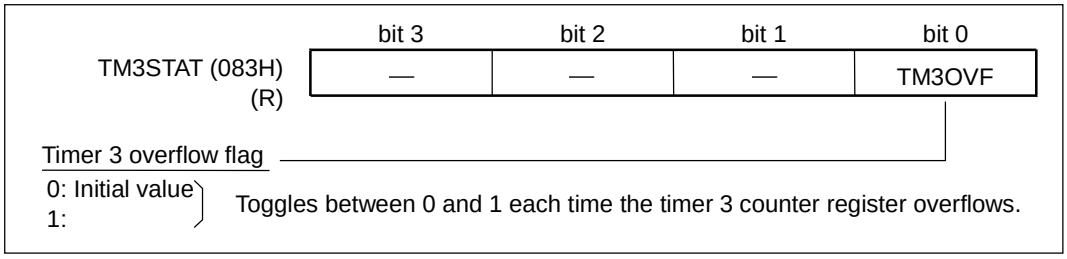
Timer 2 Register



bit 0: TM2OVF (TiMer 2 OVerFlow)

This bit indicates that the timer counter register has overflowed.
This bit toggles between "0" and "1" whenever overflow occurs.
At system reset, TM2OVF is cleared to "0".

Timer 3 Register



bit 0: TM3OVF (TiMer 3 OVerFlow)

This bit indicates that the timer counter register has overflowed.
This bit toggles between "0" and "1" whenever overflow occurs.
At system reset, TM3OVF is cleared to "0".

[Supplement] List of Timer Registers

Timer 2 Registers

Name	Symbol	Address	R/W	Initial value
Timer 2 data register L	TM2DL	076H	R/W	0H
Timer 2 data register H	TM2DH	077H		0H
Timer 2 counter register L	TM2CL	07AH	R/W	0H
Timer 2 counter register H	TM2CH	07BH		0H
Timer 2 control register 0	TM2CON0	07EH	R/W	0AH
Timer 2 control register 1	TM2CON1	07FH		0CH
Timer 2 status register	TM2STAT	082H	R	0EH

Timer 3 Registers

Name	Symbol	Address	R/W	Initial value
Timer 3 data register L	TM3DL	078H	R/W	0H
Timer 3 data register H	TM3DH	079H		0H
Timer 3 counter register L	TM3CL	07CH	R/W	0H
Timer 3 counter register H	TM3CH	07DH		0H
Timer 3 control register 0	TM3CON0	080H	R/W	0EH
Timer 3 control register 1	TM3CON1	081H		0CH
Timer 3 status register	TM3STAT	083H	R	0EH

7.4 Timer Operation

7.4.1 Timer Clock

The timer clock can be selected as TBCCLK (low-speed clock: 32.768 kHz), HSCLK (high-speed clock), or an external clock. By using timer 2 overflow signals as clocks for timer 3, the timers can be used in pairs as 16-bit timers.

If the high-speed clock (HSCLK) is to be used, after setting ENOSC (bit 1 of FCON), wait at least 10 ms in the ceramic oscillation mode or 300 μs in the RC oscillation mode before operating the timer.

The external clock is input to a port assigned as a secondary function port. In the case of timer 2, PB.2/T2CK is used as the input pin for the external clock. In the case of timer 3, PB.3/T3CK is used as the input pin for the external clock. Since the external clock is sampled by the system clock (CLK), the high and low levels of the external clock should be longer than 1 cycle of the system clock (CLK).

7.4.2 Timer Data Registers

TM2DL, TM2DH, TM3DL and TM3DH are 4-bit registers.

In the auto-reload mode, the timer data registers save values that are reloaded into the timer counter registers when the timer counter registers overflow.

Each timer data register can be read/written by software. Writing to timer data registers does not change the contents of the timer counter registers.

7.4.3 Timer Counter Registers

TM2CL and TM2CH, and TM3CL and TM3CH are 8-bit binary counters that are incremented at the falling edge of the timer clock.

Each timer counter register can be read/written by software. However, if the CPU clock and timer clock are different, values that are read or written during the count operation cannot be guaranteed. If an external clock is used as the timer clock, reading/writing is always possible.

When a value is written to any timer counter register, the same value is also written to the corresponding timer data register.

7.4.4 Timer Interrupt Requests and Overflow Flags

Timers generate timer interrupt requests when the timer counter register overflows. The overflow flag toggles between "1" and "0" at each overflow.

Figure 7-3 indicates the operation timing for timer counter register overflow. Table 7-1 lists timer interrupts.

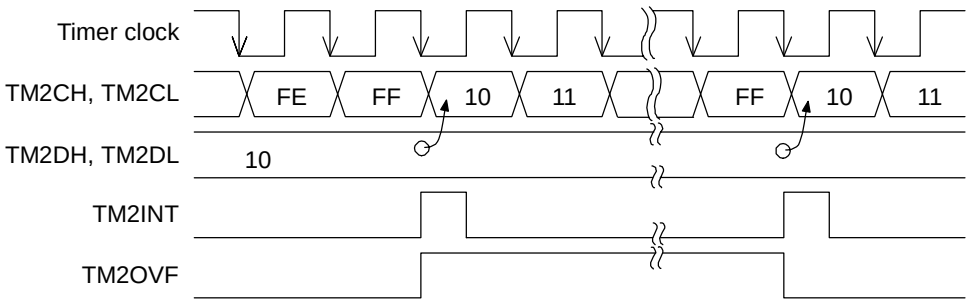


Figure 7-3 Timer Counter Register Overflow Timing (for Timer 2)

Table 7-1 List of Timer Interrupts

Interrupt factor	Symbol	IRQ flag (IRQ2)	IE flag (IE2)	Interrupt vector address
Timer 2 interrupt	TM2INT	QTM2	ETM2	0024H
Timer 3 interrupt	TM3INT	QTM3	ETM3	0026H

When the master interrupt enable flag (MIE) is set to "1" with the interrupt enable flags (ETM2, 3) set to "1", and a timer overflow occurs, a CPU interrupt request is generated.

7.4.5 Auto-Reload Mode Operation

Timers 2 and 3 can be used as auto-reload mode timers. The setup method is as follows.

- Timer 2: Set FMEAS2 (bit 2 of TM2CON0) to "0".
- Timer 3: No setup needed.

In the auto-reload mode, each time the timer counter register overflows, the timer data register value is reloaded into the timer counter register, and counting begins from the value. Setting the RUN bits (TM2RUN, TM3RUN) for each timer control register to "1" will restart the count, and resetting to "0" stops the count.

In the 16-bit timer mode for timers 2 and 3 the TM3RUN bit is disabled, and start/stop is controlled with the TM2RUN bit.

Figure 7-4 shows auto-reload mode timing for pulse generation when timers 2 and 3 are used as a 16-bit timer.

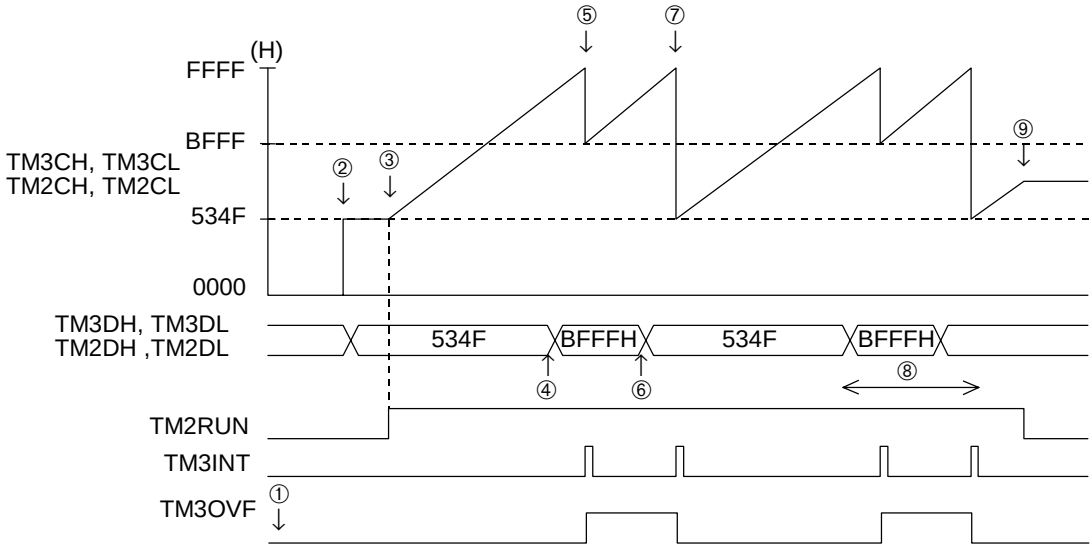


Figure 7-4 Auto-Reload Mode Timing

The operation procedures are as follows.

① Write 534FH to the timer data and timer counter registers.
TM3DH = TM3CH = 5H (bits 15–12)
TM3DL = TM3CL = 3H (bits 11–8)
TM2DH = TM2CH = 4H (bits 7–4)
TM2DL = TM2CL = FH (bits 3–0)

② If TM2CON and TM3CON are set to auto-reload mode and TM2RUN is set to "1", the timer counter register will start to count from 534FH.

③ Before the timer counter register overflows, write the next reload value BFFFH to the timer data register.

④ When the timer counter register overflows, BFFFH is set to the timer counter register, timer interrupt TM3INT is generated and timer 3 overflow flag TM3OVF toggles. The timer counter register continues to count up from BFFFH.

⑤ Before the timer counter register overflows, write the next reload value 534FH to the timer data register.

⑥ When the timer counter register overflows, 534FH is set to the timer counter register, timer interrupt TM3INT is generated and timer 3 overflow flag TM3OVF toggles. The timer counter register resumes counting from address 534FH.

⑦ Repeat steps 3 through 6.

⑧ Halt the count by resetting TM2RUN to "0".

Figure 7-5 shows TM2RUN count start/halt timing.

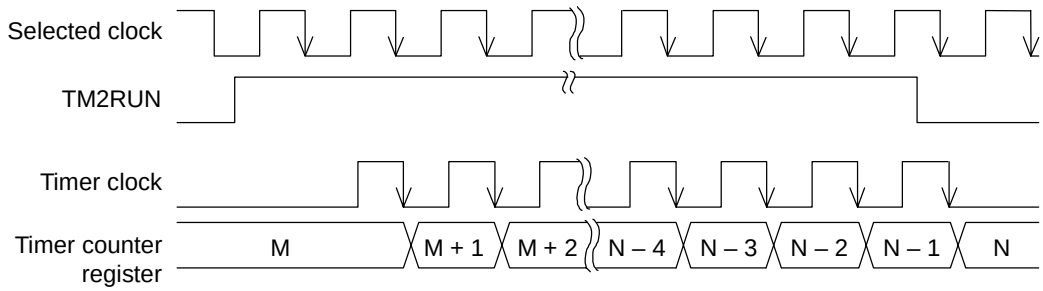


Figure 7-5 TM2RUN Count Start/Halt Timing

When TM2RUN is set to "1", the timer counter starts to count from the second falling edge of the selected clock. When TM2RUN is reset to "0", the counter stops counting at the falling edge of the selected clock which appears immediately after the TM2RUN falling edge.

7.4.6 Frequency Measurement Mode Operation

The frequency measurement mode is used to measure the frequency of the RC oscillator clock, which has wide product variation.

Timers 2 and 3 can be used in the frequency measurement mode. These timers are set as follows for the frequency measurement mode:

- Timer 2: Set FMEAS2 (bit 2 of TM2CON0) to "1", and set TM2RUN (bit 0 of TM2CON0) to "0".
- Timer 3: Set TM3RUN (bit 0 of TM3CON0) to "0".

The count obtained in the frequency measurement mode can be used to determine the auto-reload mode timer data register value, thereby making the timer overflow to generate various signals with required cycles. During serial transmission, the timer 3 interrupt signal (TM3INT) is used as the baud rate clock.

Figure 7-6 indicates frequency measurement mode timing when timers 2 and 3 are used as a 16-bit timer.

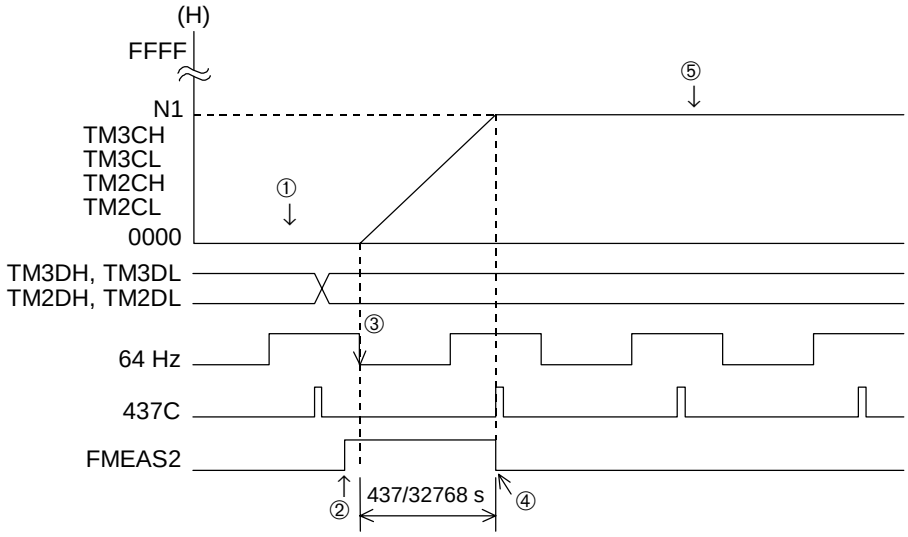


Figure 7-6 Frequency Measurement Mode Timing

The operation sequence for Figure 7-6 is as follows.

① Timer 3 control registers 0 and 1 (TM3CON0, TM3CON1) are set for 16-bit timer mode, and the timer counter and timer data register are cleared to "0". Enable the high-speed clock by the frequency control register (FCON) and the timer clock is set to HSCLK.

② Wait 10 ms or more in the ceramic oscillation mode or 300 µs or more in the RC oscillation mode after starting the high-speed clock and set FMEAS2 to "1" to enter the frequency measurement mode.

③ When FMEAS2 is "1", the counter starts at the 64 Hz falling edge.

④ When the 437C signal is "1", FMEAS2 is reset to "0", and the counter stops at the falling edge of the next clock. The 437C signal is a pulse signal which rises in 437/32768 second after the 64 Hz falling edge.

⑤ Timer counter register value N1 is read.

Assuming that the ceramic oscillation clock is exactly 2 MHz, value N1 read from the timer counter register is:

N1 = 2000000 × 437/32768
= 26672 (decimal)
= 6830 (hexadecimal)
= 0110 1000 0011 0000 (binary)
(truncated)

Because 437/32768 second is equivalent to 128 clocks at 9600 Hz (more precisely, 9598 Hz), a division of the count by 128 provides the frequency ratio (N2) between 2 MHz and 9600 Hz. Because $128 = 2^7$, that can be determined by merely truncating the righthand seven digits of N1 (binary), yielding:

N2 = 26672/128 = 011010000 (binary)
= D0 (hexadecimal)
= 208 (decimal)

This indicates that 9600 Hz is about 208 times the cycle of 2 MHz, which means that the timer data register should be set to FF30H so that the counter overflows every 208 counts of the 2 MHz clock in auto-reload mode. As a result, overflow produces a TM3INT cycle t_{TM3INT} of

$t_{TM3INT} = 1/2000000 \times 208 = 0.104$ ms (9615 Hz)

In the same way, assuming that RC oscillation clock is 600 kHz due to manufacturing variation, we get

N1 = 600000 × 437/32768 = 8001 (decimal)
= 1F41 (hexadecimal)
= 0001 1111 0100 0001 (binary)
(truncated)

Truncating the righthand seven digits of N1 (binary), we get

N2 = 8001/128 = 000111110 (binary)
= 3E (hexadecimal)
= 62 (decimal)

Set the timer data register to FFC2H so that the counter overflows every 62 counts of the 600 kHz clock in auto-reload mode. As a result, overflow produces a TM3INT cycle t_{TM3INT} of

$t_{TM3INT} = 1/600000 \times 62 = 0.10333$ ms (9677 Hz)

In this way the frequency measurement mode can be applied to generate TM3INT signals with precision cycles. These TM3INT signals can be supplied to the serial port as a baud rate clock.

Changing the value of N2 makes it possible to generate baud rates of 4800 Hz, 2400 Hz or user-defined rates. The precision of the generated baud rate clock is within ±2% for 9600 Hz, and within ±1% for 4800 Hz or lower.

Figure 7-7 illustrates the operation of baud rate clock generation for an RC oscillator clock frequency of 600 kHz.

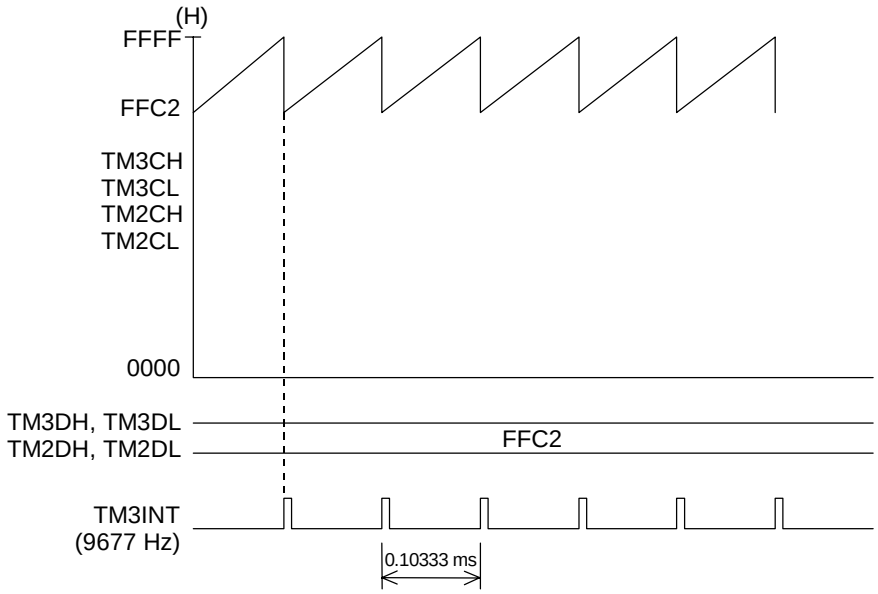


Figure 7-7 Baud Rate Clock Generation

Chapter 8

100 Hz Timer Counter (100HzTC)

8. 100 Hz Timer Counter (100HzTC)

8.1 Overview

The 100 Hz timer counter has a circuit that divides the TBC6 output (512 Hz) of the time base counter to generate a 10 Hz interrupt. The 100 Hz timer consists of a 5/6-base counter and two decimal counters.

8.2 100 Hz Timer Counter Configuration

Figure 8-1 indicates the configuration of the 100 Hz timer counter.

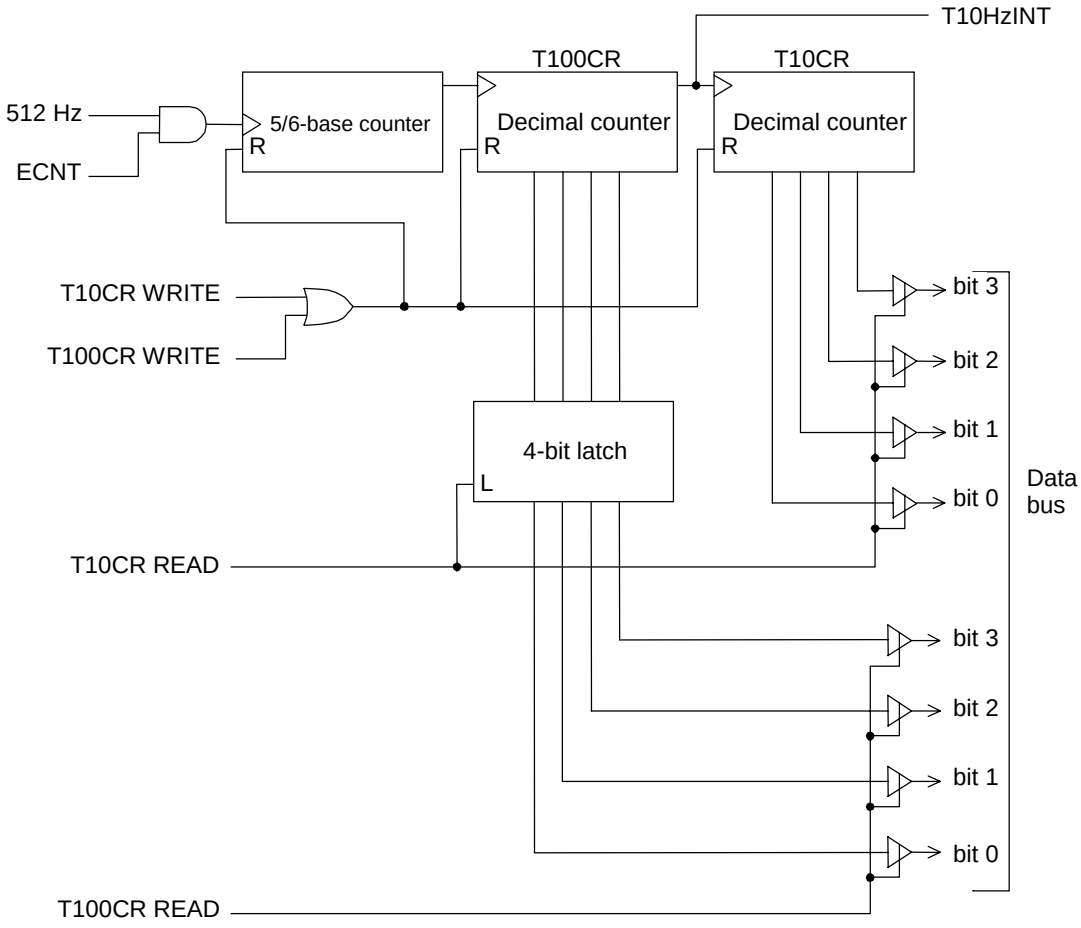
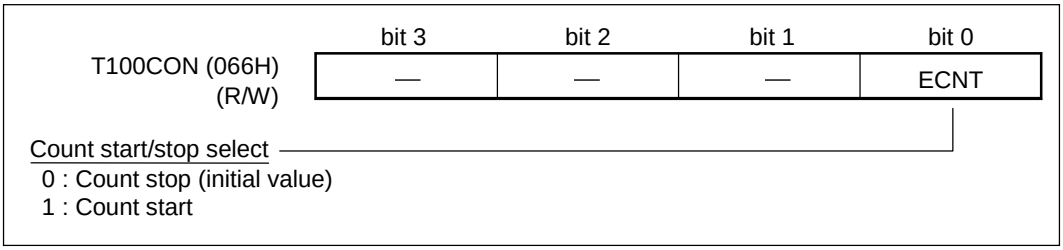


Figure 8-1 100 Hz Timer Counter Configuration

8.3 100 Hz Timer Counter Registers

(1) 100 Hz timer counter control register (T100CON)

This is a 4-bit special function register (SFR) controlling the 100 Hz timer counter.

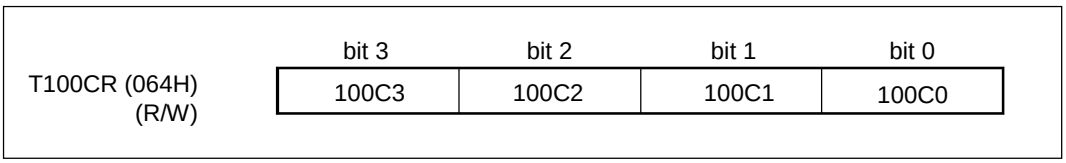


bit 0: ECNT
This bit controls count start/stop for the 100 Hz timer counter internal counter. Count starts when set to "1". At system reset the value is reset to "0" and counting is stopped.

(2) 100 Hz counter register (T100CR)

This is a 4-bit special function register (SFR) to read the 100 Hz counter of the 100 Hz timer counter. The content of the T100CR is latched by a 4-bit latch in T10CR read operation, so the value of the T100CR must always be read after reading T10CR.

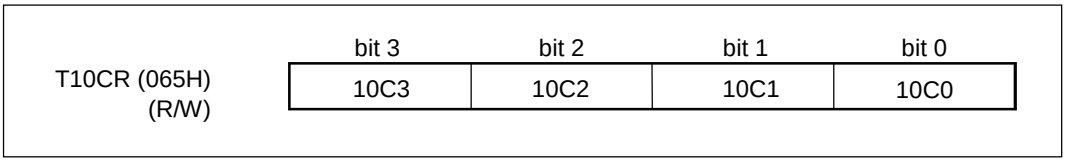
When data is written in T100CR, both T100CR and T10CR are reset to "0".



(3) 10 Hz counter register (T10CR)

A 4-bit special function register (SFR) to read the 10 Hz counter in the 100 Hz timer counter.

When data is written in T10CR, both T100CR and T10CR are reset to "0".



8.4 100 Hz Timer Counter Operation

The 100 Hz timer counter begins counting when bit 0 (ECNT) of the 100 Hz timer counter control register (T100CON) is set to "1". The 512 Hz output of the time base counter is divided into 100 Hz by the 5/6-base counter.

The 100 Hz signal is input to the 100 Hz counter (T100CR) and the carry output of that counter is input to the 10 Hz counter (T10CR). The T10HzINT signal, which is the carry output (10 Hz) of the T100CR 100 Hz counter, also generates an interrupt request, setting bit 3 (Q10Hz) of interrupt request registers 3 (IRQ3) to "1".

If either T100CR or T10CR is written to, both are reset to "0". The write data used has no significance. For example, the "MOV T100CR,A" instruction is not dependent on the contents of the accumulator.

If T10CR is read, the contents of T100CR at that time are latched to the 4-bit latch. Therefore, the contents of T100CR at the time T10CR is read can be read correctly.

Chapter 9

Watchdog Timer (WDT)

9. Watchdog Timer (WDT)

9.1 Overview

The watchdog timer is a circuit to detect CPU malfunction. The WDT consists of a 9-bit watchdog timer counter (WTDC) counting the 256 Hz output of the TBC7 of the time base counter (TBC), and a watchdog timer control register (WDTCON) to start and clear WDTC.

9.2 Watchdog Timer Configuration

Figure 9-1 shows the configuration of the watchdog timer.

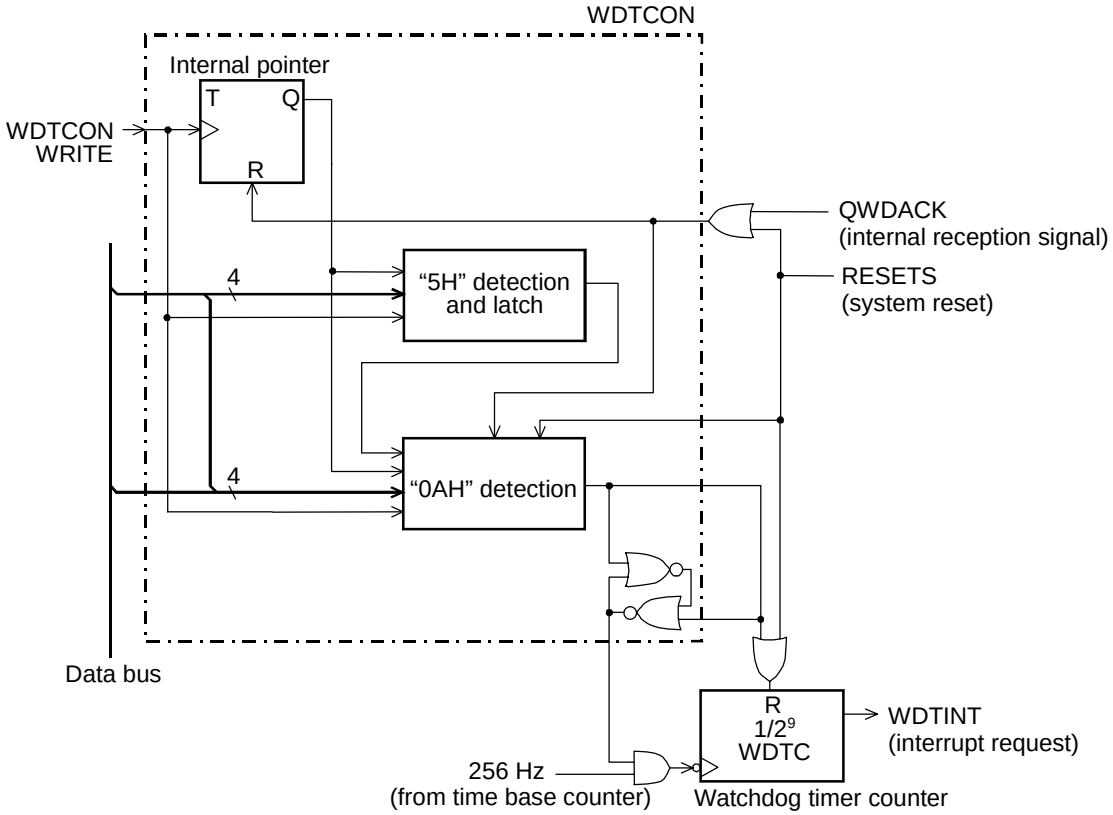


Figure 9-1 Watchdog Timer Configuration

9.3 Watchdog Timer Control Register (WDTCON)

The watchdog timer control register (WDTCON) is a 4-bit write only special function register (SFR) used to start/clear the watchdog timer counter (WDTC).

	bit 3	bit 2	bit 1	bit 0
WDTCON (09FH) (W)	d3	d2	d1	d0

9.4 Watchdog Timer Operation

At system reset, WDTC (watchdog timer counter) stops counting.

WDTC begins counting by writing "5H" to WDTCON (watchdog timer control register) while the internal pointer is "0", and then writing "0AH" (while the internal pointer is "1").

The internal pointer is cleared to "0" at system reset or when WDTC overflows, and toggles every time a write operation to WDTCON is performed.

After WDTC is activated, WDTC is cleared by writing "5H" to WDTCON while the internal pointer is "0", and then writing "0AH" while the internal pointer is "1". When WDTC overflows (1FFH→000H), a watchdog timer interrupt request (WDTINT) is generated. WDTINT cannot be disabled by the software (non-maskable interrupt) and has the highest level of interrupt priority.

The WDTC overflow cycle (T) is given by:

$$T = \frac{128 \times 512}{32768\ (\text{Hz})} = 2\ \text{s}$$

The minus deviation (t) of the WDTC overflow cycle is given by:

$$t = \frac{128}{32768\ (\text{Hz})} = \text{approximately } 3.9\ \text{ms}$$

Therefore, the WDTC clear cycle (Ct) can be computed as follows.

$$Ct = T - t = 2\ \text{s} - 3.9\ \text{ms} = 1.9961\ \text{s}$$

If 32.768 kHz is to be used as the low-speed clock, the software must be programmed to clear WDTC within 1.9961 s.

If the CPU malfunctions due to a power failure or other factor and the WDTC cannot be cleared normally, WDTC will overflow and WDTINT will be generated. Program the watchdog timer interrupt routine to handle recovery operations by returning to the normal routine.

Note:

The watchdog timer cannot detect all operating faults. If the CPU malfunctions but WDTC can still be cleared, a fault will not be detected.

Figure 9-2 shows a flowchart of watchdog timer processing.

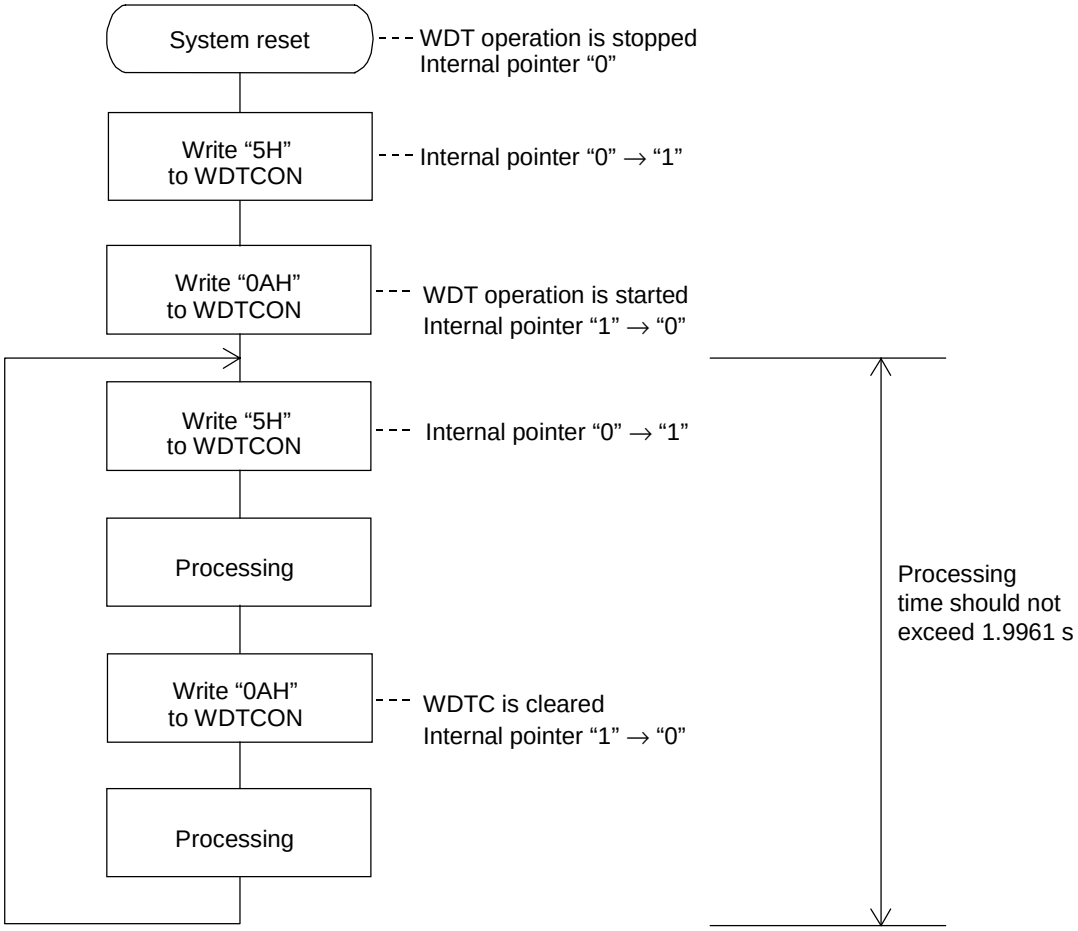


Figure 9-2 Watchdog Timer Processing Flowchart

Figure 9-3 shows the timing chart for watchdog timer operation.

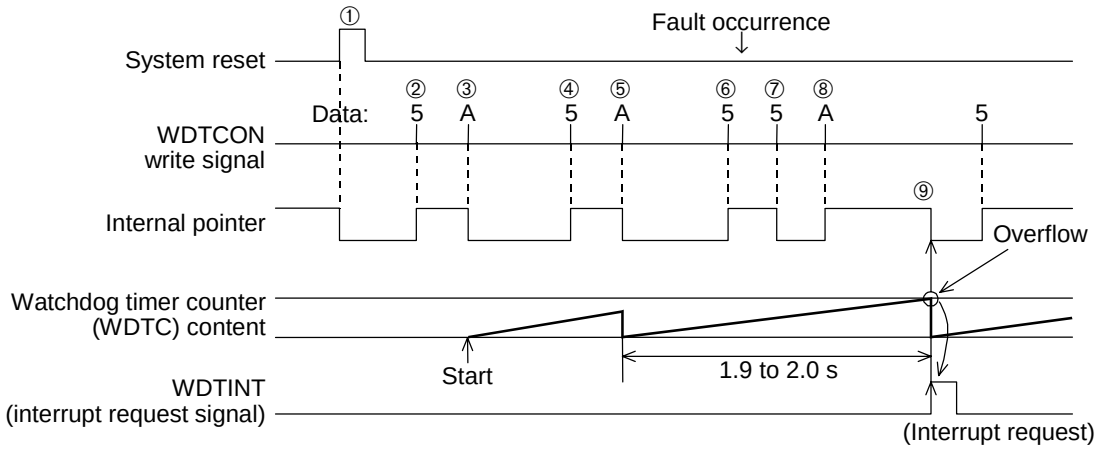


Figure 9-3 Watchdog Timer Operation Timing Chart

The watchdog timer operating sequence is shown below.

① System reset clears the internal pointer and WDTC.

② Write "5H" to WDTCON. (Internal pointer 0→1)

③ Write "0AH" to WDTCON to start WDTC. (Internal pointer 1→0)

④ Write "5H" to WDTCON. (Internal pointer 0→1)

⑤ Write "0AH" to WDTCON to clear WDTC. (Internal pointer 1→0)

⑥ Write "5H" to WDTCON. (Internal pointer 0→1)

⑦ After a fault occurs, "5H" is written to WDTCON but is not accepted since the internal pointer is "1". (Internal pointer 1→0)

⑧ "0AH" is written to WDTCON, but since the internal pointer is "0" and the write of "5H" in step ⑦ was not accepted, WDTC will not be cleared. (Internal pointer 0→1)

⑨ Because WDTC was not cleared, overflow of WDTC will generate the watchdog timer interrupt WDTINT. At this time, the internal pointer is cleared to "0".

Chapter 10

Ports (INPUT, OUTPUT, I/O PORT)

10. Ports (INPUT, OUTPUT, I/O PORT)

10.1 Overview

The ML63295A has two 4-bit input ports, six 4-bit output ports and six 4-bit I/O ports.

The V_{DDI} (interface power supply) pin supplies power to the ports.

If a port is to be connected to an external device that operates on a different power supply, the power supply of the external device must be fed to the V_{DDI} pin.


Note:

Since V_{DDI} is separated from the positive power supply pin (V_{DD}), power must be supplied to the V_{DDI} pin.

10.2 Ports List

The ports of the ML63295A are shown in Table 10-1.

Table 10-1 Ports List

Port	I/O	Interrupt	Secondary function	Page
Port 0	I	●	●	10-2
Port 1			●	
Port 2	O			10-9
Port 3				
Port 4			●	10-13
Port 5				
Port 6				
Port 7				
Port 8	I/O	●	●	10-21
Port 9				
Port A				
Port B		●	●	10-30
Port C		●	●	10-37
Port E		●	●	10-45

10.3 Port 0, Port 1 (P0.0–P0.3, P1.0–P1.3)

10.3.1 Port 0, Port 1 Configuration

The ML63295A has 4-bit input-only ports Port 0 and Port 1.

Figure 10-1 shows the configuration of ports 0 and 1.

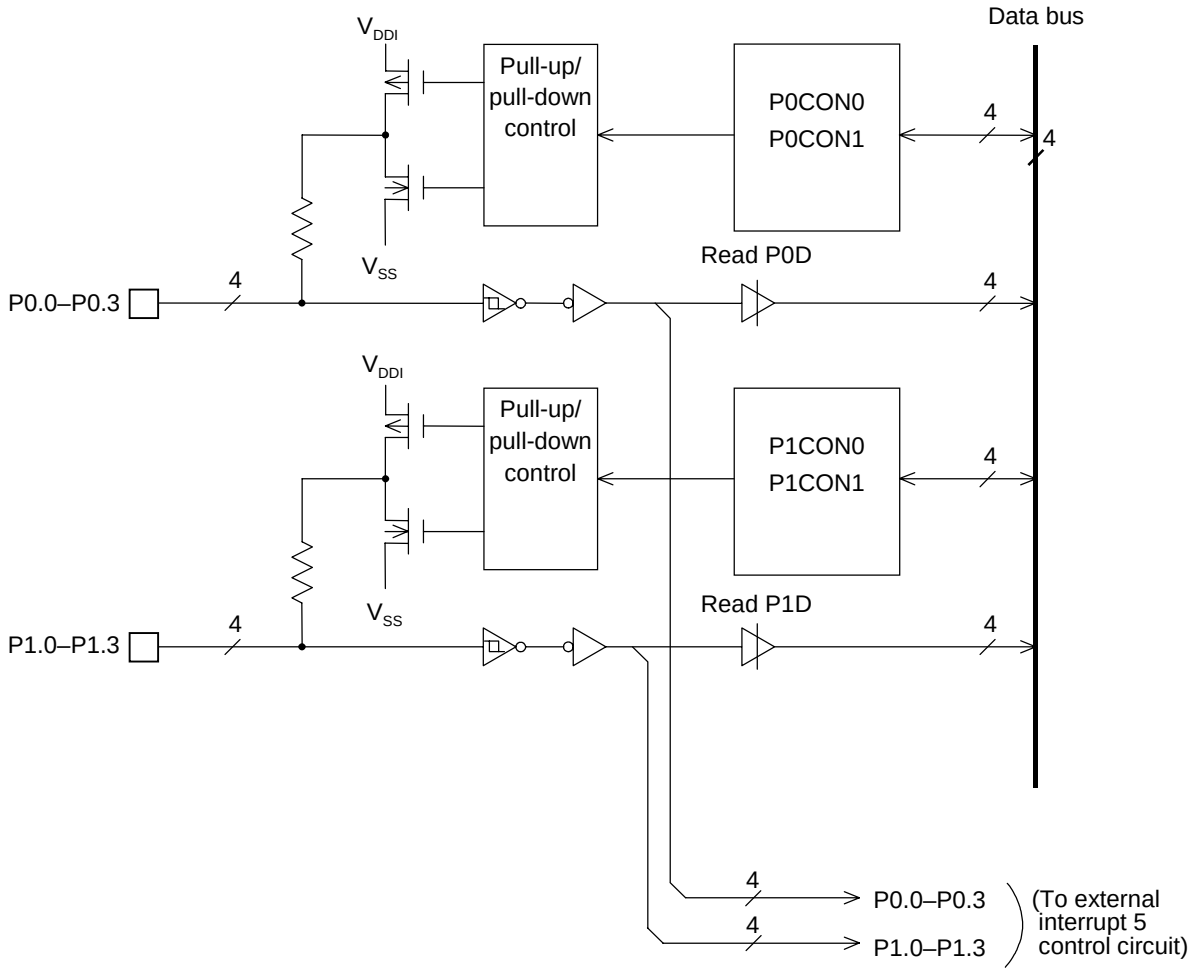


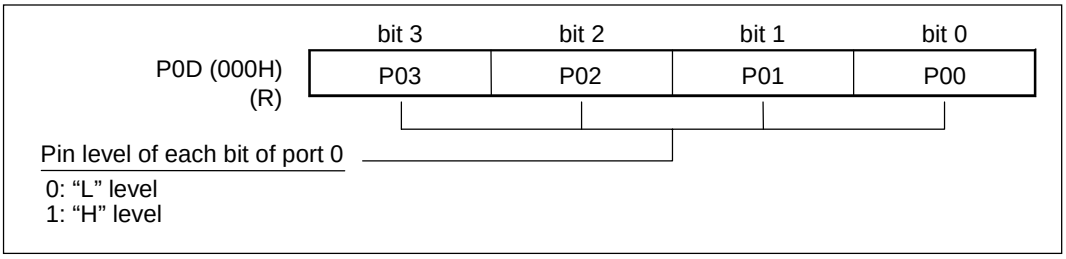
Figure 10-1 Input-Only Port (Port 0, Port 1) Configuration

10.3.2 Port 0, Port 1 Registers

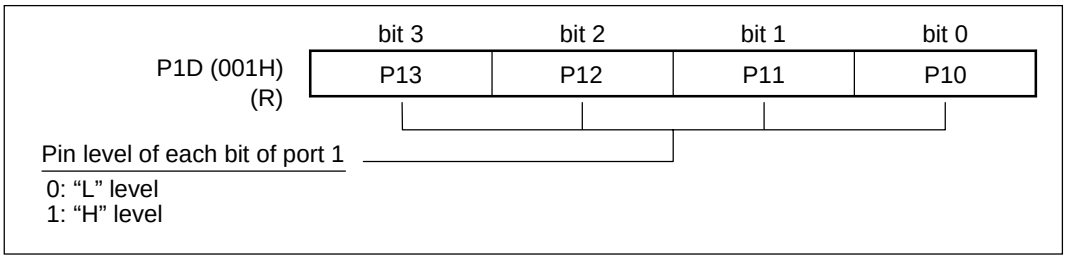
(1) Port 0, Port 1 data registers (P0D, P1D)

The port 0 data register (P0D) and the port 1 data register (P1D) are 4-bit read-only special function registers (SFRs) used to read the pin level of each bit of ports 0 and 1.

- Port 0



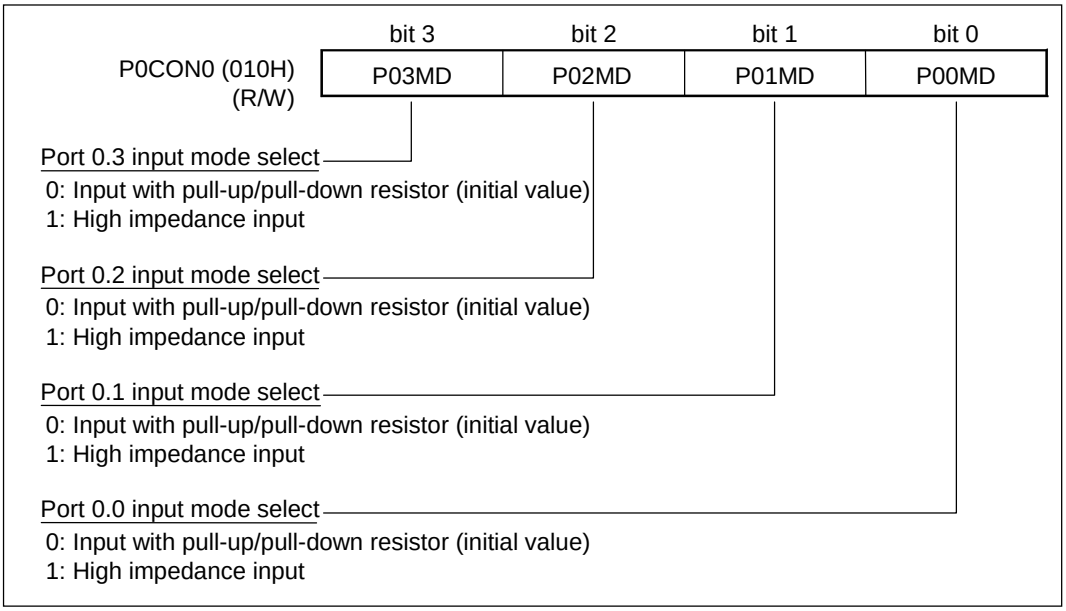
- Port 1

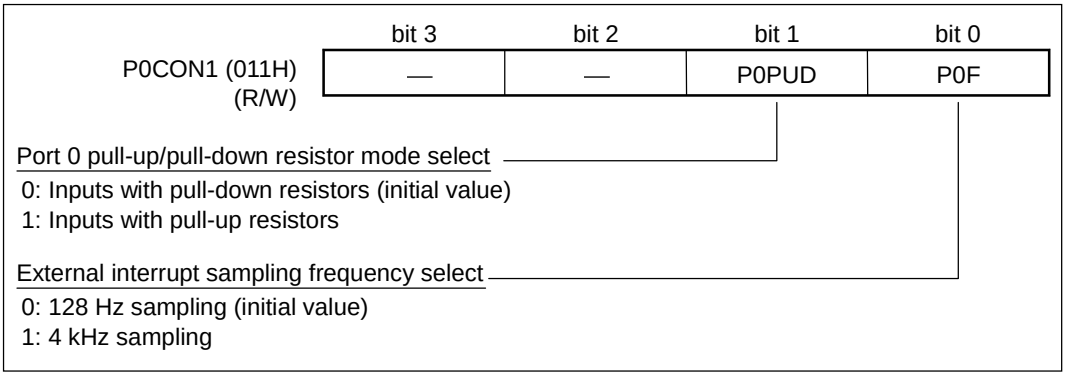


(2) Port 0, Port 1 control registers (P0CON0, P0CON1, P1CON0, P1CON1)

The port 0 control registers 0/1 (P0CON0, P0CON1) and the port 1 control registers 0/1 (P1CON0, P1CON1) are 4-bit special function registers (SFRs) that select input with pull-up or pull-down resistor for each bit and select the external interrupt sampling frequency of Ports 0 and 1 secondary function.

- Port 0

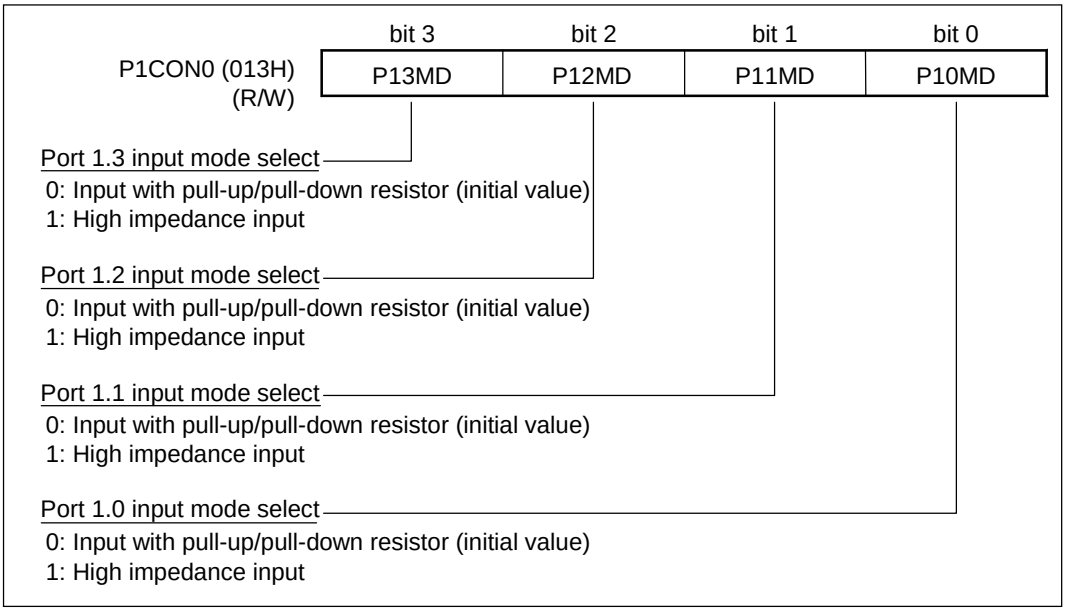


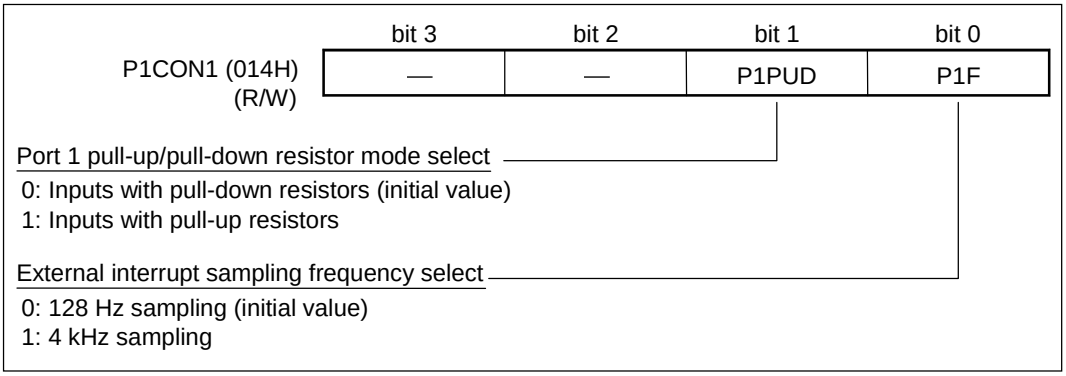


bit 1: P0PUD

This bit is used to select pull-up or pull-down resistors when any of the port 0 pins are selected by P0CON0 as an input with pull-up/pull-down resistor.
Setting P0PUD to "0" selects pull-down resistors, and setting to "1" selects pull-up resistors.
Individual specification of pull-down or pull-up resistor for the pins of port 0.0 to 0.3 is not possible.

- Port 1





bit 1: P1PUD

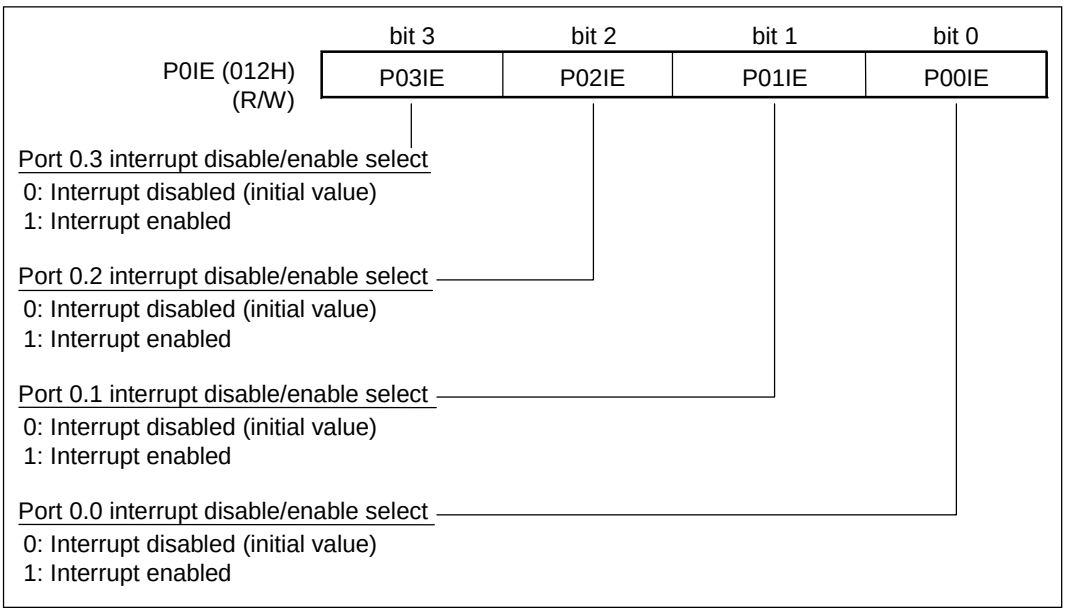
This bit is used to select pull-up or pull-down resistors when any of the port 1 pins are selected by P1CON0 as an input with pull-up/pull-down resistor.
Setting P1PUD to "0" selects pull-down resistors, and setting to "1" selects pull-up resistors.
Individual specification of pull-down or pull-up resistor for the pins of port 1.0 to 1.3 is not possible.

(3) Port 0, Port 1 interrupt enable registers (P0IE, P1IE)

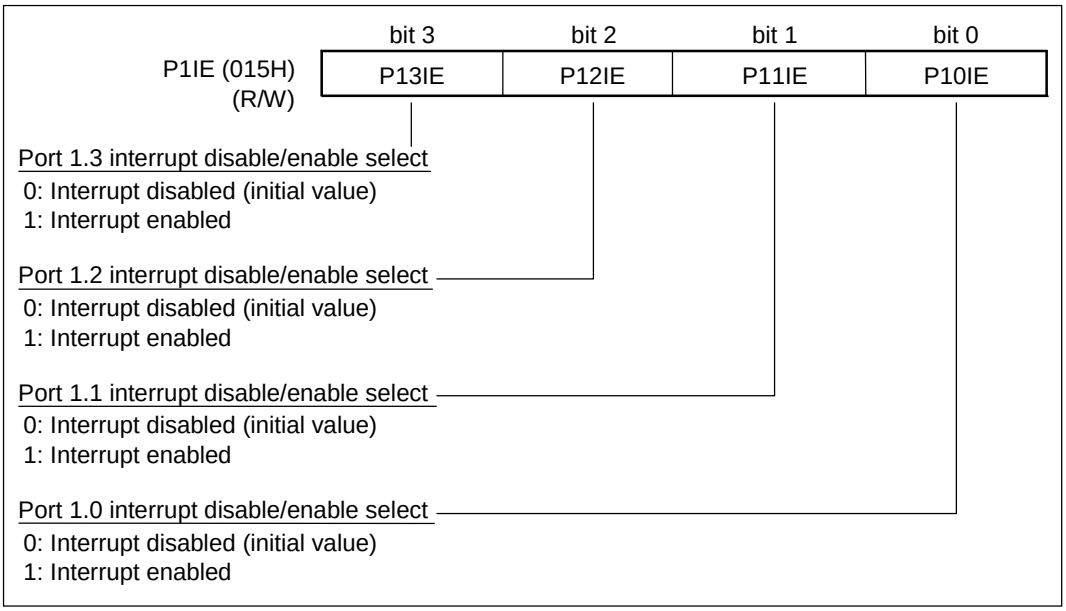
The port 0 interrupt enable register (P0IE) and the port 1 interrupt enable register (P1IE) are 4-bit special function registers (SFRs) that enable/disable individual bits when port 0 and port 1 are used as external interrupt.

At system reset, all bits in P0IE and P1IE are cleared to "0" and ports 0 and 1 are initialized to the interrupt disabled state.

- Port 0



- Port 1



10.3.3 Port 0, Port 1 External Interrupt Function (External Interrupt 5)

An external interrupt (external interrupt 5) is assigned to port 0 and port 1 as a secondary function. Individual bits can be enabled/disabled for external interrupt 5.

External interrupt generation for each input of port 0 and port 1 is triggered by the falling edge of either the 128 Hz or 4 kHz sampling clock from the time base counter.

After the port level changes, interrupt request signal XI5INT is output and external interrupt 5 request flag (QXI5) is set. The maximum time delay from the change in port level until setting QXI5 is one cycle of the sampling clock (128 Hz or 4 kHZ).

Because the port 0 and port 1 external interrupt 5 is set by a level change at any of the port 0 or port 1 inputs, each bit of the port must be read to determine which bit of port 0 or port 1 generated the interrupt.

The interrupt vector address for external interrupt 5 is 001EH.

Figure 10-2 shows an equivalent circuit of external interrupt 5 control.

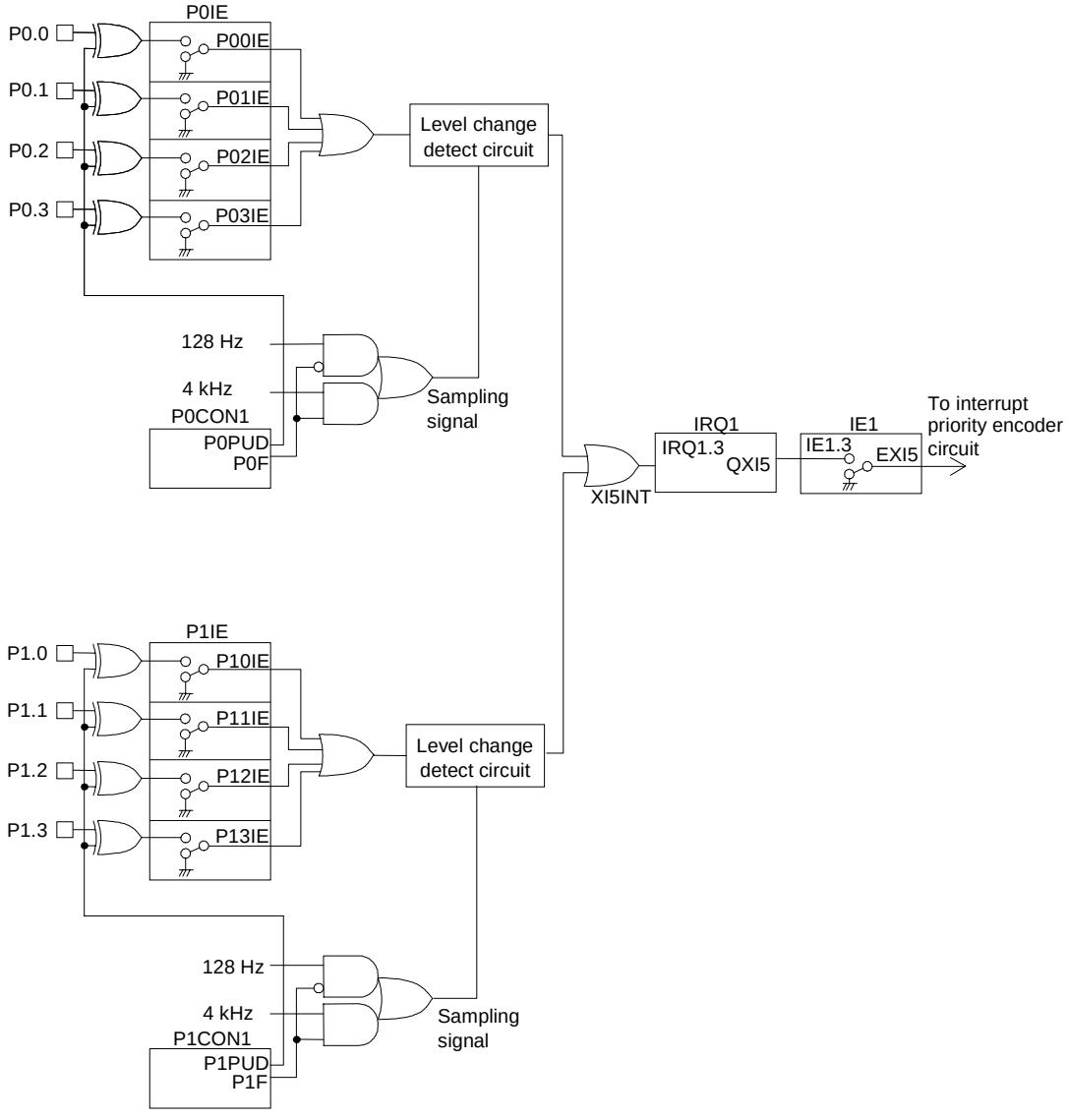


Figure 10-2 Equivalent Circuit of External Interrupt 5 Control

Figure 10-3 shows the timing for generation of external interrupt 5.

(a) P0PUD and P1PUD = "0" (initial value: inputs with pull-down resistors) setting

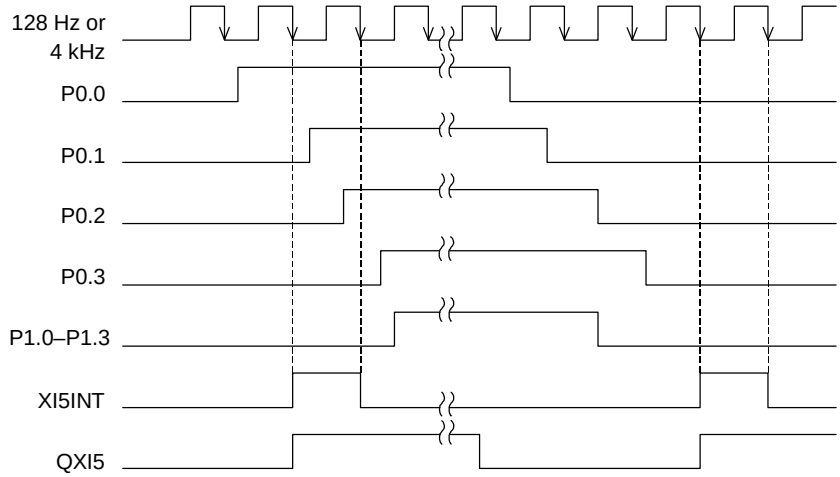
- When all P0.0 to P0.3 and P1.0 to P1.3 inputs are at a "L" level
  External interrupt 5 is generated when any port 0 or port 1 input changes to a "H" level.

- When any of P0.0 to P0.3 or P1.0 to P1.3 inputs is at a "H" level
  External interrupt 5 is generated when all the port 0 and port 1 inputs change to a "L" level.

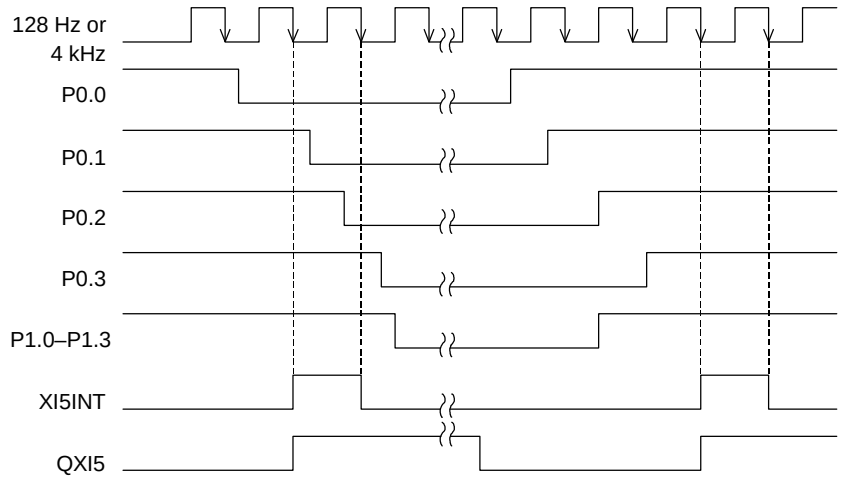
(b) P0PUD and P1PUD = "1" (inputs with pull-up resistors) setting

- When all P0.0 to P0.3 and P1.0 to P1.3 inputs are at a "H" level
  External interrupt 5 is generated when any port 0 or port 1 input changes to a "L" level.

- When any of P0.0 to P0.3 or P1.0 to P1.3 inputs is at a "L" level
  External interrupt 5 is generated when all the port 0 and port 1 inputs change to a "H" level.



(a) When P0PUD = "0" and P1PUD = "0"



(b) When P0PUD = "1" and P1PUD = "1"

Figure 10-3 Interrupt Generation Timing of External Interrupt 5

10.4 Port 2, Port 3 (P2.0–P2.3, P3.0–P3.3)

10.4.1 Port 2, Port 3 Configuration

The ML63295A has 4-bit output-only ports Port 2 and Port 3.

Figure 10-4 shows the configuration of port 2 and port 3.

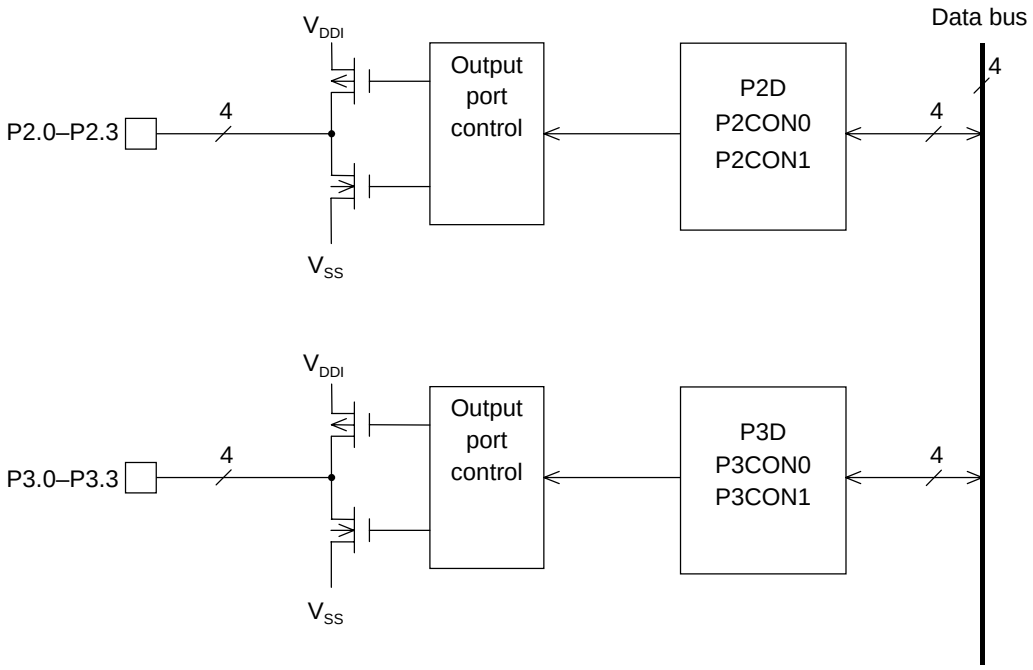


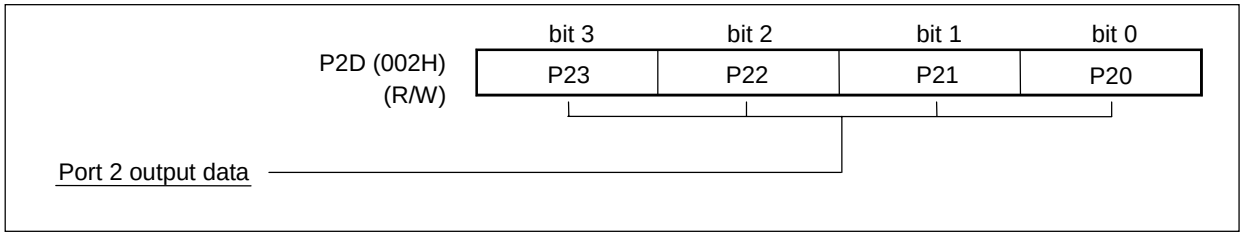
Figure 10-4 Output-Only Port (Port 2, Port 3) Configuration

10.4.2 Port 2, Port 3 Registers

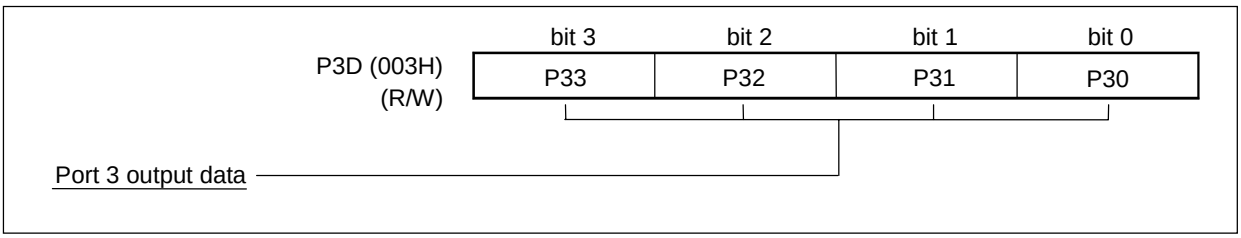
(1) Port 2, Port 3 data registers (P2D, P3D)

The port 2 data register (P2D) and port 3 data register (P3D) are 4-bit special function registers (SFRs) used to set the output values for ports 2 and 3.

- Port 2



- Port 3



At system reset all bits in the port 2 and port 3 data registers (P2D, P3D) are set to "0". When data is written to the port data register, the actual pin change timing is at the rising edge of the system clock for state 2 (S2) of the write instruction.

Figure 10-5 shows port change timing.

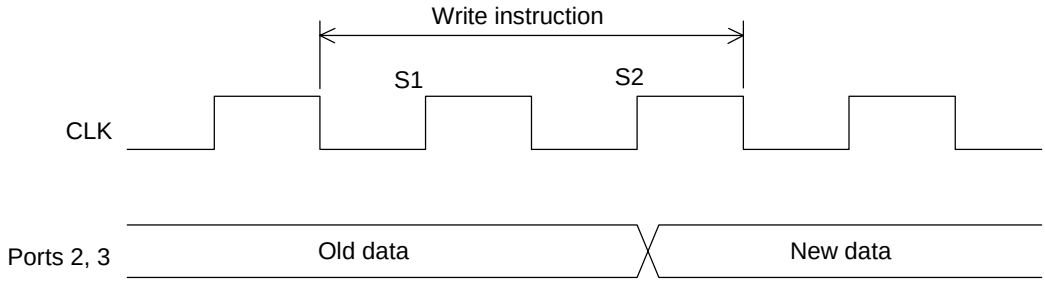


Figure 10-5 Port Change Timing

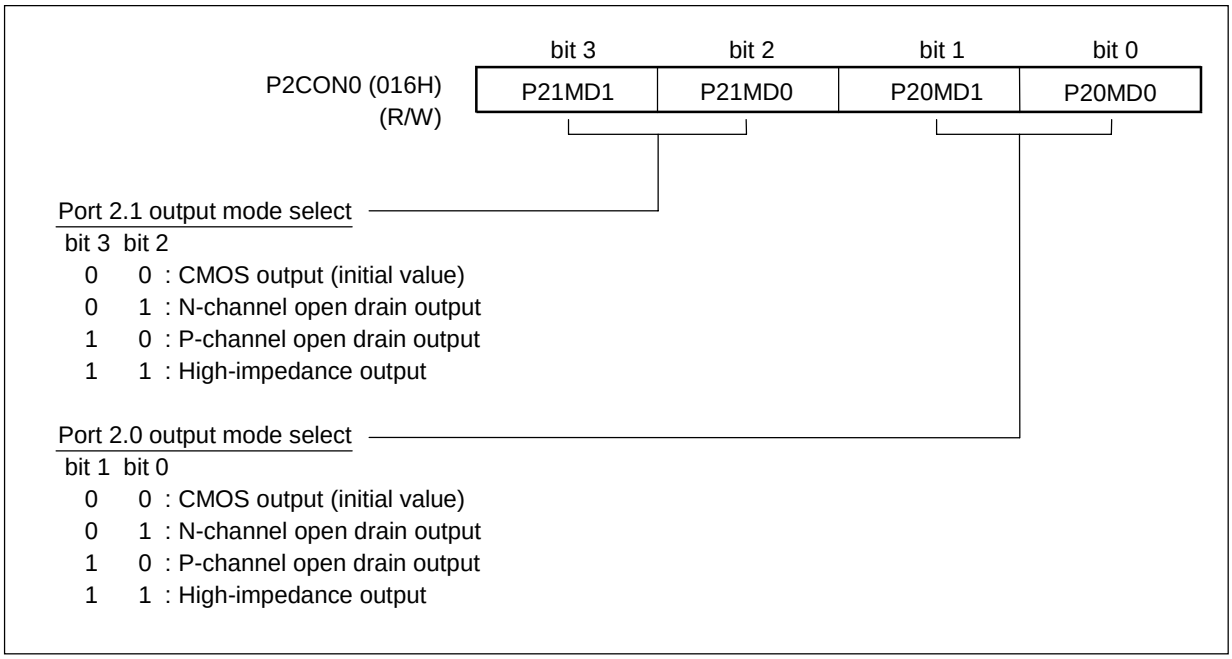
(2) Port 2, Port 3 control registers (P2CON0, P2CON1, P3CON0, P3CON1)

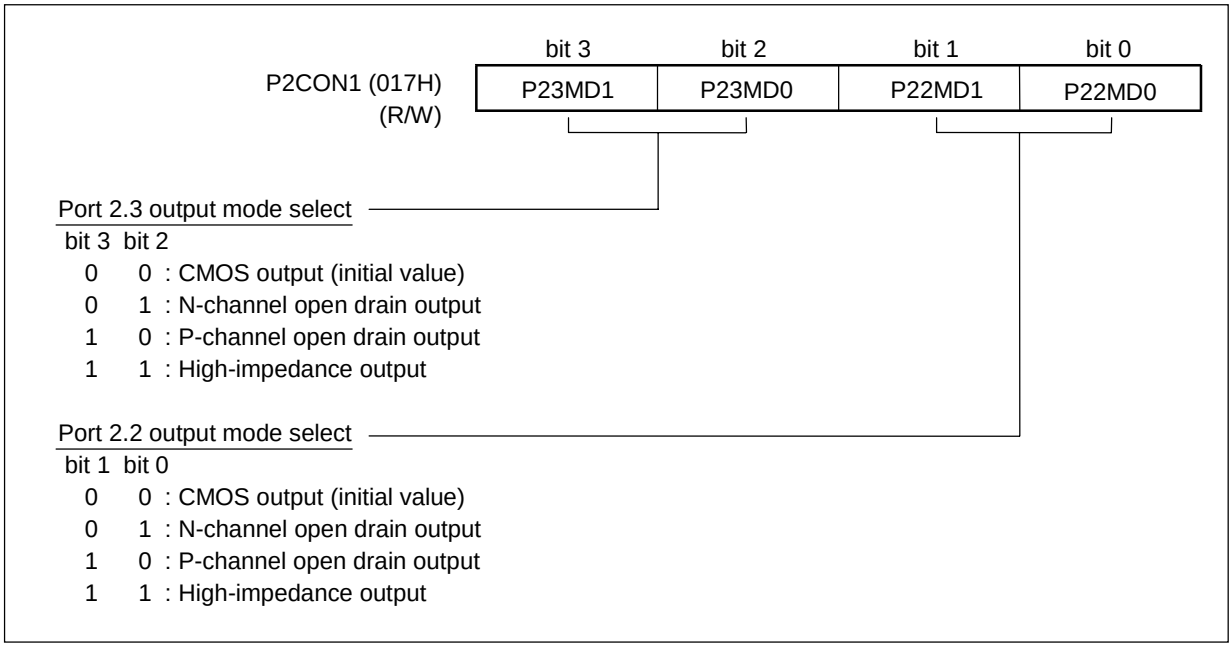
The port 2 control registers 0/1 (P2CON0, P2CON1) and port 3 control registers 0/1 (P3CON0, P3CON1) are 4-bit special function registers (SFRs) used to select port output modes.

The output mode may be CMOS output, N-channel open drain output, P-channel open drain output, or high-impedance output.

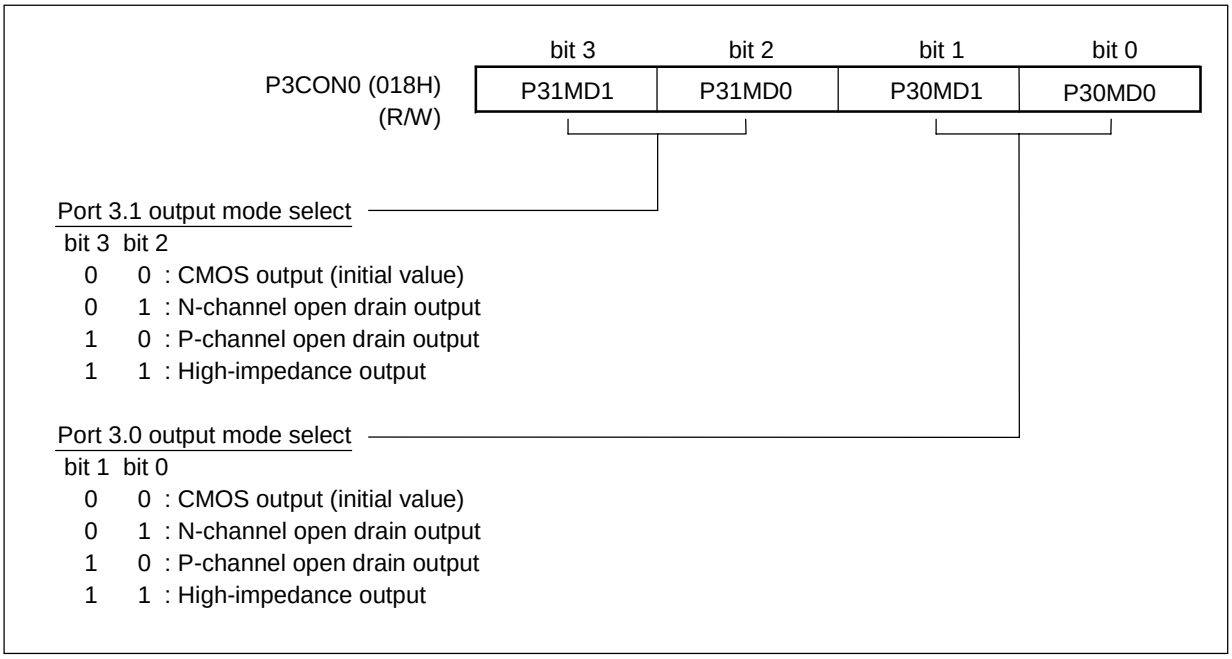
At system reset all bits in P2CON0, P2CON1, P3CON0 and P3CON1 are set to "0", and all ports are initialized to CMOS output mode.

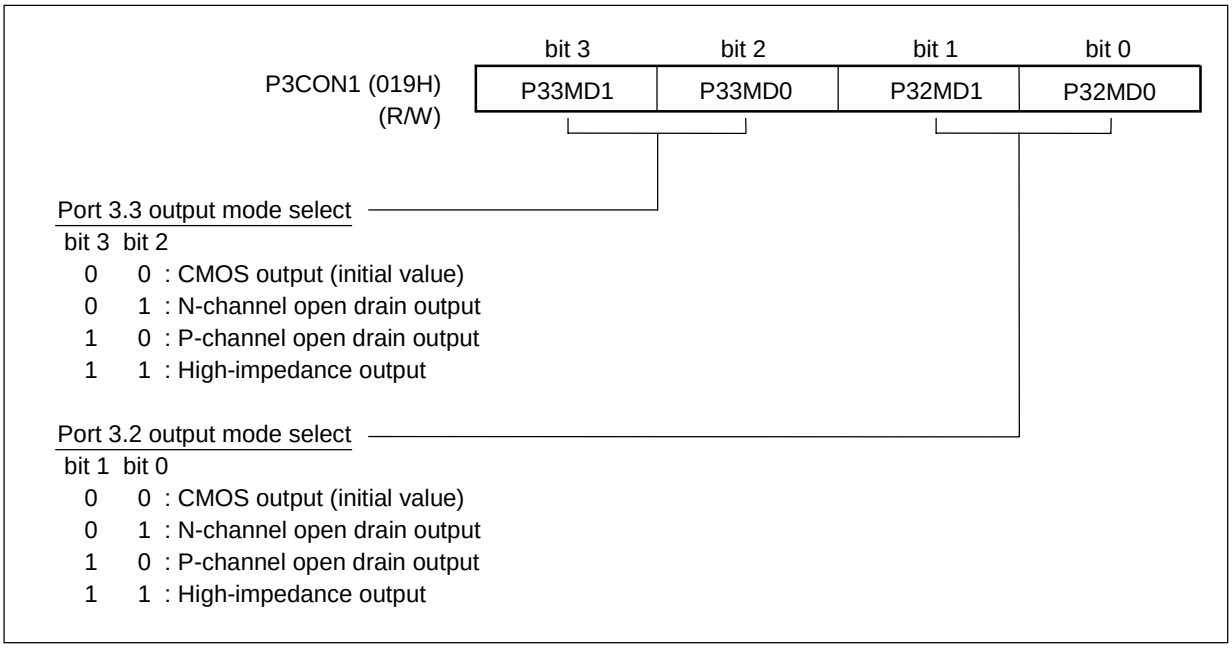
- Port 2





- Port 3


bit 3
bit 2
bit 1
bit 0
P3CON0 (018H)
(R/W)
P31MD1
P31MD0
P30MD1
P30MD0
Port 3.1 output mode select
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port 3.0 output mode select
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output


bit 3
bit 2
bit 1
bit 0
P3CON1 (019H)
(R/W)
P33MD1
P33MD0
P32MD1
P32MD0
Port 3.3 output mode select
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port 3.2 output mode select
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output

10.5 Port 4, Port 5, Port 6, Port 7 (P4.0–P4.3, P5.0–P5.3, P6.0–P6.3, P7.0–P7.3)

10.5.1 Port 4, Port 5, Port 6, Port 7 Configuration

The ML63295A has 4-bit output ports Port 4, Port 5, Port 6, and Port 7.

Figure 10-6 shows the configurations of port 4, port 5, port 6 and port 7.

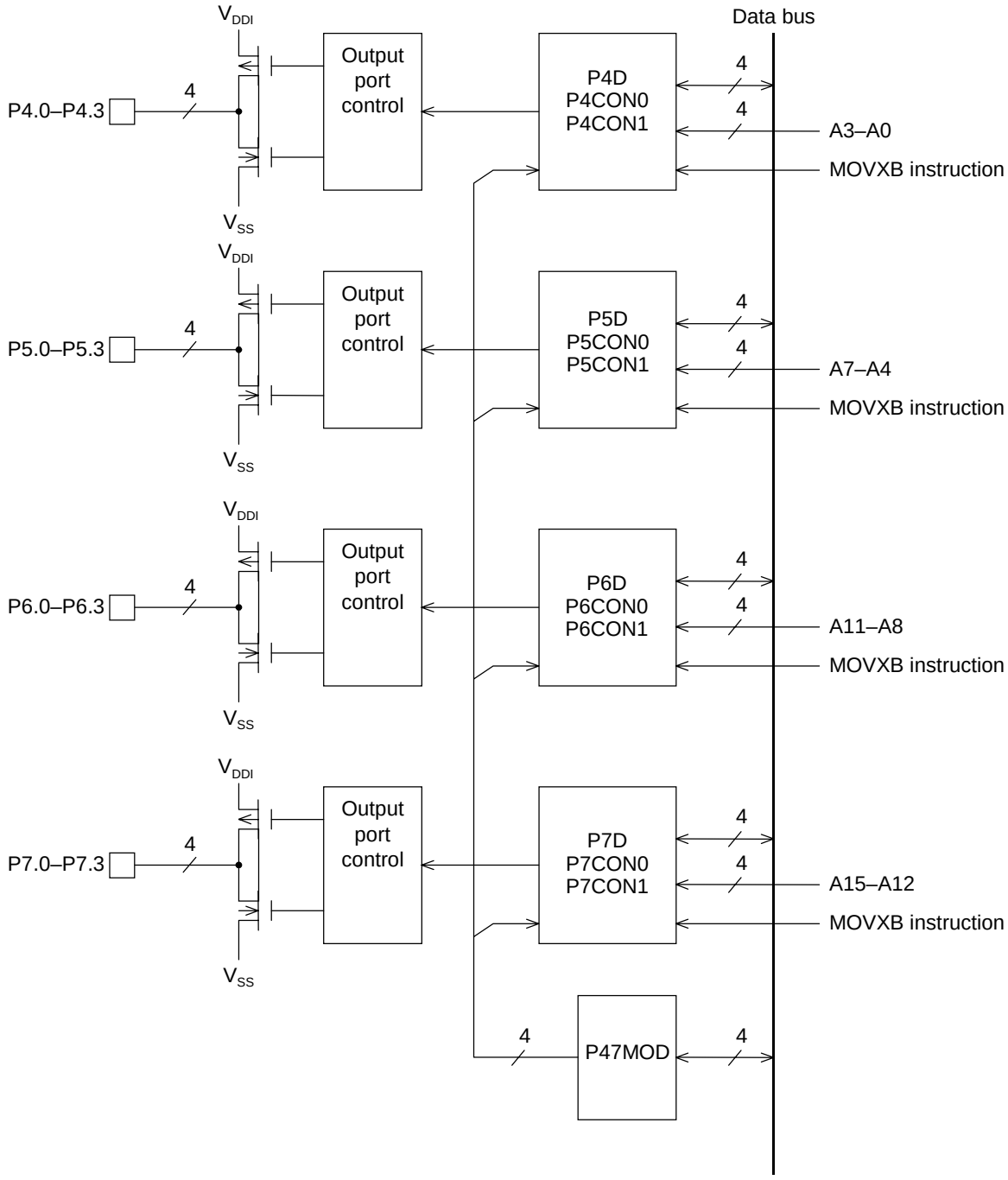


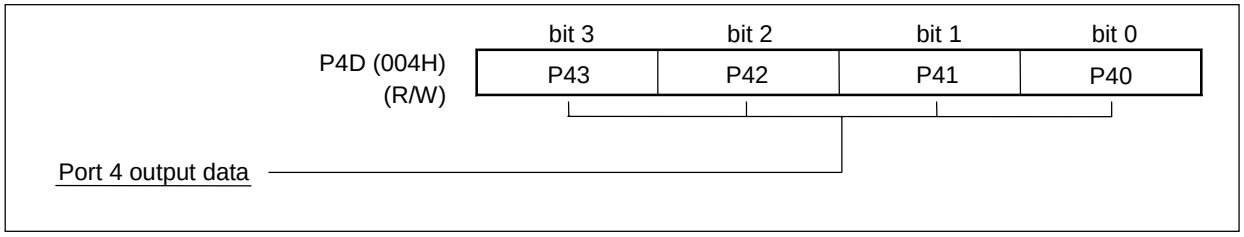
Figure 10-6 Output-Only Port (Port 4, Port 5, Port 6, Port 7) Configuration

10.5.2 Port 4, Port 5, Port 6, Port 7 Registers

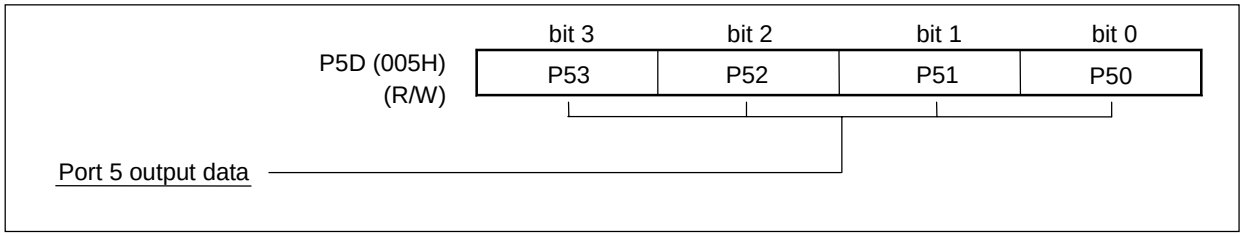
(1) Port 4, Port 5, Port 6, Port 7 data registers (P4D, P5D, P6D, P7D)

The port 4 data register (P4D), port 5 data register (P5D), port 6 data register (P6D) and port 7 data register (P7D) are 4-bit special function registers (SFRs) used to set the output values for ports 4 to 7.

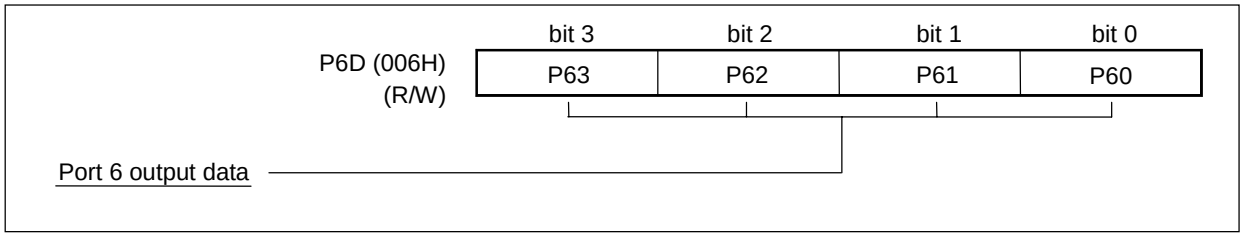
- Port 4



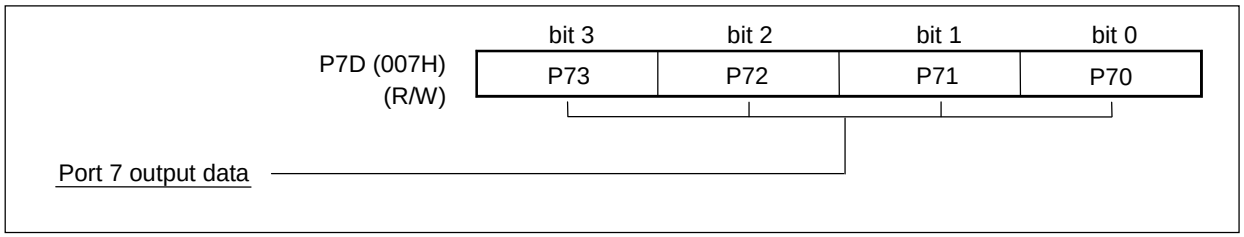
- Port 5



- Port 6



- Port 7



At system reset all bits in the port 4, port 5, port 6 and port 7 data registers (P4D, P5D, P6D, P7D) are set to "0". When data is written to a port data register, the actual pin change timing is at the positive edge of the system clock for state 2 (S2) of the write instruction.

Figure 10-7 shows port change timing.

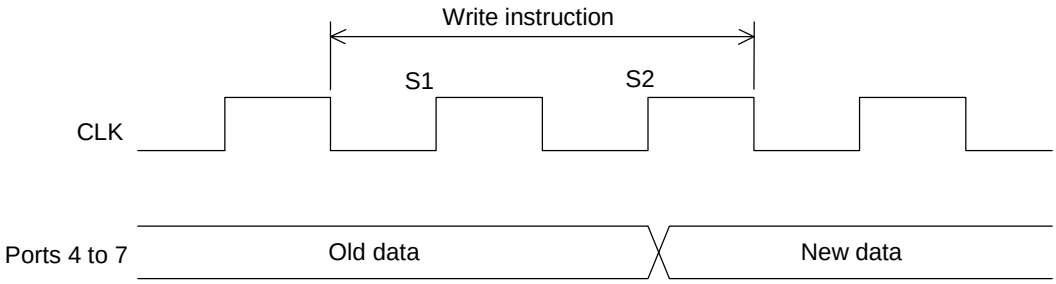


Figure 10-7 Port Change Timing

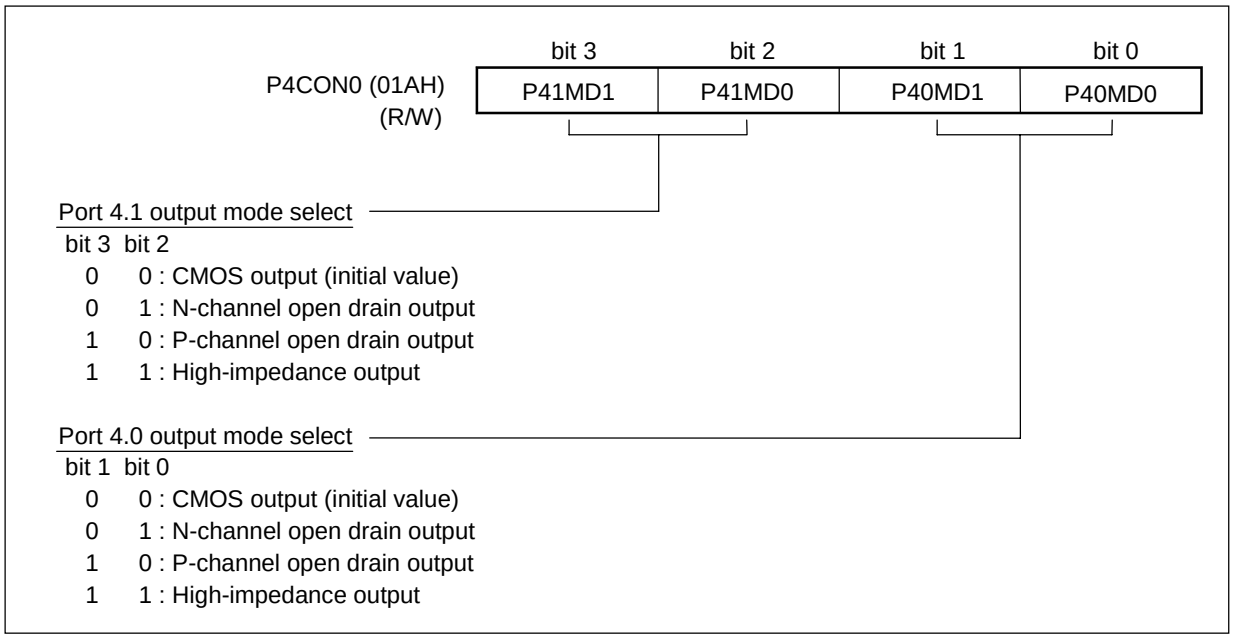
(2) Port 4, Port 5, Port 6, Port 7 control registers (P4CON0, P4CON1, P5CON0, P5CON1, P6CON0, P6CON1, P7CON0, P7CON1)

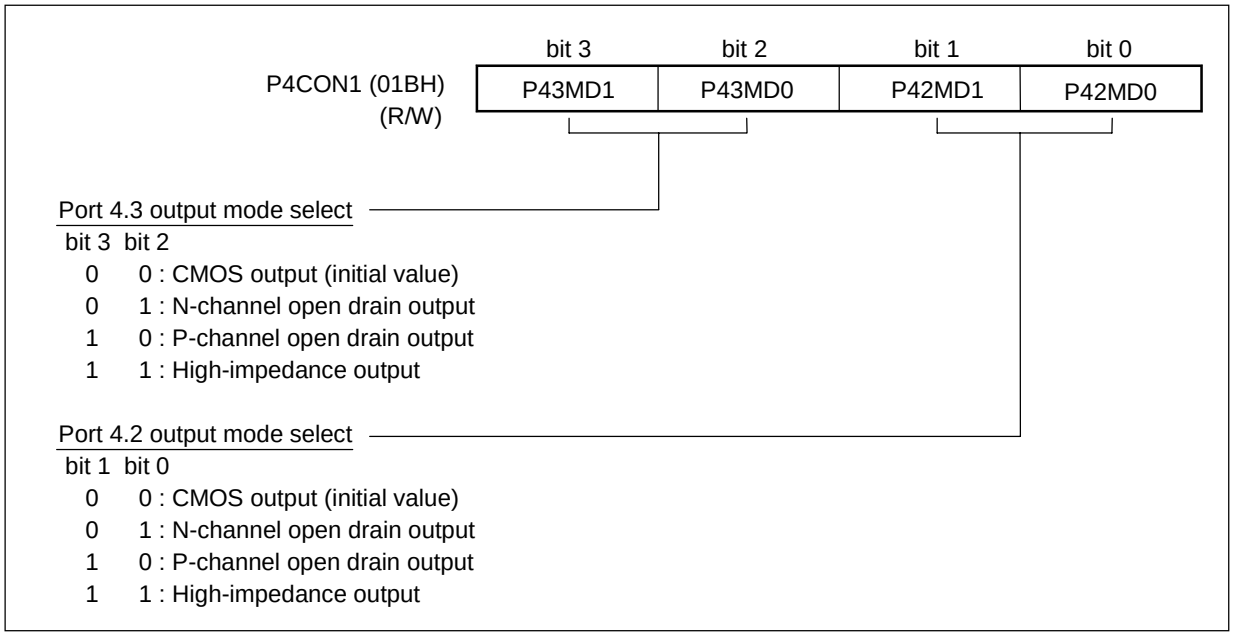
The port 4 control registers 0/1 (P4CON0, P4CON1), port 5 control registers 0/1 (P5CON0, P5CON1), port 6 control registers 0/1 (P6CON0, P6CON1) and port 7 control registers (P7CON0, P7CON1) are 4-bit special function registers (SFRs) used to select port output mode.

The output mode may be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

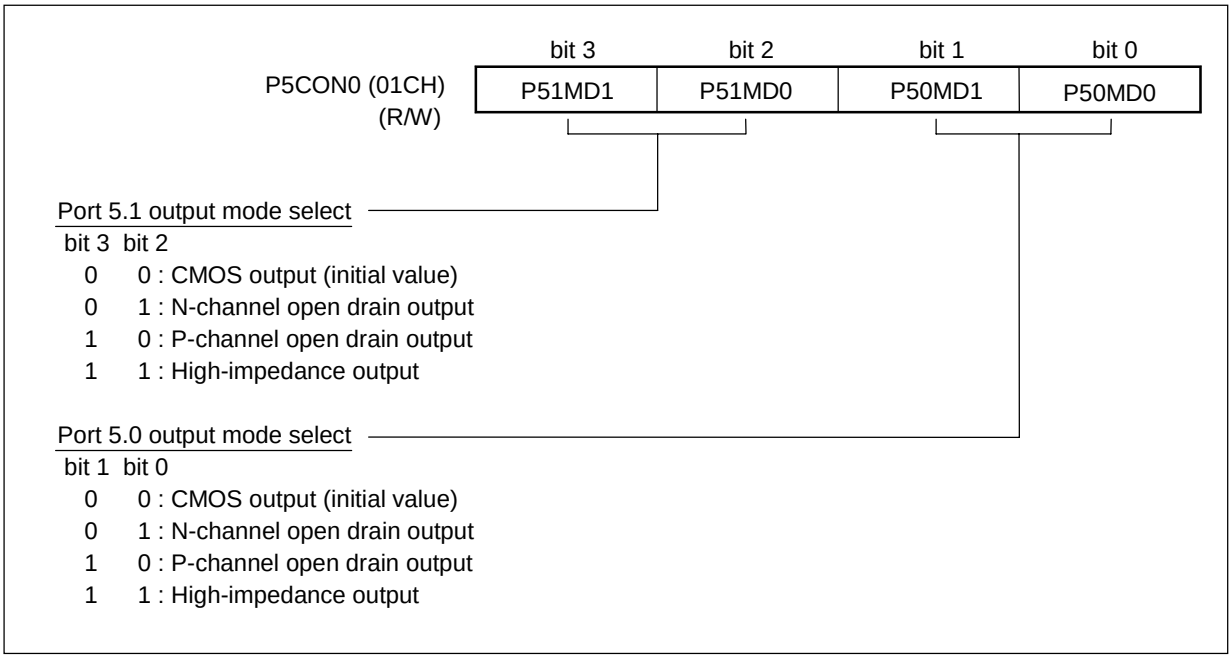
At system reset all bits in P4CON0, P4CON1, P5CON0, P5CON1, P6CON0, P6CON1, P7CON0 and P7CON1 are set to "0", and all ports are initialized to the CMOS output mode.

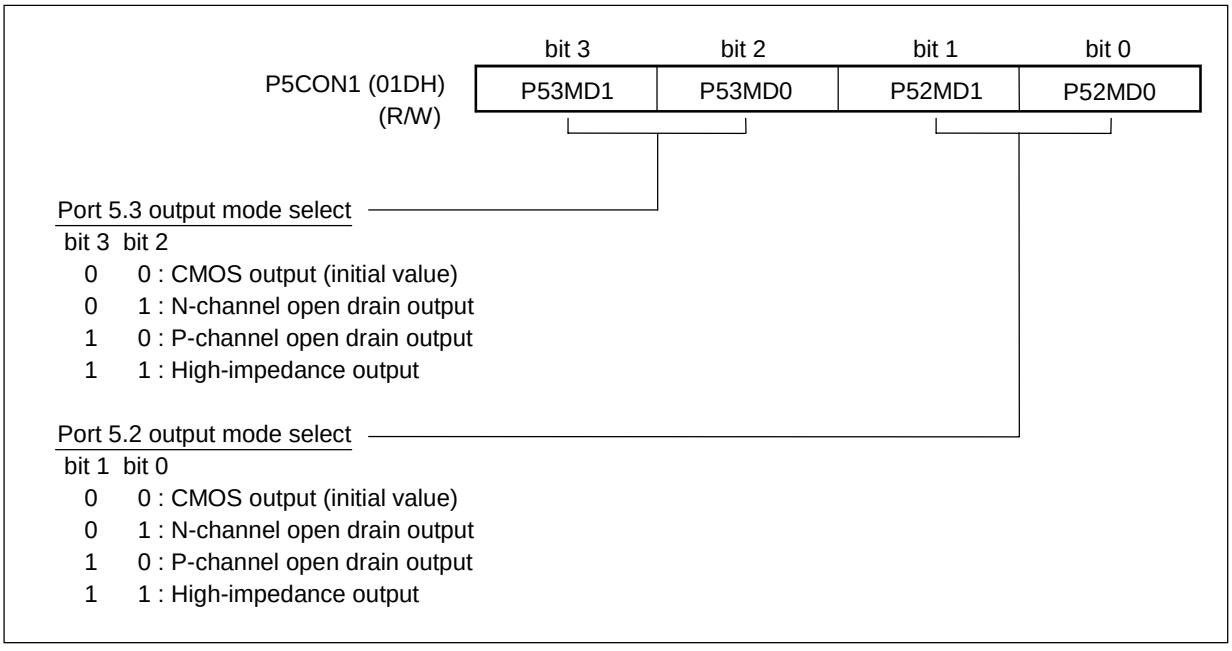
- Port 4



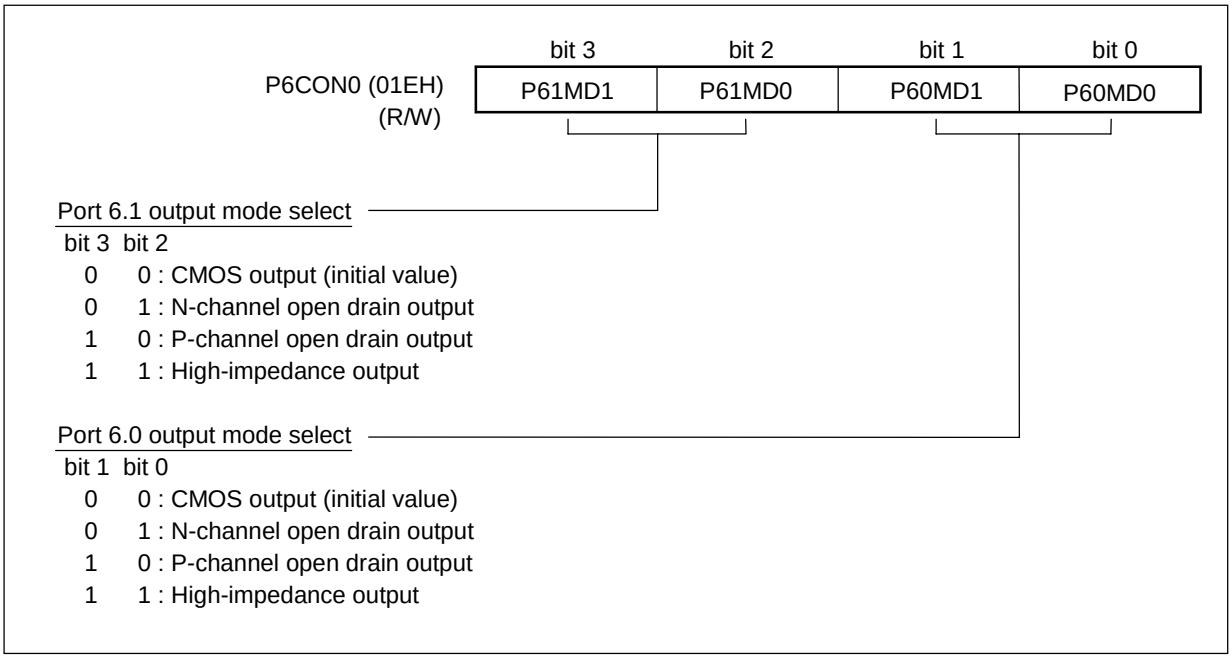


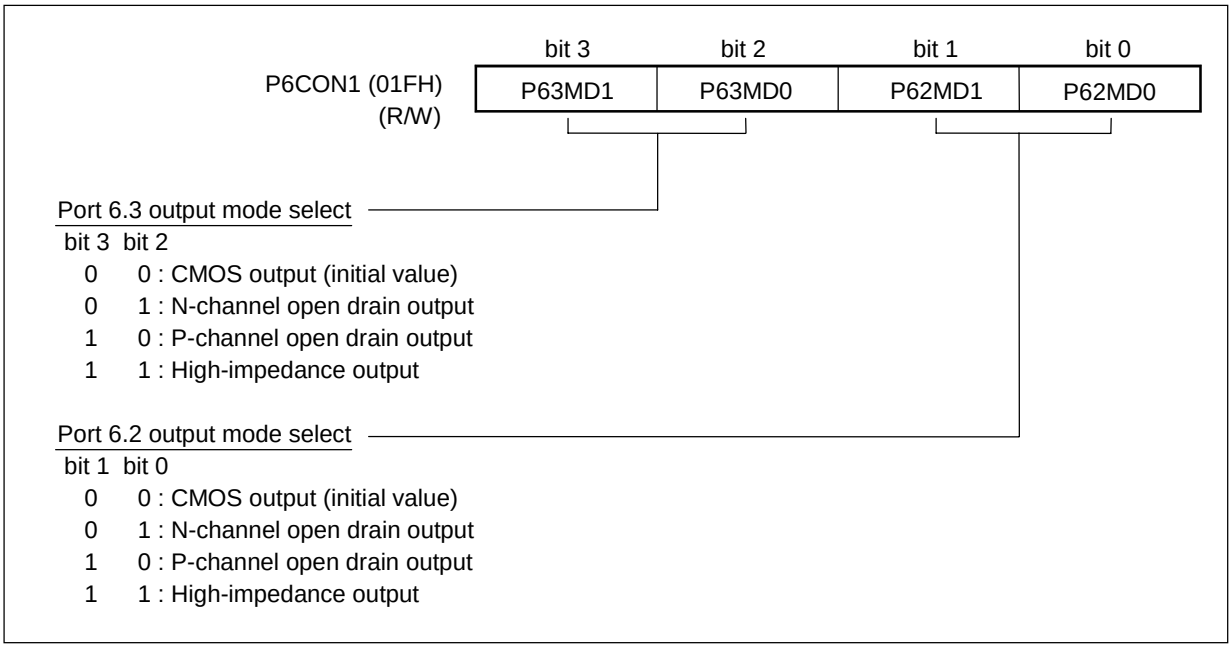
- Port 5


bit 3
bit 2
bit 1
bit 0
P5CON0 (01CH)
(R/W)
P51MD1
P51MD0
P50MD1
P50MD0
Port 5.1 output mode select
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port 5.0 output mode select
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output

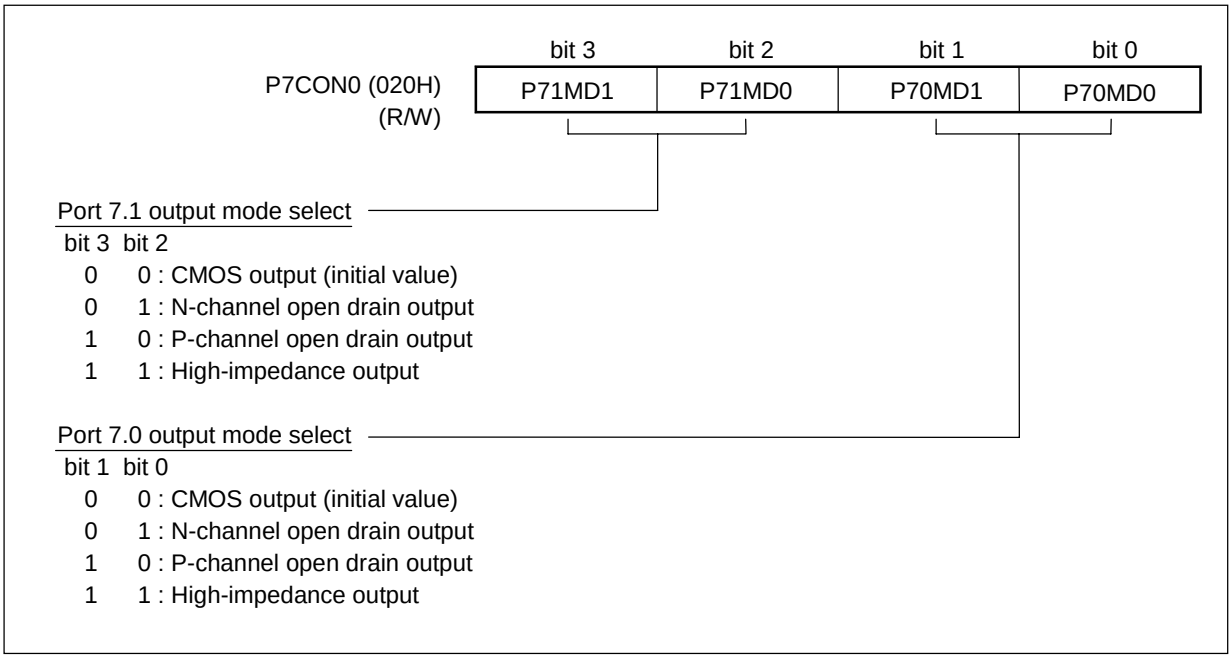

bit 3
bit 2
bit 1
bit 0
P5CON1 (01DH)
(R/W)
P53MD1
P53MD0
P52MD1
P52MD0
Port 5.3 output mode select
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port 5.2 output mode select
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output

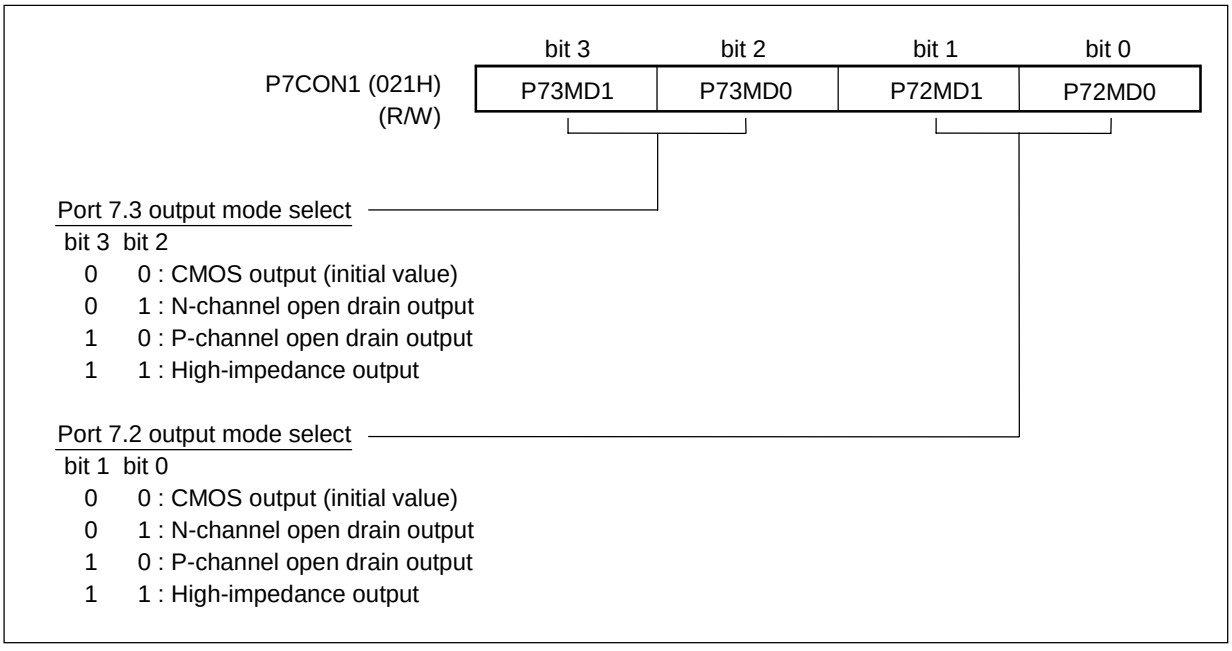
- Port 6


bit 3
bit 2
bit 1
bit 0
P6CON0 (01EH)
(R/W)
P61MD1
P61MD0
P60MD1
P60MD0
Port 6.1 output mode select
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port 6.0 output mode select
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output


bit 3
bit 2
bit 1
bit 0
P6CON1 (01FH)
(R/W)
P63MD1
P63MD0
P62MD1
P62MD0
Port 6.3 output mode select
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port 6.2 output mode select
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output

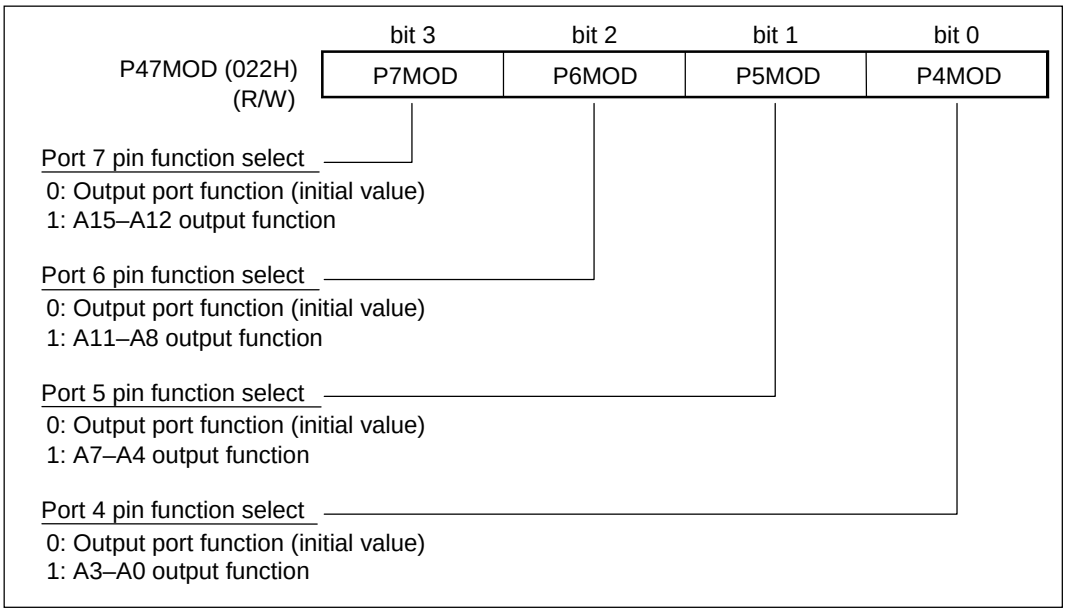
- Port 7


bit 3
bit 2
bit 1
bit 0
P7CON0 (020H)
(R/W)
P71MD1
P71MD0
P70MD1
P70MD0
Port 7.1 output mode select
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port 7.0 output mode select
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output


bit 3
bit 2
bit 1
bit 0
P7CON1 (021H)
(R/W)
P73MD1
P73MD0
P72MD1
P72MD0
Port 7.3 output mode select
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port 7.2 output mode select
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output

(3) Port 4, Port 5, Port 6, Port 7 mode register (P47MOD)

The port 47 mode register (P47MOD) is a 4-bit special function register (SFR) that enables the external memory address bus function, which is the secondary function of ports 4 to 7.



At system reset the P47MOD register is reset to "0", and all ports are set as normal output ports. When P47MOD bits are set to "1" and the MOVXB instruction executed, external memory addresses are output to the ports. If the MOVXB instruction is not executed, data register contents are output to the ports.

10.6 Port 8, Port 9, Port A (P8.0–P8.3, P9.0–P9.3, PA.0–PA.3)

The ML63295A has 4-bit input/output ports Port 8, Port 9 and Port A.

10.6.1 Port 8, Port 9, Port A Configuration

The circuit configurations for ports 8, 9 and A are shown in Figure 10-8.

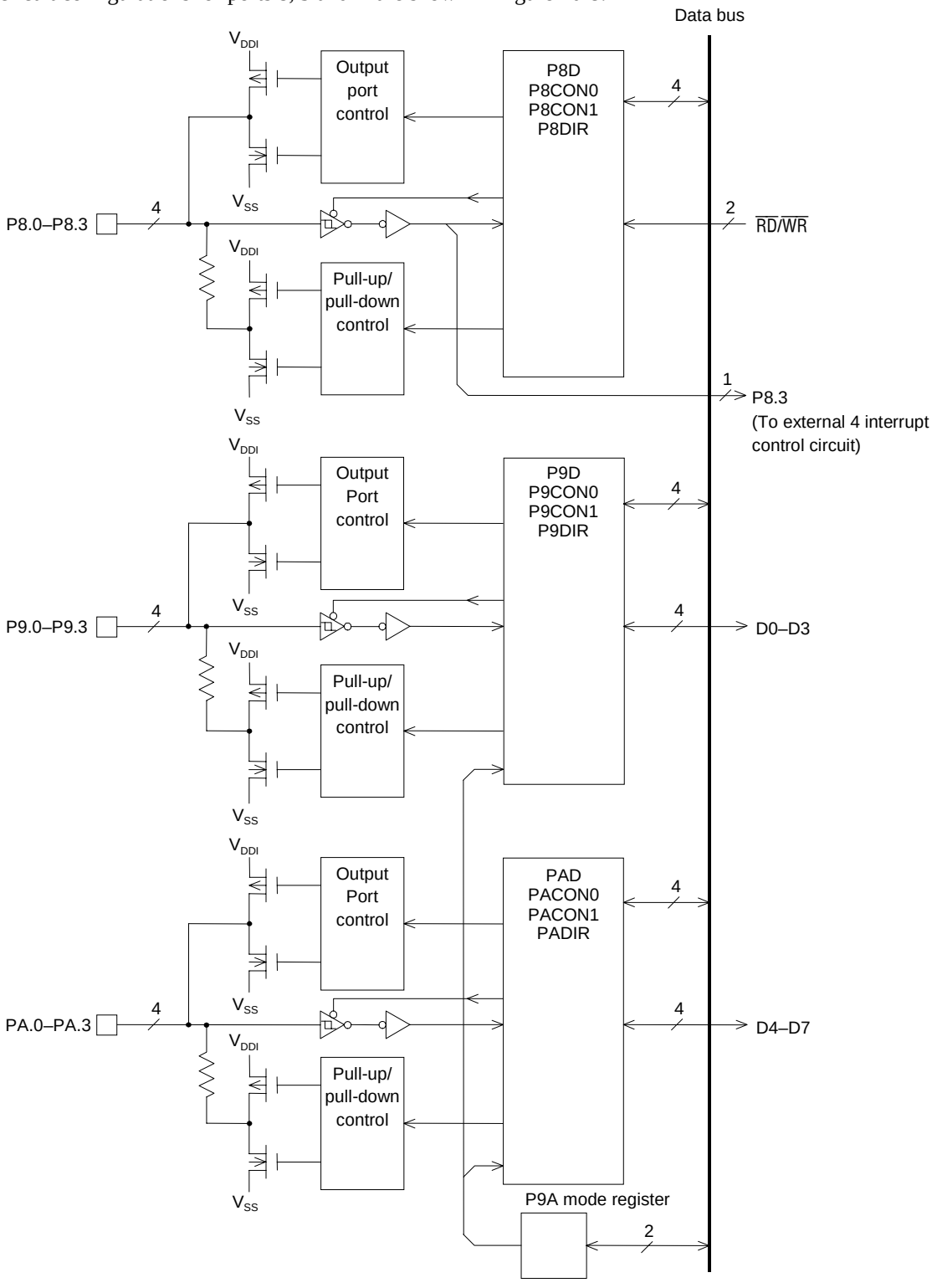


Figure 10-8 Input/Output Port (Ports 8, 9 and A) Configuration

10.6.2 Port 8, Port 9, Port A Registers

(1) Port 8, Port 9, Port A data registers (P8D, P9D, PAD)

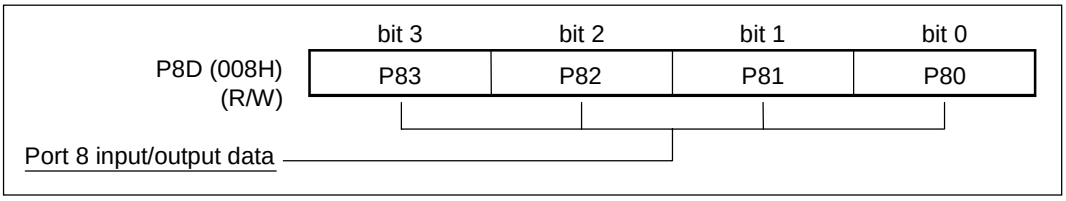
The port 8 data register (P8D), port 9 data register (P9D) and port A data register (PAD) are 4-bit special function registers (SFRs) used to set the output values for the ports.

When port direction register (P8DIR, P9DIR, PADIR) bits are set to "1" to select the output mode, the content of the corresponding port data register (P8D, P9D, PAD) is output to the port (port 8, port 9, port A).

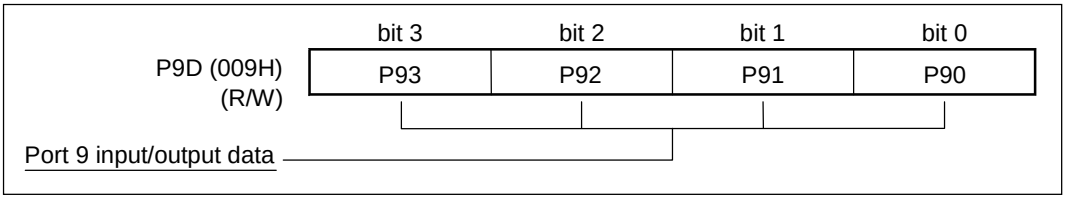
When the port data register (P8D, P9D, PAD) is read with the output mode selected, the content of the data register is read.

When the port data register (P8D, P9D, PAD) is read with port direction register bits set to "0" (input mode), the port pin levels are read.

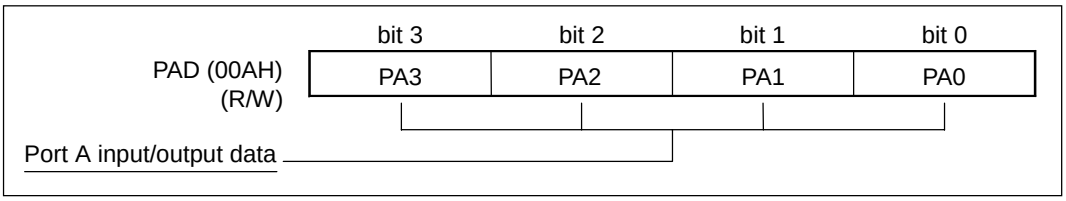
- Port 8



- Port 9



- Port A



At system reset all bits in the port 8, port 9 and A data registers are set to "0". When data is written to a port data register, the actual pin change timing is at the rising edge of the system clock for state 2 of the write instruction.
Figure 10-9 shows port change timing.

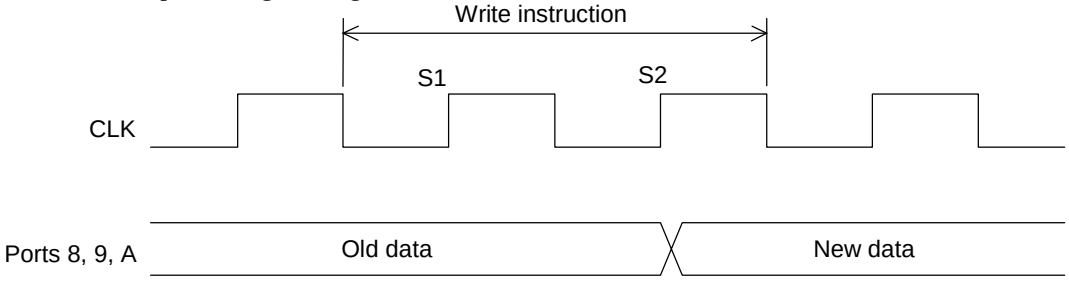


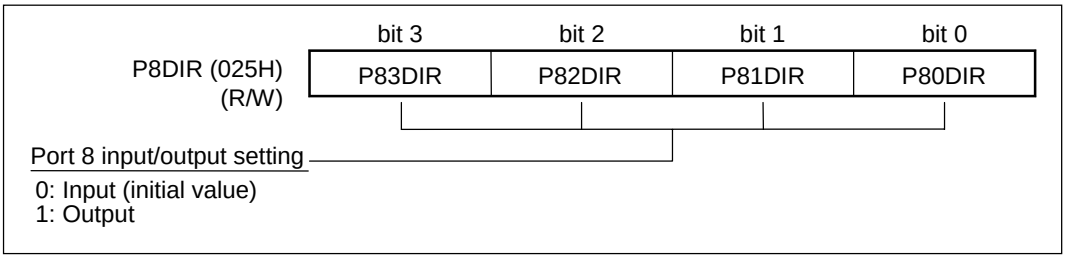
Figure 10-9 Port Change Timing

(2) Port 8, Port 9, Port A direction registers (P8DIR, P9DIR, PADIR)

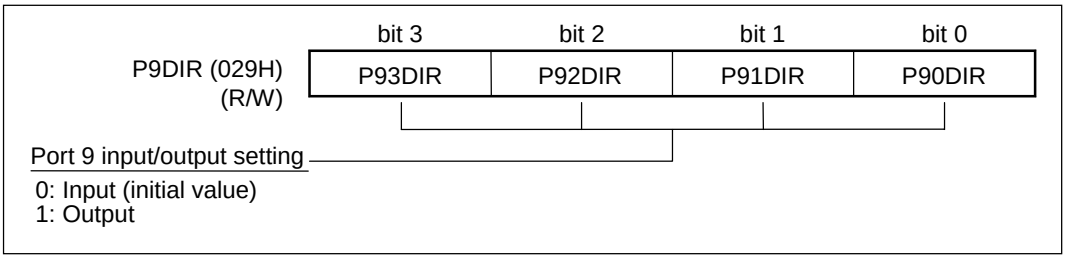
The port 8 direction register (P8DIR), port 9 direction register (P9DIR) and port A direction register (PADIR) are 4-bit special function registers (SFRs) which specify the port input/output direction for each bit. Pins corresponding to P8DIR, P9DIR and PADIR bits set to "0" are input, and those corresponding to bits set to "1" are output.

At system reset all bits in P8DIR, P9DIR and PADIR are set to "0", and ports 8, 9 and A are initialized to input mode.

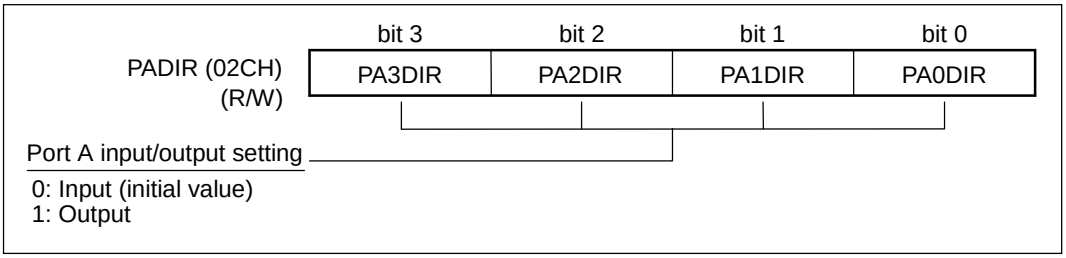
- Port 8



- Port 9



- Port A



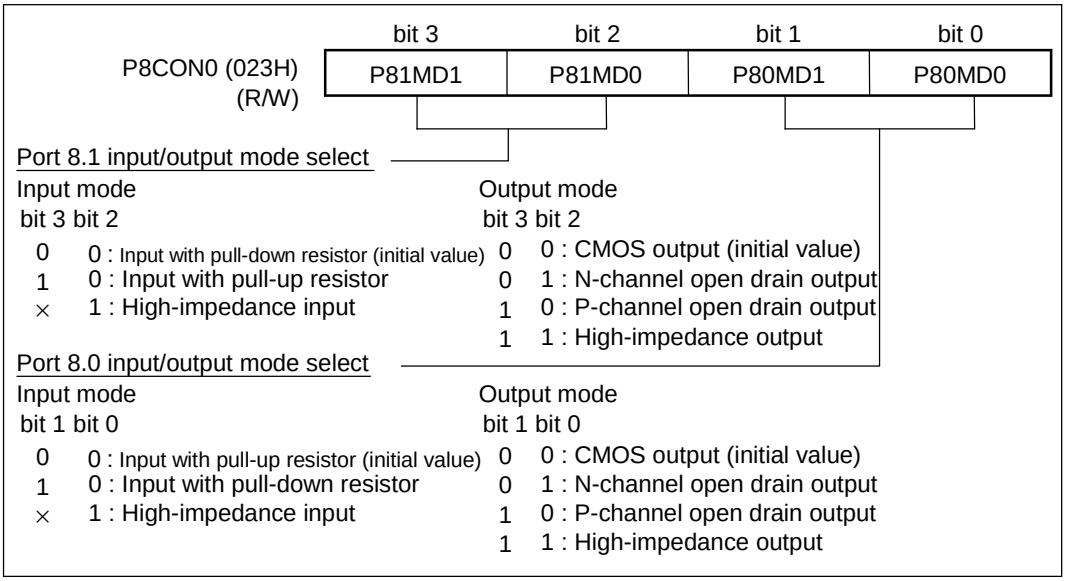
(3) Port 8, Port 9, Port A control registers (P8CON0, P8CON1, P9CON0, P9CON1, PACON0, PACON1)

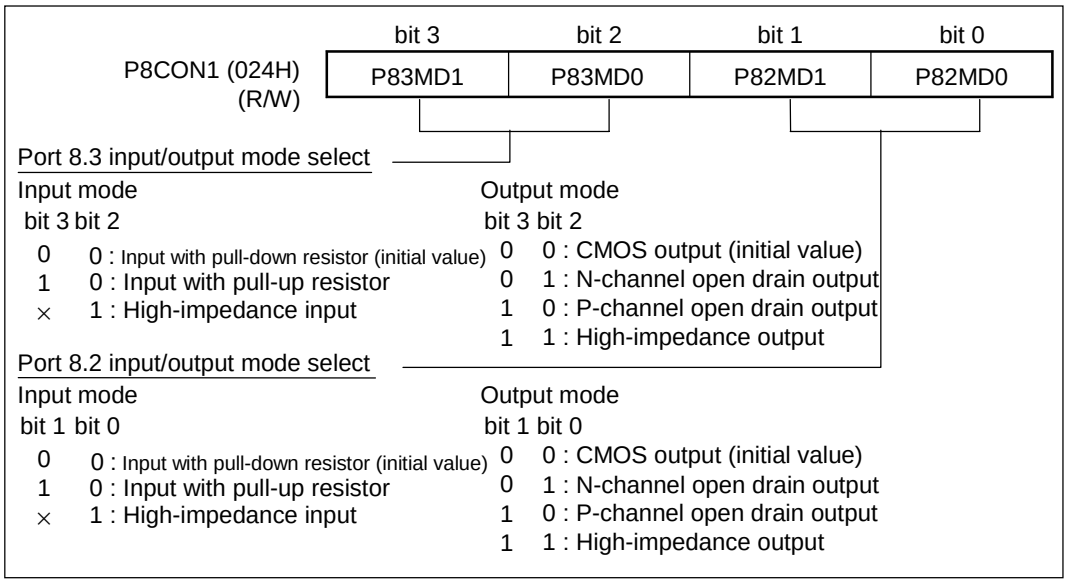
The port 8 control registers 0/1 (P8CON0, P8CON1), port 9 control registers 0/1 (P9CON0, P9CON1) and port A control registers 0/1 (PACON0, PACON1) are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode may be pull-down resistor input, pull-up resistor input or high-impedance input.

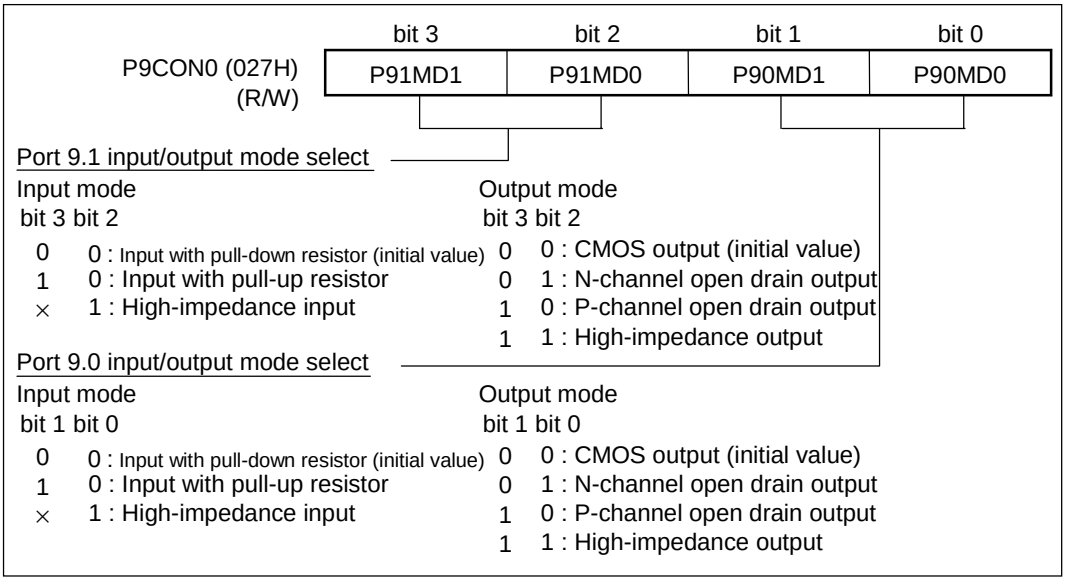
The output mode may be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

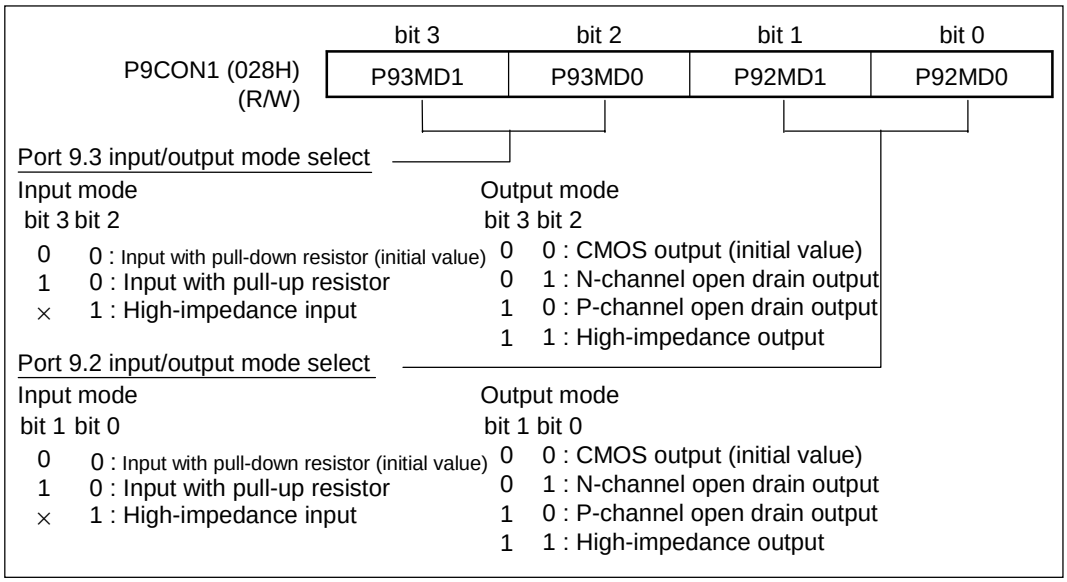
- Port 8



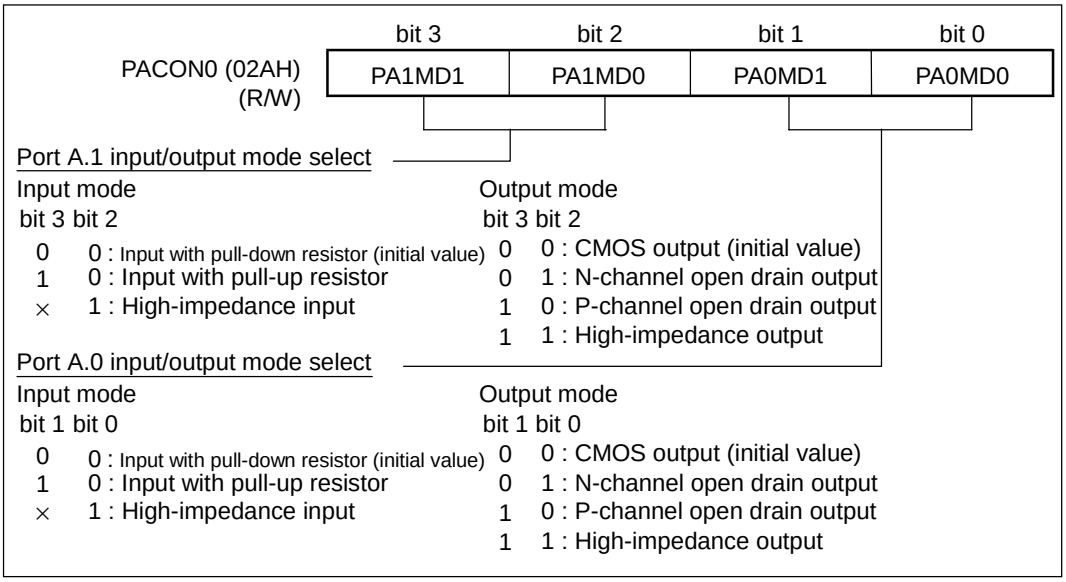


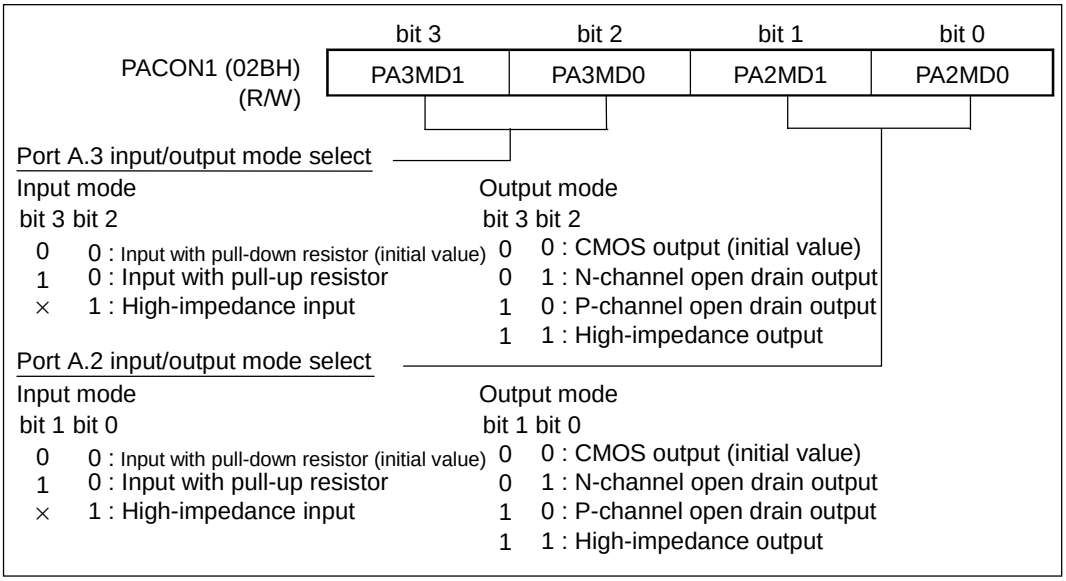
- Port 9


bit 3
bit 2
bit 1
bit 0
P9CON0 (027H)
(R/W)
P91MD1
P91MD0
P90MD1
P90MD0
Port 9.1 input/output mode select
Input mode
bit 3 bit 2
0 0 : Input with pull-down resistor (initial value)
1 0 : Input with pull-up resistor
× 1 : High-impedance input
Output mode
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port 9.0 input/output mode select
Input mode
bit 1 bit 0
0 0 : Input with pull-down resistor (initial value)
1 0 : Input with pull-up resistor
× 1 : High-impedance input
Output mode
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output


bit 3
bit 2
bit 1
bit 0
P9CON1 (028H)
(R/W)
P93MD1
P93MD0
P92MD1
P92MD0
Port 9.3 input/output mode select
Input mode
bit 3 bit 2
0 0 : Input with pull-down resistor (initial value)
1 0 : Input with pull-up resistor
× 1 : High-impedance input
Output mode
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port 9.2 input/output mode select
Input mode
bit 1 bit 0
0 0 : Input with pull-down resistor (initial value)
1 0 : Input with pull-up resistor
× 1 : High-impedance input
Output mode
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output

- Port A


bit 3 bit 2 bit 1 bit 0
PACON0 (02AH)
(R/W)
PA1MD1 PA1MD0 PA0MD1 PA0MD0
Port A.1 input/output mode select
Input mode
bit 3 bit 2
0 0 : Input with pull-down resistor (initial value)
1 0 : Input with pull-up resistor
× 1 : High-impedance input
Output mode
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port A.0 input/output mode select
Input mode
bit 1 bit 0
0 0 : Input with pull-down resistor (initial value)
1 0 : Input with pull-up resistor
× 1 : High-impedance input
Output mode
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output


bit 3 bit 2 bit 1 bit 0
PACON1 (02BH)
(R/W)
PA3MD1 PA3MD0 PA2MD1 PA2MD0
Port A.3 input/output mode select
Input mode
bit 3 bit 2
0 0 : Input with pull-down resistor (initial value)
1 0 : Input with pull-up resistor
× 1 : High-impedance input
Output mode
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port A.2 input/output mode select
Input mode
bit 1 bit 0
0 0 : Input with pull-down resistor (initial value)
1 0 : Input with pull-up resistor
× 1 : High-impedance input
Output mode
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output

(4) Port 8, Port 9, Port A mode registers (P8MOD, P9AMOD)

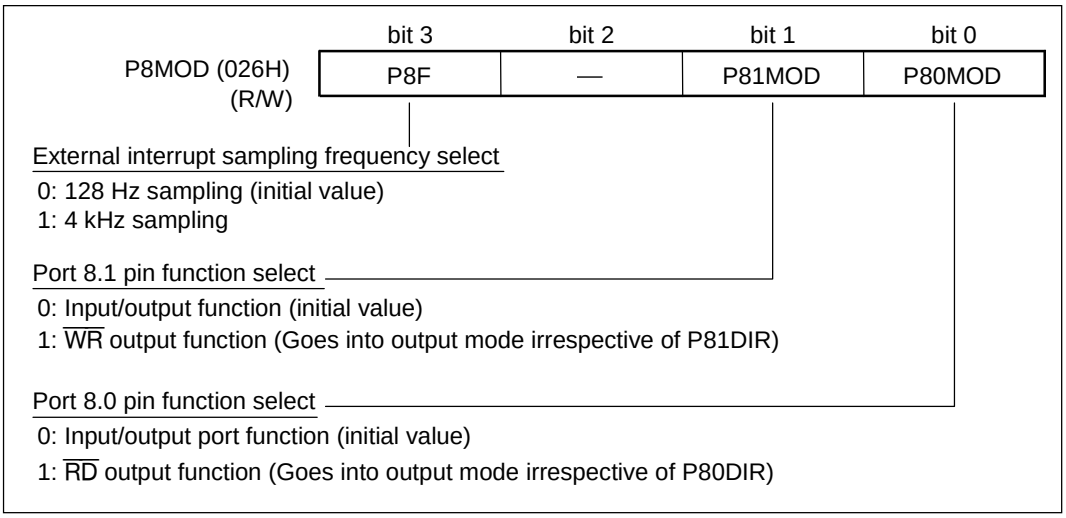
The port 8 mode register (P8MOD) and port 9A mode register (P9AMOD) are 4-bit special function registers (SFRs) used to select the sampling frequency when P8.3 is used for external interrupt and the secondary function of each port.

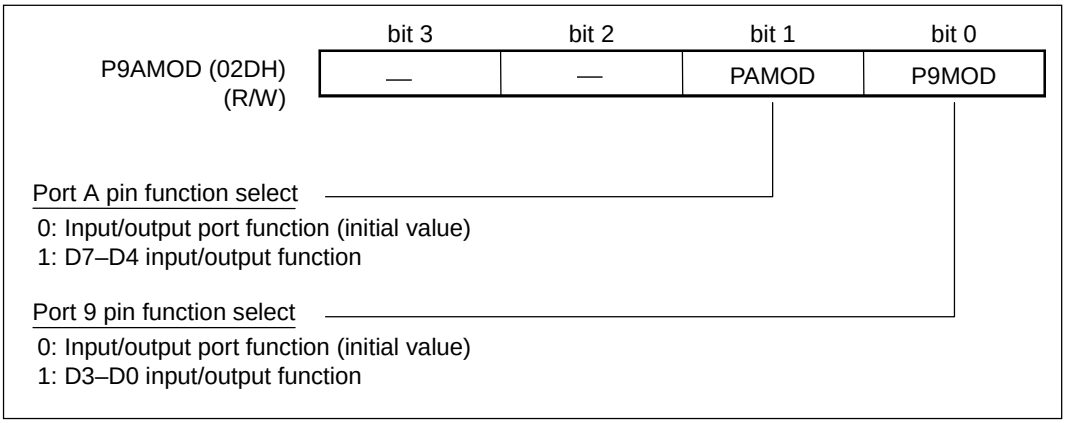
At system reset the port mode registers (P8MOD, P9AMOD) are set to "0", and ports 8, 9 and A are used as normal ports.

The port secondary functions are indicated in Table 10-2.

Table 10-2 Secondary Port Functions

Port	Secondary function	Description
P8.0	$\overline{RD}$	External memory read signal
P8.1	$\overline{WR}$	External memory write signal
P8.2	—	
P8.3	INT4	External interrupt 4
P9.0	D0	External memory data bus
P9.1	D1	
P9.2	D2	
P9.3	D3	
PA.0	D4	
PA.1	D5	
PA.2	D6	
PA.3	D7	





If each bit of P9AMOD is set to "1" and the MOVXB instruction is executed, P9 through PA perform data signaling for external memory.

Input or output is based on the contents of the MOVXB instruction. If the MOVXB instruction is not executed, P9 through PA perform the normal input/output port function.

10.6.3 Port 8.3 External Interrupt Function (External Interrupt 4)

Port 8.3 has external interrupt 4 allocated as secondary function.

External interrupt generation for P8.3 is triggered by the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal (XI4INT) is output, and the interrupt request flag (QXI4) is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

The interrupt start address for external interrupt 4 is 001CH.

Figure 10-10 shows the equivalent circuit for external interrupt 4 control.

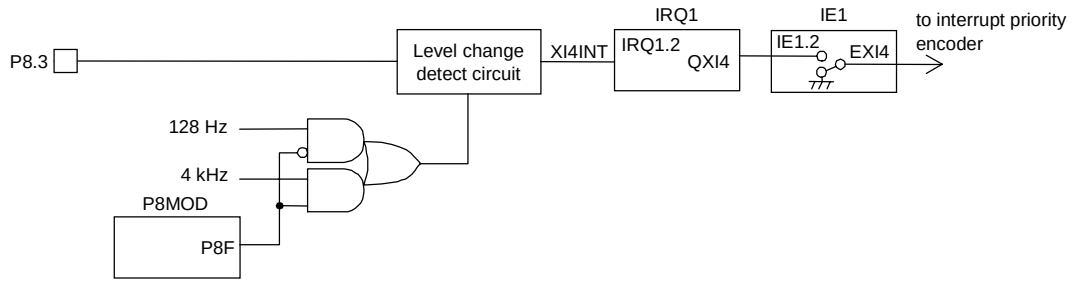


Figure 10-10 External Interrupt 4 Control Equivalent Circuit

Figure 10-11 shows the external interrupt 4 generation timing.

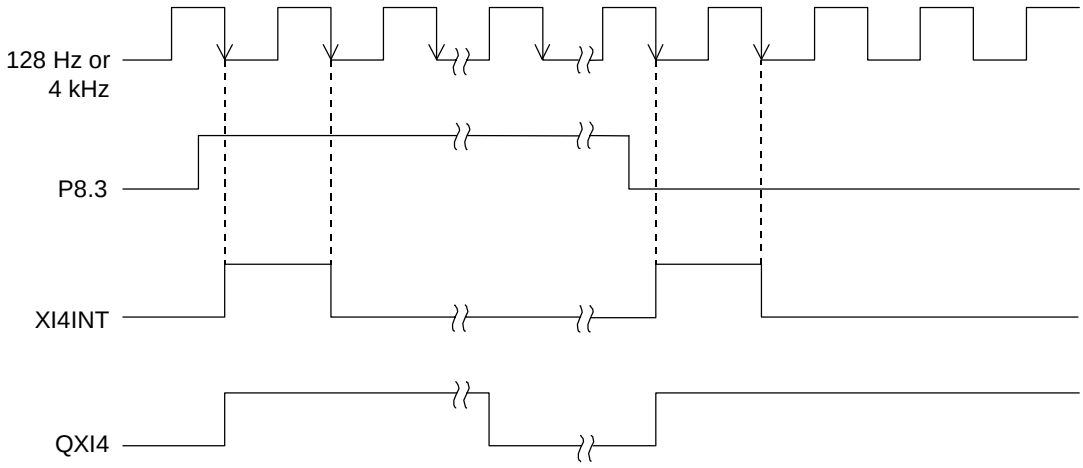


Figure 10-11 External Interrupt 4 Generation Timing

10.7 Port B (PB.0–PB.3)

The ML63295A has Port B, a 4-bit input/output port.

10.7.1 Port B Configuration

The circuit configuration for port B is shown in Figure 10-12.

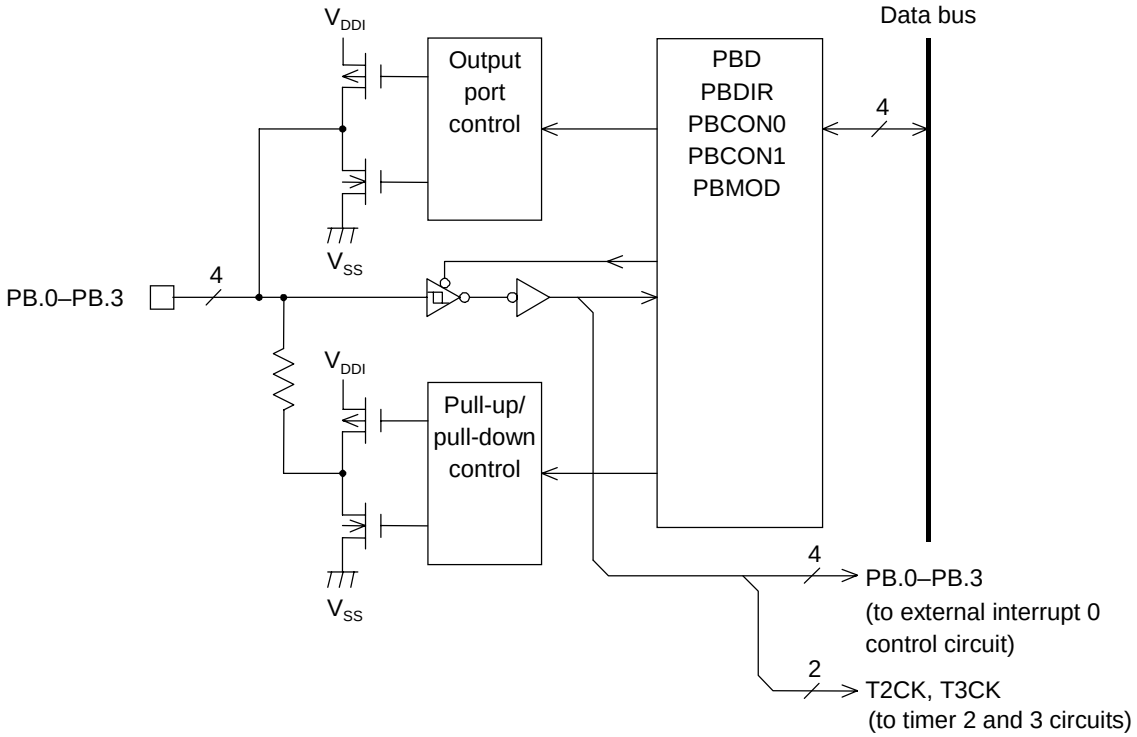


Figure 10-12 Input/Output Port (Port B) Configuration

10.7.2 Port B Registers

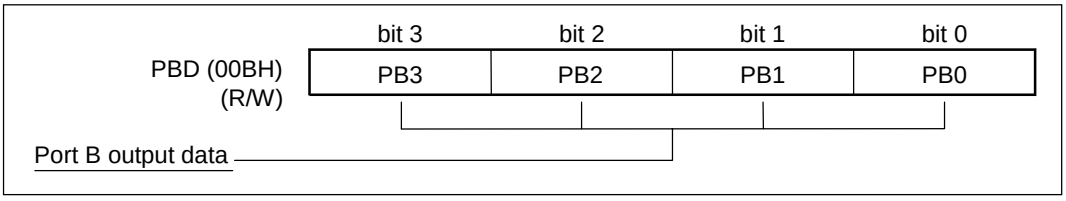
(1) Port B data register (PBD)

PBD is a 4-bit special function register used to set the output values for port B.

When port B direction register (PBDIR) bits are set to "1" to select the output mode, the content of the port B data register is output to port B.

When the port B data register is read with the output mode selected, the content of the port B data register is read.

When the port B data register is read with PBDIR bits set to "0" (input mode), the pin levels of port B are read.



At system reset all bits in the port B data register (PBD) are set to "0". When data is written to the port B data register, the actual pin change timing is at the rising edge of the system clock for state 2 of the write instruction.

Figure 10-13 indicates port change timing.

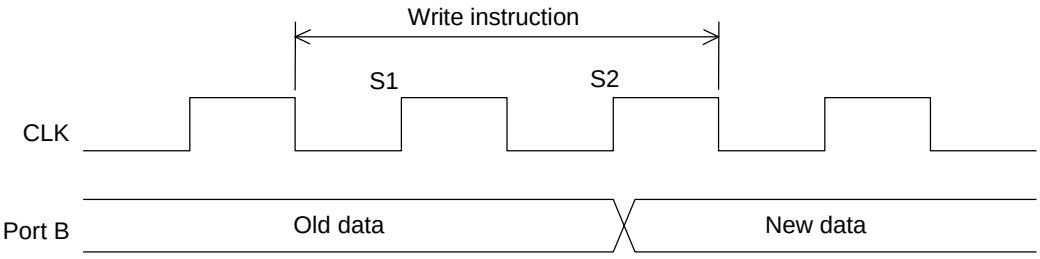
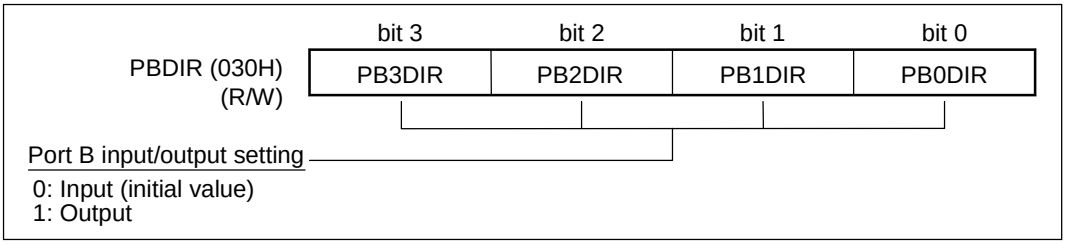


Figure 10-13 Port B Change Timing

(2) Port B direction register (PBDIR)

PBDIR is a 4-bit special function register (SFR) which specifies the port input/output direction for each bit. Pins corresponding to the PBDIR bits set to "0" are input, and those corresponding to the PBDIR bits set to "1" are output.

At system reset all bits in the port B direction register are set to "0", and port B is initialized to input mode.



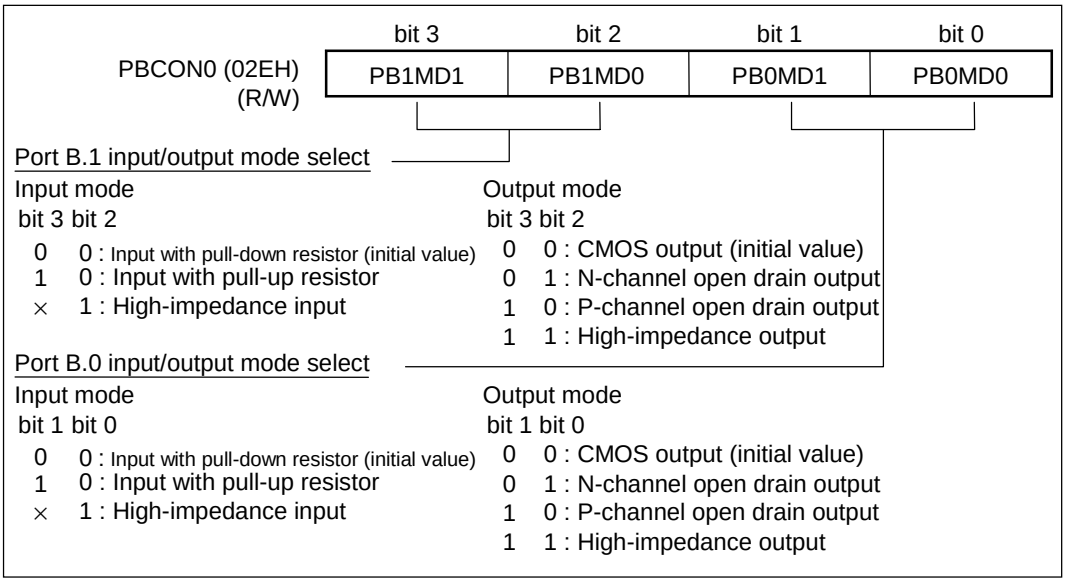
(3) Port B control registers 0/1 (PBCON0, PBCON1)

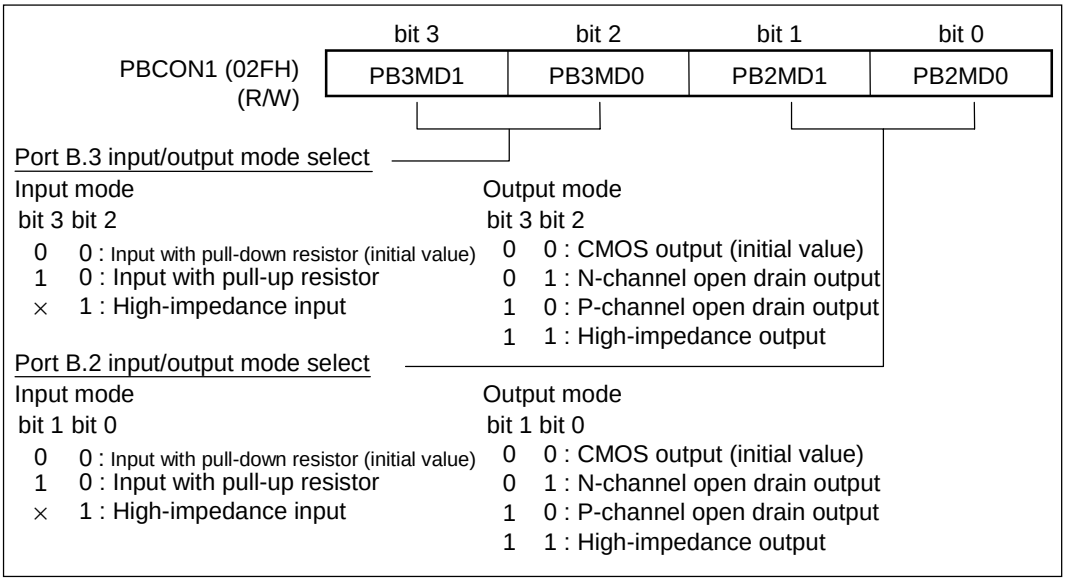
PBCON0 and PBCON1 are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode can be pull-down resistor input, pull-up resistor input or high-impedance input.

The output mode can be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

At system reset all bits in PBCON0 and PBCON1 are set to "0", and port B is initialized to pull-down resistor input mode and CMOS output mode.





(4) Port B mode register (PBMOD)

PBMOD is a 4-bit special function register (SFR) used to select the sampling frequency when port B is used as an external interrupt. It is also used to select port B secondary functions other than external interrupt.

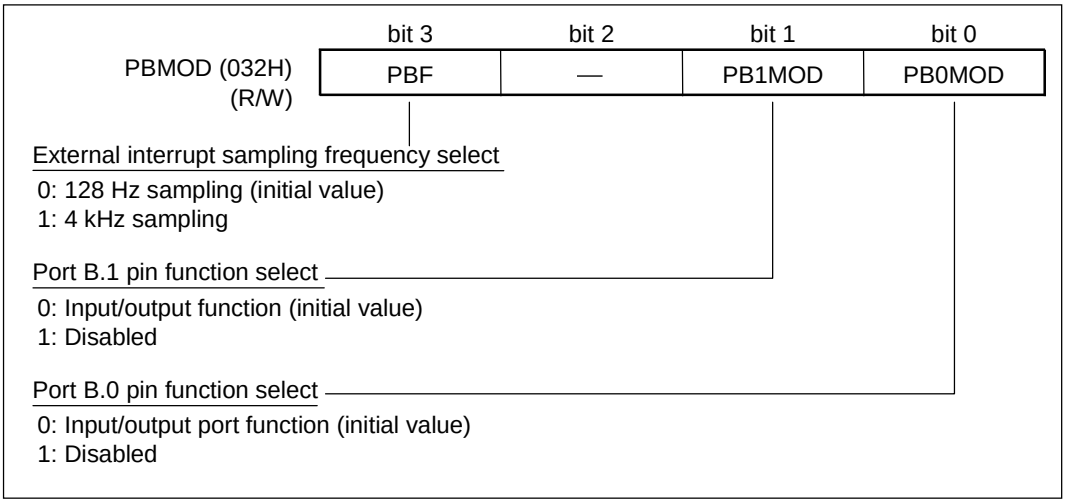
The external interrupt sampling frequency can be selected as either 128 Hz or 4 kHz.

At system reset all the valid bits in PBMOD are initialized to "0".

Port B secondary functions are indicated in Table 10-3.

Table 10-3 Port B Secondary Functions

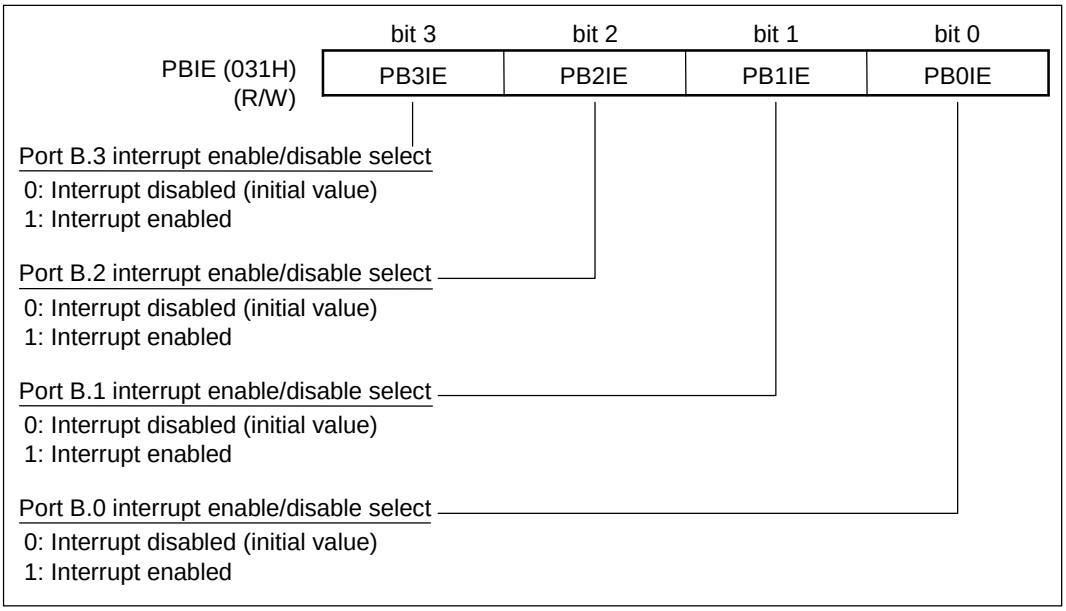
Port	Secondary function	Description
PB.2	T2CK	Timer 2 external clock input
PB.3	T3CK	Timer 3 external clock input
PB.0	INT0	External interrupt 0
PB.1		
PB.2		
PB.3		



(5) Port B interrupt enable register (PBIE)

PBIE is a 4-bit special function register (SFR) that enables/disables individual bits when port B is used as an external interrupt input.

At system reset, all bits in PBIE are set to "0" and port B is initialized to the interrupt disabled state.



10.7.3 Port B External Interrupt Function (External Interrupt 0)

Port B has external interrupt 0 allocated as secondary function. Individual bits can be enabled/disabled for external interrupt 0.

External interrupt generation for port B is triggered by the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal (XI0INT) is output, and the interrupt request flag (QXI0) is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

Because the port B external interrupt is set by a level change at any of the port B inputs, each bit of the port must be read to determine which bit of port B generated the interrupt.

The interrupt start address for external interrupt 0 is 0014H.

Figure 10-14 shows the equivalent circuit for external interrupt 0 control.

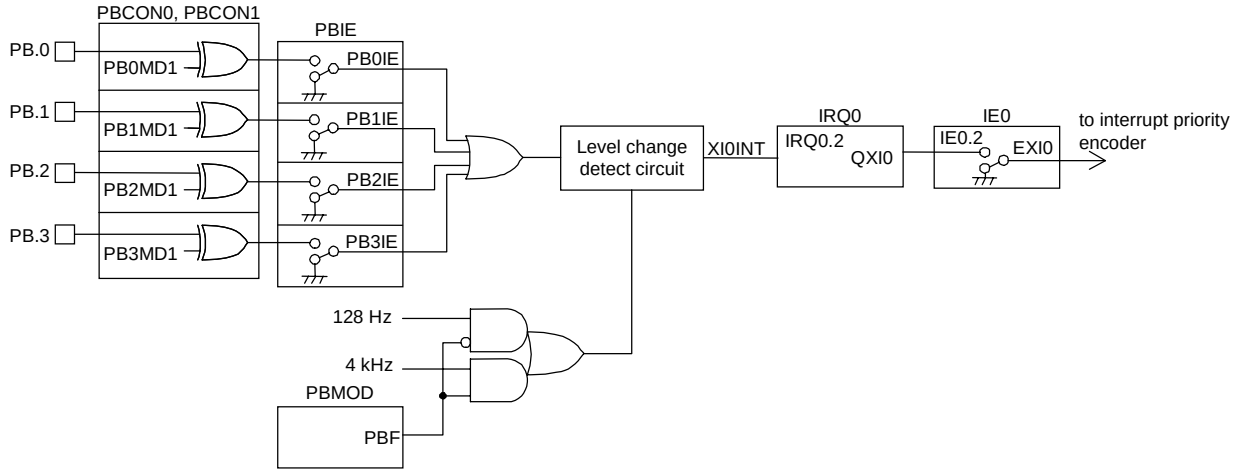


Figure 10-14 External Interrupt 0 Control Equivalent Circuit

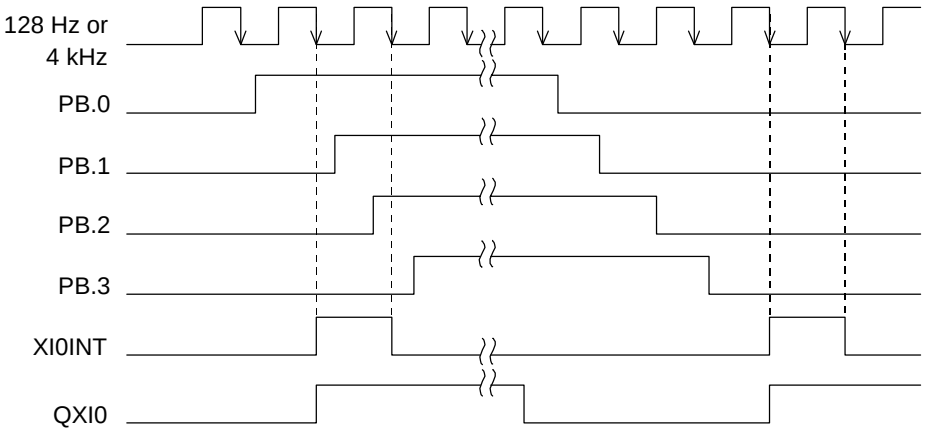
Figure 10-15 shows the external interrupt 0 generation timing.

(a) PB0MD1 to PB3MD1 = "0" (initial value: inputs with pull-down resistors or high impedance input) setting

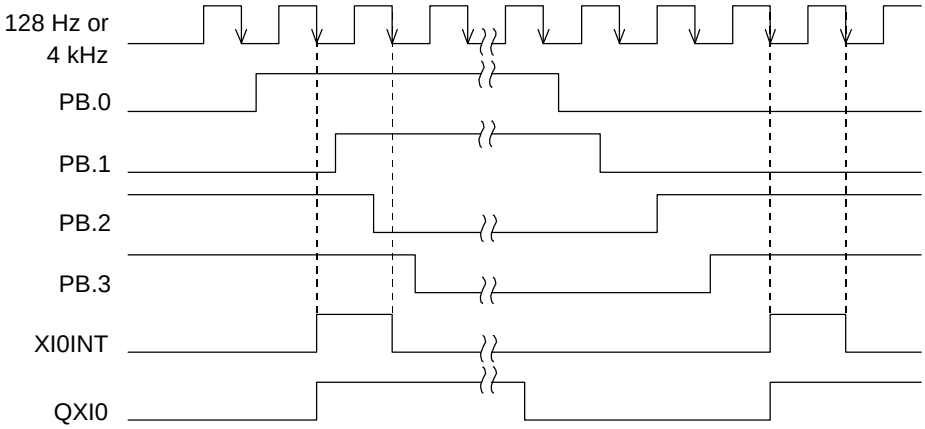
- When all PB.0 to PB.3 inputs are at a "L" level
  External interrupt 0 is generated when any port B input changes to a "H" level.
- When any of PB.0 to PB.3 inputs is at a "H" level
  External interrupt 0 is generated when all the port B inputs change to a "L" level.

(b) PB0MD1 and PB1MD1 = "0" and PB2MD1 and PB3MD1 = "1" (PB.0 and PB.1 selected as inputs with pull-down resistors or high impedance input; PB.2 and PB.3 selected as inputs with pull-up resistors or high impedance input) setting

- When both PB.0 and PB.1 inputs are at a "L" level AND both PB.2 and PB.3 inputs are at a "H" level
  External interrupt 0 is generated when either PB.0 or PB.1 input changes to a "H" level (alternatively, when either PB.2 or PB.3 input changes to a "L" level).
- When either PB.0 or PB.1 input is at a "H" level OR either PB.2 or PB.3 input is at a "L" level
  External interrupt 0 is generated when both PB.0 and PB.1 inputs change to a "L" level AND both PB.2 and PB.3 inputs change to a "H" level.



(a) When PB0MD1 to PB3MD1 = "0"



(b) When PB0MD1 and PB1MD1 = "0" and PB2MD1 and PB3MD = "1"

Figure 10-15 Interrupt Generation Timing of External Interrupt 0

10.8 Port C (PC.0–PC.3)

The ML63295A has Port C, a 4-bit input/output port.

10.8.1 Port C Configuration

The circuit configuration for port C is shown in Figure 10-16.

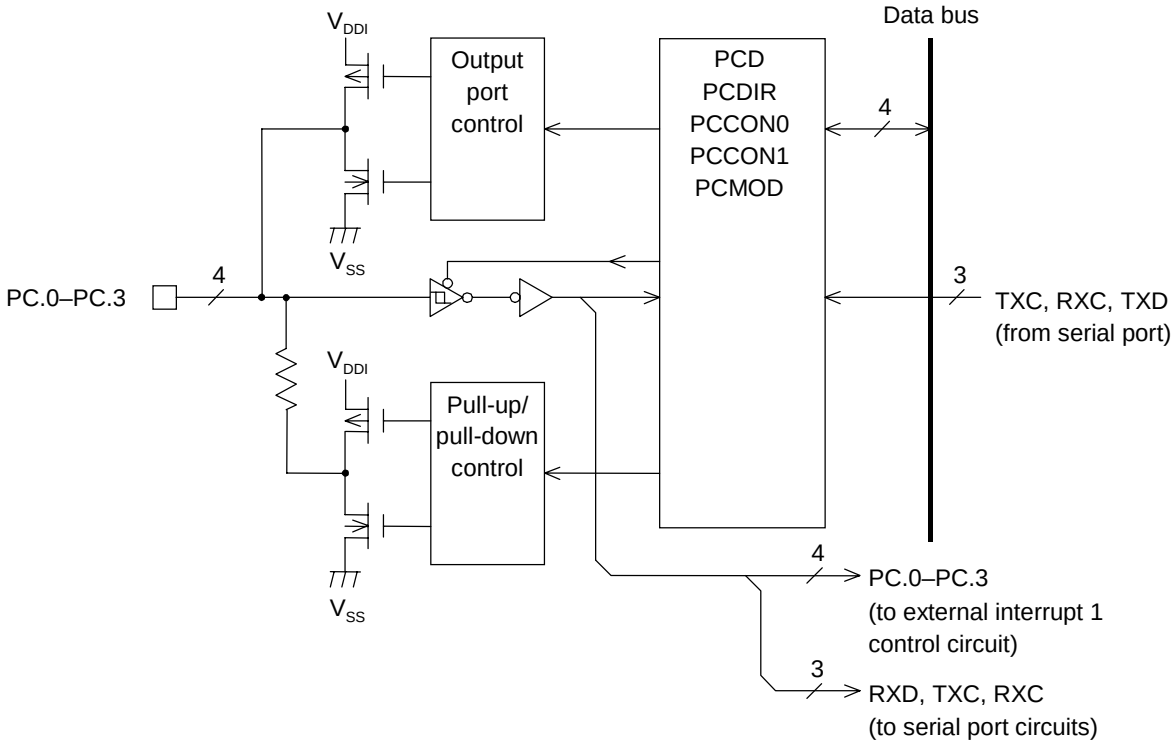


Figure 10-16 Input/Output Port (Port C) Configuration

10.8.2 Port C Registers

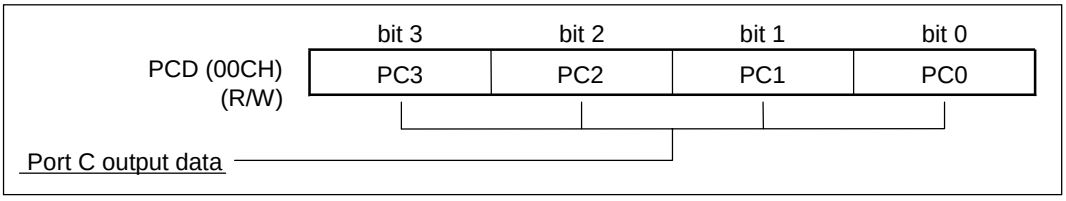
(1) Port C data register (PCD)

PCD is a 4-bit special function register used to set the output values for port C.

When port C direction register (PCDIR) bits are set to "1" to select the output mode, the content of the port C data register is output to port C.

When the port C data register is read with the output mode selected, the content of the port C data register is read.

When the port C data register is read with PCDIR bits set to "0" (input mode), the pin levels of port C are read.



At system reset all bits in the port C data register (PCD) are set to "0". When data is written to the port C data register, the actual pin change timing is at the rising edge of the system clock for state 2 of the write instruction.

Figure 10-17 indicates port change timing.

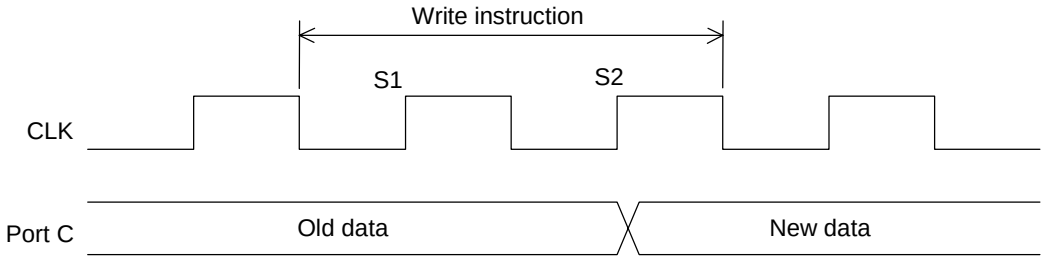
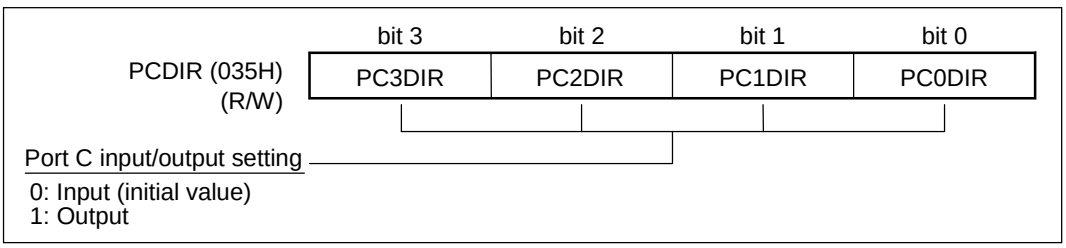


Figure 10-17 Port C Change Timing

(2) Port C direction register (PCDIR)

PCDIR is a 4-bit special function register (SFR) which specifies the port input/output direction for each bit. Pins corresponding to the PCDIR bits set to "0" are input, and those corresponding to the PCDIR bits set to "1" are output.

At system reset all bits in the port C direction register are reset to "0", and port C is initialized to input mode.



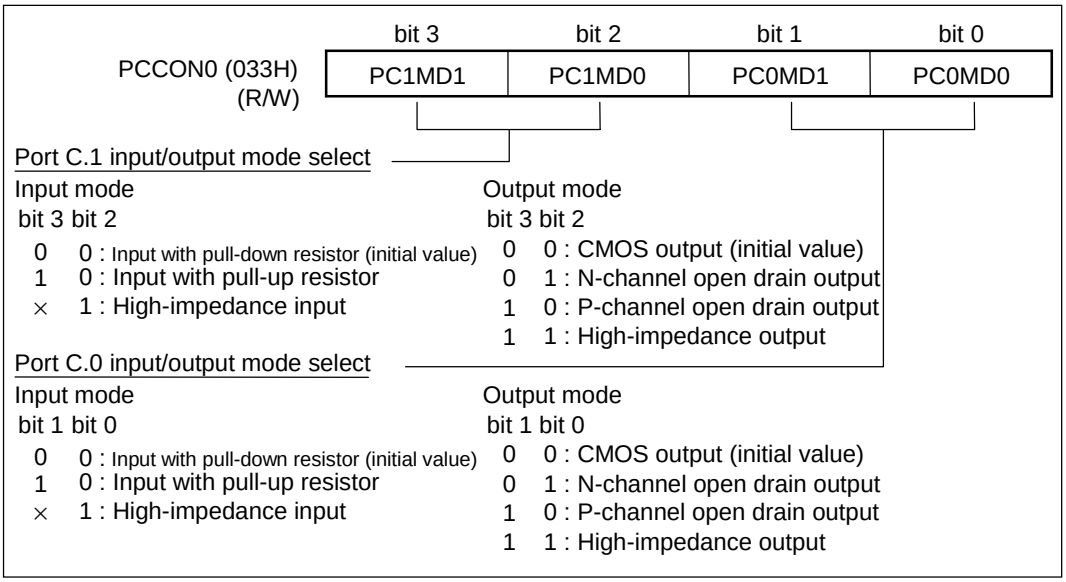
(3) Port C control registers 0/1 (PCCON0, PCCON1)

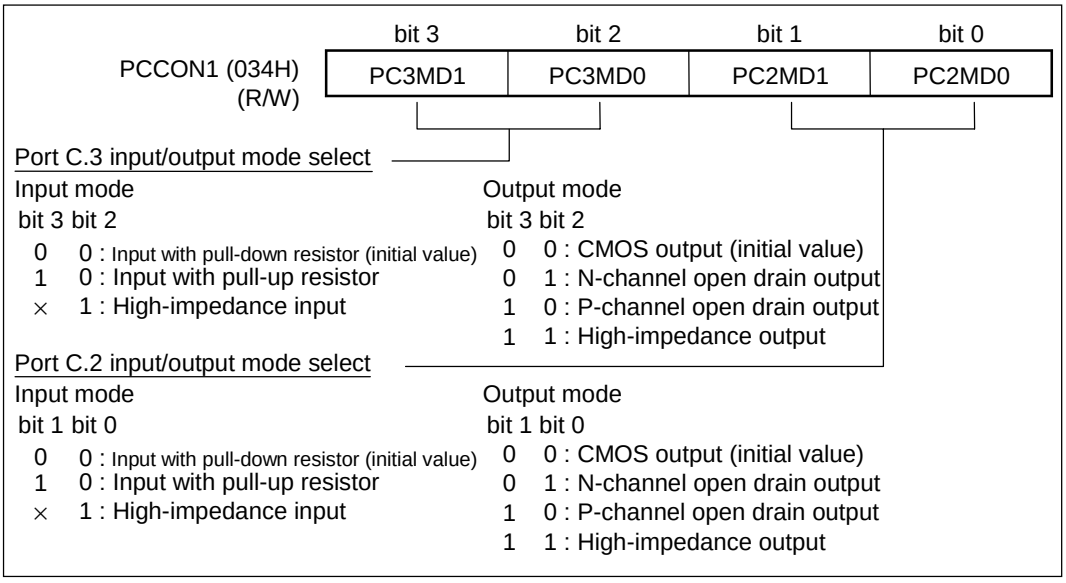
PCCON0 and PCCON1 are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode can be pull-down resistor input, pull-up resistor input or high-impedance input.

The output mode can be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

At system reset all bits in PCCON0 and PCCON1 are set to "0", and port C is initialized to pull-down resistor input mode and CMOS output mode.





(4) Port C mode registers 0/1 (PCMOD0, PCMOD1)

PCMOD0 and PCMOD1 are 4-bit special function registers (SFRs) used to select the sampling frequency when ports are used for external interrupt, and to select secondary functions other than external interrupt.

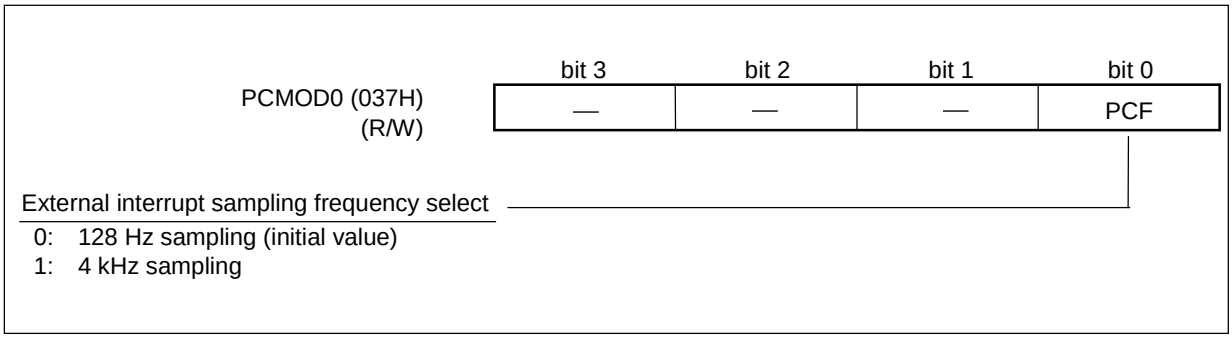
The external interrupt sampling frequency is either 128 Hz or 4 kHz.

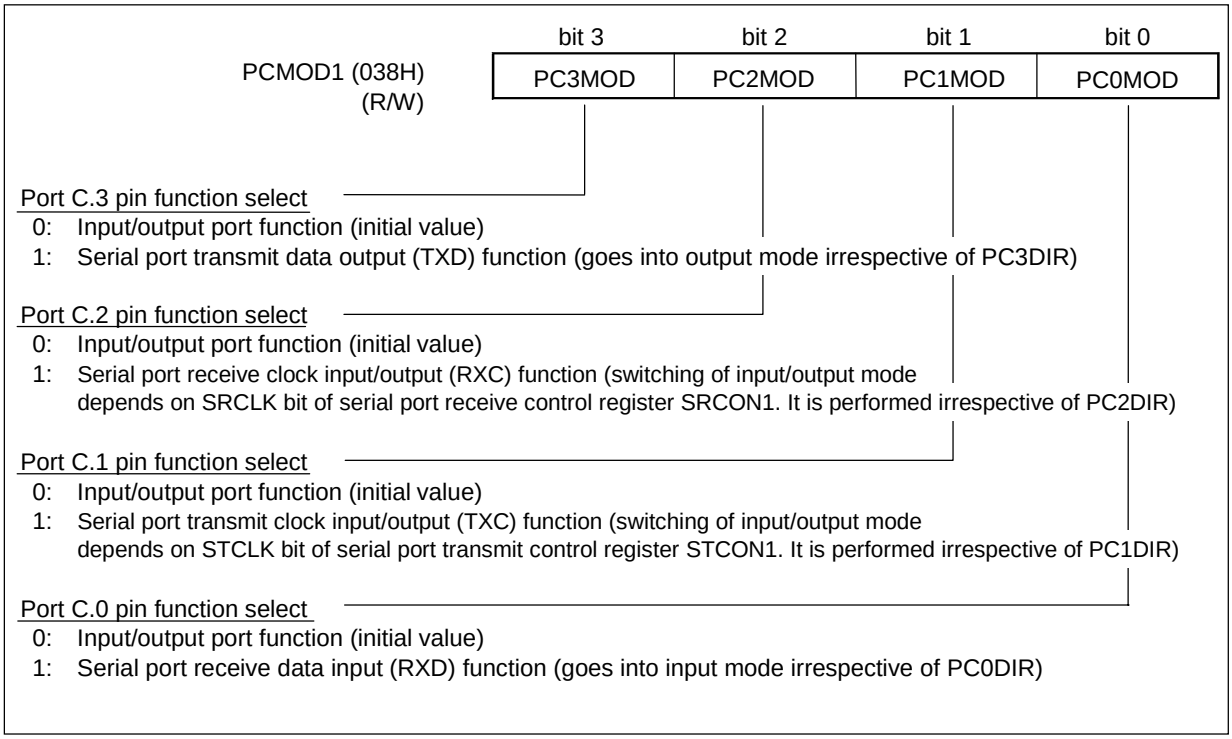
At system reset all the valid bits in the port C mode registers (PCMOD0, PCMOD1) are initialized to "0".

Port C secondary functions are indicated in Table 10-4.

Table 10-4 Port C Secondary Functions

Port	Secondary function	Description
PC.0	RXD	Serial port receive data input
PC.1	TXC	Serial port transmit clock I/O
PC.2	RXC	Serial port receive clock I/O
PC.3	TXD	Serial port transmit data output
PC.0	INT1	External interrupt 1
PC.1		
PC.2		
PC.3		

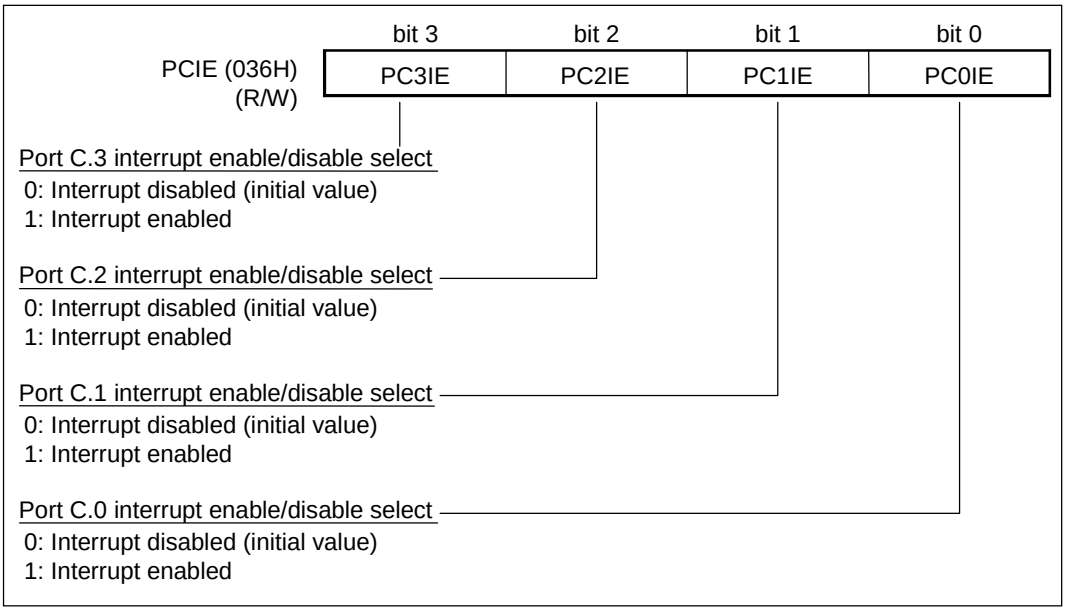

bit 3
bit 2
bit 1
bit 0
PCMOD0 (037H)
(R/W)
—
—
—
PCF
External interrupt sampling frequency select
0: 128 Hz sampling (initial value)
1: 4 kHz sampling


bit 3
bit 2
bit 1
bit 0
PCMOD1 (038H)
(R/W)
PC3MOD
PC2MOD
PC1MOD
PC0MOD
Port C.3 pin function select
0: Input/output port function (initial value)
1: Serial port transmit data output (TXD) function (goes into output mode irrespective of PC3DIR)
Port C.2 pin function select
0: Input/output port function (initial value)
1: Serial port receive clock input/output (RXC) function (switching of input/output mode depends on SRCLK bit of serial port receive control register SRCON1. It is performed irrespective of PC2DIR)
Port C.1 pin function select
0: Input/output port function (initial value)
1: Serial port transmit clock input/output (TXC) function (switching of input/output mode depends on STCLK bit of serial port transmit control register STCON1. It is performed irrespective of PC1DIR)
Port C.0 pin function select
0: Input/output port function (initial value)
1: Serial port receive data input (RXD) function (goes into input mode irrespective of PC0DIR)

(5) Port C interrupt enable register (PCIE)

PCIE is a 4-bit special function register (SFR) that enables/disables individual bits when port C is used as an external interrupt input.

At system reset, all bits in PCIE are cleared to "0" and port C is initialized to the interrupt disabled state.



10.8.3 Port C External Interrupt Function (External Interrupt 1)

Port C has external interrupt 1 allocated as secondary function. Individual bits can be enabled/disabled for external interrupt 1.

External interrupt generation for port C is triggered by the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal (XI1INT) is output, and the interrupt request flag (QXI1) is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

Because the port C external interrupt 1 is set by a level change at any of the port C inputs, each bit of the port must be read to determine which bit of port C generated the interrupt.

The interrupt start address for external interrupt 1 is 0016H.

Figure 10-18 shows the equivalent circuit for external interrupt 1 control.

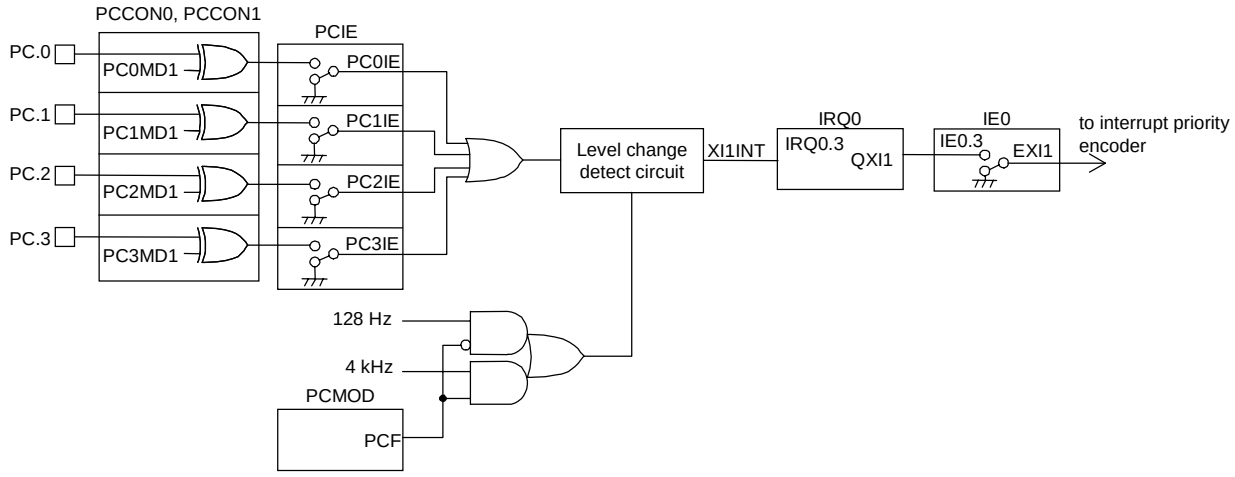


Figure 10-18 External Interrupt 1 Control Equivalent Circuit

Figure 10-19 shows the external interrupt 1 generation timing.

(a) PC0MD1 to PC3MD1 = "0" (initial value: inputs with pull-down resistors or high impedance input) setting

- When all PC.0 to PC.3 inputs are at a "L" level
  External interrupt 1 is generated when any port C input changes to a "H" level.

- When any of PC.0 to PC.3 inputs is at a "H" level
  External interrupt 1 is generated when all the port B inputs change to a "L" level.

(b) PC0MD1 and PC1MD1 = "0" and PC2MD1 and PC3MD1 = "1" (PC.0 and PC.1 selected as inputs with pull-down resistors or high impedance input; PC.2 and PC.3 selected as inputs with pull-up resistors or high impedance input) setting

- When both PC.0 and PC.1 inputs are at a "L" level AND both PC.2 and PC.3 inputs are at a "H" level
  External interrupt 1 is generated when either PC.0 or PC.1 input changes to a "H" level (alternatively, when either PC.2 or PC.3 input changes to a "L" level).

- When either PC.0 or PC.1 input is at a "H" level OR either PC.2 or PC.3 input is at a "L" level External interrupt 1 is generated when both PC.0 and PC.1 inputs change to a "L" level AND both PC.2 and PC.3 inputs change to a "H" level.

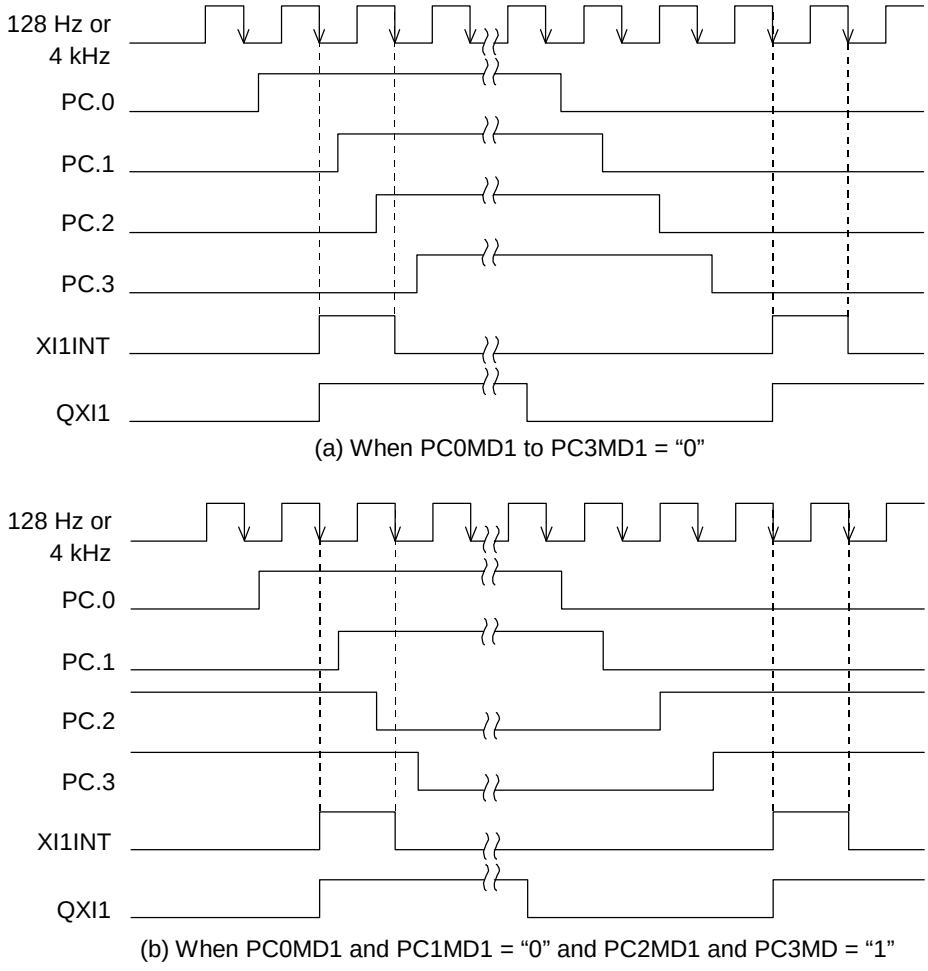


Figure 10-19 Interrupt Generation Timing of External Interrupt 1

10.9 Port E (PE.0–PE.3)

The ML63295A has Port E, a 4-bit input/output port.

10.9.1 Port E Configuration

The circuit configuration for port E is shown in Figure 10-20.

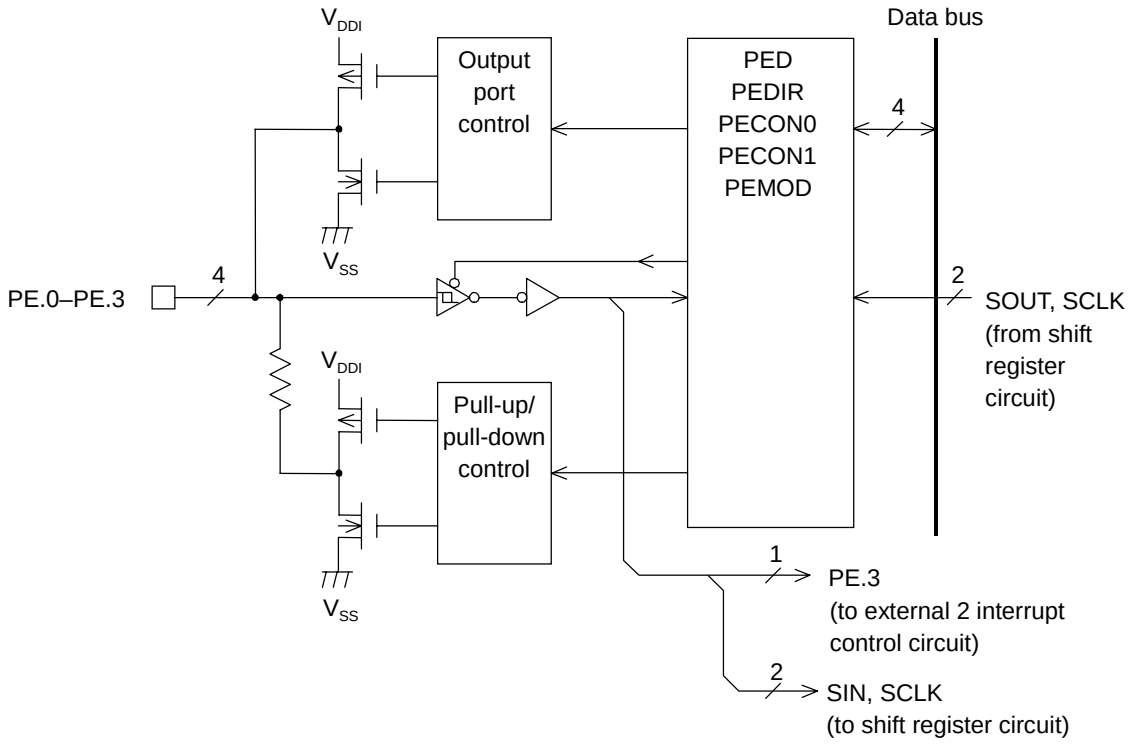


Figure 10-20 Input/Output Port (Port E) Configuration

10.9.2 Port E Registers

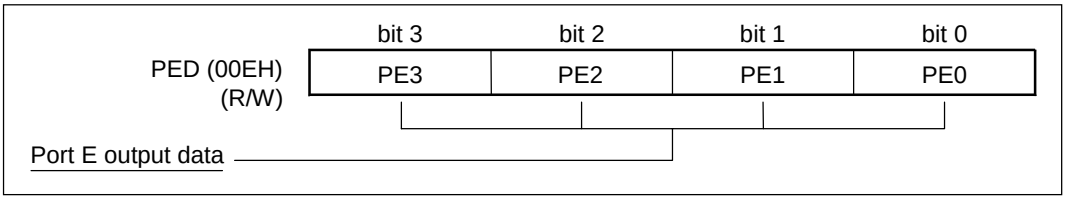
(1) Port E data register (PED)

PED is a 4-bit special function register used to set the output values for port E.

When port E direction register (PEDIR) bits are set to "1" to select the output mode, the content of the port E data register is output to port E.

When the port E data register is read with the output mode selected, the content of the port E data register is read.

When the port E data register is read with PEDIR bits set to "0" (input mode), the pin levels of port E are read.



At system reset all bits in the port E data register (PED) are reset to "0". When data is written to the port E data register, the pin change timing is at the rising edge of the system clock for state 2 of the write instruction.

Figure 10-21 indicates port change timing

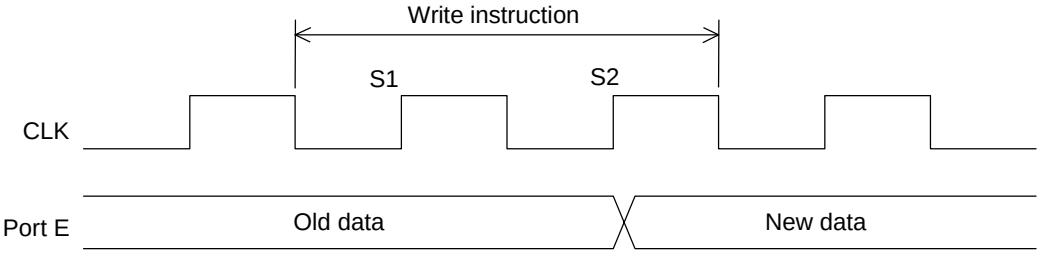
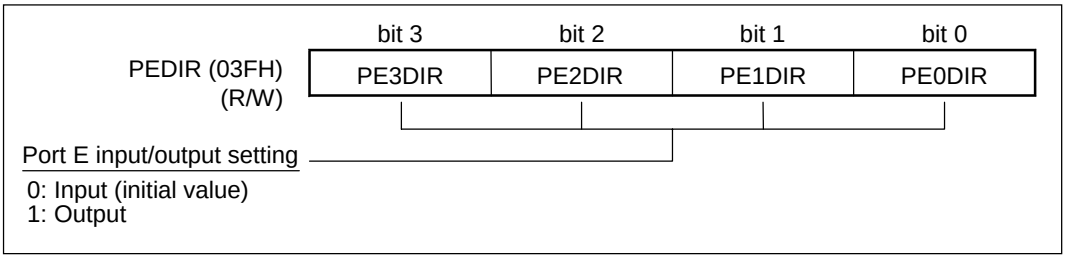


Figure 10-21 Port E Change Timing

(2) Port E direction register (PEDIR)

PEDIR is a 4-bit special function register (SFR) which specifies the port input/output direction for each bit. Pins corresponding to the PEDIR bits set to "0" are input, and those corresponding to the PEDIR bits set to "1" are output.

At system reset all bits in the port E direction register are set to "0", and port E is initialized to input mode.



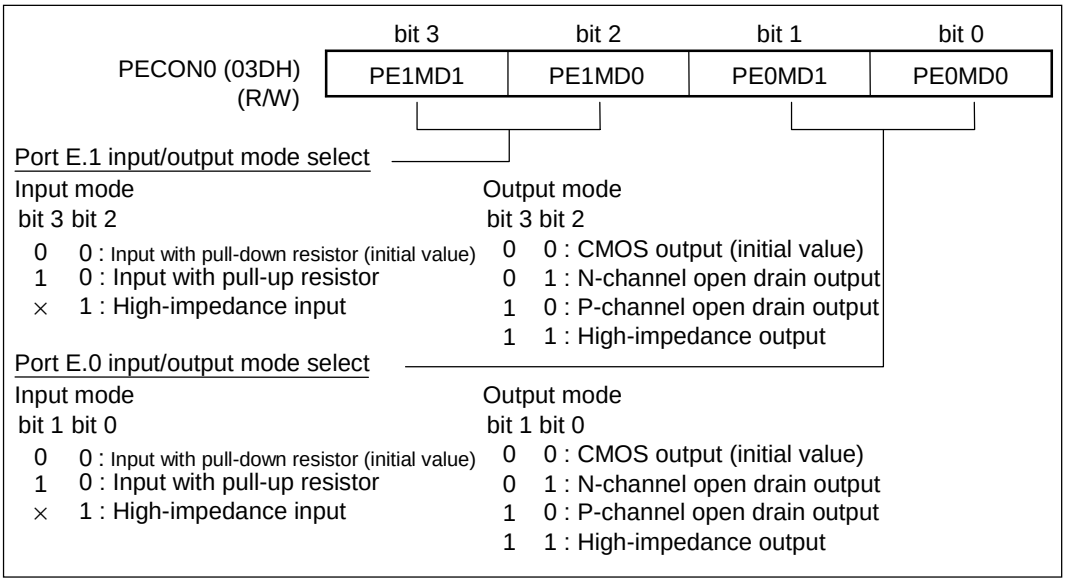
(3) Port E control registers 0/1 (PECON0, PECON1)

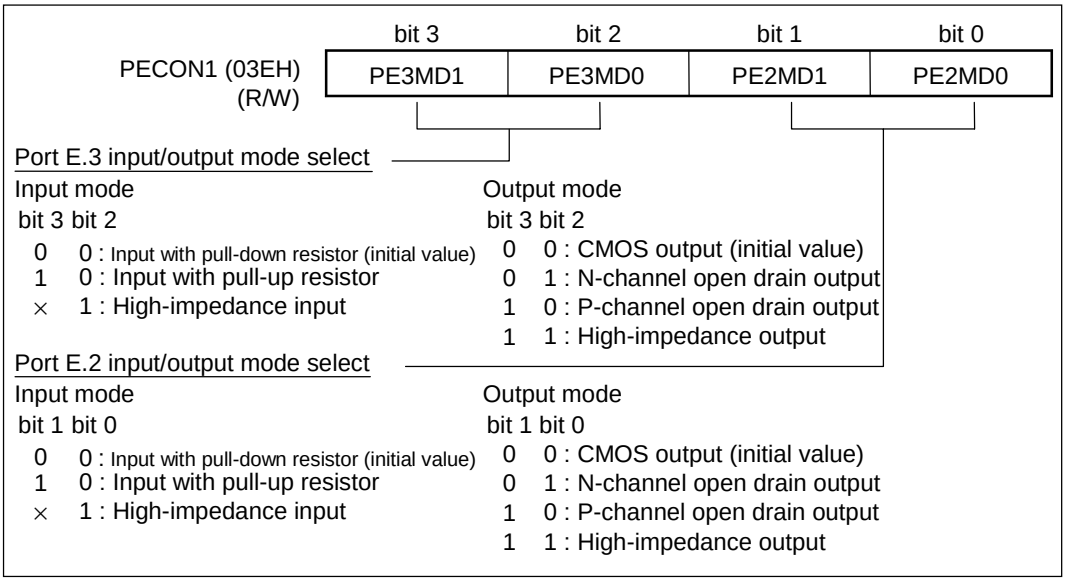
PECON0 and PECON1 are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode can be pull-down resistor input, pull-up resistor input or high-impedance input.

The output mode can be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

At system reset all bits in PECON0 and PECON1 are set to "0", and port E is initialized to pull-down resistor input mode and CMOS output mode.





(4) Port E mode register (PEMOD)

PEMOD is a 4-bit special function register (SFR) used to select the sampling frequency when PE.3 is used as an external interrupt. It is also used to select port E secondary functions other than external interrupt.

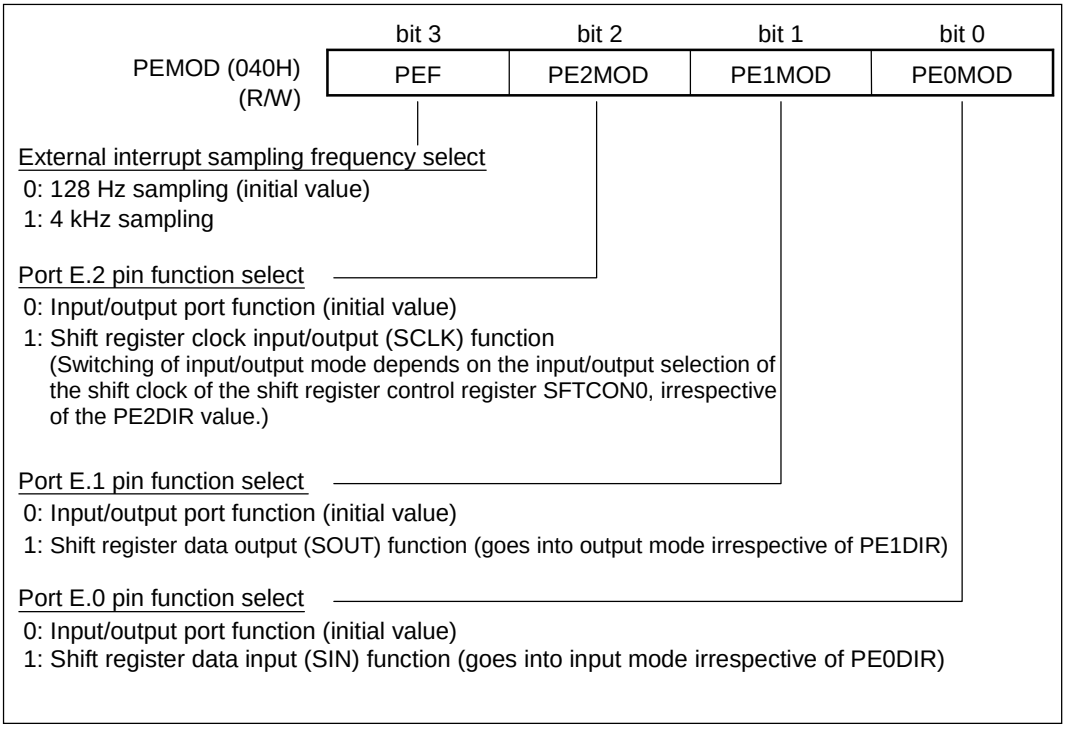
The external interrupt sampling frequency can be selected as either 128 Hz or 4 kHz.

At system reset all bits in PEMOD are initialized to "0".

Port E secondary functions are indicated in Table 10-5.

Table 10-5 Port E Secondary Functions

Port	Secondary function	Description
PE.0	SIN	Shift register data input
PE.1	SOUT	Shift register data output
PE.2	SCLK	Shift register clock I/O
PE.3	INT2	External interrupt 2



10.9.3 Port E.3 External Interrupt Function (External Interrupt 2)

Port E.3 has external interrupt 2 allocated as secondary function.

External interrupt generation for PE.3 is triggered by the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal (XI2INT) is output, and the interrupt request flag (QXI2) is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

The interrupt start address for external interrupt 2 is 0018H.

Figure 10-22 shows the equivalent circuit for external interrupt 2 control.

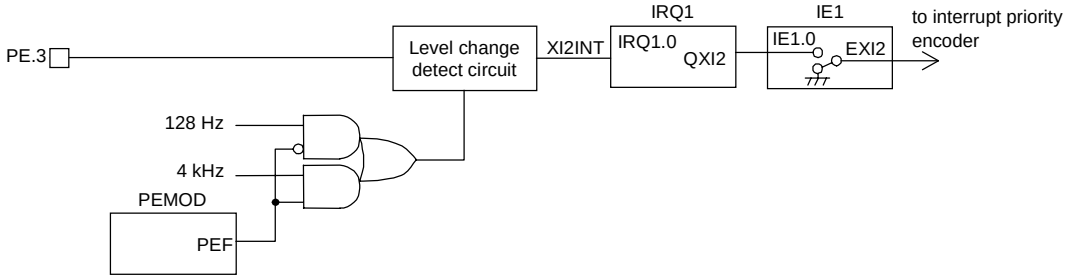


Figure 10-22 External Interrupt 2 Control Equivalent Circuit

Figure 10-23 shows the external interrupt 2 generation timing.

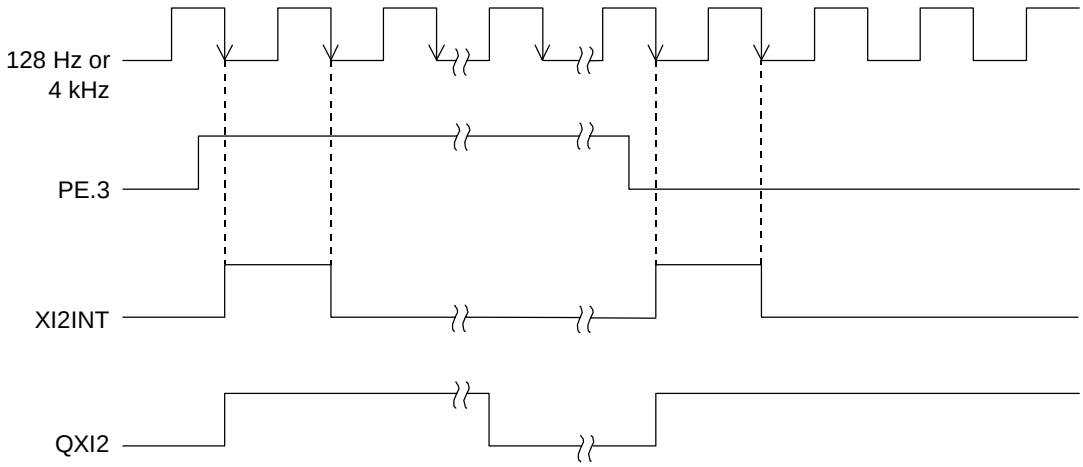


Figure 10-23 External Interrupt 2 Generation Timing

Chapter 11

External Memory Interface (EXTMEM)

11. External Memory Interface (EXTMEM)

11.1 Overview

The ML63295A uses port secondary functions to facilitate the interface with external memory. The external memory transfer instructions are used to transfer data efficiently.

Table 11-1 indicates the port secondary functions for the external memory interface.

Figure 11-1 shows the connection diagram for external memory.

Refer to Chapter 10 for information on port secondary function settings.

Table 11-1 Port Secondary Functions

Pin name	I/O	Function
P4.0/A0	O	P4, P5, P6, P7 secondary functions: Address bus signals for external memory access
P4.1/A1		
P4.2/A2		
P4.3/A3		
P5.0/A4		
P5.1/A5		
P5.2/A6		
P5.3/A7		
P6.0/A8		
P6.1/A9		
P6.2/A10		
P6.3/A11		
P7.0/A12		
P7.1/A13		
P7.2/A14		
P7.3/A15		
P9.0/D0	I/O	P9, PA secondary functions: Data bus signals for external memory access
P9.1/D1		
P9.2/D2		
P9.3/D3		
PA.0/D4		
PA.1/D5		
PA.2/D6		
PA.3/D7		
P8.0/$\overline{RD}$	O	P8.0 secondary functions: Read signal (negative logic) for external memory access
P8.1/$\overline{WR}$	O	P8.1 secondary functions: Write signal (negative logic) for external memory access

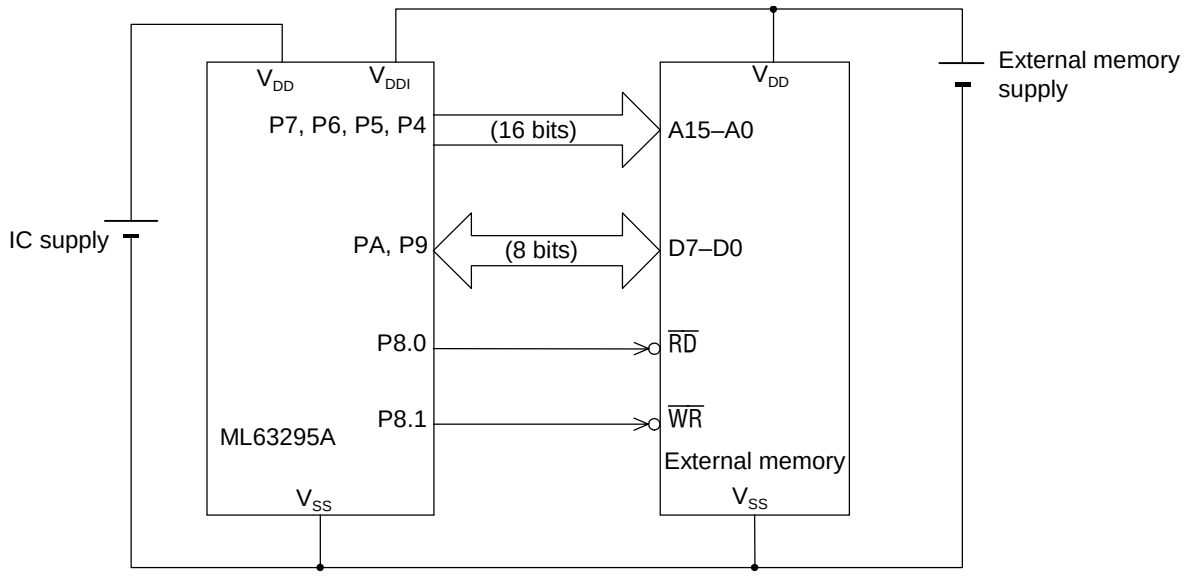


Figure 11-1 Connection to External Memory

11.2 External Memory Address Space

A maximum of 16 address lines can be selected as port secondary functions, allowing access to 64 Kbytes of external memory.

Chip select (CS) can be used for ports other than those set for secondary functions to expand the external memory space above 64 Kbytes. For example (Figure 11-2), if port 3 (P3.3–P3.0) is used for chip select, the external memory space will be

64 Kbytes × 4 = 256 Kbytes.

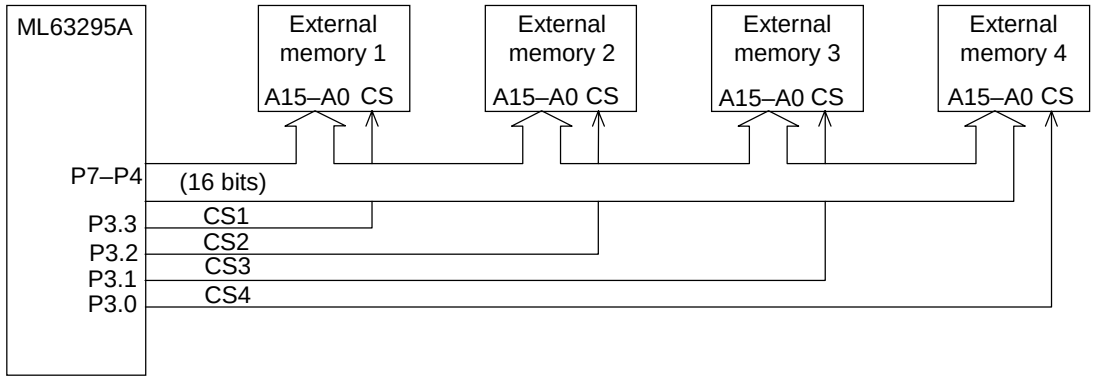


Figure 11-2 Example of Memory Expansion with Chip Select (CS)

11.3 Setting Port Secondary Functions

Port secondary functions are set to access external memory. Refer to Chapter 10 for information on the required registers.

Unless an external memory transfer instruction is executed, P4 to P7, P9 and PA will be as specified in the port control register (that is, normal output and I/O port).

When P8.0 and P8.1 are set for secondary functions they are immediately allocated to read signal ($\overline{RD}$) and write signal ($\overline{WR}$).

11.4 Write to External Memory

The following external memory transfer instructions are executed to write to external memory.

MOVXB [RA],obj
or
MOVXB xadr16,obj

Figure 11-3 shows the timing for external memory write.

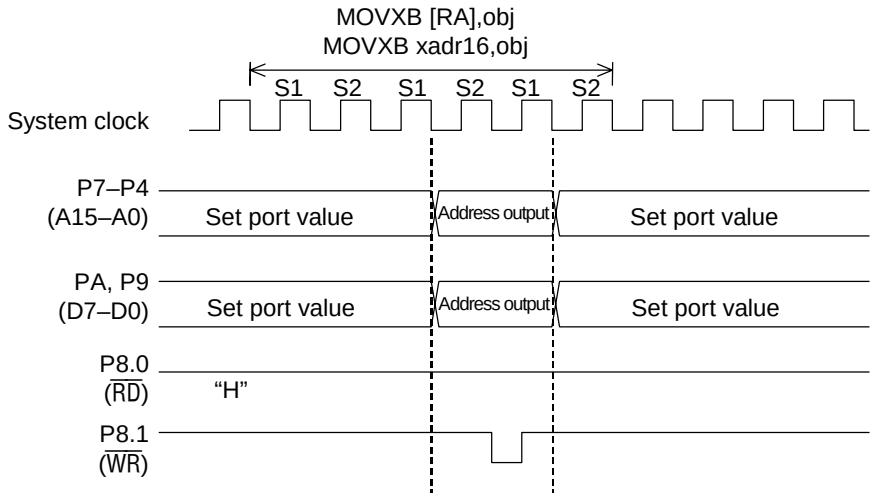


Figure 11-3 Timing for External Memory Write

11.5 Read from External Memory

The following external memory transfer instructions are executed to read from external memory.

MOVXB obj,[RA]
or
MOVXB obj,xadr16

Figure 11-4 shows the timing for external memory read.

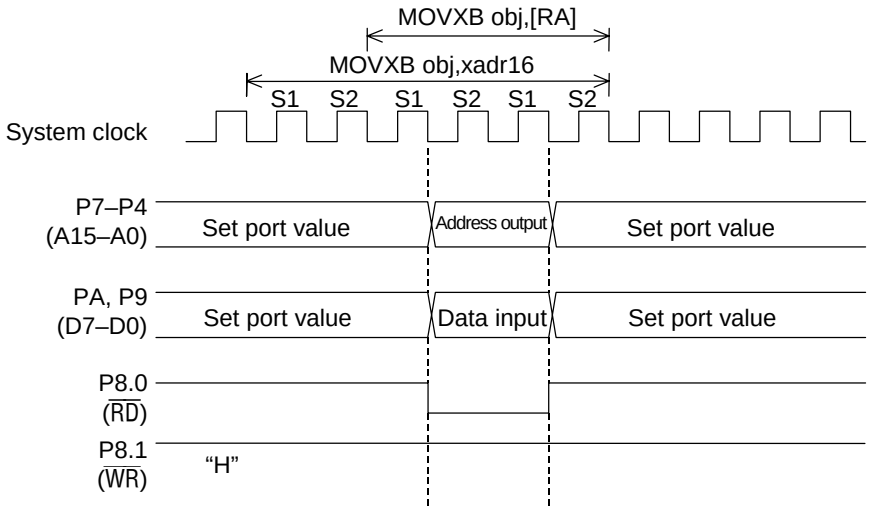


Figure 11-4 External Memory Read Timing

Chapter 12

Melody Driver (MELODY)

12. Melody Driver (MELODY)

12.1 Overview

The ML63295A has an internal melody circuit and buzzer circuit.

While automatically reading melody data in ROM (program memory) as specified by an MSA instruction, the melody circuit outputs a melody signal via the MD and MDB pins.

The melody circuit can select 29 different tones, 63 different tone lengths, and 15 different tempos.

The buzzer circuit has four different buzzer output modes at a frequency of 4 kHz. The buzzer driver signal is output via the MD and MDB pins.

Melody output is a higher priority operation than buzzer output.

12.2 Melody Driver Configuration

The melody driver configuration is shown in Figure 12-1.

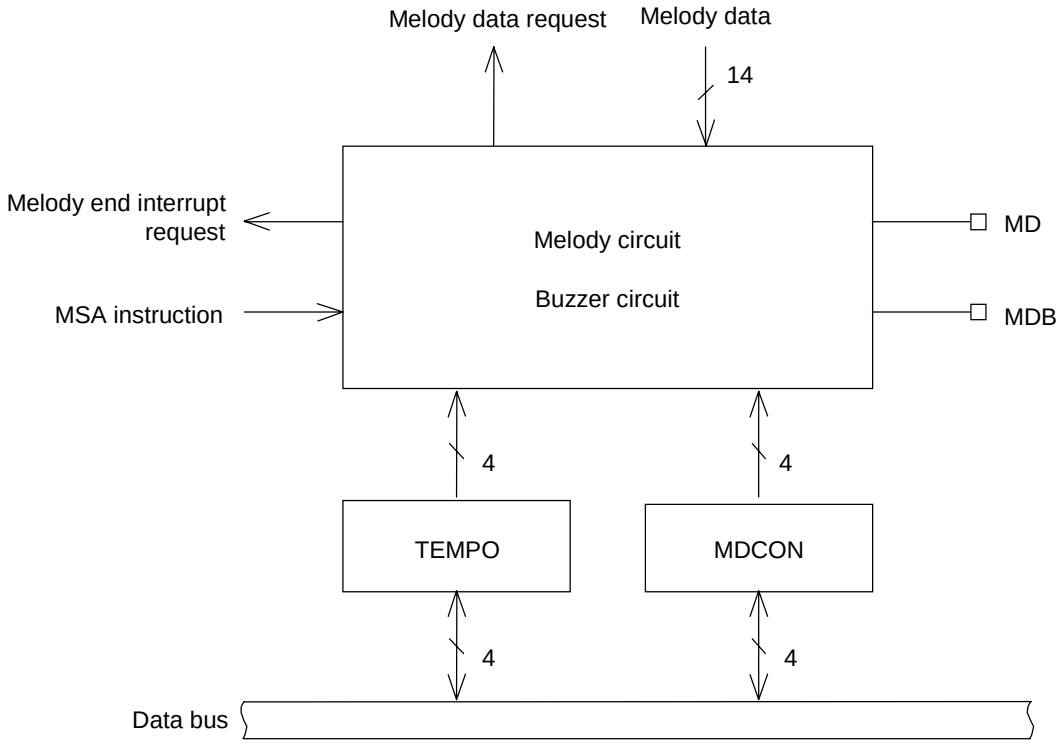
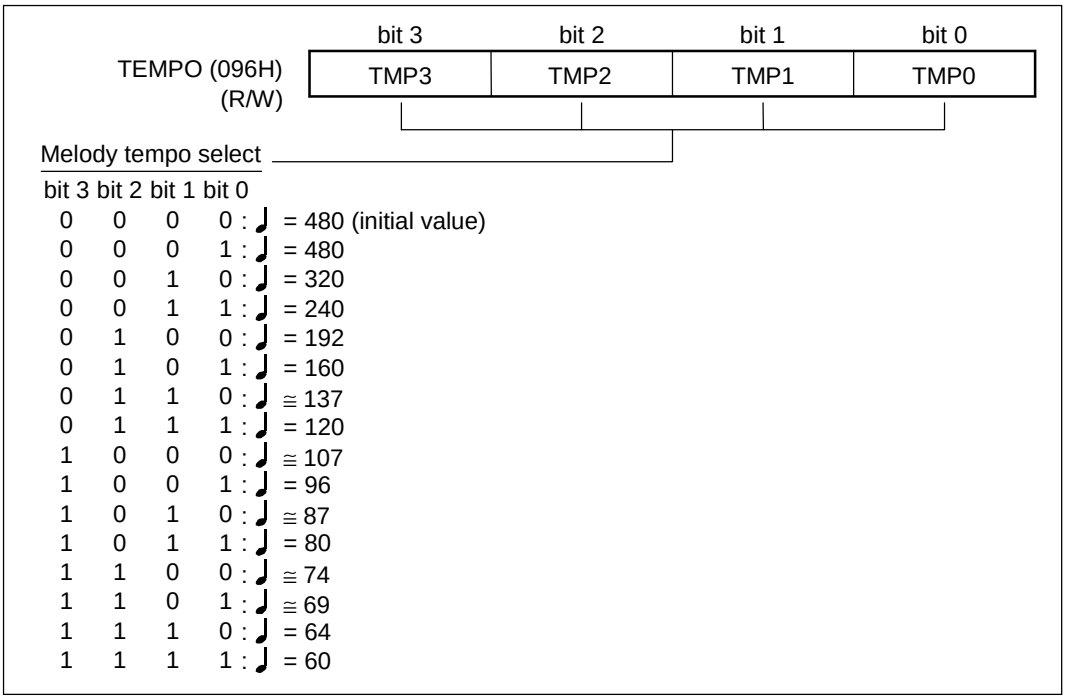


Figure 12-1 Melody Driver Configuration

12.3 Melody Driver Registers

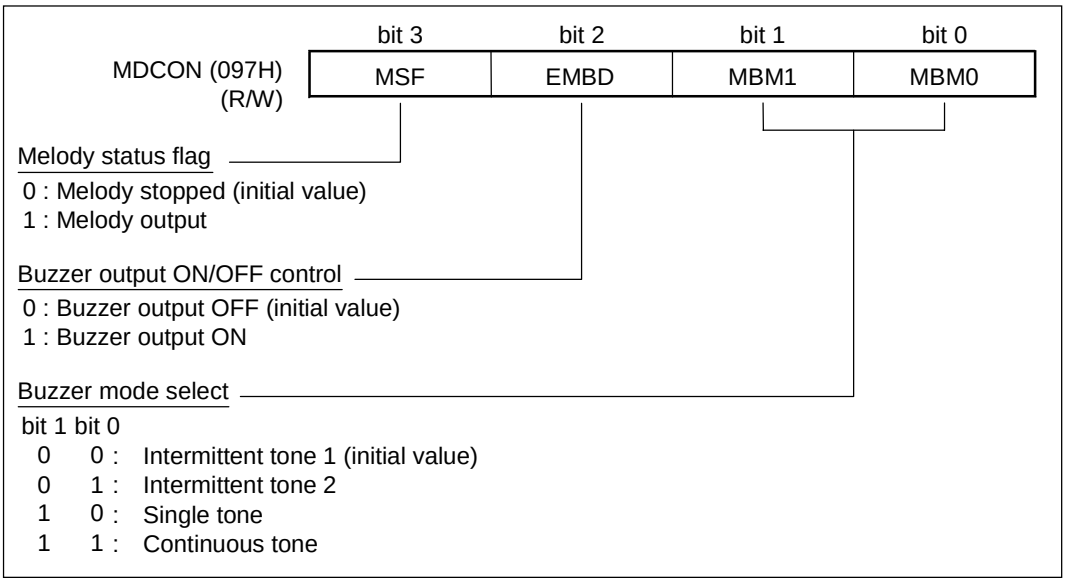
(1) Tempo Register (TEMPO)

TEMPO is a 4-bit special function register (SFR) that sets the tempo of the melody driver.



(2) Melody Driver Control Register (MDCON)

MDCON is a 4-bit special function register (SFR) that controls output of the melody driver.



bit 3: MSF

This flag indicates the melody output status.
When an MSA instruction starts the melody, MSF is set to "1". After output of the last melody data (END bit is "1"), MSF is cleared to "0".
Setting MSF to "0" during melody output will forcibly stop the melody output. If forcibly stopped, the melody output cannot be restarted at the address at which it was stopped.
At system reset, MSF is cleared to "0".

Note:

If MSF (bit 3 of MDCON) is set to "0" to stop melody output forcibly, it is required to set the stop address on the ROM table to the end-data address (8000H). In this case, set MSF to "0" after writing the melody end data that consists of two words of melody (silence with the END bit being "1") data. If this programming is not executed, melody output may not be stopped even if MSF is set to "0". Example programming is shown below.

```
;*Program part**********
      DI                    ; 0. Disable master interrupt (MIE).
      MSA   MDSTOP_DATA     ; 1. Write melody end data to the melody circuit.
      MOV   A, #0           ; 2. Set the MSF to "0".
      MOV   MDCON,A         ;
      MOV   A, #1101b       ; 3. Clear melody end interrupt request (QMD).
      AND   IRQ0, A         ;
      EI                    ; 4. Enable master interrupt (MIE).
;*ROM table data part****
;*Provide two words of melody data so that a melody will always be terminated even if a melody
;*request is issued twice.
MDSTOP_DATA:
      DW    8000H           ; Silence data 1
      DW    8000H           ; Silence data 2
;************************
```

In the EASE63180 Emulator, melody output will be stopped only by setting MSF to "0"; writing melody end data is not needed.

bit 2: EMBD

This bit turns the buzzer output ON or OFF.
At system reset, EMBD is cleared to "0" and buzzer output is turned OFF.
In the single tone output mode, setting EMBD to "1" turns ON the buzzer output. After the second falling edge of the 32 Hz output, EMBD is cleared to "0" and buzzer output is turned OFF.
If melody output is started during buzzer output, EMBD is cleared to "0" and the buzzer output is turned OFF.

bit 1, 0: MBM1, MBM0

These bits select the buzzer output mode.
Output of two types of intermittent tones, a single tone or a continuous tone can be selected.
At system reset, MBM1 and MBM0 are cleared to "0", selecting output of intermittent tone 1.

Buzzer output mode	Waveform
Intermittent tone 1	Intermittent tone waveform synchronized to 8 Hz output of time base counter
Intermittent tone 2	Intermittent tone waveform synchronized to the logical AND of 8 Hz signal output and a "L" level of 1 Hz signal output of the time base counter
Single tone	Single tone waveform beginning when EMBD is set to "1" until second falling edge of 32 Hz output of time base counter
Continuous tone	Continuous tone waveform that is constant while EMBD is "1"

Figure 12-2 shows the output waveforms of the melody driver output pins.

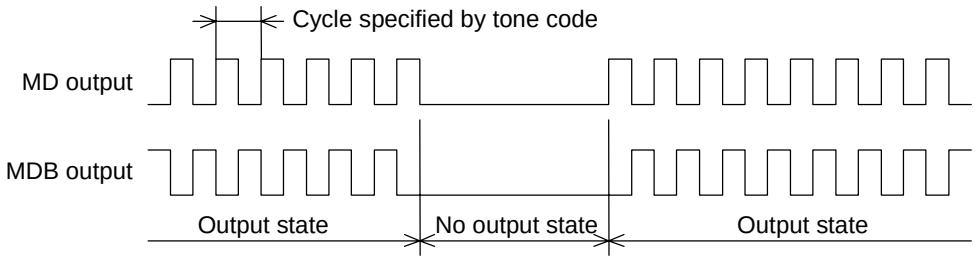


Figure 12-2 Output Waveforms of Melody Driver Output Pins

12.4 Melody Circuit Operation

After the melody tempo is set in the tempo register (TEMP), execution of an MSA instruction will start operation of the melody circuit.

The melody circuit outputs melody data while automatically reading melody data in ROM (program memory) as specified by an MSA instruction. When the last melody data is read (END bit is "1"), the melody circuit generates a melody end interrupt request. At this time, if an MSA instruction is executed, after the last melody data is output, melody output will continue from the melody data specified by the MSA instruction. If an MSA instruction is not executed, the melody output will stop after the last melody data is output.

MSF (bit 3 of MDCON) is a flag indicating the melody output status. When MSF is "1", the melody is being output, and when "0", the melody is stopped. Setting MSF to "0" during melody output will forcibly stop the melody output. If it is required to stop melody output forcibly, describe the program according to the "Note" on page 12-3. If forcibly stopped, the melody output cannot be restarted at the address at which it was stopped.

12.4.1 Tempo Data

Tempo data defines the basic tone length. Tempo data is set in the tempo register (TEMPO).

The tempos (number of counts per minute) set by TEMPO are shown in Table 12-1.

Table 12-1 Melody Tempo

TEMPO					Tempo
TP3–0	TP3	TP2	TP1	TP0	
0H	0	0	0	0	♩ = 480
1H	0	0	0	1	♩ = 480
2H	0	0	1	0	♩ = 320
3H	0	0	1	1	♩ = 240
4H	0	1	0	0	♩ = 192
5H	0	1	0	1	♩ = 160
6H	0	1	1	0	♩ ≅ 137
7H	0	1	1	1	♩ = 120
8H	1	0	0	0	♩ ≅ 107
9H	1	0	0	1	♩ = 96
AH	1	0	1	0	♩ ≅ 87
BH	1	0	1	1	♩ = 80
CH	1	1	0	0	♩ ≅ 74
DH	1	1	0	1	♩ ≅ 69
EH	1	1	1	0	♩ = 64
FH	1	1	1	1	♩ = 60

12.4.2 Melody Data

Melody data is 14-bit format data in the program ROM defining tone, tone length and end tone.

The melody data format is indicated in Figure 12-3.

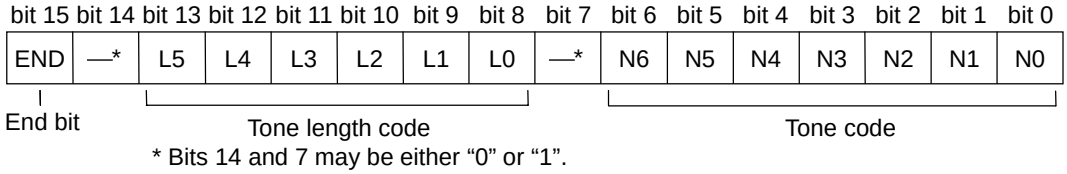


Figure 12-3 Melody Data Format

(1) Tone code

The tone code is set in bits 6 through 0 of the melody data. The frequencies that can be output by the melody circuit are defined as:

$$\frac{65536}{(N + 2)} \text{ Hz (where N is an integer from 4 to 127)}$$

The relation between N and tone code bits is:

$N = 2^6N6 + 2^5N5 + 2^4N4 + 2^3N3 + 2^2N2 + 2^1N1 + 2^0N0$

If N6 through N2 are all set to "0", there is no melody output for the time specified by the tone length code. Values for N1 and N0 are irrelevant.

Table 12-2 indicates the relations between tones and tone codes.

Table 12-2 Tone and Tone Code Correspondence

Tone	Frequency (Hz)	Tone code							
		N6	N5	N4	N3	N2	N1	N0	N6–N0
C^1	529	1	1	1	1	0	1	1	7BH
Cis^1	560	1	1	1	0	0	1	1	73H
D^1	590	1	1	0	1	1	0	1	6DH
Dis^1	624	1	1	0	0	1	1	1	67H
E^1	662	1	1	0	0	0	0	1	61H
F^1	705	1	0	1	1	0	1	1	5BH
Fis^1	745	1	0	1	0	1	1	0	56H
G^1	790	1	0	1	0	0	0	1	51H
Gis^1	840	1	0	0	1	1	0	0	4CH
A^1	886	1	0	0	1	0	0	0	48H
Ais^1	936	1	0	0	0	1	0	0	44H
B^1	993	1	0	0	0	0	0	0	40H
C^2	1057	0	1	1	1	1	0	0	3CH
Cis^2	1111	0	1	1	1	0	0	1	39H
D^2	1192	0	1	1	0	1	0	1	35H

Table 12-2 Tone and Tone Code Correspondence (continued)

Tone	Frequency (Hz)	Tone code							
		N6	N5	N4	N3	N2	N1	N0	N6–N0
Dis^2	1260	0	1	1	0	0	1	0	32H
E^2	1338	0	1	0	1	1	1	1	2FH
F^2	1394	0	1	0	1	1	0	1	2DH
Fis^2	1490	0	1	0	1	0	1	0	2AH
G^2	1560	0	1	0	1	0	0	0	28H
Gis^2	1680	0	1	0	0	1	0	1	25H
A^2	1771	0	1	0	0	0	1	1	23H
Ais^2	1872	0	1	0	0	0	0	1	21H
B^2	1986	0	0	1	1	1	1	1	1FH
C^3	2114	0	0	1	1	1	0	1	1DH
D^3	2341	0	0	1	1	0	1	0	1AH
Dis^3	2521	0	0	1	1	0	0	0	18H
E^3	2621	0	0	1	0	1	1	1	17H
Fis^3	2979	0	0	1	0	1	0	0	14H

(2) Tone length code

The tone length code is set in melody data bits 13 through 8.

Table 12-3 indicates the relation between tone length and tone length code (L5 to L0).

The tone length that is set during execution of the MSA instruction is shorter by approximately 1 to 3 ms.

When all bits are set to "0", the tone length will be the same as the minimum tone length (the tone length with only L0 set to "1").

Table 12-3 Tone Length and Tone Length Code Correspondence

Tone length	Tone length code						
	L5	L4	L3	L2	L1	L0	L5–L0
	1	1	1	1	1	1	3FH
	1	0	1	1	1	1	2FH
	0	1	1	1	1	1	1FH
	0	1	0	1	1	1	17H
	0	0	1	1	1	1	0FH
	0	0	1	0	1	1	0BH
	0	0	0	1	1	1	07H
	0	0	0	1	0	1	05H
	0	0	0	0	1	1	03H
	0	0	0	0	1	0	02H
	0	0	0	0	0	1	01H

Tone lengths specified by the tone length code and the tempo data are expressed by the following:

$1.953125 \times (TP + 1) \times (L + 1)$ ms (where TP is an integer from 1 to 15, and L is an integer from 1 to 63)

TP is a value set in the tempo register (TEMPO), and has the following bit correspondence:

$TP = 2^3TP3 + 2^2TP2 + 2^1TP1 + 2^0TP0$

L is set by the tone length code, and has a bit correspondence with the tone length code as:

$L = 2^5L5 + 2^4L4 + 2^3L3 + 2^2L2 + 2^1L1 + 2^0L0$

(3) END bit

The END bit is set in bit 15 of the melody data. When the output of the last melody data is started (END bit is "1"), the melody circuit generates a melody end interrupt request, and stops the melody after the last melody data is output.

12.4.3 Melody Circuit Application Example

An example melody is shown in Figure 12-4.

Table 12-4 lists the note codes for the melody shown in Figure 12-4.

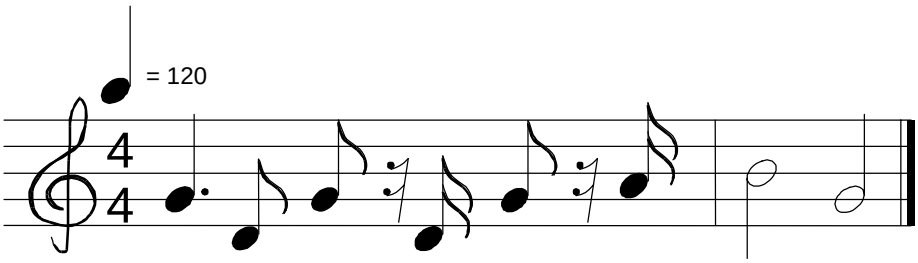


Figure 12-4 Example Melody

Table 12-4 Note Code Table

Note	Note code																Hex
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	END	—*	L5	L4	L3	L2	L1	L0	—*	N6	N5	N4	N3	N2	N1	N0	
G^2	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	2F28H
D^2	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	0F35H
G^2	0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0	0F28H
—	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0700H
D^2	0	0	0	0	0	1	1	1	0	0	1	1	0	1	0	1	0735H
G^2	0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0	0F28H
—	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0700H
A^2	0	0	0	0	0	1	1	1	0	0	1	0	0	0	1	1	0723H
B^2	0	0	1	1	1	1	1	1	0	0	0	1	1	1	1	1	3F1FH
G^2	1	0	1	1	1	1	1	1	0	0	1	0	1	0	0	0	BF28H

* Bits 14 and 7 may be "0" or "1", but in this example they are shown as "0".

12.5 Buzzer Circuit Operation

When EMBD (bit 2 of MDCON) is set to "1", a buzzer driver signal is sent to the melody driver output pins (MD, MDB).

Four buzzer output modes can be selected by MBM1 (bit 1 of MDCON) and MBM0 (bit 0 of MDCON): two types of intermittent tones, a single tone, or a continuous tone output. The buzzer output frequency is 4 kHz and has a 50% duty ratio.

In the intermittent tone 1 mode, a waveform synchronized to the 8 Hz output of the time base counter is output.

In the intermittent tone 2 mode, a waveform synchronized to the logical AND of 8 Hz signal output and a "L" level of 1 Hz signal of the time base counter is output.

In the single tone mode, output starts in synchronization with the rising edge of EMBD. At the second falling edge of the 32 Hz output of the time base counter, EMBD is cleared to "0" and output is stopped.

In the continuous tone mode, output is continued while EMBD is "1".

While the melody is being output (MSF (bit 3 of MDCON) = "1"), the buzzer output is turned OFF. If melody output is started during buzzer output, EMBD is cleared to "0", the buzzer output is stopped, and melody output is given priority.

Figure 12-5 shows the output waveforms of each mode. Shaded sections indicate the 4 kHz output frequency.

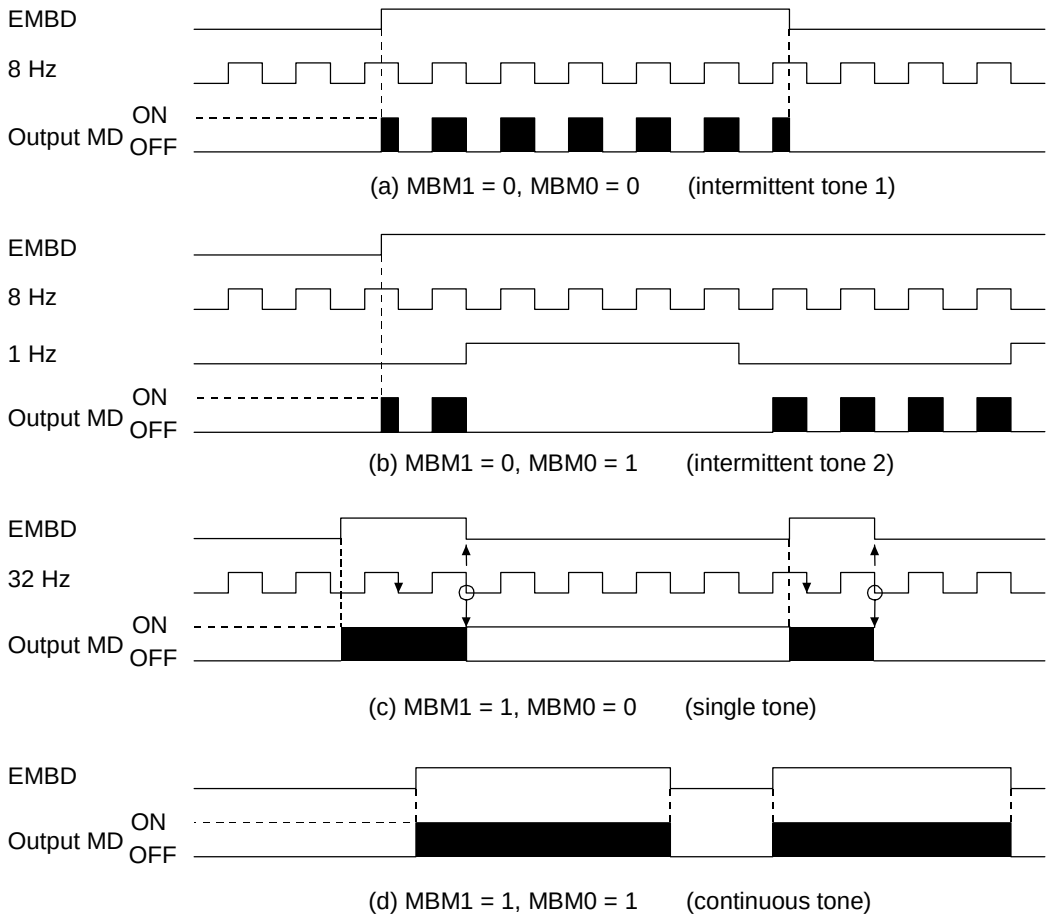


Figure 12-5 Buzzer Driver Output Waveforms in Each Output Mode

Chapter 13

Serial Port (SIO)

13. Serial Port (SIO)

13.1 Overview

The ML63295A has a built-in serial communication port (serial port) that can be selected for either synchronous or asynchronous communication.

The serial port implements the send and receive circuits in independent circuits, making it possible to send and receive simultaneously.

The send and receive modes can be UART mode (asynchronous communication mode) or synchronous mode (synchronous communication mode).

In synchronous mode an internal clock mode generates the shift clock internally, and an external clock mode receives an external shift clock.

Table 13-1 shows the serial port modes.

Table 13-1 Serial Port Modes

		Mode		Baud rate
Serial port	Send side	UART mode		Can be set to a user-specified value with timers 2, 3 (TM2, 3)
		Synchronous mode	Internal clock mode	Low-speed clock (30 to 80 kHz)
			External clock mode	From external clock
	Receive side	UART mode		• 2 TBCCLK (9600 bps) • TBCCLK (4800 bps) • 1/2 TBCCLK (2400 bps) • 1/4 TBCCLK (1200 bps)
		Synchronous mode	Internal clock mode	Low-speed clock (30 to 80 kHz)
			External clock mode	From external clock

13.2 Serial Port Configuration

Figure 13-1 indicates the serial port configuration.

The serial port consists of the send/receive clock generator circuits, the send/receive control registers, the buffer registers to store send/receive data, send/receive data transfer shift registers, and the send/receive status registers.

PC.0/RXD is the send serial data input pin, PC.3/TXD is the send serial data output pin, PC.1/TXC is the serial send clock I/O pin, and PC.2/RXC is the serial receive clock I/O pin. Set I/O and secondary functions with the port control registers as needed for each communication mode.

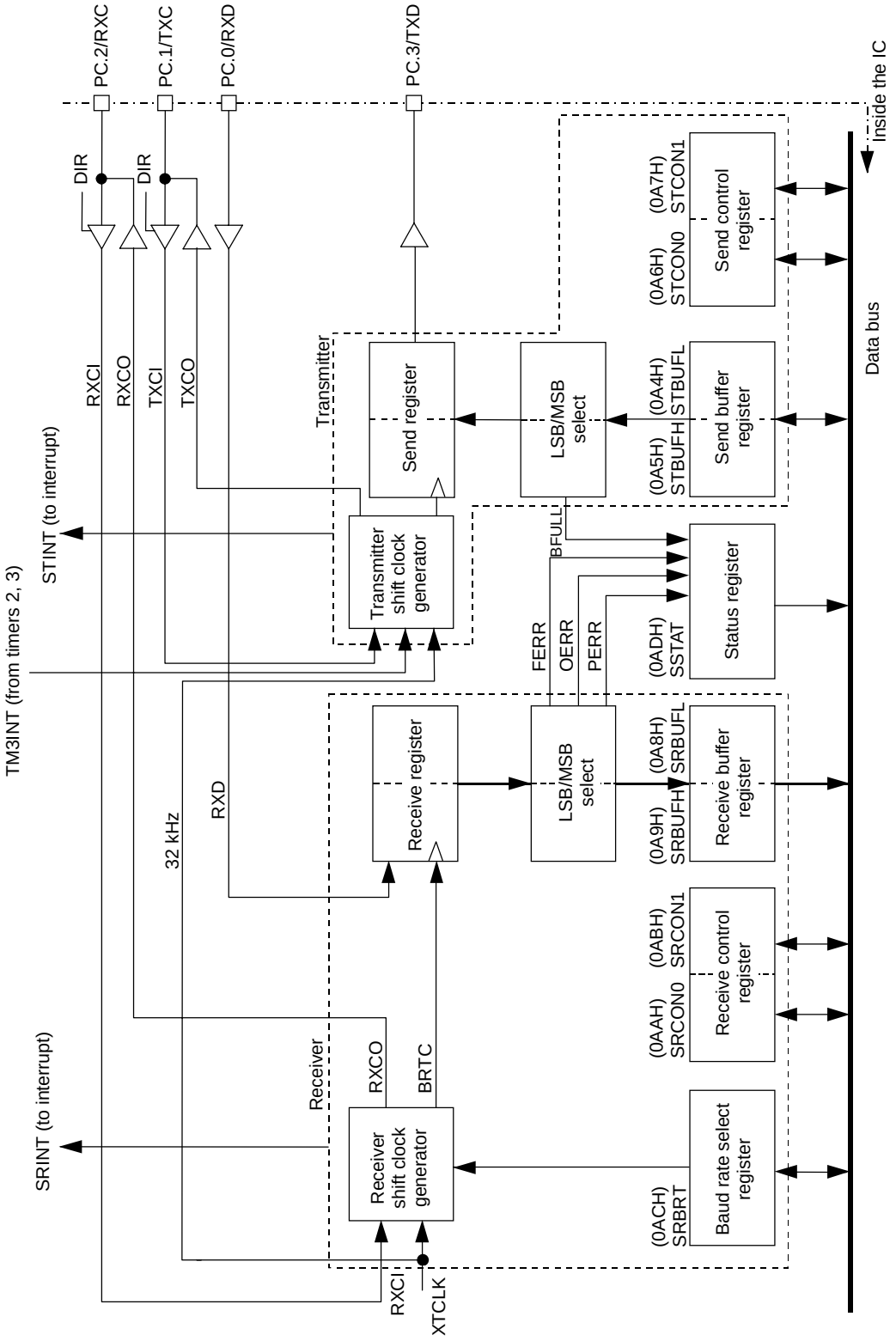
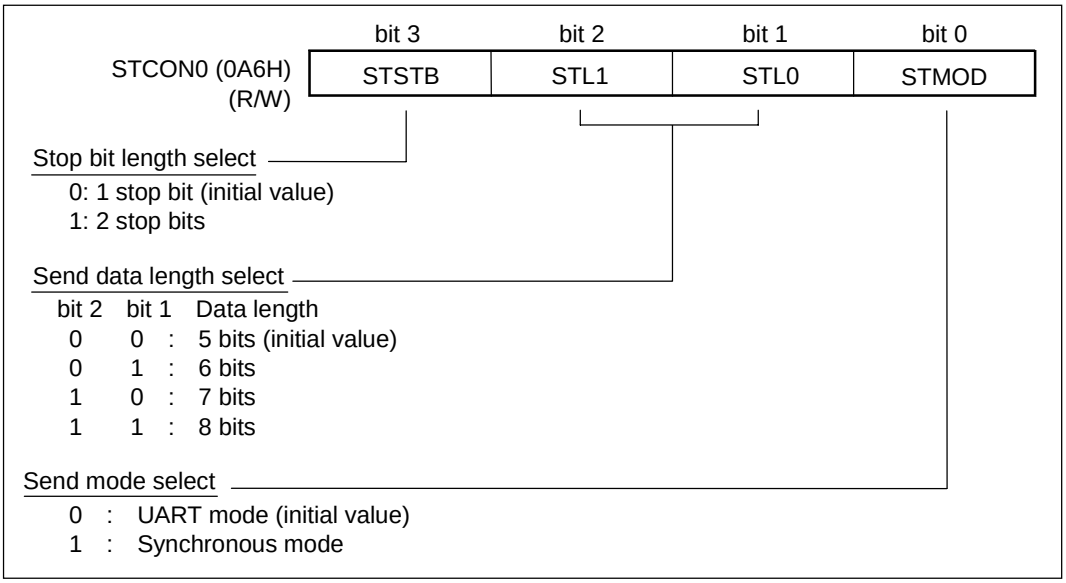


Figure 13-1 Serial Port Configuration

13.3 Serial Port Registers

(1) Send control registers 0/1 (STCON0, STCON1)

STCON0 and STCON1 are 4-bit special function registers (SFRs) to control the serial port send operation. STCON0 and STCON1 are initialized to "0" at system reset.



bit 3: STSTB (Serial Transmission STop Bit)

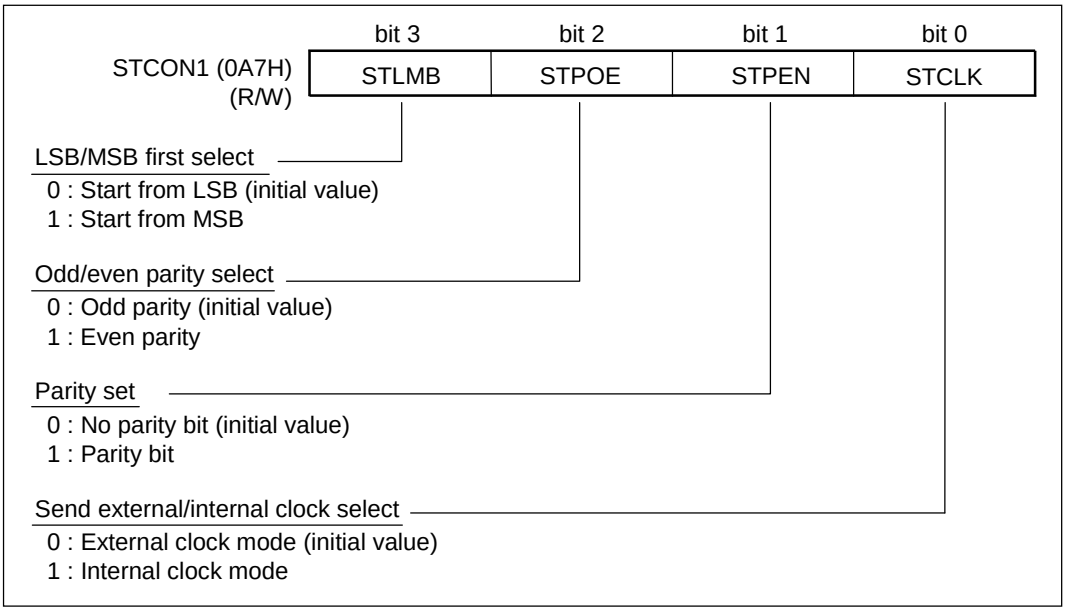
This bit specifies stop bit length. Valid only when bit 0 is "0" (UART mode).

bit 2, 1: STL1 (Serial Transmission Length select bit 1),
STL0 (Serial Transmission Length select bit 0)

These bits specify the send data length.

bit 0: STMOD (Serial Transmission MODe bit)

This bit specifies the serial port send operation mode.



bit 3: STLMB (Serial Transmission Least significant bit first or Most significant Bit first)

This bit specifies either LSB first or MSB first for send data.

bit 2: STPOE (Serial Transmission Parity Odd or Even number bit)

This bit specifies whether the parity bit is even or odd. Valid only when bit 1 is "1" (parity bit).

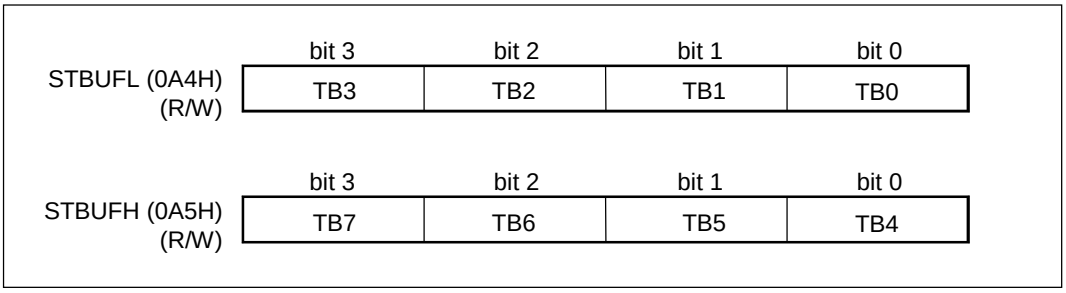
bit 1: STPEN (Serial Transmission Parity ENable bit)

This bit specifies whether or not a parity bit is added.

bit 0: STCLK (Serial Transmission CLock select bit)

This bit specifies the external/internal send clock for synchronous mode. Valid only when STMOD (bit 0 of STCON0) is "1" (synchronous mode).

(2) Send buffer registers (STBUFL, STBUFH)



STBUFL and STBUFH are 4-bit special function registers (SFRs) that set send data for serial port send operation.

LSB/MSB selection (described later) allows the data send direction (LSB or MSB first) to be specified. Both STBUFL and STBUFH are initialized to "0" at system reset.

Send operation begins when send data is set to STBUFH. Be sure to set send data to STBUFL before setting data to STBUFH.

Also set the baud rate and send mode before beginning send operation.

If send operation is already under way when send data is set to STBUFH, send for the new data begins when the prior send has ended, and at the same time an interrupt request signal (STINT) is generated. In the STINT interrupt routine the program should first write the send data to STBUFL and STBUFH to assure no pauses in the send sequence.

(3) Send register

The send register is a shift register that handles the shift operation in send. At system reset it is cleared to 00H. The send register cannot be directly accessed from the CPU.

The hardware send flow is indicated in Figure 13-2, to explain the timing for transfer of data from STBUFL/H to the send register.

First set the send mode and baud rate. When send data is set to STBUFH, the status (SSTAT) buffer full flag (BFULL) is set to "1", and unless send operation is already under way the content of STBUFL/H is transferred to the send register and send operation begins. When send operation begins the BFULL flag is reset to "0", and the next send data can be set to STBUFL/H.

If prior data send operation is not complete, the send data is held in STBUFL/H until send is completed. In this case BFULL remains set to "1". When the prior send operation is complete the send data will be transferred from STBUFL/H to the send register, and send begins.

Note:

When BFULL is "1" it is possible to set data to STBUFL/H, but prior data set to STBUFL/H that is being held there is overwritten and lost. Always set data after verifying that the BFULL flag is "0".

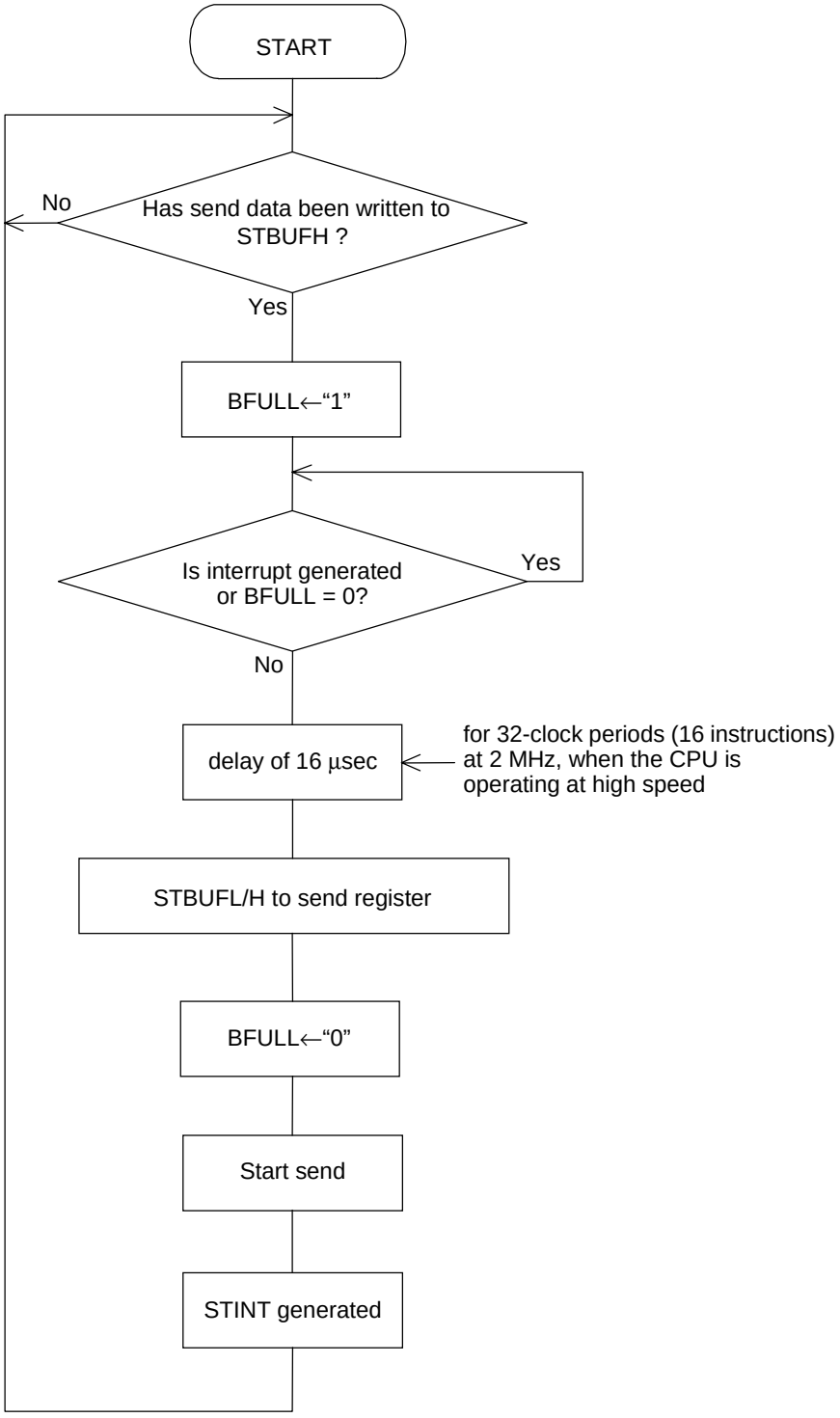
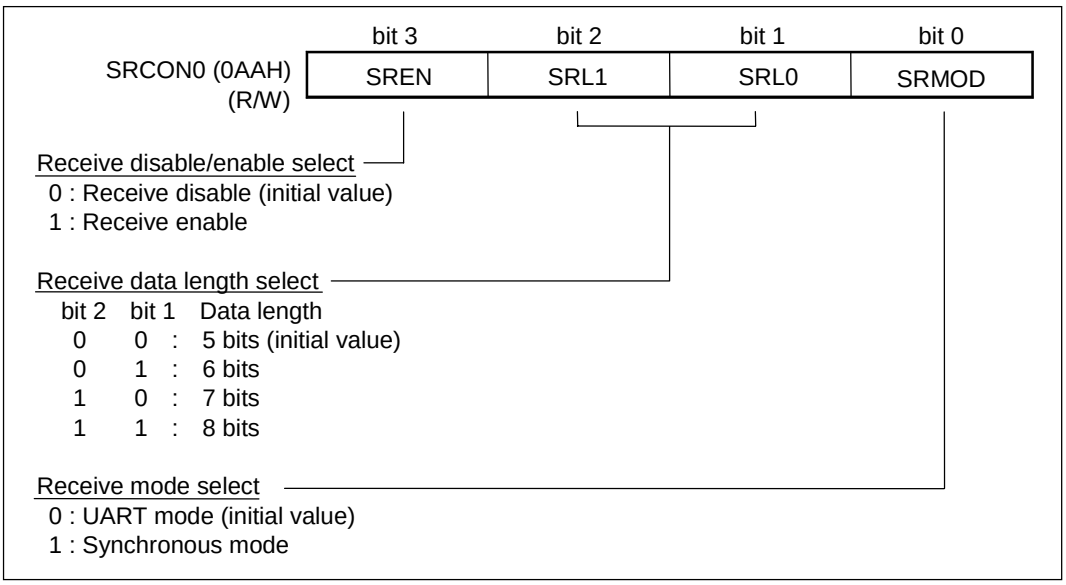


Figure 13-2 Hardware Send Operation Flow

(4) Receive control registers 0/1 (SRCON0, SRCON1)

SRCON0 and SRCON1 are 4-bit special function registers (SFRs) controlling serial port receive operation.

SRCON0 and SRCON1 are initialized to "0" at system reset.



bit 3: SREN (Serial Reception ENable bit)

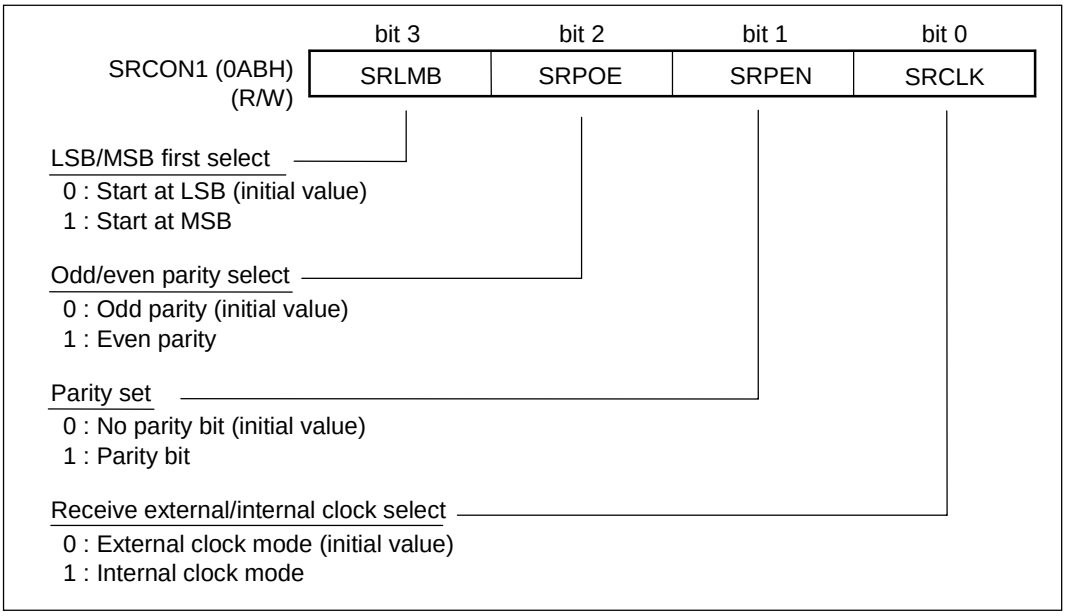
This bit specifies receive operation disable/enable. After receive is enabled in the synchronous mode, this bit is reset to "0" after receiving one frame of data. In the UART mode it does not change.

bit 2, 1: SRL1 (Serial Reception Length select bit 1),
SRL0 (Serial Reception Length select bit 0)

These bits specify the receive data length.

bit 0: SRMOD (Serial Reception MODe bit)

This bit specifies the serial port receive operation mode.



bit 3: SRLMB (Serial Reception Least significant bit first or Most significant Bit first)

This bit specifies either LSB first or MSB first for receive data.

bit 2: SRPOE (Serial Reception Parity Odd or Even number bit)

This bit specifies whether the parity bit is even or odd. Valid only when bit 1 is "1" (parity bit).

bit 1: SRPEN (Serial Reception Parity ENable bit)

This bit specifies whether or not a parity bit is added.

bit 0: SRCLK (Serial Reception CLocK select bit)

This bit specifies the external/internal receive clock for synchronous mode. Valid only when SRMOD (bit 0 of SRCON0) is "1" (synchronous mode).

(5) Receive register

The receive register is the shift register that handles shift operation at receive. It is initialized to 00H at system reset. It cannot be directly accessed by the CPU. When a receive operation is complete, the data read into the receive register is transferred to SRBUFL/H, and at the same time the receive interrupt request signal (SRINT) is generated.

(6) Receive buffer registers (SRBUFL, SRBUFH)

	bit 3	bit 2	bit 1	bit 0
SRBUFL (0A8H) (R)	RB3	RB2	RB1	RB0
SRBUFH (0A9H) (R)	RB7	RB6	RB5	RB4

SRBUFL and SRBUFH are 4-bit special function registers (SFRs) used to hold the received data in serial port reception. SRBUFL and SRBUFH are initialized to "0" at system reset.

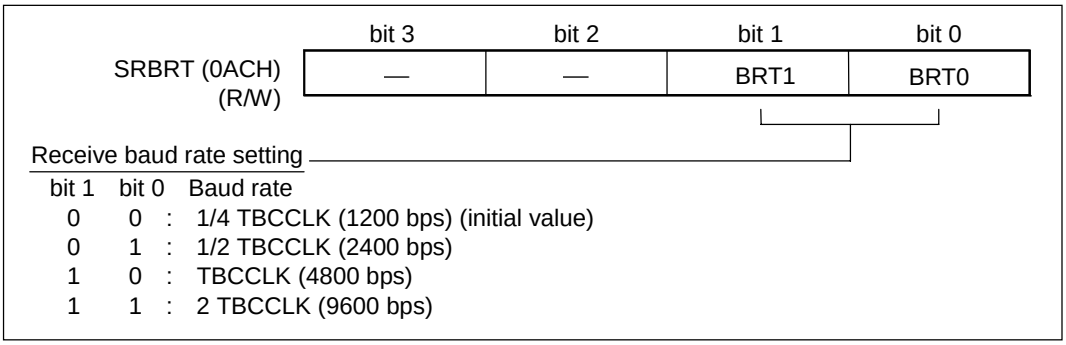
When receive operation is completed the contents of the receive register are sent to SRBUFL/H, and the receive interrupt request (SRINT) is generated. The contents of SRBUFL/H are held until the next receive operation is completed.

If data from a prior receive operation is in SRBUFL/H and new data is received, an overrun error will result. When an overrun error is generated, new received data cannot be loaded into SRBUFL/H.

(7) Receive baud rate setting register (SRBRT)

SRBRT is a 4-bit special function register (SFR) used to set the receive baud rate for serial port receive operation in UART mode.

SRBRT is initialized to 0CH at system reset.



bit 1, 0: BRT1 (Baud RaTe select bit 1), BRT0 (Baud RaTe select bit 0)

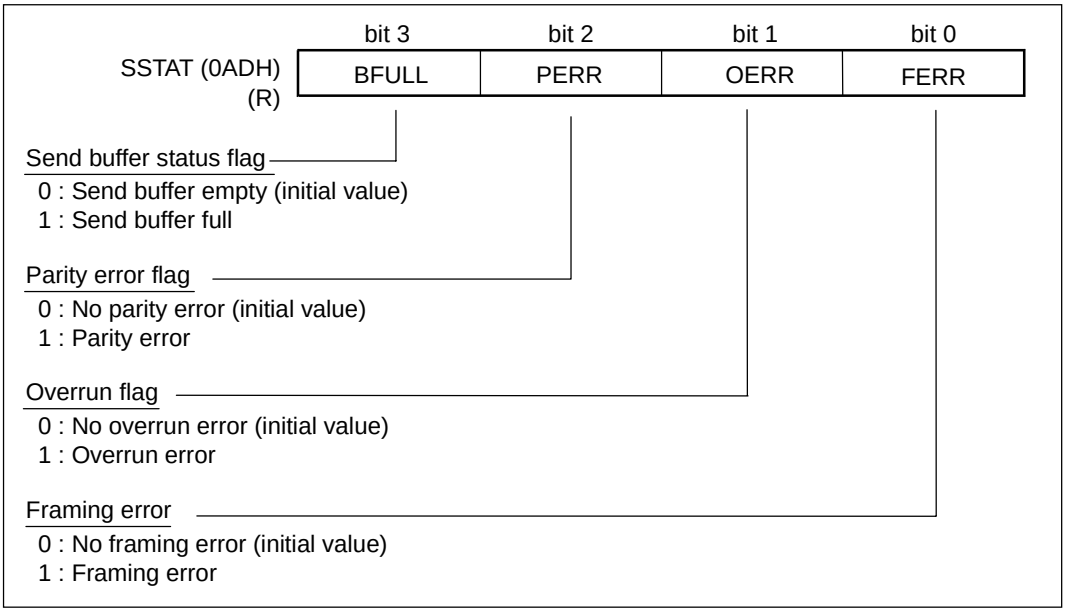
These bits set the receive baud rate.

(8) Serial port status register (SSTAT)

SSTAT is a 4-bit special function register (SFR) used to indicate the status of serial port send/receive.

SSTAT is initialized to "0" at system reset.

SSTAT is a read-only register, and the content is reset every time it is read.



bit 3: BFULL (send Buffer FULL flag)

This bit is enabled in both UART and synchronous modes, and is set to "1" when send data is set to STBUFL/H in the send mode, and reset to "0" when the send data is transferred to the send register.
When BFULL is set to "1" and send data is set (written) to STBUFL/H, the previous data set to those registers is overwritten and lost. Always set data only after verifying that the BFULL flag is "0".

bit 2: PERR (Parity ERRor flag)

This bit is enabled in both UART and synchronous modes, and is set to "1" when the parity for the received data does not match the parity bit attached to the data.

bit 1: OERR (Overrun ERRor flag)

This bit is enabled in both UART and synchronous modes, and is set to "1" when data reception is completed and the data received the previous time has still not been transferred to the CPU. In this case, the new data cannot be transferred to SRBUFL/H.

bit 0: FERR (Framing ERRor flag)

This is only enabled in the UART mode and is set to "1" in the following instances.

(1) when a "1" is detected in start bit sampling
(2) when a "0" is detected in stop bit sampling

In either case a receive interrupt request signal (SRINT) is generated.

13.4 Serial Port Operation Description

13.4.1 Data Format

(1) UART mode

The data format for the UART mode is shown in Figure 13-3.

SRCON0/1 and STCON0/1 can be set to specify a data bit length of 5 to 8 bits. The parity bit can be enabled/disabled. If enabled it can be set to even or odd. Stop bit length can be set to 1 or 2 bits.

The combination of these parameters gives a range of from 7 to 12 bits for send/receive data frames.

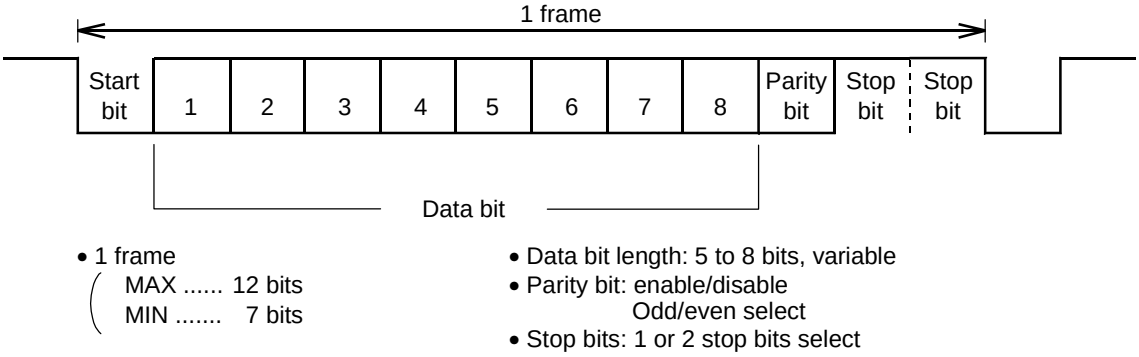


Figure 13-3 UART Mode Data Format

(2) Synchronous mode

The data format for the UART mode is shown in Figure 13-4.

SRCON0/1 and STCON0/1 can be set to specify a data bit length of 5 to 8 bits. The parity bit can be enabled/disabled, and if enabled can be set to even or odd.

The combination of these parameters gives a range of from 5 to 9 bits for send/receive data frames.

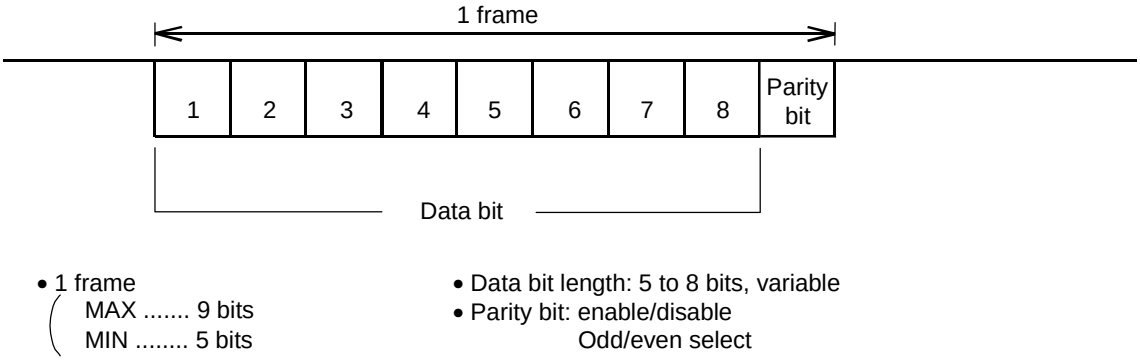


Figure 13-4 Synchronous Mode Data Format

13.4.2 Send Operation Description

The serial port send circuit has a two-stage configuration. This consists of the send register and the send buffer register (STBUFL/H), so it is possible to set send data to STBUFL/H while sending the previous data. When the BFULL flag of the serial port status register (SSTAT) is 1, however, it indicates that STBUFL/H send data has not yet been transferred to the send register. Always verify that the BFULL flag is 0 before transferring data.

(1) UART mode

The UART mode is specified by setting STMOD (bit 0 of STCON0) to "0". Figure 13-5 is the UART mode send timing chart. The UART mode send procedure is described below. The send baud rate is set first, then the timer, and then the send format (data bit length, parity bit, etc.) in STCON0 and STCON1. The TM3INT signal supplied from timers 2 and 3 is the baud rate clock.

① Set send data to STBUFL/H.

② The send data is transferred from STBUFL/H to the send register, and send operation begins. At the same time the serial port send interrupt request (STINT) is generated.

③ Verify that BFULL = "0", then after a delay of 16 μsec, set the next send data to STBUFL/H.

④ When send operation is complete, the send data set to STBUFL/H is transferred to the send register, and send operation begins. At the same time the serial port send interrupt request (STINT) is generated.

Repeat operation ③ the required number of times.

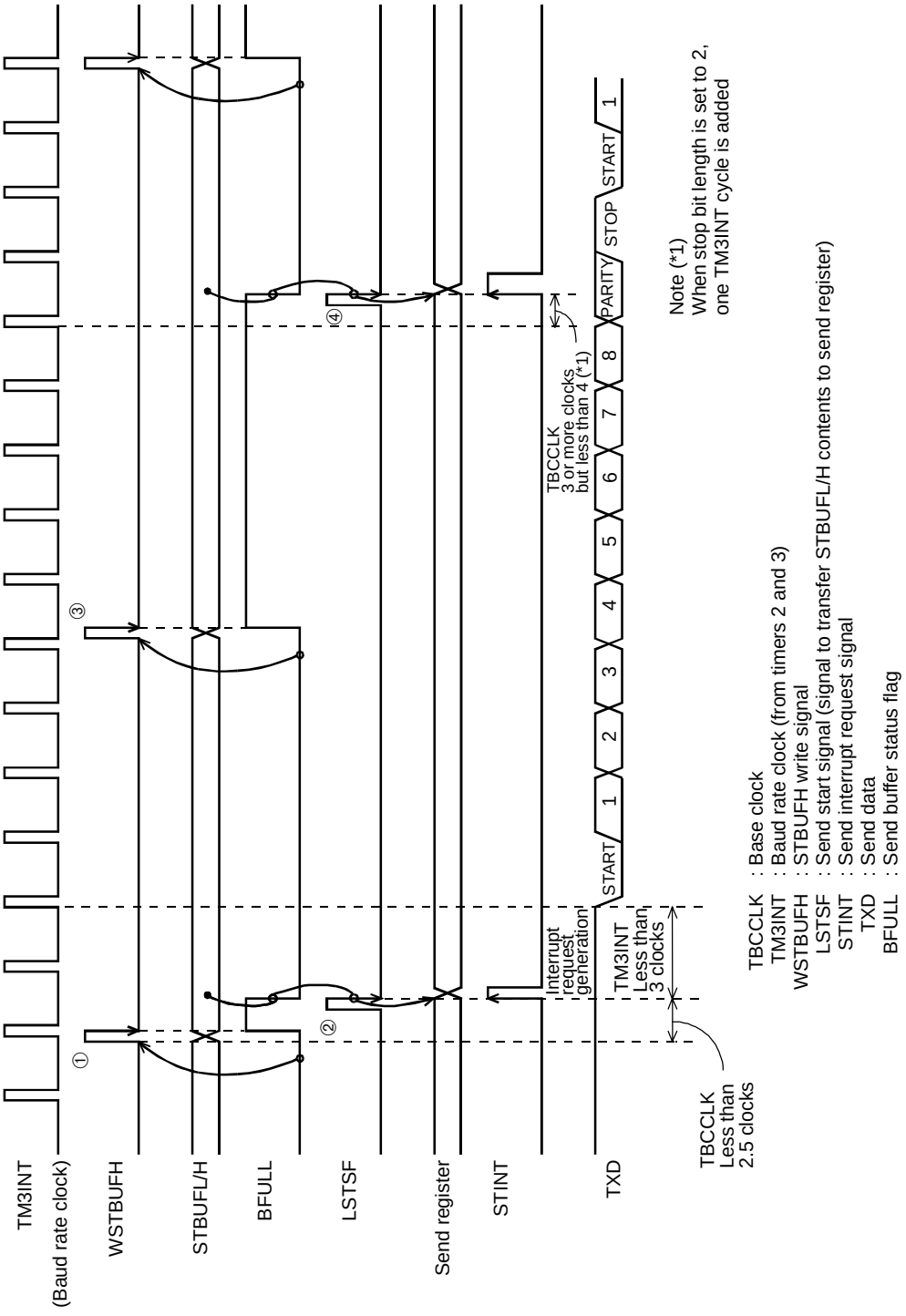


Figure 13-5 UART Mode Send Timing Chart

(for data length 8 bits, 1 stop bit, with parity bit)

(2) Synchronous internal clock mode

The synchronous internal clock mode is selected by setting STMOD (bit 0 of STCON0) to "1", and STCLK (bit 0 of STCON1) to "1".

Figure 13-6 is the send timing chart for the synchronous internal clock mode.

The synchronous internal clock send procedure is described below.

First the send format (data bit length, parity bit, etc.) is set to STCON0 and STCON1.

① Set send data to STBUFL/H.

② The send data is transferred from STBUFL/H to the send register, and send operation begins. At the same time the interrupt request signal (STINT) is generated.

③ Check that BFULL = "0", then set the next send data to STBUFL/H.

④ When the send operation is complete, the send data set to STBUFL/H is transferred to the send register, and the send operation begins. At the same time, the serial port send interrupt signal (STINT) is generated.

Repeat step ③ the required number of times.

In the synchronous internal clock mode the send baud rate is fixed at the crystal oscillation frequency, that is, the frequency (32.768 kHz) of the time base clock (TBCCLK).

After data is set to STBUFH, the send clock (TXCO) is generated between 2 and 3.5 clocks of the TBCCLK source, and a send operation starts.

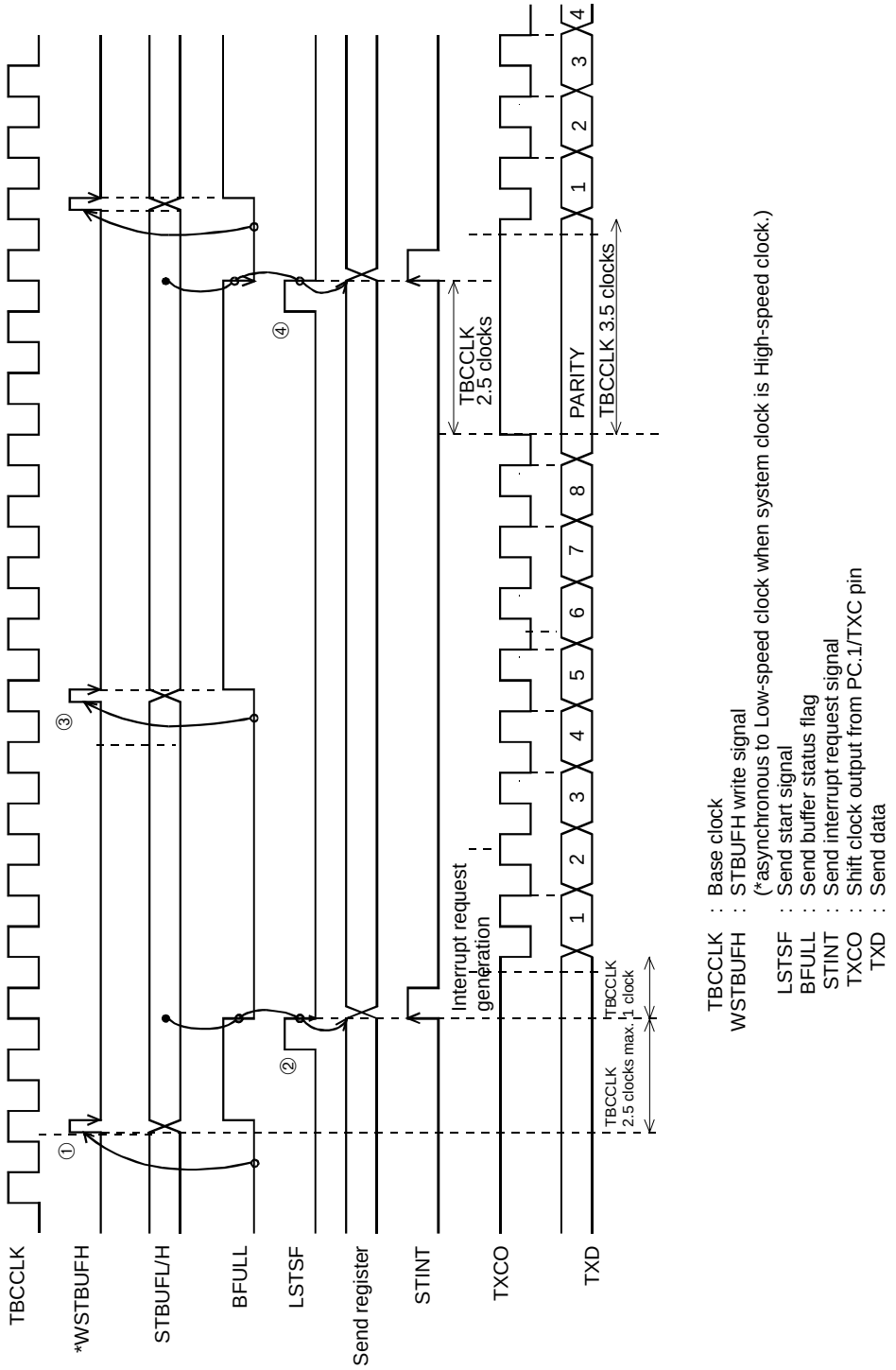


Figure 13-6 Send Timing Chart for Synchronous Internal Clock Mode

(for data length 8 bits, with parity bit)

(3) Synchronous external clock mode

The synchronous external clock mode is selected by setting STMOD (bit 0 of STCON0) to "1", and STCLK (bit 0 of STCON1) to "0".

Figure 13-7 is the send timing chart for the synchronous external clock mode.

The synchronous external clock send procedure is described below.

First set the send format (data bit length, parity bit, etc.) to STCON0 and STCON1.

① Set send data to STBUFL/H.

② The send data is transferred from STBUFL/H to the send register, and at the same time the interrupt request signal (STINT) is generated.

③ Send operation is started by the send shift clock (TXCI).

④ Check that BFULL = "0", then set the next send data to STBUFL/H.

⑤ When the send operation is complete, the send data set to STBUFL/H is transferred to the send register. At the same time, the serial port send interrupt signal (STINT) is generated.

Repeat step ④ the required number of times.

In the synchronous external clock mode the send baud rate is determined by the input shift clock (TXCI).
To send data continuously, keep an interval of at least 3.5 clocks (approx. 107 μs) of TBCCLK for one frame of clocked (TXCI) send data.

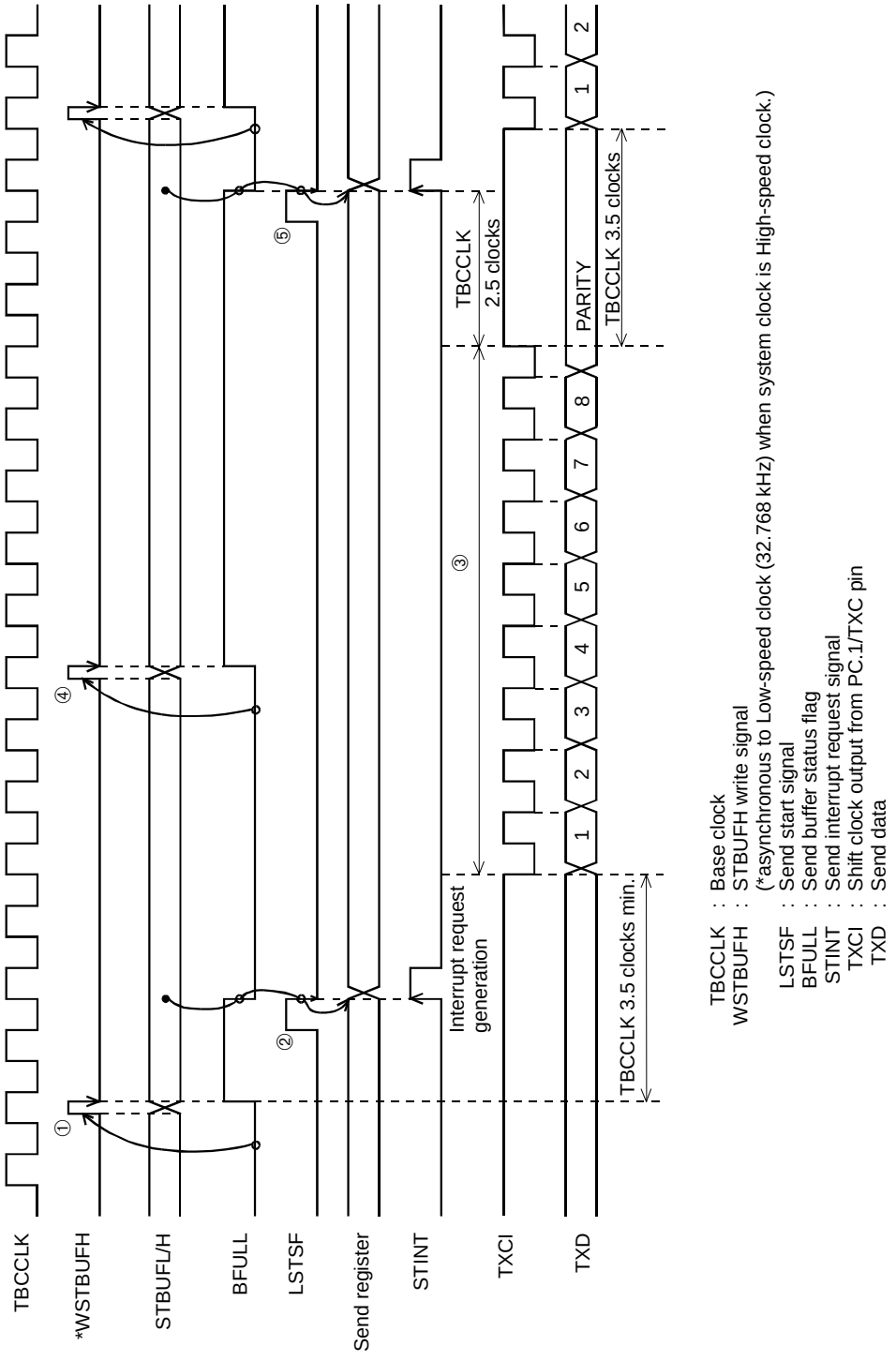


Figure 13-7 Send Timing Chart for Synchronous External Clock Mode

(for data length 8 bits, with parity bit)

13.4.3 Receive Operation Description

(1) UART mode

The UART mode is specified by setting SRMOD (bit 0 of SRCON0) to "0". Figure 13-8 is the UART mode receive timing chart. The UART mode receive procedure is described below.

First set the receive baud rate in the receive baud rate setting register (SRBRT). Supported baud rates for UART mode receive are 1/4 TBCCLK (1200 bps), 1/2 TBCCLK (2400 bps), TBCCLK (4800 bps), and 2 TBCCLK (9600 bps).

Set the receive format (data bit length, parity bit, etc.) in SRCON0 and SRCON1.

① Set SREN (bit 3 of SRCON0) to "1" to enable receive.

② At the negative edge of the receive data (RXD) start bit, receive operation will start.

③ Receive operation ends.

If a framing or overrun error occurs the FERR or OERR flag of the status register (SSTAT) will be set to "1".

④ Received data is transferred to SRBUFL/H.

If a parity error occurs, the PERR flag of the status register (SSTAT) is set to "1".

⑤ The serial port receive interrupt request (SRINT) is generated.

Receive data is received until receive is disabled (SREN = "0"). When receive is ended, reset the receive enable/disable flag (SREN) to "0".

The receive data sampling clock (SRSMPL) is based on the low-speed clock supply, not on the high-speed clock. This allows receive operations to be executed while in the energy-saving mode.

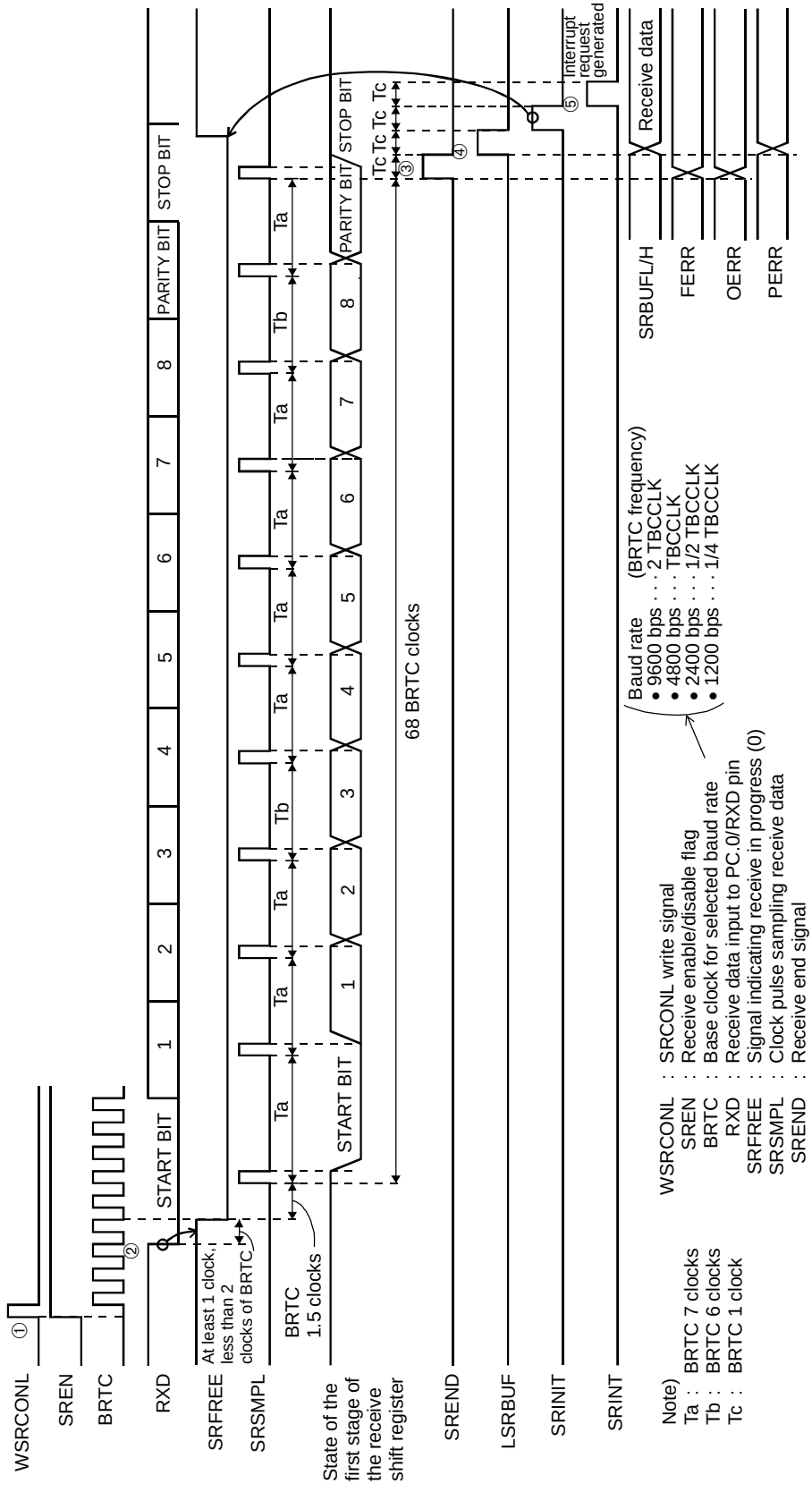


Figure 13-8 UART Mode Receive Timing Chart
(for data length 8 bits, with parity bit)

(2) Synchronous internal clock mode

The synchronous internal clock mode is selected by setting SRMOD (bit 0 of SRCON0) to "1" and SRCLK (bit 0 of SRCON1) to "1".

Figure 13-9 is the receive timing chart for the synchronous internal clock mode.

The synchronous internal clock receive procedure is indicated below.

First set the receive format (data bit length, parity bit, etc.) in SRCON1 and SRCON0.

① Set SREN (bit 3 of SRCON0) to "1" (receive enable).

② 3 to 4 BRTC clock cycles later the receive shift clock (RXCO) is generated, and the receive operation starts.

(The shift clock is supplied from the PC.2/RXC pin.)

③ At the positive edge of RXCO the data received from the PC.0/RXD pin is written to the receive register.

④ Receive operation ends.

If an overrun error occurs the OERR flag in status register (SSTAT) is set to "1".

⑤ Received data is transferred to SRBUFL/H.

If a parity error occurs, the PERR flag of status register (SSTAT) is set to "1".

⑥ The serial port receive interrupt request signal (SRINT) is generated.

⑦ At the negative edge of SRINT, SREN is reset to "0".

Repeat step ① the required number of times. In the synchronous internal clock mode the receive baud rate is fixed to TBCCLK.

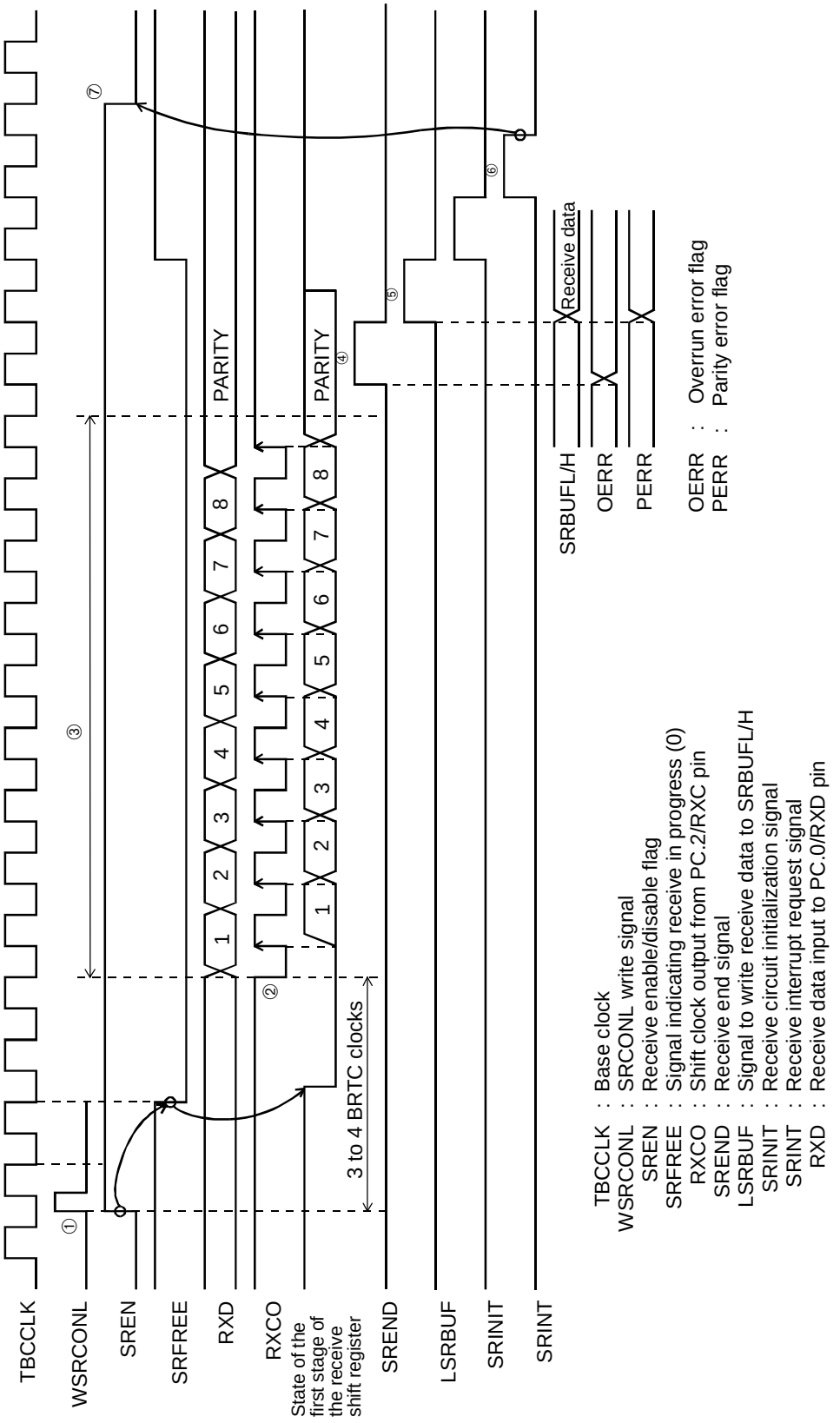


Figure 13-9 Synchronous Internal Clock Mode Receive Timing Chart

(for data length 8 bits, with parity bit)

(3) Synchronous external clock mode

The synchronous external clock mode is selected by setting SRMOD (bit 0 of SRCON0) to "1" and SRCLK (bit 0 of SRCON1) to "0".

Figure 13-10 is the receive timing chart for the synchronous external clock mode.

The synchronous external clock receive procedure is indicated below.

First set the receive format (data bit length, parity bit, etc.) in SRCON1 and SRCON0.

① Set SREN (bit 3 of SRCON0) to "1" (receive enable).

② At the positive edge of the receive shift clock input through PC.2/RXC pin, the receive data from PC.0/RXD pin is written to the receive register.

③ Receive operation ends.

If an overrun error occurs the OERR flag in status register (SSTAT) is set to "1".

④ Received data is transferred to SRBUFL/H.

If a parity error occurs, the PERR flag of status register (SSTAT) is set to "1".

⑤ The serial port receive interrupt request signal (SRINT) is generated.

⑥ At the negative edge of SRINT, SREN is reset to "0".

Repeat step ① the required number of times.

In the synchronous external clock mode the receive baud rate is determined by the external clock (RXCI). Allow at least five clocks (approx. 153 µs) of TBCCLK between the time the receive is enabled (SREN = "1") and the time the external clock (RXCI) is input.

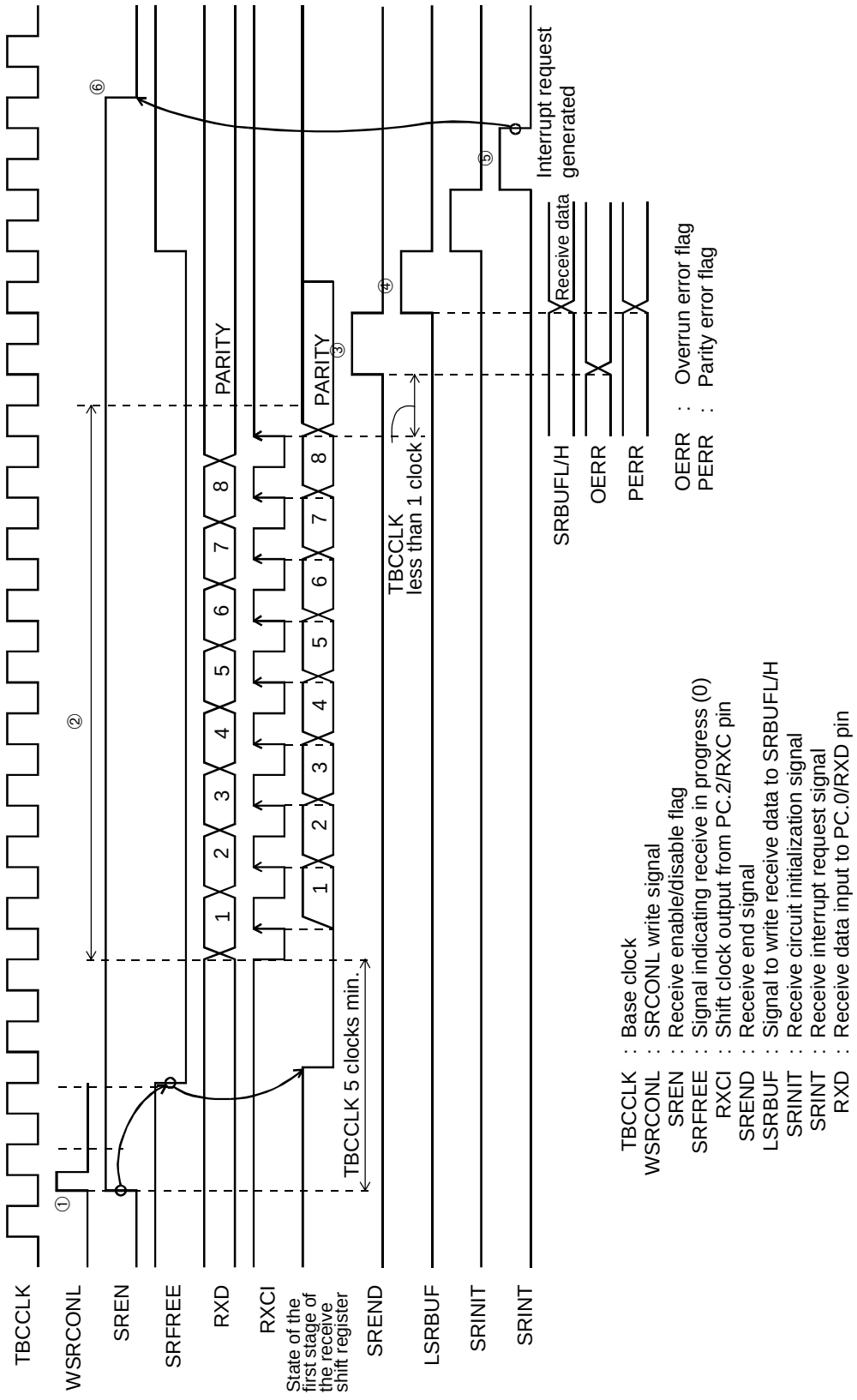


Figure 13-10 Synchronous External Clock Mode Receive Timing Chart

(for data length 8 bits, with parity bit)

13.5 Send/Receive Data LSB/MSB First Select

Either LSB first or MSB first for send can be selected by setting STLMB (bit 3 of STCON1).

Either LSB first or MSB first for receive can be selected by setting SRLMB (bit 3 of SRCON1).

13.5.1 Selecting Send Data LSB/MSB First

Set STLMB (bit 3 of STCON1) to "0" to select LSB first for send.

The correspondence between LSB first send data and the send buffer register bit is shown in Figure 13-11. In this case, the LSB is TB0 (bit 0 of STBUFL).

Set STLMB to "1" to send the MSB first.

The correspondence between MSB first send data and the send buffer register bit is shown in Figure 13-12. In this case, the MSB is TB7 (bit 3 of STBUFH).

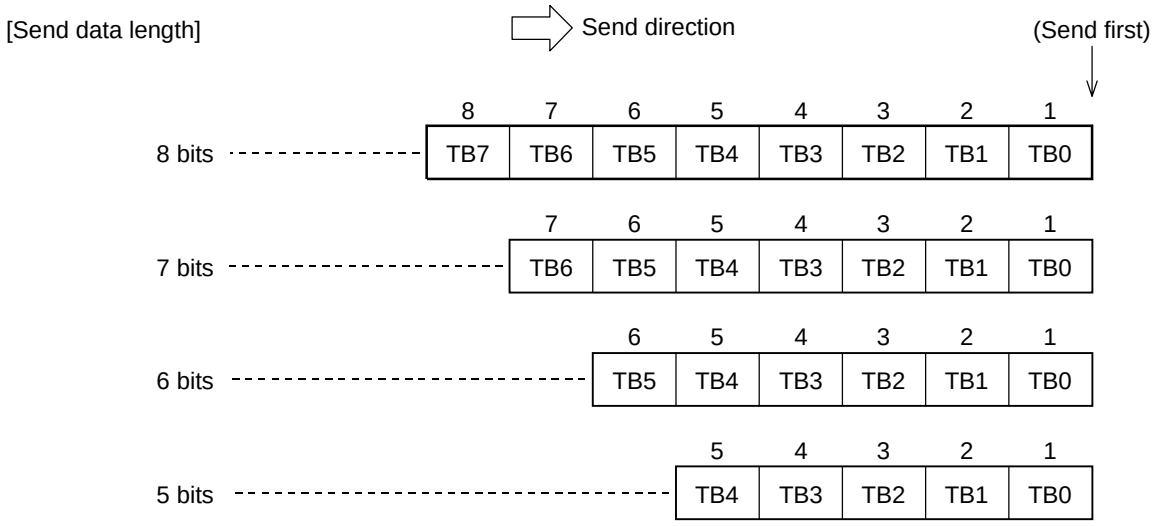


Figure 13-11 Correspondence Between LSB First Send Data and Send Buffer Register

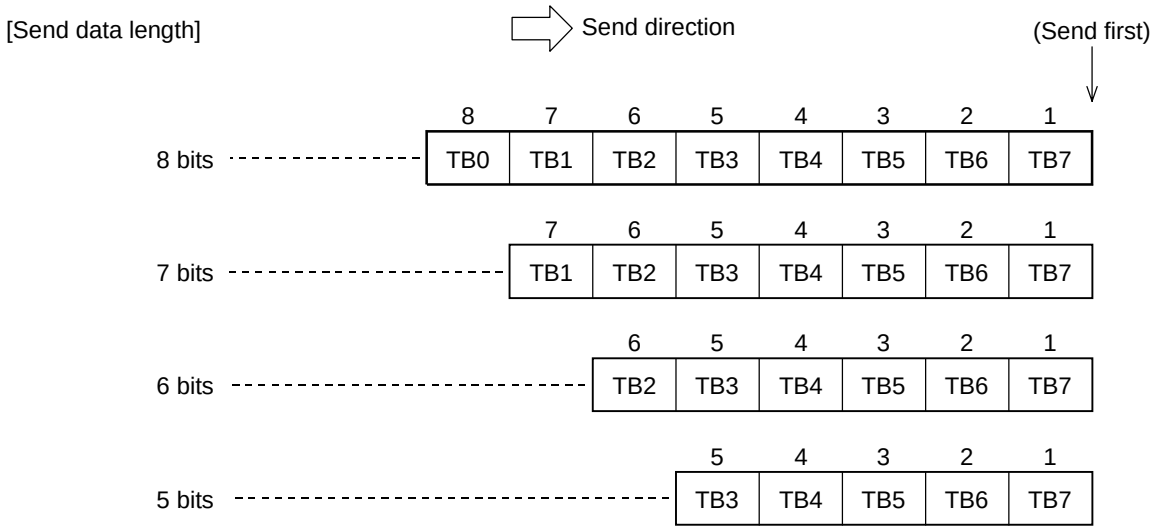


Figure 13-12 Correspondence Between MSB First Send Data and Send Buffer Register

13.5.2 Selecting Receive Data LSB/MSB First

When the LSB is first in receive data, set SRLMB (bit 3 of SRCON1) to "0".

If the MSB is first, set SRLMB to "1".

The correspondence between receive data and SRBUFL/H bits for LSB first receive is shown in Figure 13-13, and for MSB first receive in Figure 13-14.

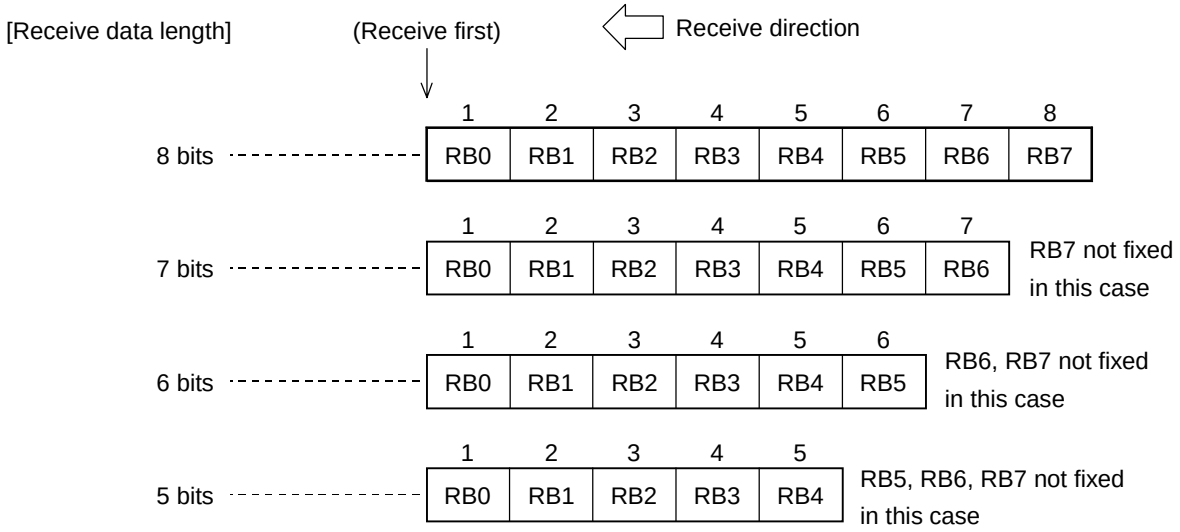


Figure 13-13 Correspondence Between LSB First Receive Data and Receive Buffer Register

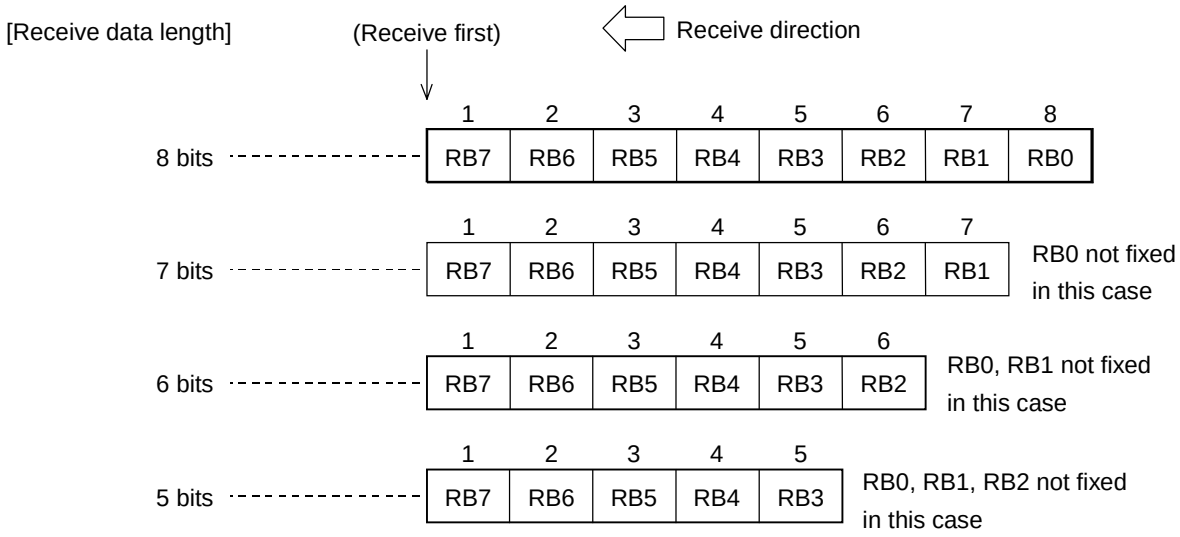


Figure 13-14 Correspondence Between MSB First Receive Data and Receive Buffer Register

Chapter 14

Shift Register (SFT)

14. Shift Register (SFT)

14.1 Overview

The ML63295A has one internal 8-bit shift register channel for clock synchronous communication.

The shift register is synchronized with the clock specified by the shift register control register 0 (SFTCON0), and can perform 8-bit data send and receive simultaneously. When 8-bit data transfer is completed, a shift register interrupt request is generated.

14.2 Shift Register Configuration

The shift register configuration is shown in Figure 14-1.

PE.0/SIN, PE.1/SOUT, and PE.2/SCLK are the shift data input pin, the shift data output pin and the shift clock input/output pin respectively. Set the secondary function by using port mode register.

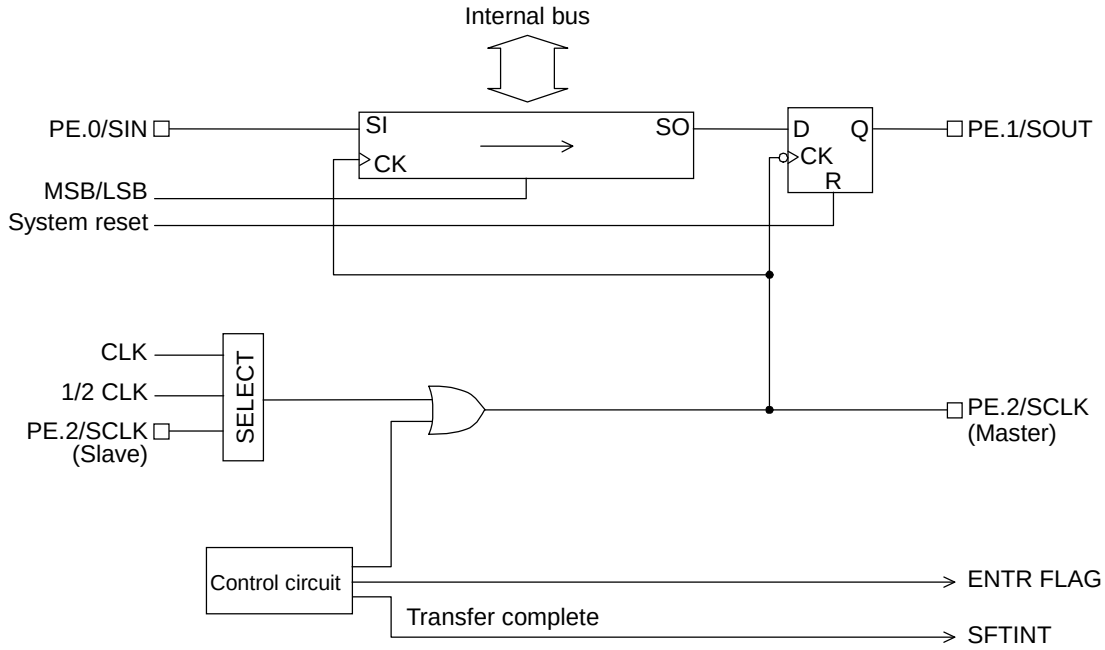


Figure 14-1 Shift Register Configuration

14.3 Shift Registers

(1) Shift registers L/H (SFTRL, SFTRH)

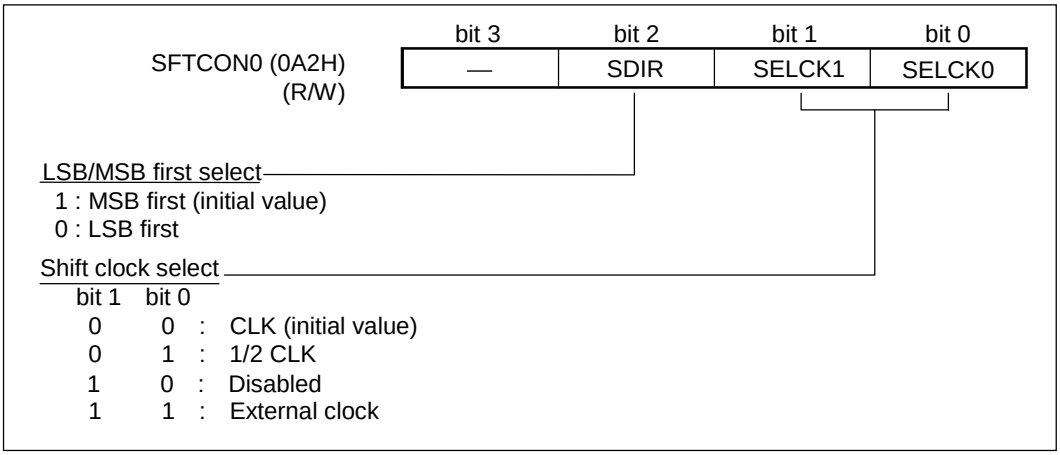
SFTRL and SFTRH are 4-bit special function registers (SFRs) used to write shift register send data and to read receive data.

	bit 3	bit 2	bit 1	bit 0
SFTRL (0A0H) (R/W)	SD3	SD2	SD1	SD0
	bit 3	bit 2	bit 1	bit 0
SFTRH (0A1H) (R/W)	SD7	SD6	SD5	SD4

SFTRL and SFTRH are set to "0" at system reset.

(2) Shift register control registers (SFTCON0, SFTCON1)

SFTCON0 and SFTCON1 are 4-bit special function registers (SFRs) that control shift register operation. At system reset both are initialized to "0".

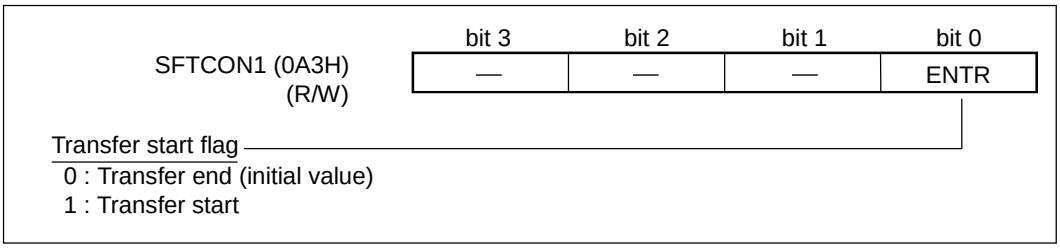


bit 2: SDIR

This bit selects the transfer order for 8-bit send/receive data.
When the SDIR bit is "0" it means MSB first, and when "1", LSB first.

bit 1, 0: SELCK1, SELCK0

These bits select the shift clock.
If set to CLK or 1/2 CLK the system operates in master mode. If set to external clock the system operates in slave mode.



bit 0: ENTR

When ENTR is set to "1", transfer starts, and when 8-bit transfer ends, it is automatically set to "0".

14.4 Shift Register Operation

The shift register can be set to master or slave mode, and to MSB first or LSB first. The send data is written to the shift register (SFTRL, SFTRH), and transfer is started by setting bit 0 (ENTR) of the shift control register 1 (SFTCON1) to "1". After 8-bit data transfer (send/receive), operation ends.

Bits 1 and 0 (SELCK1, SELCK0) of the shift control register 0 (SFTCON0) can set the shift clock to CLK or 1/2 CLK. This operation is master mode and the shift clock is output to the PE.2/SCLK pin.

When the shift clock is set to external clock, the system operates in slave mode, and operation is to the clock input through the PE.2/SCLK pin. If eight or more clocks are input consecutively, the ninth and following clocks are ignored.

In both master and slave modes, the shift register is synchronized to the shift clock falling edge, and shift-out data is output from the first bit through the PE.1/SOUT pin. In synchronization with the shift clock rising edge, shift-in data is input from the first bit through the PE.0/SIN pin.

For external devices, shift-in data changes on the falling edge of the shift clock, and shift-out data changes on the rising edge of the shift clock.

When 8-bit data transfer is complete, bit 0 (ENTR) of SFTCON1 is cleared to "0". When transfer is completed, the interrupt request signal (SFTINT) is generated (see Figure 14-2).

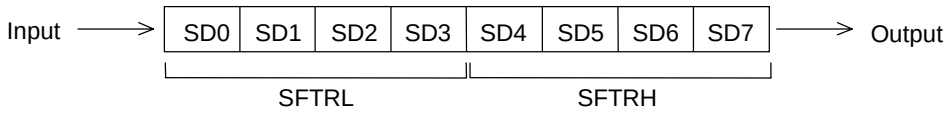
The output pin state at system reset and between transfers (from the end of one 8-bit transfer until the next transfer starts) is shown in Table 14-1 (when set to the output secondary function).

Table 14-1 Output Pin States

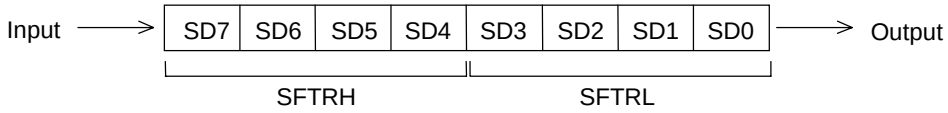
Pin name	At system reset	Between transfers
PE.2/SCLK	"H"	"H"
PE.1/SOUT	"L"	Last transfer data of transfer

MSB/LSB first is set to bit 2 (SDIR) of SFTCON0.

- SDIR = 0: MSB first mode



- SDIR = 1: LSB first mode



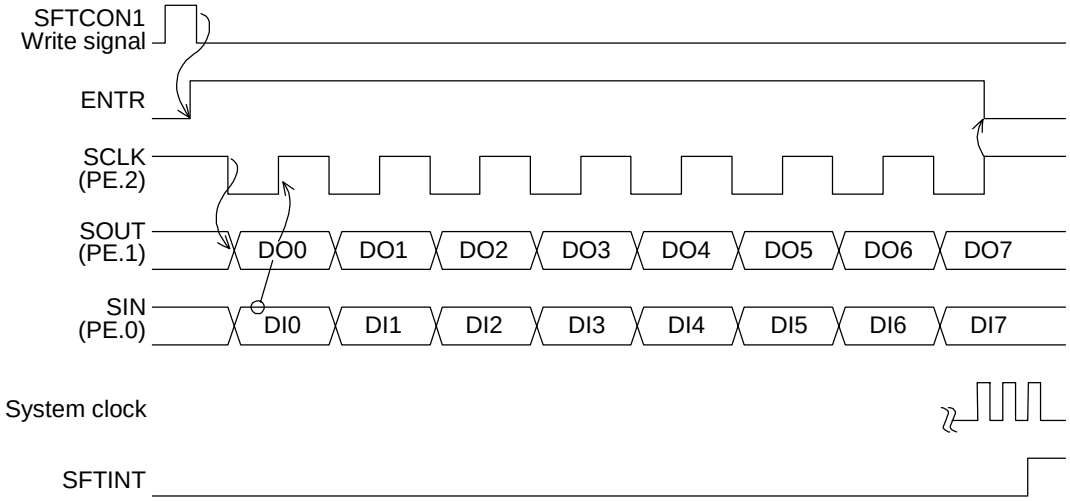


Figure 14-2 Shift Register Operation Timing

Note:

Setting the ENTR bit to "1" in the slave mode should be done when the PE.2/SCLK pin is high.

If SFTRL/SFTRH are written during transfer, the transfer data (send and receive) is destroyed. In this case, terminate the transfer and start over again.

Even when receiving only, transfer begins with setting the ENTR bit to "1".

14.5 Shift Register Application Example

An example of register setting for clock synchronous communication using shift register is described below.

(1) Set the supported port modes (secondary function).

Port control register	Master mode	
PEMOD	Bit 2 = "1"	(PE.2/SCLK)
	Bit 1 = "1"	(PE.1/SOUT)
	Bit 0 = "1"	(PE.0/SIN)

(2) Select the shift clock with SELCK1 and SELCK0 (SFTCON0 bits 1 and 0)(master/slave mode select).

(3) Select MSB first/LSB first with SDIR (SFTCON0 bit 2). ("0" for MSB first, and "1" for LSB first).

(4) Set ESFT (IE3 bit 2) to "1" and enable the shift register interrupt.

(5) Set the MIE (master interrupt enable flag) to "1", and enable all interrupts.

(6) Write send data to SFTRL and SFTRH.

(7) Set ENTR (bit 0 of SFTCON1) to "1", and start the transfer.

With the above settings the shift register begins to operate, and the CPU receives the shift register interrupt.

Whether 8-bit transfer has been completed can be checked by monitoring QSFT (bit 2 of IRQ3) or ENTR (bit 0 of SFTCON1).

Chapter 15

LCD Driver (LCD)

15. LCD Driver (LCD)

15.1 Overview

The ML63295A has an internal dot matrix LCD driver. It also has 96 segment outputs and can drive up to 3072 (96 seg. × 32 com.) dots. The LCD driver can be software-selected to all OFF, all ON or power down mode, 1/5 or 1/6 bias. In addition, by software, duty from 1/2 to 1/32 can be selected and display contrast of 16 tones can be controlled.

15.2 LCD Driver Configuration

The LCD driver configuration is shown in Figure 15-1.

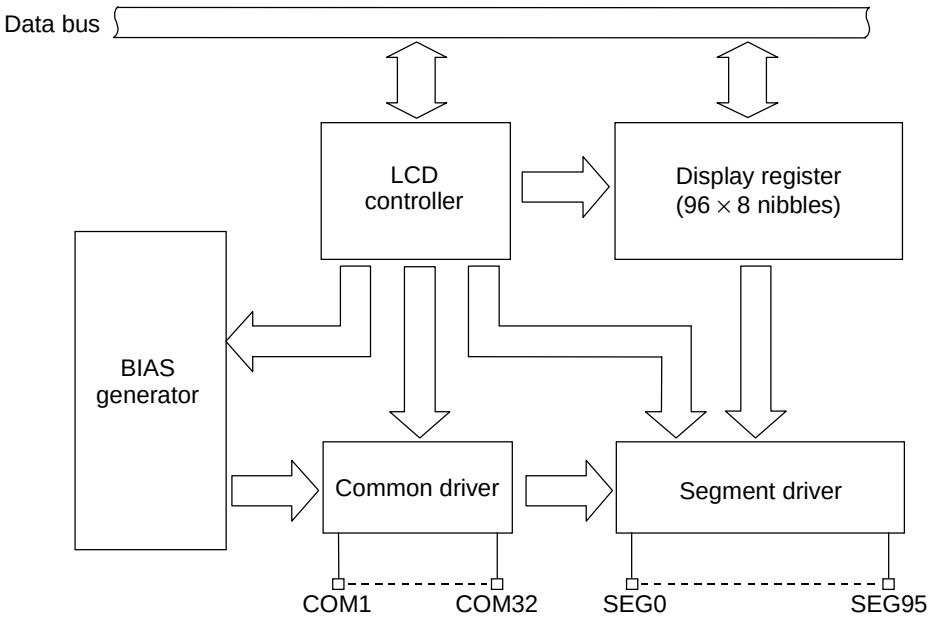
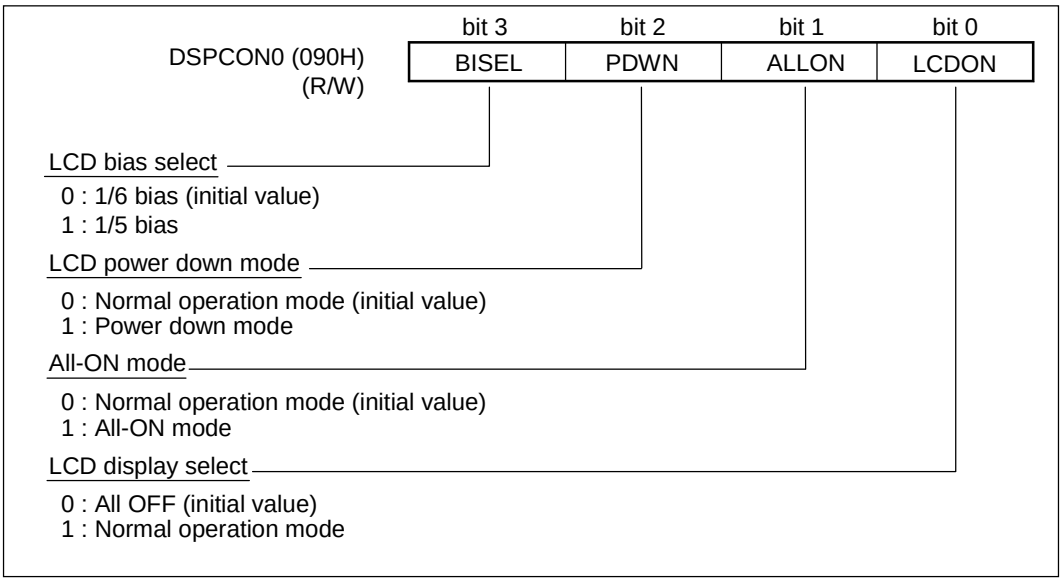


Figure 15-1 LCD Driver Configuration

15.3 LCD Driver Registers

(1) Display control register 0 (DSPCON0)

DSPCON0 is a 4-bit special function register (SFR) controlling LCD driver operation.



bit 3: BISEL

This bit selects 1/6 or 1/5 bias.
At system reset it is "0", selecting 1/6 bias.

bit 2: PDWN

This bit selects the LCD power down mode. When PDWN is set to "1", the bias generation circuit stops its voltage boosting operation and pins COM1–32 and SEG0–95 are all set to the V_{SS} level, reducing supply current. At system reset it is cleared to "0".

bit 1: ALLON

When ALLON is set to "1" all segment drivers are turned on. The ALLON bit has priority over the LCDON bit. At system reset it is cleared to "0".

bit 0: LCDON

When the LCDON bit is set to "1", the display data in the display register is output to the segment drivers. At system reset it is cleared to "0", and all segment drivers are turned off.

(2) Display control register 1 (DSPCON1)

DSPCON1 is a 4-bit special function register (SFR) used to select the LCD driver duty.

At system reset, each bit of DSPCON1 is initialized to "0".

DSPCON1 (091H) (R/W)

bit 3	bit 2	bit 1	bit 0
DT3	DT2	DT1	DT0

Duty select

bit 3	bit 2	bit 1	bit 0		
0	0	0	0	:	1/32 duty (initial value)
0	0	0	1	:	1/2 duty
0	0	1	0	:	1/4 duty
0	0	1	1	:	1/6 duty
0	1	0	0	:	1/8 duty
0	1	0	1	:	1/10 duty
0	1	1	0	:	1/12 duty
0	1	1	1	:	1/14 duty
1	0	0	0	:	1/16 duty
1	0	0	1	:	1/18 duty
1	0	1	0	:	1/20 duty
1	0	1	1	:	1/22 duty
1	1	0	0	:	1/24 duty
1	1	0	1	:	1/26 duty
1	1	1	0	:	1/28 duty
1	1	1	1	:	1/30 duty

(3) Display contrast register (DSPCNT)

DSPCNT is a 4-bit special function register (SFR) used to control display contrast.

At system reset, each bit of DSPCON1 is initialized to "0".

DSPCNT (092H) (R/W)

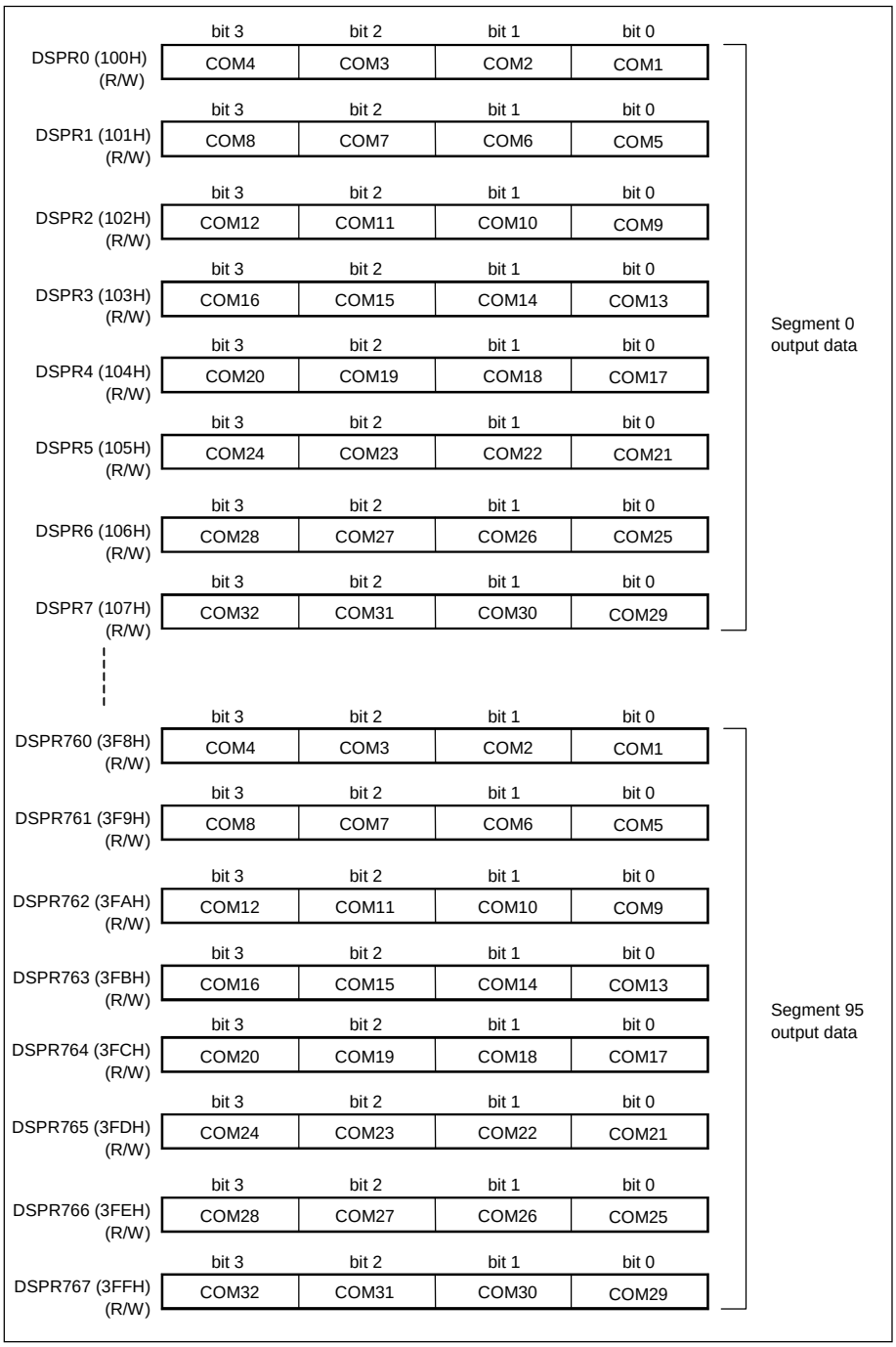
bit 3	bit 2	bit 1	bit 0
CN3	CN2	CN1	CN0

Contrast select

bit 3	bit 2	bit 1	bit 0		
0	0	0	0	:	Light (initial value)
0	0	0	1	:	
0	0	1	0	:	
0	0	1	1	:	
0	1	0	0	:	
0	1	0	1	:	
0	1	1	0	:	
0	1	1	1	:	
1	0	0	0	:	
1	0	0	1	:	
1	0	1	0	:	
1	0	1	1	:	
1	1	0	0	:	
1	1	0	1	:	
1	1	1	0	:	
1	1	1	1	:	Dark

(4) Display registers (DSPR0 to DSPR767)

DSPR0 to DSPR767 are segment output data registers for the dot matrix LCD driver allocated to RAM BANKS 1 to 3. The correspondence between display registers and segment outputs is shown below.



Note:

- When a display register bit is set to "1", the corresponding LCD dot lights. When reset to "0" it goes off.
- To keep stable display state, each individual LCD dot should be set to ON/OFF with bit operation instructions.
- At system reset the display registers (DSPR0 to DSPR767) are undefined and should be initialized.

15.4 LCD Driver Operation

The display duty is selected from 1/2 to 1/32 using DSPCON1. The frame frequency for each duty ratio is indicated in Table 15-1. Depending on the duty selected, the common signal (COM1 to COM32) is generated, and data written in synchronization with that common signal to the display registers (DSPR0 to DSPR767) is output to the segment driver. The segment driver uses bits 0 and 1 (ALLON, LCDON) of the display control register 0 (DSPCON0) to control all OFF and all ON modes.

When PDWN (bit 2 of DSPCON0) is set to "1", the LCD power down mode is enabled. In the LCD power-down mode the bias generation circuit operation stops, and the COM1–32 and SEG0–95 pins are all output at the V_{SS} level to reduce supply current.

BISEL (bit3 of DSPCON0) selects 1/6 or 1/5 bias.

DSPCNT controls the LCD contrast of 16 tones.

Table 15-1 Frame Frequency for Each Duty

DSPCON1					Duty	Frame frequency
DT3–0	DT3	DT2	DT1	DT0		
0H	0	0	0	0	1/32	64 Hz
1H	0	0	0	1	1/2	1024 Hz
2H	0	0	1	0	1/4	512 Hz
3H	0	0	1	1	1/6	approx. 341 Hz
4H	0	1	0	0	1/8	256 Hz
5H	0	1	0	1	1/10	approx. 205 Hz
6H	0	1	1	0	1/12	approx. 171 Hz
7H	0	1	1	1	1/14	approx. 146 Hz
8H	1	0	0	0	1/16	128 Hz
9H	1	0	0	1	1/18	approx. 114 Hz
0AH	1	0	1	0	1/20	approx. 102 Hz
0BH	1	0	1	1	1/22	approx. 93 Hz
0CH	1	1	0	0	1/24	approx. 85 Hz
0DH	1	1	0	1	1/26	approx. 79 Hz
0EH	1	1	1	0	1/28	approx. 73 Hz
0FH	1	1	1	1	1/30	approx. 68 Hz

Note:

When the LCD driver is not used, select the power-down mode and set all the bits of the display control register (DSPCNT) to "0" to save the supply current.

15.5 Bias Generator (BIAS)

The bias generator boosts a voltage (V_{DDE}) generated by the voltage regulator circuit up to a bias reference voltage by external capacitors connected to pins C1, C2, V_{DDX2}, and V_{DDX3}. The resistor ladder circuit divides the bias voltages V_{DD1} to V_{DD6} for an LCD driver.

In the LCD power-down mode, the bias reference voltage generation circuit stops boosting to suppress supply current.

Tables 15-2 and 15-3 list display contrast control voltages.

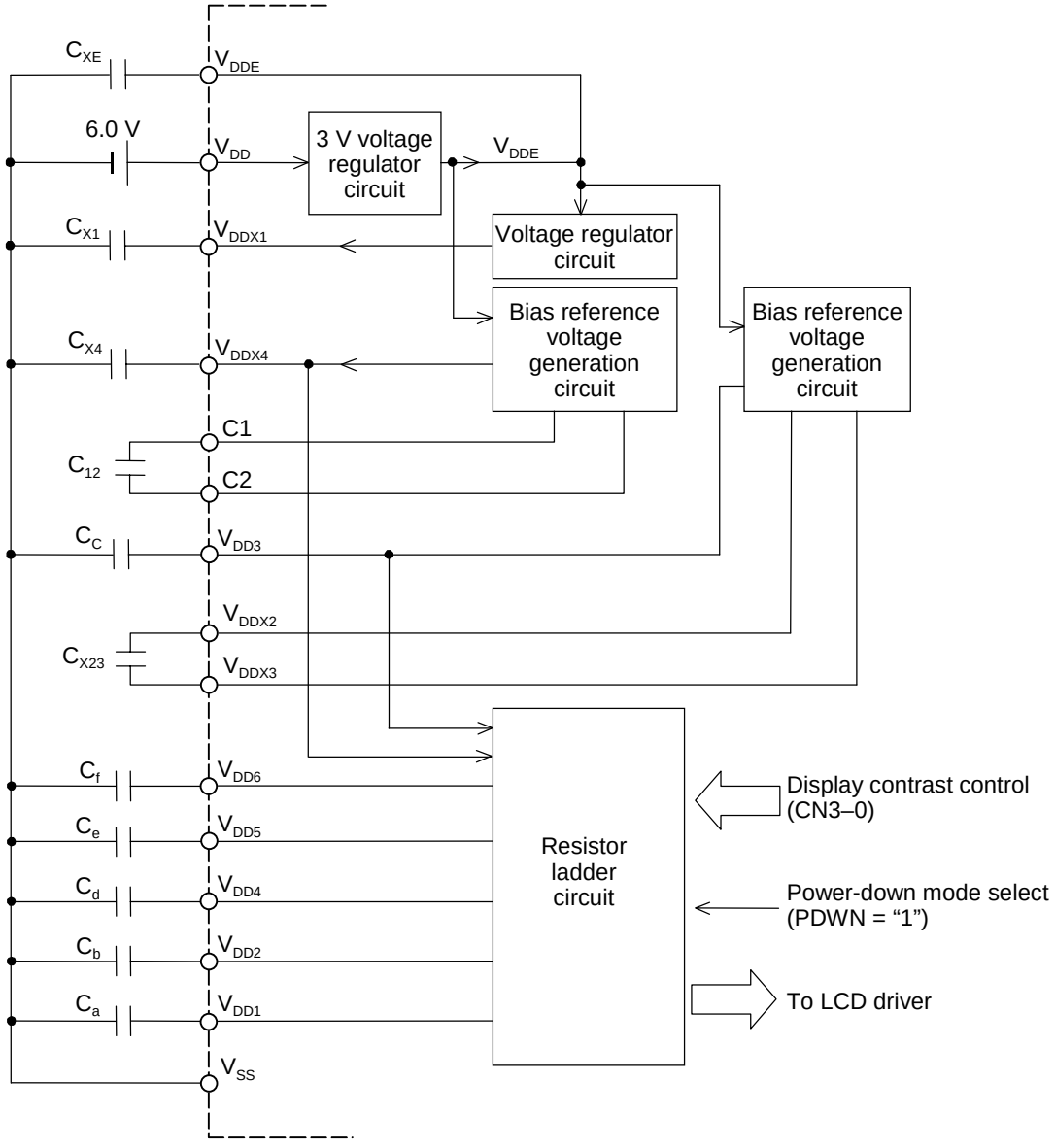


Figure 15-2 Bias Generator Circuit Configuration for 1/6 Bias (Power Supply Voltage = 6 V)

Table 15-2 Display Contrast Control Voltages (V_{DD6}) for 1/6 and 1/5 Biases

• Contrast control voltage (V_{DD6} voltage)

Ta = 25°C, V_{DD6} = 4.1 V (Typ.)

DSPCNT					V_{DD6} Voltage (V)			Display Contrast
CN0 to CN3	CN3	CN2	CN1	CN0	Min.	Typ.	Max.	
0H	0	0	0	0	—	4.1	—	Light
1H	0	0	0	1	Typ. – 0.1	4.2	Typ. + 0.1	
2H	0	0	1	0	Typ. – 0.1	4.3	Typ. + 0.1	
3H	0	0	1	1	Typ. – 0.1	4.4	Typ. + 0.1	
4H	0	1	0	0	Typ. – 0.1	4.5	Typ. + 0.1	
5H	0	1	0	1	Typ. – 0.1	4.62	Typ. + 0.1	
6H	0	1	1	0	Typ. – 0.1	4.74	Typ. + 0.1	
7H	0	1	1	1	Typ. – 0.1	4.86	Typ. + 0.1	
8H	1	0	0	0	Typ. – 0.1	5.00	Typ. + 0.1	
9H	1	0	0	1	Typ. – 0.1	5.14	Typ. + 0.1	
0AH	1	0	1	0	Typ. – 0.1	5.29	Typ. + 0.1	
0BH	1	0	1	1	Typ. – 0.1	5.44	Typ. + 0.1	
0CH	1	1	0	0	Typ. – 0.1	5.60	Typ. + 0.1	
0DH	1	1	0	1	Typ. – 0.1	5.77	Typ. + 0.1	
0EH	1	1	1	0	Typ. – 0.1	5.95	Typ. + 0.1	
0FH	1	1	1	1	Typ. – 0.1	6.14	Typ. + 0.1	Dark

Ta = 25°C, V_{DD6} = 4.0 V (Min.)

DSPCNT					V_{DD6} Voltage (V)			Display Contrast
CN0 to CN3	CN3	CN2	CN1	CN0	Min.	Typ.	Max.	
0H	0	0	0	0	—	4.0	—	Light
1H	0	0	0	1	Typ. – 0.1	4.1	Typ. + 0.1	
2H	0	0	1	0	Typ. – 0.1	4.2	Typ. + 0.1	
3H	0	0	1	1	Typ. – 0.1	4.3	Typ. + 0.1	
4H	0	1	0	0	Typ. – 0.1	4.4	Typ. + 0.1	
5H	0	1	0	1	Typ. – 0.1	4.52	Typ. + 0.1	
6H	0	1	1	0	Typ. – 0.1	4.64	Typ. + 0.1	
7H	0	1	1	1	Typ. – 0.1	4.76	Typ. + 0.1	
8H	1	0	0	0	Typ. – 0.1	4.90	Typ. + 0.1	
9H	1	0	0	1	Typ. – 0.1	5.04	Typ. + 0.1	
0AH	1	0	1	0	Typ. – 0.1	5.19	Typ. + 0.1	
0BH	1	0	1	1	Typ. – 0.1	5.34	Typ. + 0.1	
0CH	1	1	0	0	Typ. – 0.1	5.50	Typ. + 0.1	
0DH	1	1	0	1	Typ. – 0.1	5.67	Typ. + 0.1	
0EH	1	1	1	0	Typ. – 0.1	5.85	Typ. + 0.1	
0FH	1	1	1	1	Typ. – 0.1	6.04	Typ. + 0.1	Dark

• Contrast control voltage (V_{DD6} voltage)

Ta = 25°C, V_{DD6} = 4.2 V (Max.)

DSPCNT					V_{DD6} Voltage (V)			Display Contrast
CN0 to CN3	CN3	CN2	CN1	CN0	Min.	Typ.	Max.	
0H	0	0	0	0	—	4.2	—	Light
1H	0	0	0	1	Typ. – 0.1	4.3	Typ. + 0.1	
2H	0	0	1	0	Typ. – 0.1	4.4	Typ. + 0.1	
3H	0	0	1	1	Typ. – 0.1	4.5	Typ. + 0.1	
4H	0	1	0	0	Typ. – 0.1	4.6	Typ. + 0.1	
5H	0	1	0	1	Typ. – 0.1	4.72	Typ. + 0.1	
6H	0	1	1	0	Typ. – 0.1	4.84	Typ. + 0.1	
7H	0	1	1	1	Typ. – 0.1	4.96	Typ. + 0.1	
8H	1	0	0	0	Typ. – 0.1	5.10	Typ. + 0.1	
9H	1	0	0	1	Typ. – 0.1	5.24	Typ. + 0.1	
0AH	1	0	1	0	Typ. – 0.1	5.39	Typ. + 0.1	
0BH	1	0	1	1	Typ. – 0.1	5.54	Typ. + 0.1	
0CH	1	1	0	0	Typ. – 0.1	5.70	Typ. + 0.1	
0DH	1	1	0	1	Typ. – 0.1	5.87	Typ. + 0.1	
0EH	1	1	1	0	Typ. – 0.1	6.05	Typ. + 0.1	
0FH	1	1	1	1	Typ. – 0.1	6.24	Typ. + 0.1	Dark

Table 15-3 Display Contrast Control Voltages (V_{DD1}, V_{DD2}, V_{DD4}, V_{DD5})

(Ta = 25°C, V_{SS} = 0 V)

BISEL	Mode	Power Supply	Voltage (V)		
			Min.	Typ.	Max.
0	1/6 bias	V_{DD1}	Typ. – 0.1	$1/6 \times V_{DD6}$	Typ. + 0.1
		V_{DD2}	Typ. – 0.1	$2/6 \times V_{DD6}$	Typ. + 0.1
		V_{DD4}	Typ. – 0.1	$4/6 \times V_{DD6}$	Typ. + 0.1
		V_{DD5}	Typ. – 0.1	$5/6 \times V_{DD6}$	Typ. + 0.1
1	1/5 bias	V_{DD1}	Typ. – 0.1	$1/5 \times V_{DD6}$	Typ. + 0.1
		V_{DD2}	Typ. – 0.1	$2/5 \times V_{DD6}$	Typ. + 0.1
		V_{DD4}	Typ. – 0.1	$3/5 \times V_{DD6}$	Typ. + 0.1
		V_{DD5}	Typ. – 0.1	$4/5 \times V_{DD6}$	Typ. + 0.1

15.6 LCD Driver Output Waveform

Figures 15-4 (a) and 15-4 (c) show the output waveforms for 1/32 duty and 1/6 bias, and Figures 15-5 (a) and 15-5 (c) show the output waveforms for 1/16 duty and 1/5 bias.

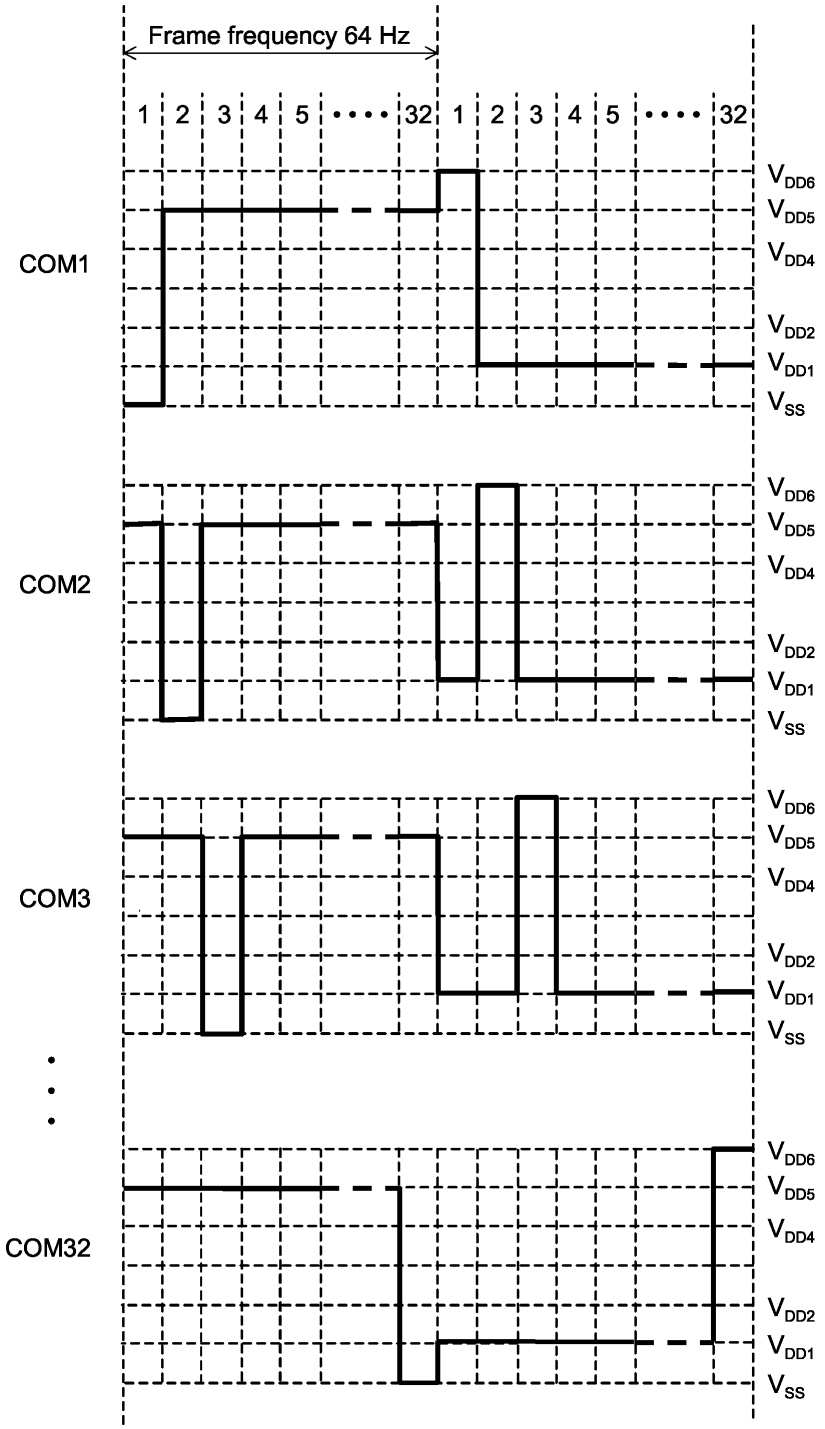


Figure 15-4 (a) 1/32 Duty, 1/6 Bias Common Output Waveform

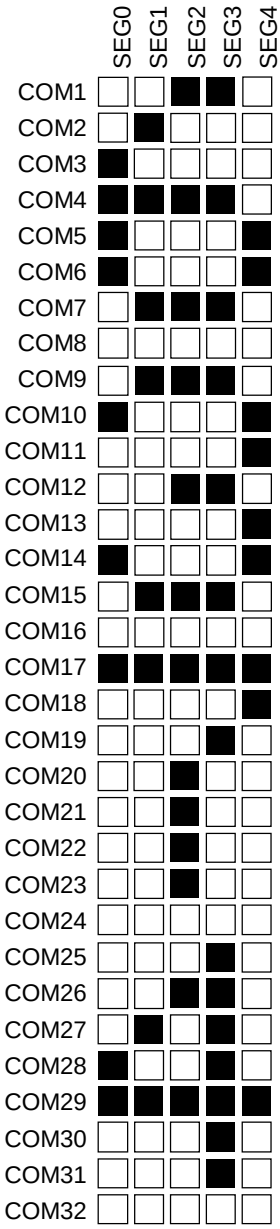


Figure 15-4 (b) 1/32 Duty, 1/6 Bias Dot Display Example

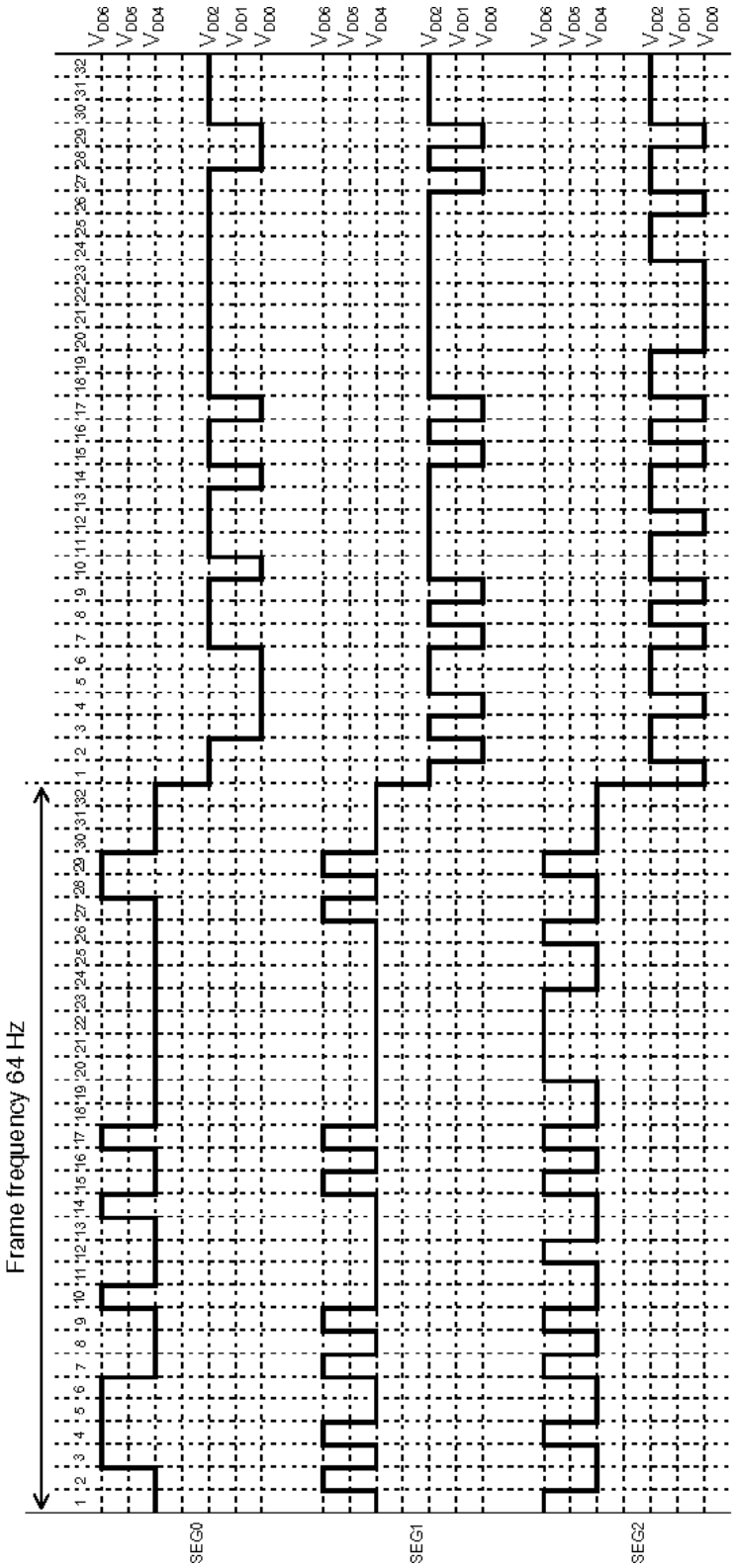


Figure 15-4 (c) 1/32 Duty, 1/6 Bias Segment Output Waveform

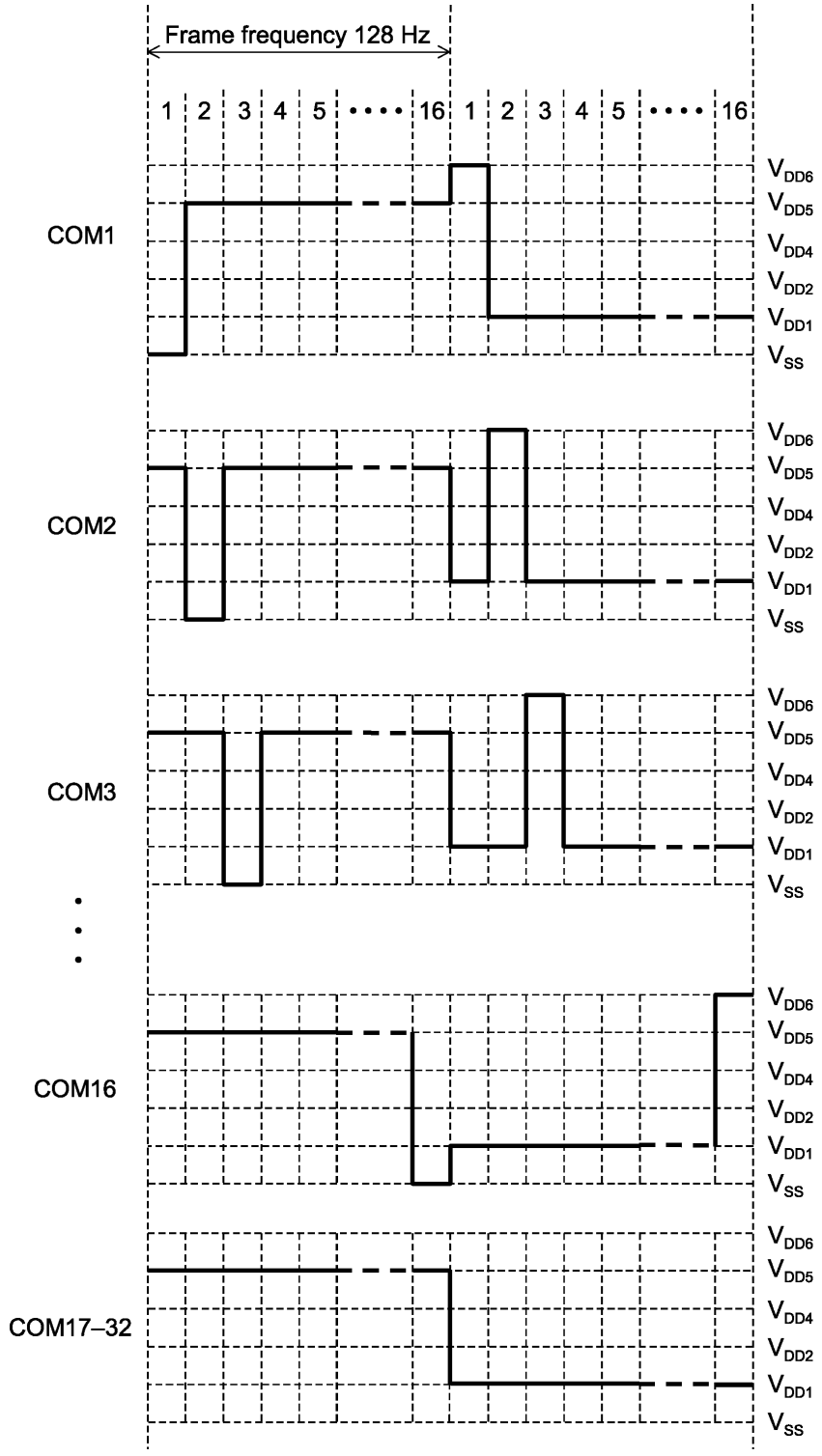


Figure 15-5 (a) 1/16 Duty, 1/5 Bias Common Output Waveform

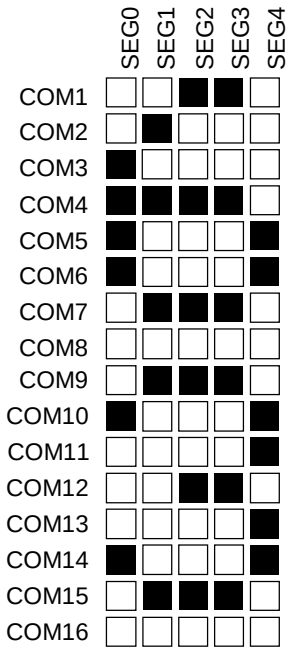


Figure 15-5 (b) 1/16 Duty, 1/5 Bias Dot Display Example

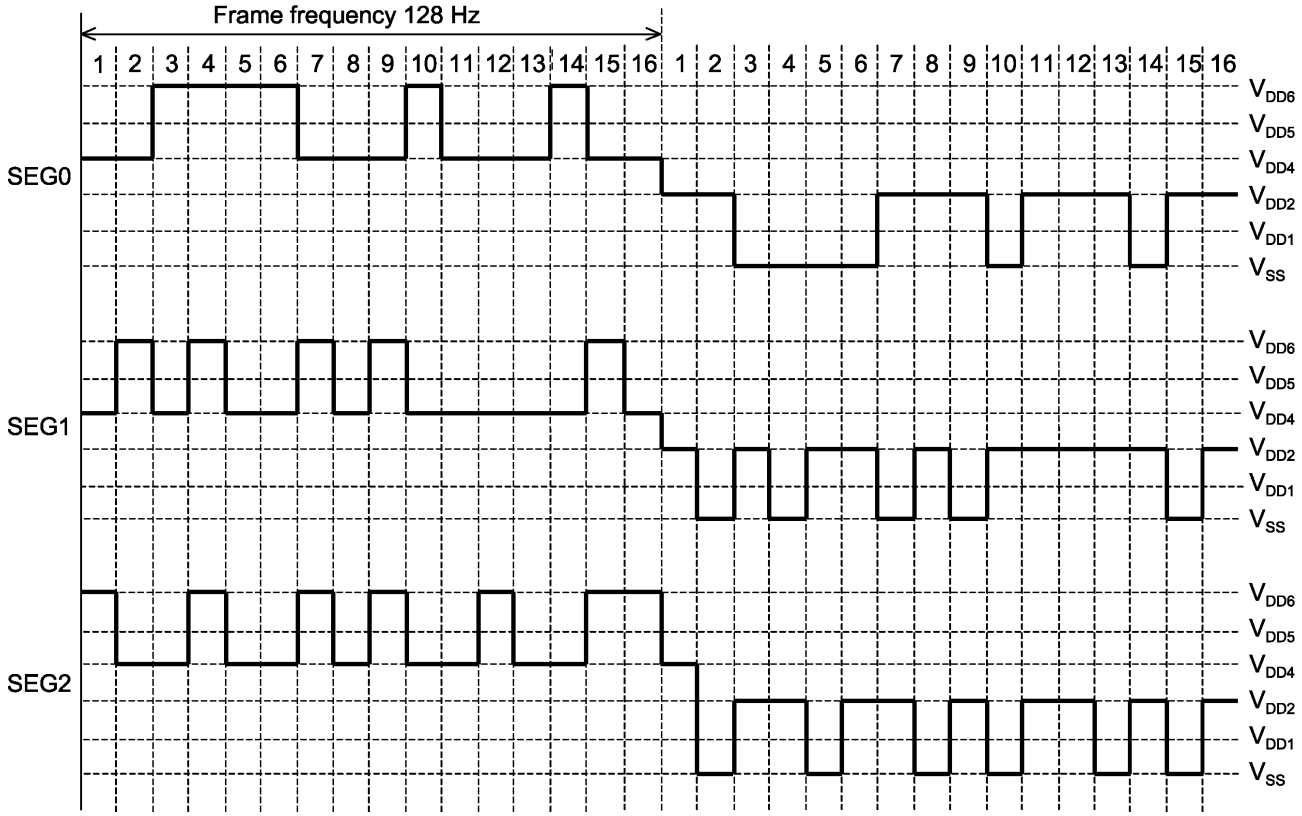


Figure 15-5 (c) 1/16 Duty, 1/5 Bias Segment Output Waveform

Chapter 16

Multiplication/Division Circuit (MULDIV)

16. Multiplication/Division Circuit (MULDIV)

16.1 Overview

The ML63295A has an 8-bit × 8-bit = 16-bit multiplication (MUL) and a 16-bit/8-bit = 16-bit division (DIV), implemented with an internal circuit.

The registers used are shown in Table 16-1.

Table 16-1 Registers Used in Multiplication and Division Circuit

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Value at system reset
Multiplication/division condition register	MDCR	086H	OV	EF	DIVS	MULS	R/W	0H
C register L	CRL	087H	CR3	CR2	CR1	CR0	R/W	0H
C register H	CRH	088H	CR7	CR6	CR5	CR4	R/W	0H
D register L	DRL	089H	DR3	DR2	DR1	DR0	R/W	0H
D register H	DRH	08AH	DR7	DR6	DR5	DR4	R/W	0H
E register L	ERL	08BH	ER3	ER2	ER1	ER0	R/W	0H
E register H	ERH	08CH	ER7	ER6	ER5	ER4	R/W	0H
F register L	FRL	08DH	FR3	FR2	FR1	FR0	R/W	0H
F register H	FRH	08EH	FR7	FR6	FR5	FR4	R/W	0H

For multiplication the C register is multiplied by the E register. The result is stored in the DC register (D: high-order 8 bits, C: low-order 8 bits) after 5 machine cycles.

For division the D register is divided by the E register. The result is stored in the DC register (dividend) and F register (remainder) after 10 machine cycles.

16.2 Multiplication and Division Registers

16.2.1 Calculation Registers

The multiplication and division calculation registers (CRL, CRH, DRL, DRH, ERL, ERH, FRL, FRH) are 4-bit special function registers (SFRs), used to set multiplier, multiplicand, divisor, and dividend and store results.

	bit 3	bit 2	bit 1	bit 0
CRL (087H) (R/W)	CR3	CR2	CR1	CR0
CRH (088H) (R/W)	CR7	CR6	CR5	CR4

	bit 3	bit 2	bit 1	bit 0
DRL (089H) (R/W)	DR3	DR2	DR1	DR0
DRH (08AH) (R/W)	DR7	DR6	DR5	DR4

	bit 3	bit 2	bit 1	bit 0
ERL (08BH) (R/W)	ER3	ER2	ER1	ER0
ERH (08CH) (R/W)	ER7	ER6	ER5	ER4

	bit 3	bit 2	bit 1	bit 0
FRL (08DH) (R/W)	FR3	FR2	FR1	FR0
FRH (08EH) (R/W)	FR7	FR6	FR5	FR4

The multiplication and division calculation registers are used as follows.

[Multiplication]

DR•CR←CR × ER

CR (CRH, CRL): Holds the multiplicand. After multiplication, holds the low-order 8 bits of the result.

ER (ERH, ERL): Holds the multiplier. After multiplication, holds data.

DR (DRH, DRL): After execution, the high-order 8 bits of the result are stored.

If the result of multiplication cannot be stored in the low-order 8 bits (DR is not 0), the multiplication/division condition register (MDCR) OV flag is set to "1". When bit 0 (MULS) of MDCR is set to "1", multiplication starts, and the result is output to the appropriate registers five machine cycles later.

[Division]

DR•CR←DR•CR/ER

FR←DR•CR mod ER

DR (DRH, DRL): The high-order 8 bits of the number being divided are set here. After execution, this register holds the high-order 8 bits of the result.

CR (CRH, CRL): The low-order 8 bits of the number being divided are set here. After execution, this register holds the low-order 8 bits of the result.

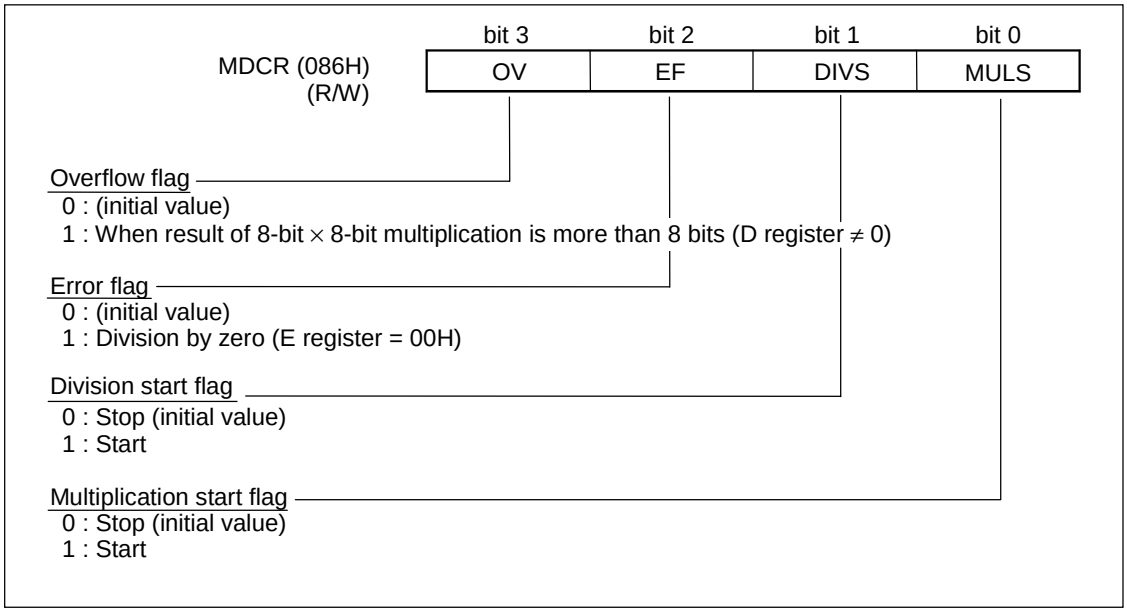
ER (ERH, ERL): The divisor is set here. After execution, this register holds data.

FR (FRH, FRL): After execution, this register holds the remainder.

If division is executed with ER = 00H (division by zero), the MDCR EF flag is set to "1". After division by zero the DC register value is 0FFFFH, and the pre-execution value from the C register is set to the F register. When bit 1 (DIVS) of MDCR is set to "1", division begins and the result is output to the appropriate registers ten machine cycles later.

16.2.2 Multiplication/Division Condition Register

The multiplication/division condition register (MDCR) is a 4-bit special function register (SFR) with a multiplication/division start flag and a status flag indicating the status of the operation when finished.



bit 3: OV (OVerflow flag)

Set to "1" when there is a carry (D register other than 00H) to the high-order 8 bits in multiplication, and otherwise cleared to "0".
This bit is initialized to "0" at system reset.

bit 2: EF (Error Flag)

Set to "1" when the E register is "0" in division, and otherwise cleared to "0".
This bit is initialized to "0" at system reset.

bit 1: DIVS (DIV Start)

Division is started when this bit is set to "1", and is completed in ten machine cycles. When division is complete DIVS is reset to "0".
This bit initializes to "0" at system reset.

bit 0: MULS (MUL Start)

This flag starts multiplication when set to "1", and multiplication is completed in five machine cycles. MULS is cleared to "0" when multiplication is completed.
This bit is reset to "0" at system reset.

16.3 Multiplication/Division Execution

Multiplication and division execution is handled as follows:

[Multiplication]

1. Multiplicand set to C register (CRH, CRL)
2. Multiplier set to E register (ERH, ERL)
3. MDCR MULS flag set to "1".

[Division]

1. High-order 8 bits of number being divided set to D register (DRH, DRL), and low-order 8 bits to C register (CRH, CRL).
2. Divisor set to E register (ERH, ERL).
3. MDCR DIVS flag set to "1".

Chapter 17

Battery Low Detect Circuit (BLD)

17. Battery Low Detect Circuit (BLD)

17.1 Overview

The ML63295A has an internal battery low detect circuit (BLD).

The battery low detect circuit detects when the battery voltage (supply voltage V_{DD}) falls below the judgment voltage value. Two levels of judgment voltage can be selected by the BLDCON bits.

Judgment voltage values (Ta = 25°C): 4.5 ±0.1 V, 5.1 ±0.1 V

Note:

When verifying BLD operation, the operation must be verified with an evaluation sample device.

17.2 Battery Low Detect Circuit Configuration

The battery low detect circuit consists of a judgment circuit and a judgment voltage select circuit. Figure 17-1 shows the circuit configuration.

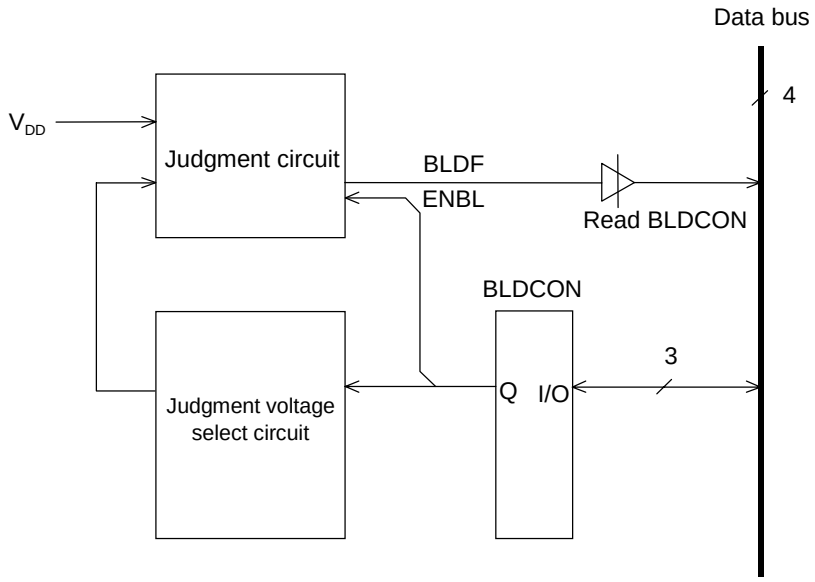


Figure 17-1 Battery Low Detect Circuit

17.3 Judgment Voltage

The value of the judgment voltage is selected by the software by setting the LD1 (bit 1 of BLDCON) and LD0 (bit 0 of BLDCON) bits.

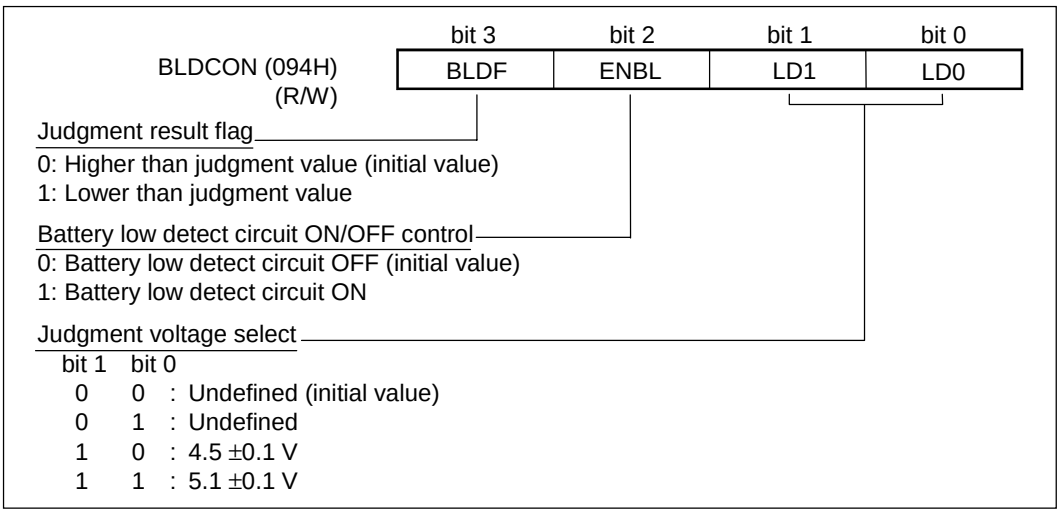
Table 17-1 lists judgment voltage and precision values.

Table 17-1 Judgment Voltage

LD1	LD0	Judgment voltage (V)	Precision (V)	Remarks
1	0	4.5	±0.1	Ta = 25°C
1	1	5.1	±0.1	Ta = 25°C

17.4 Battery Low Detect Circuit Register

- Battery low detect control register (BLDCON)
  BLDCON is a 4-bit special function register (SFR) that controls the battery low detect circuit.



bit 3: BLDF

This flag indicates the judgment result of the battery low detect circuit.
This bit is set to "1" when V_{DD} is lower than the judgment voltage selected by LD0 and LD1, and is set to "0" when V_{DD} is higher. This bit is "0" when the BLD circuit stops operation.
This bit is read-only and writes are invalid.

bit 2: ENBL

This bit turns the battery low detect circuit ON or OFF.
When ENBL is set to "1", the battery low detect circuit is ON. When ENBL is set to "0", the battery low detect circuit is OFF.
At system reset, this bit is cleared to "0".

bit 1, 0: LD1, LD0

These bits select the judgment voltage.
At system reset, these bits are cleared to "0".

17.5 Battery Low Detect Circuit Operation

The battery low detect circuit is turned ON or OFF by ENBL (bit 2 of BLDCON), and outputs to BLDF (bit 3 of BLDCON) the result of a comparison with the judgment voltage.

ENBL is the enable control bit for the battery low detect circuit. Setting ENBL to "1" turns ON the battery low detect circuit. Setting ENBL to "0" turns OFF the battery low detect circuit and BLD current supply drops to zero.

BLDF is the judgment result flag. If BLDF is "1", the power supply voltage is lower than the judgment voltage. If BLDF is "0", the power supply voltage is higher than the judgment voltage. BLDF is valid when ENBL is "1".

The judgment circuit of the battery low detect circuit requires time to become stable. Therefore, after setting ENBL to "1", wait at least 1 ms before reading BLDF. No load should be applied to the power supply voltage during the detection.

Figure 17-2 shows an example operation timing.

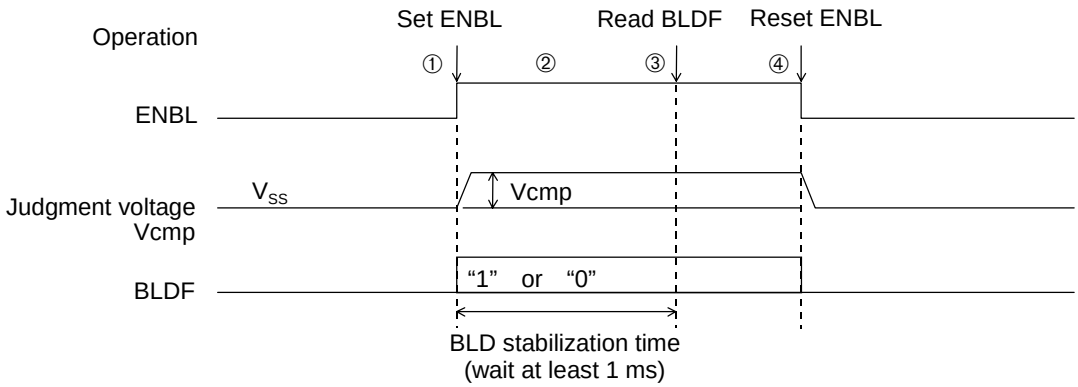


Figure 17-2 Operation Timing Example

Figure 17-2 shows the following operations.

① ENBL is set to "1" to turn ON the BLD.

② Operation starts with no load applied to power supply system and waits for BLD stabilization time interval (at least 1 ms).

③ Judgment result flag (BLDF) is read.

④ ENBL is cleared to "0".

Chapter 18

Power Supply Circuit (POWER)

18. Power Supply Circuit (POWER)

18.1 Overview

The ML63295A has incorporated in it a voltage regulator circuit for the internal logic power supply (V_{DDL}), a voltage regulator circuit for the low-speed oscillation circuit (V_{DDX1}), a circuit for generating bias reference voltages (V_{DDX4} and V_{DD3}), a resistor ladder circuit for generating bias voltages (V_{DD1}, V_{DD2}, V_{DD4}, V_{DD5}, and V_{DD6}), and a voltage regulator circuit for an external power supply (V_{DDE}).

Power supply voltage range: 3.5 to 7.2 V

18.2 Power Supply Circuit Configuration

Figure 18-1 shows the configuration of the power supply circuit.

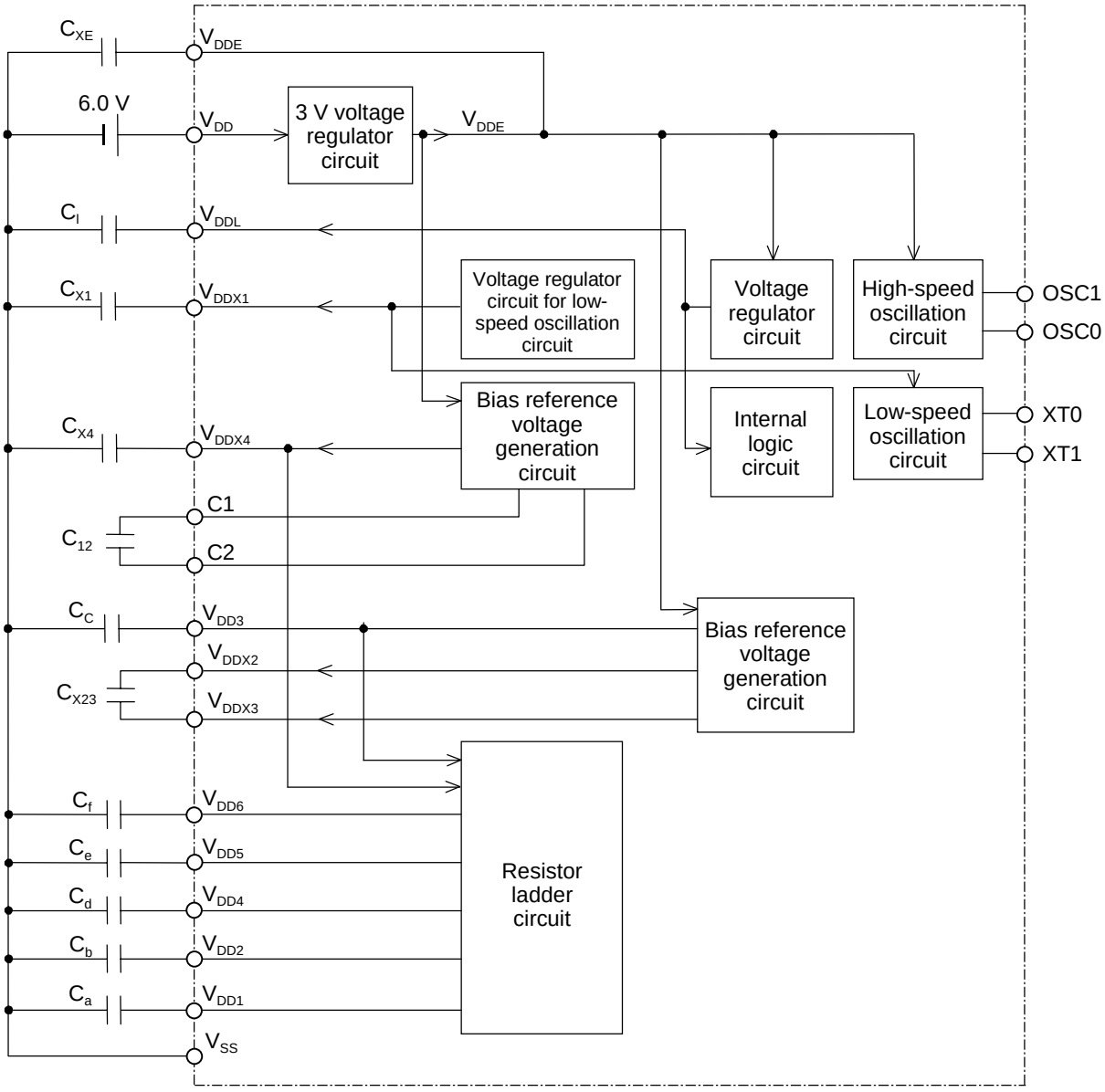


Figure 18-1 Power Supply Circuit Configuration (Power Supply Voltage = 6 V)

18.3 Power Supply Circuit Operation

The output of the internal logic power supply V_{DDL} is forcibly switched to the V_{DD} level when the time base counter is reset and goes down to 1.5 V immediately after the reset state is released. Further the V_{DDL} output goes up to the V_{DDE} level when ENOSC (bit 1 of FCON) is set to "1" and returns to about 1.5 V when ENOSC is set to "0".

The output of the power supply V_{DDX1} for the low-speed oscillation circuit is forcibly switched to the V_{DD} level when the time base counter is reset and goes down to about 1.5 V after the reset state is released.

The output of the external power supply V_{DDE} is forcibly switched to the V_{DD} level when the time base counter is reset and goes down to about 3 V after the reset state is released.

Figure 18-2 shows waveforms of the power supply circuit.

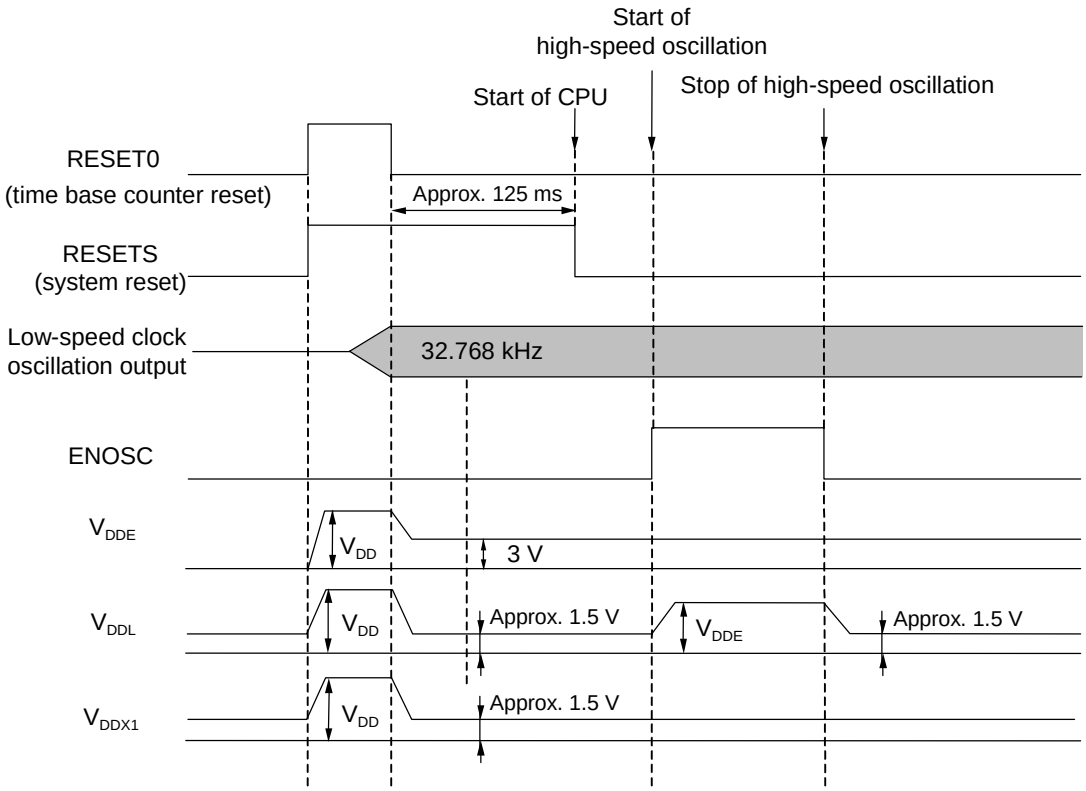


Figure 18-2 Power Supply Circuit Waveforms

Appendixes

Appendix A List of Special Function Registers

The Special Function Registers of the ML63295A are listed in Table A.

"—" indicates an invalid bit.

Table A Special Function Register List

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Port 0 data register	P0D	000H	P03	P02	P01	P00	R	Undefined
Port 1 data register	P1D	001H	P13	P12	P11	P10	R	Undefined
Port 2 data register	P2D	002H	P23	P22	P21	P20	R/W	0H
Port 3 data register	P3D	003H	P33	P32	P31	P30	R/W	0H
Port 4 data register	P4D	004H	P43	P42	P41	P40	R/W	0H
Port 5 data register	P5D	005H	P53	P52	P51	P50	R/W	0H
Port 6 data register	P6D	006H	P63	P62	P61	P60	R/W	0H
Port 7 data register	P7D	007H	P73	P72	P71	P70	R/W	0H
Port 8 data register	P8D	008H	P83	P82	P81	P80	R/W	0H
Port 9 data register	P9D	009H	P93	P92	P91	P90	R/W	0H
Port A data register	PAD	00AH	PA3	PA2	PA1	PA0	R/W	0H
Port B data register	PBD	00BH	PB3	PB2	PB1	PB0	R/W	0H
Port C data register	PCD	00CH	PC3	PC2	PC1	PC0	R/W	0H
Reserved		00DH						
Port E data register	PED	00EH	PE3	PE2	PE1	PE0	R/W	0H
Reserved		00FH						
Port 0 control register 0	P0CON0	010H	P03MD	P02MD	P01MD	P00MD	R/W	0H
Port 0 control register 1	P0CON1	011H	—	—	P0PUD	P0F	R/W	0CH
Port 0 interrupt enable register	P0IE	012H	P03IE	P02IE	P01IE	P00IE	R/W	0H
Port 1 control register 0	P1CON0	013H	P13MD	P12MD	P11MD	P10MD	R/W	0H
Port 1 control register 1	P1CON1	014H	—	—	P1PUD	P1F	R/W	0CH
Port 1 interrupt enable register	P1IE	015H	P13IE	P12IE	P11IE	P10IE	R/W	0H
Port 2 control register 0	P2CON0	016H	P21MD1	P21MD0	P20MD1	P20MD0	R/W	0H
Port 2 control register 1	P2CON1	017H	P23MD1	P23MD0	P22MD1	P22MD0	R/W	0H
Port 3 control register 0	P3CON0	018H	P31MD1	P31MD0	P30MD1	P30MD0	R/W	0H
Port 3 control register 1	P3CON1	019H	P33MD1	P33MD0	P32MD1	P32MD0	R/W	0H
Port 4 control register 0	P4CON0	01AH	P41MD1	P41MD0	P40MD1	P40MD0	R/W	0H
Port 4 control register 1	P4CON1	01BH	P43MD1	P43MD0	P42MD1	P42MD0	R/W	0H
Port 5 control register 0	P5CON0	01CH	P51MD1	P51MD0	P50MD1	P50MD0	R/W	0H
Port 5 control register 1	P5CON1	01DH	P53MD1	P53MD0	P52MD1	P52MD0	R/W	0H
Port 6 control register 0	P6CON0	01EH	P61MD1	P61MD0	P60MD1	P60MD0	R/W	0H
Port 6 control register 1	P6CON1	01FH	P63MD1	P63MD0	P62MD1	P62MD0	R/W	0H
Port 7 control register 0	P7CON0	020H	P71MD1	P71MD0	P70MD1	P70MD0	R/W	0H
Port 7 control register 1	P7CON1	021H	P73MD1	P73MD0	P72MD1	P72MD0	R/W	0H
Port 47 mode register	P47MOD	022H	P7MOD	P6MOD	P5MOD	P4MOD	R/W	0H
Port 8 control register 0	P8CON0	023H	P81MD1	P81MD0	P80MD1	P80MD0	R/W	0H
Port 8 control register 1	P8CON1	024H	P83MD1	P83MD0	P82MD1	P82MD0	R/W	0H
Port 8 direction register	P8DIR	025H	P83DIR	P82DIR	P81DIR	P80DIR	R/W	0H

Table A Special Function Register List (continued)

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Port 8 mode register	P8MOD	026H	P8F	—	P81MOD	P80MOD	R/W	4H
Port 9 control register 0	P9CON0	027H	P91MD1	P91MD0	P90MD1	P90MD0	R/W	0H
Port 9 control register 1	P9CON1	028H	P93MD1	P93MD0	P92MD1	P92MD0	R/W	0H
Port 9 direction register	P9DIR	029H	P93DIR	P92DIR	P91DIR	P90DIR	R/W	0H
Port A control register 0	PACON0	02AH	PA1MD1	PA1MD0	PA0MD1	PA0MD0	R/W	0H
Port A control register 1	PACON1	02BH	PA3MD1	PA3MD0	PA2MD1	PA2MD0	R/W	0H
Port A direction register	PADIR	02CH	PA3DIR	PA2DIR	PA1DIR	PA0DIR	R/W	0H
Port 9A mode register	P9AMOD	02DH	—	—	PAMOD	P9MOD	R/W	0CH
Port B control register 0	PBCON0	02EH	PB1MD1	PB1MD0	PB0MD1	PB0MD0	R/W	0H
Port B control register 1	PBCON1	02FH	PB3MD1	PB3MD0	PB2MD1	PB2MD0	R/W	0H
Port B direction register	PBDIR	030H	PB3DIR	PB2DIR	PB1DIR	PB0DIR	R/W	0H
Port B interrupt enable register	PBIE	031H	PB3IE	PB2IE	PB1IE	PB0IE	R/W	0H
Port B mode register	PBMOD	032H	PBF	—	PB1MOD	PB0MOD	R/W	4H
Port C control register 0	PCCON0	033H	PC1MD1	PC1MD0	PC0MD1	PC0MD0	R/W	0H
Port C control register 1	PCCON1	034H	PC3MD1	PC3MD0	PC2MD1	PC2MD0	R/W	0H
Port C direction register	PCDIR	035H	PC3DIR	PC2DIR	PC1DIR	PC0DIR	R/W	0H
Port C interrupt enable register	PCIE	036H	PC3IE	PC2IE	PC1IE	PC0IE	R/W	0H
Port C mode register 0	PCMOD0	037H	—	—	—	PCF	R/W	0EH
Port C mode register 1	PCMOD1	038H	PC3MOD	PC2MOD	PC1MOD	PC0MOD	R/W	0H
Reserved		039H to 03CH						
Port E control register 0	PECON0	03DH	PE1MD1	PE1MD0	PE0MD1	PE0MD0	R/W	0H
Port E control register 1	PECON1	03EH	PE3MD1	PE3MD0	PE2MD1	PE2MD0	R/W	0H
Port E direction register	PEDIR	03FH	PE3DIR	PE2DIR	PE1DIR	PE0DIR	R/W	0H
Port E mode register	PEMOD	040H	PEF	PE2MOD	PE1MOD	PE0MOD	R/W	0H
Reserved		041H to 04FH						
Interrupt enable register 0	IE0	050H	EXI1	EXI0	EMD	—	R/W	1H
Interrupt enable register 1	IE1	051H	EXI5	EXI4	—	EXI2	R/W	2H
Interrupt enable register 2	IE2	052H	ETM3	ETM2	—	—	R/W	3H
Interrupt enable register 3	IE3	053H	E10Hz	ESFT	EST	ESR	R/W	0H
Interrupt enable register 4	IE4	054H	E2Hz	E4Hz	E16Hz	E32Hz	R/W	0H
Interrupt request register 0	IRQ0	055H	QXI1	QXI0	QMD	QWDT	R/W	0H
Interrupt request register 1	IRQ1	056H	QXI5	QXI4	—	QXI2	R/W	2H
Interrupt request register 2	IRQ2	057H	QTM3	QTM2	—	—	R/W	3H
Interrupt request register 3	IRQ3	058H	Q10Hz	QSFT	QST	QSR	R/W	0H
Interrupt request register 4	IRQ4	059H	Q2Hz	Q4Hz	Q16Hz	Q32Hz	R/W	0H
Reserved		05AH to 05FH						
Time base counter register 0	TBCR0	060H	16Hz	32Hz	64Hz	128Hz	R/W	0H
Time base counter register 1	TBCR1	061H	1Hz	2Hz	4Hz	8Hz	R/W	0H

Table A Special Function Register List (continued)

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Frequency control register	FCON	062H	—	OSCSEL	ENOSC	CPUCLK	R/W	8H
Reserved		063H						
100 Hz counter register	T100CR	064H	100C3	100C2	100C1	100C0	R/W	Undefined
10 Hz counter register	T10CR	065H	10C3	10C2	10C1	10C0	R/W	0H
100 Hz timer counter control register	T100CON	066H	—	—	—	ECNT	R/W	0EH
Reserved		067H to 075H						
Timer 2 data register L	TM2DL	076H	T2D3	T2D2	T2D1	T2D0	R/W	0H
Timer 2 data register H	TM2DH	077H	T2D7	T2D6	T2D5	T2D4	R/W	0H
Timer 3 data register L	TM3DL	078H	T3D3	T3D2	T3D1	T3D0	R/W	0H
Timer 3 data register H	TM3DH	079H	T3D7	T3D6	T3D5	T3D4	R/W	0H
Timer 2 counter register L	TM2CL	07AH	T2C3	T2C2	T2C1	T2C0	R/W	0H
Timer 2 counter register H	TM2CH	07BH	T2C7	T2C6	T2C5	T2C4	R/W	0H
Timer 3 counter register L	TM3CL	07CH	T3C3	T3C2	T3C1	T3C0	R/W	0H
Timer 3 counter register H	TM3CH	07DH	T3C7	T3C6	T3C5	T3C4	R/W	0H
Timer 2 control register 0	TM2CON0	07EH	—	FMEAS2	—	TM2RUN	R/W	0AH
Timer 2 control register 1	TM2CON1	07FH	—	—	TM2CL1	TM2CL0	R/W	0CH
Timer 3 control register 0	TM3CON0	080H	—	—	—	TM3RUN	R/W	0EH
Timer 3 control register 1	TM3CON1	081H	—	—	TM3CL1	TM3CL0	R/W	0CH
Timer 2 status register	TM2STAT	082H	—	—	—	TM2OVF	R	0EH
Timer 3 status register	TM3STAT	083H	—	—	—	TM3OVF	R	0EH
Reserved		084H and 085H						
Multiplication/division condition register	MDCR	086H	OV	EF	DIVS	MULS	R/W	0H
C register L	CRL	087H	CR3	CR2	CR1	CR0	R/W	0H
C register H	CRH	088H	CR7	CR6	CR5	CR4	R/W	0H
D register L	DRL	089H	DR3	DR2	DR1	DR0	R/W	0H
D register H	DRH	08AH	DR7	DR6	DR5	DR4	R/W	0H
E register L	ERL	08BH	ER3	ER2	ER1	ER0	R/W	0H
E register H	ERH	08CH	ER7	ER6	ER5	ER4	R/W	0H
F register L	FRL	08DH	FR3	FR2	FR1	FR0	R/W	0H
F register H	FRH	08EH	FR7	FR6	FR5	FR4	R/W	0H
Reserved		08FH						
Display control register 0	DSPCON0	090H	BISEL	PDWN	ALLON	LCDON	R/W	0H
Display control register 1	DSPCON1	091H	DT3	DT2	DT1	DT0	R/W	0H
Display contrast register	DSPCNT	092H	CN3	CN2	CN1	CN0	R/W	0H
Reserved		093H						

Table A Special Function Register List (continued)

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Battery low detect control register	BLDCON	094H	BLDF	ENBL	LD1	LD0	R/W	0H
Tempo register	TEMPO	096H	TMP3	TMP2	TMP1	TMP0	R/W	0H
Melody driver control register	MDCON	097H	MSF	EMBD	MBM1	MBM0	R/W	0H
Reserved		098H to 09EH						
Watchdog timer control register	WDTCON	09FH	d3	d2	d1	d0	W	—
Shift register L	SFTRL	0A0H	SD3	SD2	SD1	SD0	R/W	0H
Shift register H	SFTRH	0A1H	SD7	SD6	SD5	SD4	R/W	0H
Shift register control register 0	SFTCON0	0A2H	—	SDIR	SELCK1	SELCK0	R/W	8H
Shift register control register 1	SFTCON1	0A3H	—	—	—	ENTR	R/W	0EH
Serial port send buffer L	STBUFL	0A4H	TB3	TB2	TB1	TB0	R/W	0H
Serial port send buffer H	STBUFH	0A5H	TB7	TB6	TB5	TB4	R/W	0H
Serial port send control register 0	STCON0	0A6H	STSTB	STL1	STL0	STMOD	R/W	0H
Serial port send control register 1	STCON1	0A7H	STLMB	STPOE	STPEN	STCLK	R/W	0H
Serial port receive buffer L	SRBUFL	0A8H	RB3	RB2	RB1	RB0	R	0H
Serial port receive buffer H	SRBUFH	0A9H	RB7	RB6	RB5	RB4	R	0H
Serial port receive control register 0	SRCON0	0AAH	SREN	SRL1	SRL0	SRMOD	R/W	0H
Serial port receive control register 1	SRCON1	0ABH	SRLMB	SRPOE	SRPEN	SRCLK	R/W	0H
Serial port receive baud rate setting register	SRBRT	0ACH	—	—	BRT1	BRT0	R/W	0CH
Serial port status register	SSTAT	0ADH	BFULL	PERR	OERR	FERR	R	0H
Reserved		0AEH to 0F1H						
RA register 0	RA0	0F2H	a3	a2	a1	a0	R/W	0H
RA register 1	RA1	0F3H	a7	a6	a5	a4	R/W	0H
RA register 2	RA2	0F4H	a11	a10	a9	a8	R/W	0H
RA register 3	RA3	0F5H	a15	a14	a13	a12	R/W	0H
Register stack pointer	RSP	0F6H	rsp3	rsp2	rsp1	rsp0	R/W	0H
Stack pointer	SP	0F7H	sp3	sp2	sp1	sp0	R	0H
Reserved		0F8H						
Y register	Y	0F9H	y3	y2	y1	y0	R/W	0H
X register	X	0FAH	x3	x2	x1	x0	R/W	0H
L register	L	0FBH	l3	l2	l1	l0	R/W	0H
H register	H	0FCH	h3	h2	h1	h0	R/W	0H
Current bank register	CBR	0FDH	c3	c2	c1	c0	R/W	0H
Extra bank register	EBR	0FEH	e3	e2	e1	e0	R/W	0H
Master interrupt enable register	MIEF	0FFH	—	—	—	MIE	R	0EH

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 0	DSPR0	100H	SEG0	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 1	DSPR1	101H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 2	DSPR2	102H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 3	DSPR3	103H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 4	DSPR4	104H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 5	DSPR5	105H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 6	DSPR6	106H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 7	DSPR7	107H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 8	DSPR8	108H	SEG1	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 9	DSPR9	109H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 10	DSPR10	10AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 11	DSPR11	10BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 12	DSPR12	10CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 13	DSPR13	10DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 14	DSPR14	10EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 15	DSPR15	10FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 16	DSPR16	110H	SEG2	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 17	DSPR17	111H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 18	DSPR18	112H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 19	DSPR19	113H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 20	DSPR20	114H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 21	DSPR21	115H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 22	DSPR22	116H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 23	DSPR23	117H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 24	DSPR24	118H	SEG3	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 25	DSPR25	119H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 26	DSPR26	11AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 27	DSPR27	11BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 28	DSPR28	11CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 29	DSPR29	11DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 30	DSPR30	11EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 31	DSPR31	11FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 32	DSPR32	120H	SEG4	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 33	DSPR33	121H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 34	DSPR34	122H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 35	DSPR35	123H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 36	DSPR36	124H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 37	DSPR37	125H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 38	DSPR38	126H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 39	DSPR39	127H		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 40	DSPR40	128H	SEG5	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 41	DSPR41	129H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 42	DSPR42	12AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 43	DSPR43	12BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 44	DSPR44	12CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 45	DSPR45	12DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 46	DSPR46	12EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 47	DSPR47	12FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 48	DSPR48	130H	SEG6	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 49	DSPR49	131H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 50	DSPR50	132H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 51	DSPR51	133H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 52	DSPR52	134H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 53	DSPR53	135H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 54	DSPR54	136H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 55	DSPR55	137H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 56	DSPR56	138H	SEG7	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 57	DSPR57	139H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 58	DSPR58	13AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 59	DSPR59	13BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 60	DSPR60	13CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 61	DSPR61	13DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 62	DSPR62	13EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 63	DSPR63	13FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 64	DSPR64	140H	SEG8	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 65	DSPR65	141H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 66	DSPR66	142H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 67	DSPR67	143H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 68	DSPR68	144H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 69	DSPR69	145H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 70	DSPR70	146H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 71	DSPR71	147H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 72	DSPR72	148H	SEG9	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 73	DSPR73	149H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 74	DSPR74	14AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 75	DSPR75	14BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 76	DSPR76	14CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 77	DSPR77	14DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 78	DSPR78	14EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 79	DSPR79	14FH		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 80	DSPR80	150H	SEG10	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 81	DSPR81	151H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 82	DSPR82	152H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 83	DSPR83	153H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 84	DSPR84	154H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 85	DSPR85	155H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 86	DSPR86	156H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 87	DSPR87	157H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 88	DSPR88	158H	SEG11	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 89	DSPR89	159H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 90	DSPR90	15AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 91	DSPR91	15BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 92	DSPR92	15CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 93	DSPR93	15DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 94	DSPR94	15EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 95	DSPR95	15FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 96	DSPR96	160H	SEG12	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 97	DSPR97	161H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 98	DSPR98	162H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 99	DSPR99	163H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 100	DSPR100	164H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 101	DSPR101	165H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 102	DSPR102	166H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 103	DSPR103	167H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 104	DSPR104	168H	SEG13	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 105	DSPR105	169H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 106	DSPR106	16AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 107	DSPR107	16BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 108	DSPR108	16CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 109	DSPR109	16DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 110	DSPR110	16EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 111	DSPR111	16FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 112	DSPR112	170H	SEG14	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 113	DSPR113	171H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 114	DSPR114	172H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 115	DSPR115	173H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 116	DSPR116	174H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 117	DSPR117	175H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 118	DSPR118	176H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 119	DSPR119	177H		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 120	DSPR120	178H	SEG15	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 121	DSPR121	179H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 122	DSPR122	17AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 123	DSPR123	17BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 124	DSPR124	17CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 125	DSPR125	17DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 126	DSPR126	17EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 127	DSPR127	17FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 128	DSPR128	180H	SEG16	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 129	DSPR129	181H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 130	DSPR130	182H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 131	DSPR131	183H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 132	DSPR132	184H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 133	DSPR133	185H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 134	DSPR134	186H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 135	DSPR135	187H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 136	DSPR136	188H	SEG17	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 137	DSPR137	189H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 138	DSPR138	18AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 139	DSPR139	18BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 140	DSPR140	18CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 141	DSPR141	18DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 142	DSPR142	18EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 143	DSPR143	18FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 144	DSPR144	190H	SEG18	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 145	DSPR145	191H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 146	DSPR146	192H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 147	DSPR147	193H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 148	DSPR148	194H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 149	DSPR149	195H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 150	DSPR150	196H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 151	DSPR151	197H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 152	DSPR152	198H	SEG19	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 153	DSPR153	199H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 154	DSPR154	19AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 155	DSPR155	19BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 156	DSPR156	19CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 157	DSPR157	19DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 158	DSPR158	19EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 159	DSPR159	19FH		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 160	DSPR160	1A0H	SEG20	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 161	DSPR161	1A1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 162	DSPR162	1A2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 163	DSPR163	1A3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 164	DSPR164	1A4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 165	DSPR165	1A5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 166	DSPR166	1A6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 167	DSPR167	1A7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 168	DSPR168	1A8H	SEG21	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 169	DSPR169	1A9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 170	DSPR170	1AAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 171	DSPR171	1ABH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 172	DSPR172	1ACH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 173	DSPR173	1ADH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 174	DSPR174	1AEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 175	DSPR175	1AFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 176	DSPR176	1B0H	SEG22	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 177	DSPR177	1B1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 178	DSPR178	1B2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 179	DSPR179	1B3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 180	DSPR180	1B4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 181	DSPR181	1B5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 182	DSPR182	1B6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 183	DSPR183	1B7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 184	DSPR184	1B8H	SEG23	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 185	DSPR185	1B9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 186	DSPR186	1BAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 187	DSPR187	1BBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 188	DSPR188	1BCH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 189	DSPR189	1BDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 190	DSPR190	1BEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 191	DSPR191	1BFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 192	DSPR192	1C0H	SEG24	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 193	DSPR193	1C1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 194	DSPR194	1C2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 195	DSPR195	1C3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 196	DSPR196	1C4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 197	DSPR197	1C5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 198	DSPR198	1C6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 199	DSPR199	1C7H		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 200	DSPR200	1C8H	SEG25	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 201	DSPR201	1C9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 202	DSPR202	1CAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 203	DSPR203	1CBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 204	DSPR204	1CCH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 205	DSPR205	1CDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 206	DSPR206	1CEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 207	DSPR207	1CFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 208	DSPR208	1D0H	SEG26	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 209	DSPR209	1D1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 210	DSPR210	1D2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 211	DSPR211	1D3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 212	DSPR212	1D4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 213	DSPR213	1D5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 214	DSPR214	1D6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 215	DSPR215	1D7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 216	DSPR216	1D8H	SEG27	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 217	DSPR217	1D9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 218	DSPR218	1DAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 219	DSPR219	1DBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 220	DSPR220	1DCH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 221	DSPR221	1DDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 222	DSPR222	1DEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 223	DSPR223	1DFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 224	DSPR224	1E0H	SEG28	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 225	DSPR225	1E1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 226	DSPR226	1E2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 227	DSPR227	1E3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 228	DSPR228	1E4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 229	DSPR229	1E5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 230	DSPR230	1E6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 231	DSPR231	1E7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 232	DSPR232	1E8H	SEG29	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 233	DSPR233	1E9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 234	DSPR234	1EAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 235	DSPR235	1EBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 236	DSPR236	1ECH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 237	DSPR237	1EDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 238	DSPR238	1EEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 239	DSPR239	1EFH		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 240	DSPR240	1F0H	SEG30	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 241	DSPR241	1F1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 242	DSPR242	1F2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 243	DSPR243	1F3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 244	DSPR244	1F4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 245	DSPR245	1F5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 246	DSPR246	1F6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 247	DSPR247	1F7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 248	DSPR248	1F8H	SEG31	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 249	DSPR249	1F9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 250	DSPR250	1FAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 251	DSPR251	1FBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 252	DSPR252	1FCH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 253	DSPR253	1FDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 254	DSPR254	1FEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 255	DSPR255	1FFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 256	DSPR256	200H	SEG32	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 257	DSPR257	201H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 258	DSPR258	202H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 259	DSPR259	203H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 260	DSPR260	204H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 261	DSPR261	205H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 262	DSPR262	206H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 263	DSPR263	207H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 264	DSPR264	208H	SEG33	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 265	DSPR265	209H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 266	DSPR266	20AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 267	DSPR267	20BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 268	DSPR268	20CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 269	DSPR269	20DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 270	DSPR270	20EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 271	DSPR271	20FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 272	DSPR272	210H	SEG34	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 273	DSPR273	211H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 274	DSPR274	212H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 275	DSPR275	213H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 276	DSPR276	214H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 277	DSPR277	215H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 278	DSPR278	216H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 279	DSPR279	217H		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 280	DSPR280	218H	SEG35	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 281	DSPR281	219H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 282	DSPR282	21AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 283	DSPR283	21BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 284	DSPR284	21CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 285	DSPR285	21DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 286	DSPR286	21EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 287	DSPR287	21FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 288	DSPR288	220H	SEG36	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 289	DSPR289	221H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 290	DSPR290	222H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 291	DSPR291	223H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 292	DSPR292	224H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 293	DSPR293	225H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 294	DSPR294	226H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 295	DSPR295	227H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 296	DSPR296	228H	SEG37	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 297	DSPR297	229H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 298	DSPR298	22AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 299	DSPR299	22BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 300	DSPR300	22CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 301	DSPR301	22DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 302	DSPR302	22EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 303	DSPR303	22FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 304	DSPR304	230H	SEG38	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 305	DSPR305	231H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 306	DSPR306	232H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 307	DSPR307	233H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 308	DSPR308	234H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 309	DSPR309	235H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 310	DSPR310	236H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 311	DSPR311	237H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 312	DSPR312	238H	SEG39	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 313	DSPR313	239H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 314	DSPR314	23AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 315	DSPR315	23BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 316	DSPR316	23CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 317	DSPR317	23DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 318	DSPR318	23EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 319	DSPR319	23FH		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 320	DSPR320	240H	SEG40	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 321	DSPR321	241H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 322	DSPR322	242H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 323	DSPR323	243H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 324	DSPR324	244H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 325	DSPR325	245H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 326	DSPR326	246H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 327	DSPR327	247H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 328	DSPR328	248H	SEG41	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 329	DSPR329	249H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 330	DSPR330	24AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 331	DSPR331	24BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 332	DSPR332	24CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 333	DSPR333	24DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 334	DSPR334	24EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 335	DSPR335	24FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 336	DSPR336	250H	SEG42	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 337	DSPR337	251H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 338	DSPR338	252H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 339	DSPR339	253H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 340	DSPR340	254H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 341	DSPR341	255H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 342	DSPR342	256H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 343	DSPR343	257H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 344	DSPR344	258H	SEG43	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 345	DSPR345	259H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 346	DSPR346	25AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 347	DSPR347	25BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 348	DSPR348	25CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 349	DSPR349	25DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 350	DSPR350	25EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 351	DSPR351	25FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 352	DSPR352	260H	SEG44	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 353	DSPR353	261H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 354	DSPR354	262H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 355	DSPR355	263H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 356	DSPR356	264H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 357	DSPR357	265H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 358	DSPR358	266H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 359	DSPR359	267H		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 360	DSPR360	268H	SEG45	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 361	DSPR361	269H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 362	DSPR362	26AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 363	DSPR363	26BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 364	DSPR364	26CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 365	DSPR365	26DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 366	DSPR366	26EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 367	DSPR367	26FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 368	DSPR368	270H	SEG46	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 369	DSPR369	271H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 370	DSPR370	272H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 371	DSPR371	273H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 372	DSPR372	274H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 373	DSPR373	275H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 374	DSPR374	276H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 375	DSPR375	277H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 376	DSPR376	278H	SEG47	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 377	DSPR377	279H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 378	DSPR378	27AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 379	DSPR379	27BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 380	DSPR380	27CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 381	DSPR381	27DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 382	DSPR382	27EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 383	DSPR383	27FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 384	DSPR384	280H	SEG48	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 385	DSPR385	281H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 386	DSPR386	282H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 387	DSPR387	283H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 388	DSPR388	284H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 389	DSPR389	285H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 390	DSPR390	286H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 391	DSPR391	287H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 392	DSPR392	288H	SEG49	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 393	DSPR393	289H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 394	DSPR394	28AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 395	DSPR395	28BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 396	DSPR396	28CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 397	DSPR397	28DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 398	DSPR398	28EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 399	DSPR399	28FH		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 400	DSPR400	290H	SEG50	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 401	DSPR401	291H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 402	DSPR402	292H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 403	DSPR403	293H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 404	DSPR404	294H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 405	DSPR405	295H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 406	DSPR406	296H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 407	DSPR407	297H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 408	DSPR408	298H	SEG51	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 409	DSPR409	299H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 410	DSPR410	29AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 411	DSPR411	29BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 412	DSPR412	29CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 413	DSPR413	29DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 414	DSPR414	29EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 415	DSPR415	29FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 416	DSPR416	2A0H	SEG52	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 417	DSPR417	2A1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 418	DSPR418	2A2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 419	DSPR419	2A3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 420	DSPR420	2A4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 421	DSPR421	2A5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 422	DSPR422	2A6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 423	DSPR423	2A7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 424	DSPR424	2A8H	SEG53	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 425	DSPR425	2A9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 426	DSPR426	2AAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 427	DSPR427	2ABH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 428	DSPR428	2ACH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 429	DSPR429	2ADH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 430	DSPR430	2AEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 431	DSPR431	2AFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 432	DSPR432	2B0H	SEG54	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 433	DSPR433	2B1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 434	DSPR434	2B2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 435	DSPR435	2B3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 436	DSPR436	2B4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 437	DSPR437	2B5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 438	DSPR438	2B6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 439	DSPR439	2B7H		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 440	DSPR440	2B8H	SEG55	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 441	DSPR441	2B9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 442	DSPR442	2BAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 443	DSPR443	2BBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 444	DSPR444	2BCH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 445	DSPR445	2BDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 446	DSPR446	2BEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 447	DSPR447	2BFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 448	DSPR448	2C0H	SEG56	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 449	DSPR449	2C1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 450	DSPR450	2C2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 451	DSPR451	2C3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 452	DSPR452	2C4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 453	DSPR453	2C5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 454	DSPR454	2C6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 455	DSPR455	2C7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 456	DSPR456	2C8H	SEG57	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 457	DSPR457	2C9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 458	DSPR458	2CAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 459	DSPR459	2CBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 460	DSPR460	2CCH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 461	DSPR461	2CDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 462	DSPR462	2CEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 463	DSPR463	2CFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 464	DSPR464	2D0H	SEG58	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 465	DSPR465	2D1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 466	DSPR466	2D2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 467	DSPR467	2D3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 468	DSPR468	2D4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 469	DSPR469	2D5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 470	DSPR470	2D6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 471	DSPR471	2D7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 472	DSPR472	2D8H	SEG59	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 473	DSPR473	2D9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 474	DSPR474	2DAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 475	DSPR475	2DBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 476	DSPR476	2DCH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 477	DSPR477	2DDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 478	DSPR478	2DEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 479	DSPR479	2DFH		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 480	DSPR480	2E0H	SEG60	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 481	DSPR481	2E1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 482	DSPR482	2E2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 483	DSPR483	2E3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 484	DSPR484	2E4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 485	DSPR485	2E5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 486	DSPR486	2E6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 487	DSPR487	2E7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 488	DSPR488	2E8H	SEG61	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 489	DSPR489	2E9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 490	DSPR490	2EAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 491	DSPR491	2EBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 492	DSPR492	2ECH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 493	DSPR493	2EDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 494	DSPR494	2EEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 495	DSPR495	2EFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 496	DSPR496	2F0H	SEG62	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 497	DSPR497	2F1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 498	DSPR498	2F2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 499	DSPR499	2F3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 500	DSPR500	2F4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 501	DSPR501	2F5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 502	DSPR502	2F6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 503	DSPR503	2F7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 504	DSPR504	2F8H	SEG63	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 505	DSPR505	2F9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 506	DSPR506	2FAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 507	DSPR507	2FBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 508	DSPR508	2FCH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 509	DSPR509	2FDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 510	DSPR510	2FEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 511	DSPR511	2FFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 512	DSPR512	300H	SEG64	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 513	DSPR513	301H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 514	DSPR514	302H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 515	DSPR515	303H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 516	DSPR516	304H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 517	DSPR517	305H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 518	DSPR518	306H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 519	DSPR519	307H		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 520	DSPR520	308H	SEG65	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 521	DSPR521	309H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 522	DSPR522	30AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 523	DSPR523	30BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 524	DSPR524	30CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 525	DSPR525	30DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 526	DSPR526	30EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 527	DSPR527	30FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 528	DSPR528	310H	SEG66	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 529	DSPR529	311H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 530	DSPR530	312H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 531	DSPR531	313H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 532	DSPR532	314H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 533	DSPR533	315H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 534	DSPR534	316H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 535	DSPR535	317H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 536	DSPR536	318H	SEG67	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 537	DSPR537	319H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 538	DSPR538	31AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 539	DSPR539	31BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 540	DSPR540	31CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 541	DSPR541	31DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 542	DSPR542	31EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 543	DSPR543	31FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 544	DSPR544	320H	SEG68	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 545	DSPR545	321H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 546	DSPR546	322H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 547	DSPR547	323H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 548	DSPR548	324H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 549	DSPR549	325H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 550	DSPR550	326H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 551	DSPR551	327H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 552	DSPR552	328H	SEG69	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 553	DSPR553	329H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 554	DSPR554	32AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 555	DSPR555	32BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 556	DSPR556	32CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 557	DSPR557	32DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 558	DSPR558	32EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 559	DSPR559	32FH		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 560	DSPR560	330H	SEG70	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 561	DSPR561	331H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 562	DSPR562	332H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 563	DSPR563	333H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 564	DSPR564	334H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 565	DSPR565	335H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 566	DSPR566	336H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 567	DSPR567	337H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 568	DSPR568	338H	SEG71	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 569	DSPR569	339H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 570	DSPR570	33AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 571	DSPR571	33BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 572	DSPR572	33CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 573	DSPR573	33DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 574	DSPR574	33EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 575	DSPR575	33FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 576	DSPR576	340H	SEG72	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 577	DSPR577	341H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 578	DSPR578	342H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 579	DSPR579	343H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 580	DSPR580	344H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 581	DSPR581	345H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 582	DSPR582	346H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 583	DSPR583	347H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 584	DSPR584	348H	SEG73	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 585	DSPR585	349H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 586	DSPR586	34AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 587	DSPR587	34BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 588	DSPR588	34CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 589	DSPR589	34DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 590	DSPR590	34EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 591	DSPR591	34FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 592	DSPR592	350H	SEG74	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 593	DSPR593	351H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 594	DSPR594	352H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 595	DSPR595	353H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 596	DSPR596	354H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 597	DSPR597	355H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 598	DSPR598	356H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 599	DSPR599	357H		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 600	DSPR600	358H	SEG75	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 601	DSPR601	359H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 602	DSPR602	35AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 603	DSPR603	35BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 604	DSPR604	35CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 605	DSPR605	35DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 606	DSPR606	35EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 607	DSPR607	35FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 608	DSPR608	360H	SEG76	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 609	DSPR609	361H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 610	DSPR610	362H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 611	DSPR611	363H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 612	DSPR612	364H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 613	DSPR613	365H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 614	DSPR614	366H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 615	DSPR615	367H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 616	DSPR616	368H	SEG77	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 617	DSPR617	369H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 618	DSPR618	36AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 619	DSPR619	36BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 620	DSPR620	36CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 621	DSPR621	36DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 622	DSPR622	36EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 623	DSPR623	36FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 624	DSPR624	370H	SEG78	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 625	DSPR625	371H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 626	DSPR626	372H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 627	DSPR627	373H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 628	DSPR628	374H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 629	DSPR629	375H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 630	DSPR630	376H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 631	DSPR631	377H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 632	DSPR632	378H	SEG79	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 633	DSPR633	379H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 634	DSPR634	37AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 635	DSPR635	37BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 636	DSPR636	37CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 637	DSPR637	37DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 638	DSPR638	37EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 639	DSPR639	37FH		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 640	DSPR640	380H	SEG80	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 641	DSPR641	381H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 642	DSPR642	382H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 643	DSPR643	383H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 644	DSPR644	384H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 645	DSPR645	385H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 646	DSPR646	386H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 647	DSPR647	387H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 648	DSPR648	388H	SEG81	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 649	DSPR649	389H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 650	DSPR650	38AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 651	DSPR651	38BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 652	DSPR652	38CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 653	DSPR653	38DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 654	DSPR654	38EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 655	DSPR655	38FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 656	DSPR656	390H	SEG82	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 657	DSPR657	391H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 658	DSPR658	392H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 659	DSPR659	393H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 660	DSPR660	394H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 661	DSPR661	395H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 662	DSPR662	396H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 663	DSPR663	397H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 664	DSPR664	398H	SEG83	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 665	DSPR665	399H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 666	DSPR666	39AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 667	DSPR667	39BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 668	DSPR668	39CH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 669	DSPR669	39DH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 670	DSPR670	39EH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 671	DSPR671	39FH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 672	DSPR672	3A0H	SEG84	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 673	DSPR673	3A1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 674	DSPR674	3A2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 675	DSPR675	3A3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 676	DSPR676	3A4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 677	DSPR677	3A5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 678	DSPR678	3A6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 679	DSPR679	3A7H		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 680	DSPR680	3A8H	SEG85	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 681	DSPR681	3A9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 682	DSPR682	3AAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 683	DSPR683	3ABH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 684	DSPR684	3ACH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 685	DSPR685	3ADH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 686	DSPR686	3AEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 687	DSPR687	3AFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 688	DSPR688	3B0H	SEG86	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 689	DSPR689	3B1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 690	DSPR690	3B2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 691	DSPR691	3B3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 692	DSPR692	3B4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 693	DSPR693	3B5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 694	DSPR694	3B6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 695	DSPR695	3B7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 696	DSPR696	3B8H	SEG87	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 697	DSPR697	3B9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 698	DSPR698	3BAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 699	DSPR699	3BBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 700	DSPR700	3BCH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 701	DSPR701	3BDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 702	DSPR702	3BEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 703	DSPR703	3BFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 704	DSPR704	3C0H	SEG88	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 705	DSPR705	3C1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 706	DSPR706	3C2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 707	DSPR707	3C3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 708	DSPR708	3C4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 709	DSPR709	3C5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 710	DSPR710	3C6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 711	DSPR711	3C7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 712	DSPR712	3C8H	SEG89	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 713	DSPR713	3C9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 714	DSPR714	3CAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 715	DSPR715	3CBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 716	DSPR716	3CCH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 717	DSPR717	3CDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 718	DSPR718	3CEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 719	DSPR719	3CFH		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 720	DSPR720	3D0H	SEG90	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 721	DSPR721	3D1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 722	DSPR722	3D2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 723	DSPR723	3D3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 724	DSPR724	3D4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 725	DSPR725	3D5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 726	DSPR726	3D6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 727	DSPR727	3D7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 728	DSPR728	3D8H	SEG91	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 729	DSPR729	3D9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 730	DSPR730	3DAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 731	DSPR731	3DBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 732	DSPR732	3DCH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 733	DSPR733	3DDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 734	DSPR734	3DEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 735	DSPR735	3DFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 736	DSPR736	3E0H	SEG92	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 737	DSPR737	3E1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 738	DSPR738	3E2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 739	DSPR739	3E3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 740	DSPR740	3E4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 741	DSPR741	3E5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 742	DSPR742	3E6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 743	DSPR743	3E7H		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 744	DSPR744	3E8H	SEG93	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 745	DSPR745	3E9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 746	DSPR746	3EAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 747	DSPR747	3EBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 748	DSPR748	3ECH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 749	DSPR749	3EDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 750	DSPR750	3EEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 751	DSPR751	3EFH		COM32	COM31	COM30	COM29	R/W	Undefined
Display register 752	DSPR752	3F0H	SEG94	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 753	DSPR753	3F1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 754	DSPR754	3F2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 755	DSPR755	3F3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 756	DSPR756	3F4H		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 757	DSPR757	3F5H		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 758	DSPR758	3F6H		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 759	DSPR759	3F7H		COM32	COM31	COM30	COM29	R/W	Undefined

Table A Special Function Register List (continued)

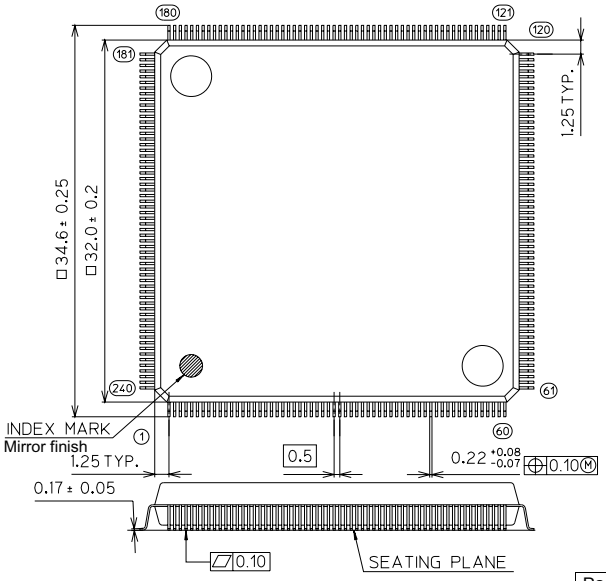
Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 760	DSPR760	3F8H	SEG95	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 761	DSPR761	3F9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 762	DSPR762	3FAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 763	DSPR763	3FBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 764	DSPR764	3FCH		COM20	COM19	COM18	COM17	R/W	Undefined
Display register 765	DSPR765	3FDH		COM24	COM23	COM22	COM21	R/W	Undefined
Display register 766	DSPR766	3FEH		COM28	COM27	COM26	COM25	R/W	Undefined
Display register 767	DSPR767	3FFH		COM32	COM31	COM30	COM29	R/W	Undefined

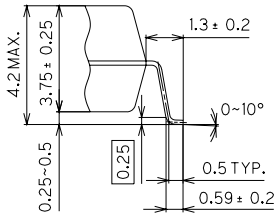
Appendix B Package Dimensions

ML63295A-xxxGA

(Unit: mm)

QFP240-P-3232-0.50-BK4





Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	7.82 TYP.
Rev. No./Last Revised	2/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

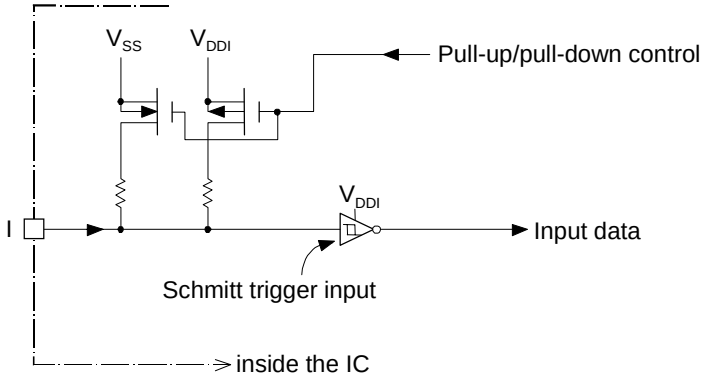
Figure B-1 240-Pin QFP (QFP240-P-3232-0.50-BK4)

Notes for Mounting the Surface Mount Type Package

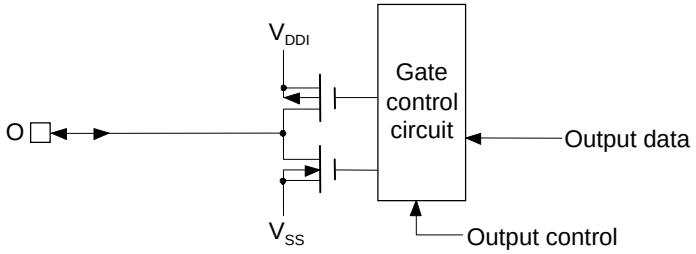
The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Appendix C Input/Output Circuit Configuration

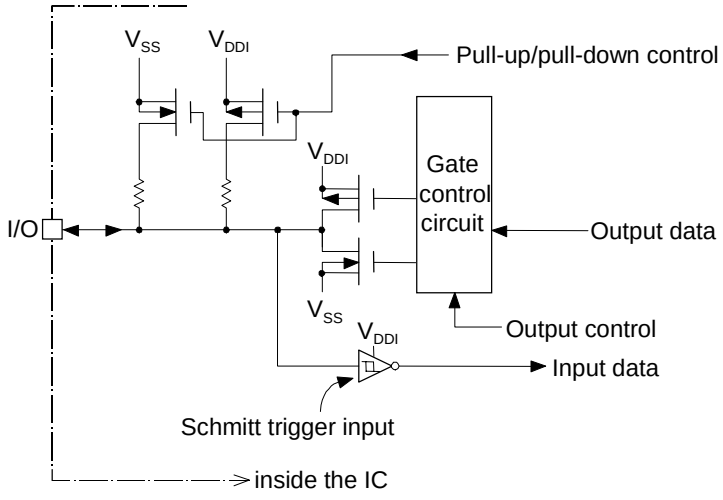
(1) Input Port (P0.0–P0.3, P1.0–P1.3)



(2) Output Port (P2.0–P2.3, P3.0–P3.3, P4.0–P4.3, P5.0–P5.3, P6.0–P6.3, P7.0–P7.3)

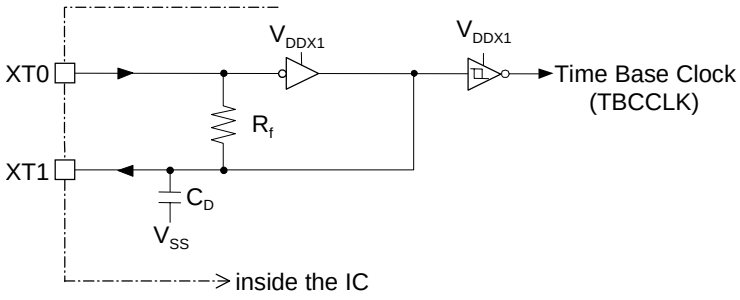


(3) I/O Port (P8.0–P8.3, P9.0–P9.3, PA.0–PA.3, PB.0–PB.3, PC.0–PC.3, PE.0–PE.3)

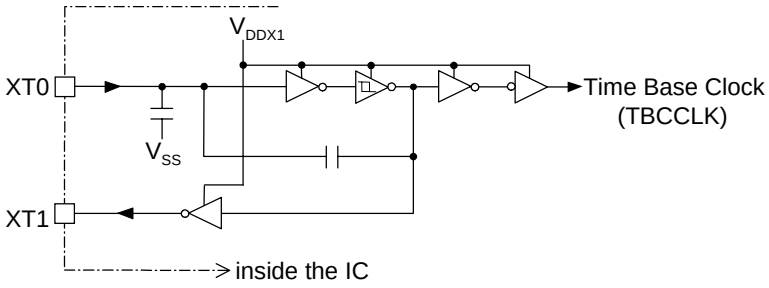


(4) Low-Speed Oscillation Circuit

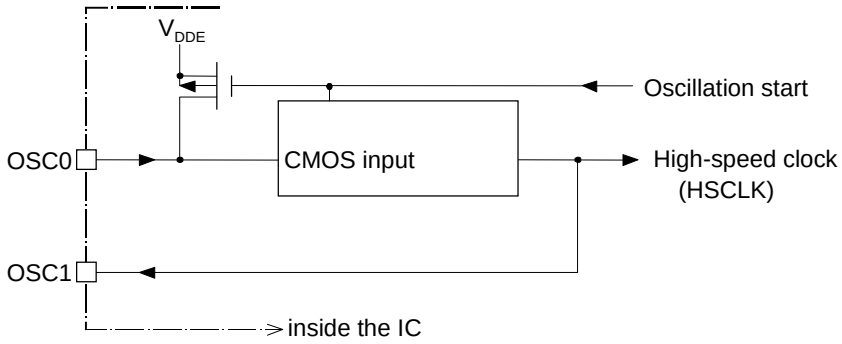
Crystal oscillation mode



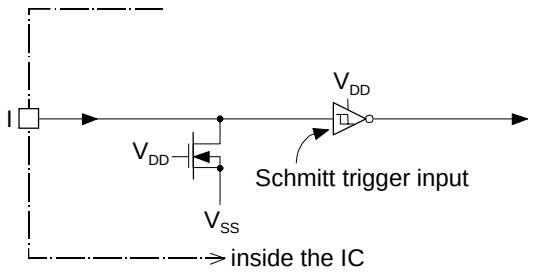
RC oscillation mode



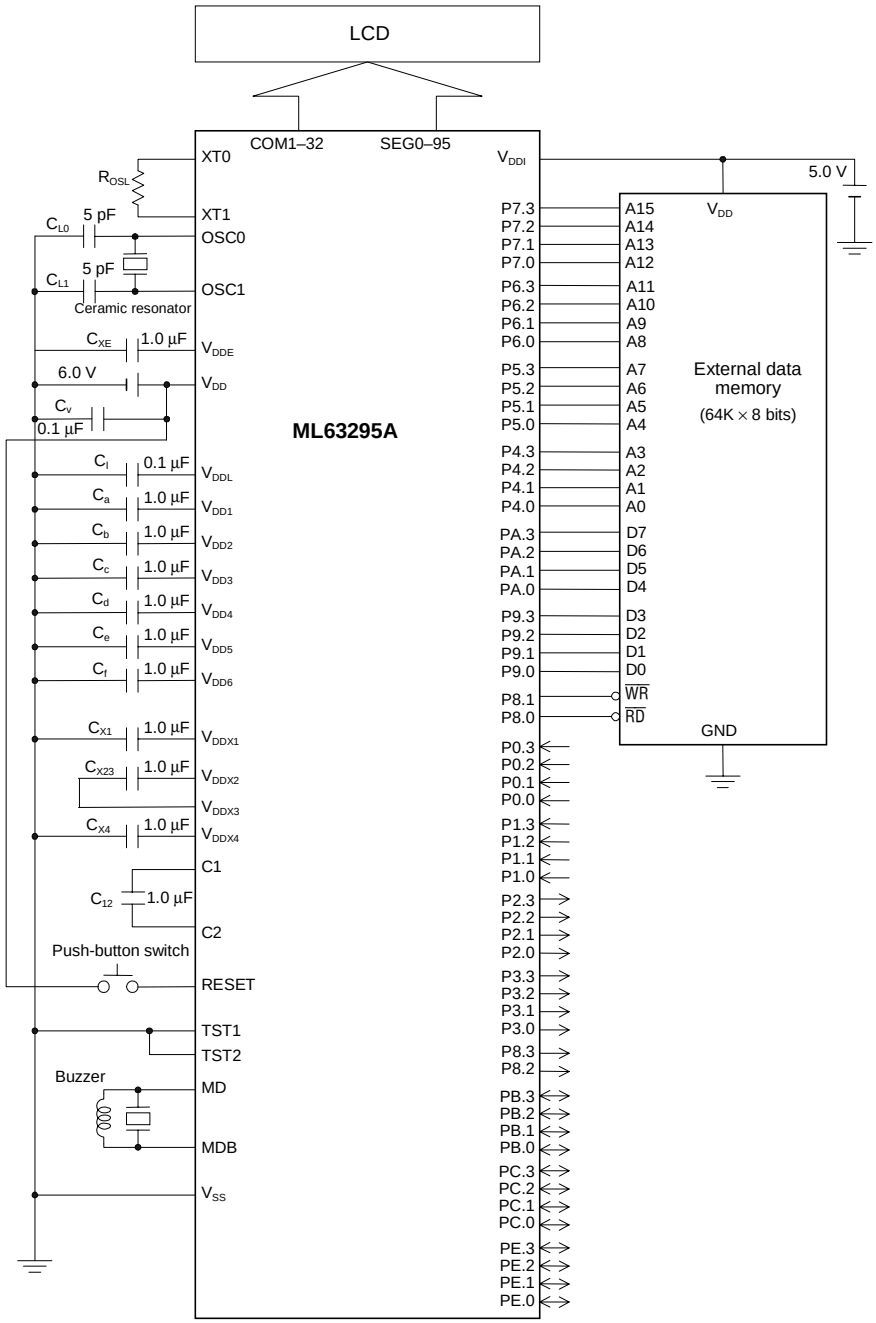
(5) High-Speed Oscillation Circuit



(6) RESET, TST1, and TST2 Inputs



Appendix D Peripheral Circuit Example



- RC oscillation is selected by mask option for low-speed oscillation.
- The power supply for the ports is shared with V_{DD}.
- C_V is an IC power supply bypass capacitor.
- Capacitance values for C_a, C_b, C_c, C_d, C_e, C_f, C_X, C_{X23}, C_{X4}, C_{12}, C_l, C_{XE}, C_{L0} and C_{L1} are only for reference.

Figure D-1 Peripheral Circuit Example

Note:

V_{DDI} is the power supply pin for input, output and I/O ports.
V_{DDI} must be connected to the positive power supply pin (V_{DD}) of the chip or the power supply pin of the external equipment.

Appendix E Electrical Characteristics

Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V_{DD1}	Ta = 25°C	–0.3 to +1.5	V
Power Supply Voltage 2	V_{DD2}	Ta = 25°C	–0.3 to +2.5	V
Power Supply Voltage 3	V_{DD3}	Ta = 25°C	–0.3 to +6.5	V
Power Supply Voltage 4	V_{DD4}	Ta = 25°C	–0.3 to +4.5	V
Power Supply Voltage 5	V_{DD5}	Ta = 25°C	–0.3 to +5.5	V
Power Supply Voltage 6	V_{DD6}	Ta = 25°C	–0.3 to +6.5	V
Power Supply Voltage 7	V_{DDX1}	Ta = 25°C	–0.3 to +2.0	V
Power Supply Voltage 8	V_{DDX4}	Ta = 25°C	–0.3 to +6.5	V
Power Supply Voltage 9	V_{DD}	Ta = 25°C	–0.3 to +7.5	V
Power Supply Voltage 10	V_{DDI}	Ta = 25°C	–0.3 to +6.0	V
Power Supply Voltage 11	V_{DDL}	Ta = 25°C	–0.3 to +6.0	V
Power Supply Voltage 12	V_{DDE}	Ta = 25°C	–0.3 to +6.0	V
Input Voltage 1	V_{IN1}	V_{DD} input, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Input Voltage 2	V_{IN2}	V_{DDI} input, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output Voltage 1	V_{OUT1}	V_{DD1} output, Ta = 25°C	–0.3 to V_{DD1} + 0.3	V
Output Voltage 2	V_{OUT2}	V_{DD2} output, Ta = 25°C	–0.3 to V_{DD2} + 0.3	V
Output Voltage 3	V_{OUT3}	V_{DD3} output, Ta = 25°C	–0.3 to V_{DD3} + 0.3	V
Output Voltage 4	V_{OUT4}	V_{DD4} output, Ta = 25°C	–0.3 to V_{DD4} + 0.3	V
Output Voltage 5	V_{OUT5}	V_{DD5} output, Ta = 25°C	–0.3 to V_{DD5} + 0.3	V
Output Voltage 6	V_{OUT6}	V_{DD6} output, Ta = 25°C	–0.3 to V_{DD6} + 0.3	V
Output Voltage 7	V_{OUT7}	V_{DDX1} output, Ta = 25°C	–0.3 to V_{DDX1} + 0.3	V
Output Voltage 8	V_{OUT8}	V_{DDX4} output, Ta = 25°C	–0.3 to V_{DDX4} + 0.3	V
Output Voltage 9	V_{OUT11}	V_{DD} output, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Output Voltage 10	V_{OUT12}	V_{DDI} output, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output Voltage 11	V_{OUT13}	V_{DDE} output, Ta = 25°C	–0.3 to V_{DDE} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

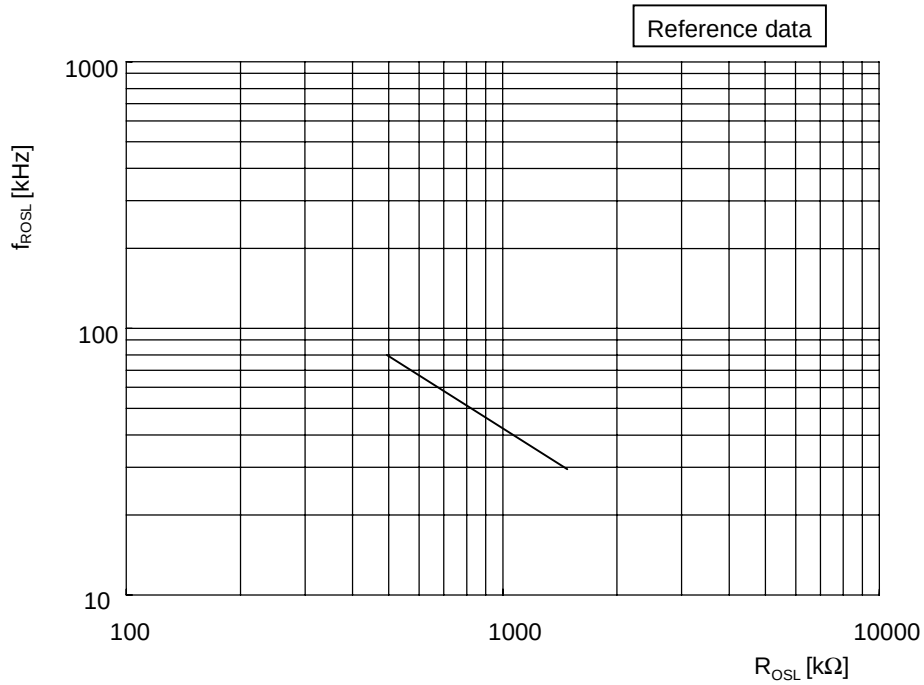
Recommended Operating Conditions

(V_{SS} = 0 V)

Parameter	Symbol	Condition		Range	Unit
Operating Temperature	T_{OP}	—		–20 to +70	°C
Operating Voltage	V_{DD}	—		3.5 to 7.2	V
	V_{DDI}	—		1.8 to 5.5	V
Crystal Oscillation Frequency	f_{XT}	C_G = 5 to 25 pF		32.768 to 76.8	kHz
Low-Speed RC Oscillation Frequency	f_{ROSL}	R_{OSL} = 1.5 MΩ		32k ±30%	Hz
		R_{OSL} = 700 kΩ		60k ±30%	
		R_{OSL} = 500 kΩ		80k ±30%	
Ceramic Oscillation Frequency	f_{CM}	V_{DD} = 3.5 to 7.2 V		200k to 2M	Hz
High-Speed RC Oscillation Frequency	f_{ROSH}	V_{DD} = 3.5 to 7.2 V	R_{OSH} = 100 kΩ	700k ±30%	Hz
			R_{OSH} = 75 kΩ	1M ±30%	
			R_{OSH} = 51 kΩ	1.35M ±30%	
			R_{OSH} = 30 kΩ	2M ±30%	

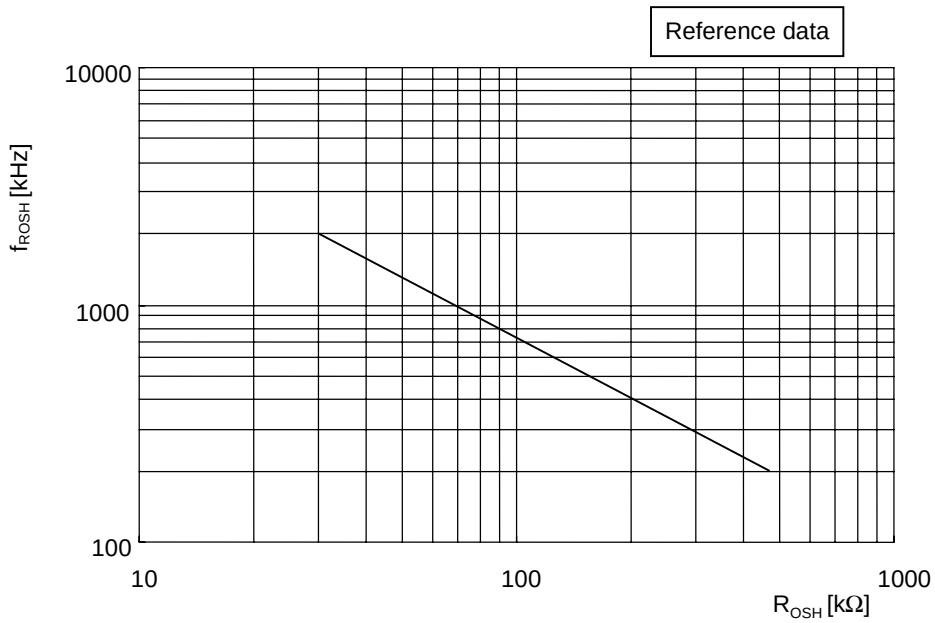
- Typical characteristics of low-speed RC oscillation

(V_{DD} = 6.0 V, V_{DDI} = 3.0 V)



- Typical characteristics of high-speed RC oscillation

(V_{DD} = 6.0 V, V_{DDI} = 3.0 V)



DC Characteristics

(V_{DD} = 3.5 to 7.2 V, V_{DDI} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DDE} Voltage	V_{DDE}	I_{OUT} = 0 to 15 mA, Ta = 25°C	2.7	3.0	3.3	V	1
V_{DDE} Voltage Temperature Deviation	ΔV_{DDE}	—	—	–4.0	—	mV/°C	
V_{DDL} Voltage	V_{DDL}	High-speed clock oscillation stopped	1.0	1.5	2.0	V	
		During operation at high-speed clock oscillation (V_{DD} = 3.5 to 7.2 V)	1.2	—	3.3		
Crystal Oscillation Start Voltage	V_{STA}	Oscillation start time: within 5 seconds	3.5	—	—		
Crystal Oscillation Hold Voltage	V_{HOLD}	—	3.5	—	—		
Crystal Oscillation Stop Detect Time	T_{STOP}	—	0.1	—	5.0	ms	
External Crystal Oscillator Capacitance	C_G	—	5	—	25	pF	
Internal Crystal Oscillator Capacitance	C_D	—	20	25	30		
External Ceramic Oscillator Capacitance	C_{L0}, C_{L1}	CSA2.00MG (Murata MFG.-make) used V_{DDE} = 3.0 V	—	30	—		
Internal RC Oscillator Capacitance	C_{OS}	—	8	12	16		
POR Voltage	V_{POR1}	V_{DD} = 6.0 V	0	—	0.7	V	
Non-POR Voltage	V_{POR2}	V_{DD} = 6.0 V	2.0	—	6.0		
BLD Judgment Voltage	V_{BLDC}	LD1 = 1, LD0 = 1, Ta = 25°C	5.00	5.10	5.20	V	—
		LD1 = 1, LD0 = 0, Ta = 25°C	4.40	4.50	4.60		
BLD Judgment Voltage Temperature Deviation	ΔV_{BLDC}	V_{BLDC} = 5.10 V (LD1 = 1, LD0 = 1)	—	–3.5	—	mV/°C	
		V_{BLDC} = 4.50 V (LD1 = 1, LD0 = 0)	—	–2.3	—		

Notes: 1. "T_{STOP}" indicates that if the crystal oscillator stops over the value of T_{STOP}, the system reset occurs.
2. "POR" denotes Power On Reset.
3. "V_{POR1}" indicates that POR occurs when V_{DD} falls from V_{DD} to V_{POR1} and again rises up to V_{DD}
4. "V_{POR2}" indicates that POR does not occur when V_{DD} falls from V_{DD} to V_{POR2} and again rises up to V_{DD}.

DC Characteristics (continued)

(V_{DD} = 6.0 V, V_{DDI} = 3.0 V, V_{SS} = 0 V, 1/6 bias, DSPCNT = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU in HALT state, LCD is being driven, no panel load (Crystal oscillation: 32.768 kHz) (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	11.0	14.5	µA	1
			Ta = –20 to +70°C	—	11.0	19.5		
		CPU in HALT state, LCD is being driven, no panel load (RC oscillation: R_{OSL} = 1.5 MΩ) (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	14.5	18.0		
			Ta = –20 to +70°C	—	14.5	23.0		
Supply Current 2	I_{DD2}	CPU in HALT state, LCD in Power Down mode (Crystal oscillation: 32.768 kHz) (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	4.0	5.0		
			Ta = –20 to +70°C	—	4.0	6.5		
		CPU in HALT state, LCD in Power Down mode (RC oscillation: R_{OSL} = 1.5 MΩ) (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	7.0	8.0		
			Ta = –20 to +70°C	—	7.0	9.5		
Supply Current 3	I_{DD3}	CPU operating at low speed, LCD is being driven, no panel load (Crystal oscillation: 32.768 kHz) (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	20.5	29.0		
			Ta = –20 to +70°C	—	20.5	34.0		
		CPU operating at low speed, LCD is being driven, no panel load (RC oscillation: R_{OSL} = 1.5 MΩ) (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	24.5	33.0		
			Ta = –20 to +70°C	—	24.5	38.0		
Supply Current 4	I_{DD4}	CPU operating at high-speed oscillation (1 MHz RC oscillation, R_{OSH} = 75 kΩ)		—	1100	1700		
Supply Current 5	I_{DD5}	CPU operating at high-speed oscillation (2 MHz ceramic oscillation)		—	1500	2000		

DC Characteristics (continued)

(V_{DD} = 3.5 to 7.2 V, V_{DDI} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DD6} Voltage	V_{DD6}	1/6 bias, 1/5 bias	4.0	4.1	4.2	V	1
V_{DD5} Voltage	V_{DD5}	1/6 bias	Typ. – 0.1	5/6 × V_{DD6}	Typ. + 0.1		
		1/5 bias	Typ. – 0.1	4/5 × V_{DD6}	Typ. + 0.1		
V_{DD4} Voltage	V_{DD4}	1/6 bias	Typ. – 0.1	4/6 × V_{DD6}	Typ. + 0.1		
		1/5 bias	Typ. – 0.1	3/5 × V_{DD6}	Typ. + 0.1		
V_{DD2} Voltage	V_{DD2}	1/6 bias	Typ. – 0.1	2/6 × V_{DD6}	Typ. + 0.1		
		1/5 bias	Typ. – 0.1	2/5 × V_{DD6}	Typ. + 0.1		
V_{DD1} Voltage	V_{DD1}	1/6 bias	Typ. – 0.1	1/6 × V_{DD6}	Typ. + 0.1		
		1/5 bias	Typ. – 0.1	1/5 × V_{DD6}	Typ. + 0.1		

Note: "V_{DD6}" changes in the range from 4.10 to 6.14 V (Typ. value) according to the value of Display Contrast register (DSPCNT).

(V_{DD} = 3.5 to 7.2 V, V_{DDI} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DDE} Voltage Temperature Deviation	ΔV_{DDE}	—	—	–4.0	—	mV/°C	1
V_{DD6} Voltage	V_{DD6}	1/6 bias, 1/5 bias	3.6	4.1	4.6	V	
V_{DD5} Voltage	V_{DD5}	1/6 bias	Typ. – 0.5	5/6 × V_{DD6}	Typ. + 0.5		
		1/5 bias	Typ. – 0.5	4/5 × V_{DD6}	Typ. + 0.5		
V_{DD4} Voltage	V_{DD4}	1/6 bias	Typ. – 0.5	4/6 × V_{DD6}	Typ. + 0.5		
		1/5 bias	Typ. – 0.5	3/5 × V_{DD6}	Typ. + 0.5		
V_{DD2} Voltage	V_{DD2}	1/6 bias	Typ. – 0.5	2/6 × V_{DD6}	Typ. + 0.5		
		1/5 bias	Typ. – 0.5	2/5 × V_{DD6}	Typ. + 0.5		
V_{DD1} Voltage	V_{DD1}	1/6 bias	Typ. – 0.5	1/6 × V_{DD6}	Typ. + 0.5		
		1/5 bias	Typ. – 0.5	1/5 × V_{DD6}	Typ. + 0.5		

Note: "V_{DD6}" changes in the range from 4.10 to 6.14 V (Typ. value) according to the value of Display Contrast register (DSPCNT).

- Contrast control voltage (V_{DD6} voltage)

Ta = 25°C, V_{DD6} = 4.1 V (Typ.)

DSPCNT					V_{DD6} Voltage (V)			Display Contrast
CN0 to CN3	CN3	CN2	CN1	CN0	Min.	Typ.	Max.	
0H	0	0	0	0	—	4.1	—	Light
1H	0	0	0	1	Typ. – 0.1	4.2	Typ. + 0.1	
2H	0	0	1	0	Typ. – 0.1	4.3	Typ. + 0.1	
3H	0	0	1	1	Typ. – 0.1	4.4	Typ. + 0.1	
4H	0	1	0	0	Typ. – 0.1	4.5	Typ. + 0.1	
5H	0	1	0	1	Typ. – 0.1	4.62	Typ. + 0.1	
6H	0	1	1	0	Typ. – 0.1	4.74	Typ. + 0.1	
7H	0	1	1	1	Typ. – 0.1	4.86	Typ. + 0.1	
8H	1	0	0	0	Typ. – 0.1	5.00	Typ. + 0.1	
9H	1	0	0	1	Typ. – 0.1	5.14	Typ. + 0.1	
0AH	1	0	1	0	Typ. – 0.1	5.29	Typ. + 0.1	
0BH	1	0	1	1	Typ. – 0.1	5.44	Typ. + 0.1	
0CH	1	1	0	0	Typ. – 0.1	5.60	Typ. + 0.1	
0DH	1	1	0	1	Typ. – 0.1	5.77	Typ. + 0.1	
0EH	1	1	1	0	Typ. – 0.1	5.95	Typ. + 0.1	
0FH	1	1	1	1	Typ. – 0.1	6.14	Typ. + 0.1	Dark

Ta = 25°C, V_{DD6} = 4.0 V (Min.)

DSPCNT					V_{DD6} Voltage (V)			Display Contrast
CN0 to CN3	CN3	CN2	CN1	CN0	Min.	Typ.	Max.	
0H	0	0	0	0	—	4.0	—	Light
1H	0	0	0	1	Typ. – 0.1	4.1	Typ. + 0.1	
2H	0	0	1	0	Typ. – 0.1	4.2	Typ. + 0.1	
3H	0	0	1	1	Typ. – 0.1	4.3	Typ. + 0.1	
4H	0	1	0	0	Typ. – 0.1	4.4	Typ. + 0.1	
5H	0	1	0	1	Typ. – 0.1	4.52	Typ. + 0.1	
6H	0	1	1	0	Typ. – 0.1	4.64	Typ. + 0.1	
7H	0	1	1	1	Typ. – 0.1	4.76	Typ. + 0.1	
8H	1	0	0	0	Typ. – 0.1	4.90	Typ. + 0.1	
9H	1	0	0	1	Typ. – 0.1	5.04	Typ. + 0.1	
0AH	1	0	1	0	Typ. – 0.1	5.19	Typ. + 0.1	
0BH	1	0	1	1	Typ. – 0.1	5.34	Typ. + 0.1	
0CH	1	1	0	0	Typ. – 0.1	5.50	Typ. + 0.1	
0DH	1	1	0	1	Typ. – 0.1	5.67	Typ. + 0.1	
0EH	1	1	1	0	Typ. – 0.1	5.85	Typ. + 0.1	
0FH	1	1	1	1	Typ. – 0.1	6.04	Typ. + 0.1	Dark

- Contrast control voltage (V_{DD6} voltage)

Ta = 25°C, V_{DD6} = 4.2 V (Max.)

DSPCNT					V_{DD6} Voltage (V)			Display Contrast
CN0 to CN3	CN3	CN2	CN1	CN0	Min.	Typ.	Max.	
0H	0	0	0	0	—	4.2	—	Light
1H	0	0	0	1	Typ. – 0.1	4.3	Typ. + 0.1	
2H	0	0	1	0	Typ. – 0.1	4.4	Typ. + 0.1	
3H	0	0	1	1	Typ. – 0.1	4.5	Typ. + 0.1	
4H	0	1	0	0	Typ. – 0.1	4.6	Typ. + 0.1	
5H	0	1	0	1	Typ. – 0.1	4.72	Typ. + 0.1	
6H	0	1	1	0	Typ. – 0.1	4.84	Typ. + 0.1	
7H	0	1	1	1	Typ. – 0.1	4.96	Typ. + 0.1	
8H	1	0	0	0	Typ. – 0.1	5.10	Typ. + 0.1	
9H	1	0	0	1	Typ. – 0.1	5.24	Typ. + 0.1	
0AH	1	0	1	0	Typ. – 0.1	5.39	Typ. + 0.1	
0BH	1	0	1	1	Typ. – 0.1	5.54	Typ. + 0.1	
0CH	1	1	0	0	Typ. – 0.1	5.70	Typ. + 0.1	
0DH	1	1	0	1	Typ. – 0.1	5.87	Typ. + 0.1	
0EH	1	1	1	0	Typ. – 0.1	6.05	Typ. + 0.1	
0FH	1	1	1	1	Typ. – 0.1	6.24	Typ. + 0.1	Dark

DC Characteristics (continued)

(V_{DD} = 6.0 V, V_{DDI} = V_{DDE} = 3.0 V, V_{DD1} = 1.0 V, V_{DD2} = 2.0 V, V_{DD3} = 3.0 V, V_{DD4} = 4.0 V, V_{DD5} = 5.0 V, V_{DD6} = 6.0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P2.0 to P2.3) ⋮ (PC.0 to PC.3) (PE.0 to PE.3)	I_{OH1}	$V_{OH1} = V_{DDI} – 0.5$ V	V_{DDI} = 3.0 V	–6.0	–3.5	–1.0	mA	2
			V_{DDI} = 5.0 V	–8.5	–5.0	–1.5		
	I_{OL1}	V_{OL1} = 0.5 V	V_{DDI} = 3.0 V	1.0	3.0	6.0		
			V_{DDI} = 5.0 V	1.5	3.7	8.5		
Output Current 2 (MD, MDB)	I_{OH2}	$V_{OH2} = V_{DDE} – 0.7$ V	V_{DDE} = 3.0 V	–11.0	–6.0	–2.0		
	I_{OL2}	V_{OL2} = 0.7 V	V_{DDE} = 3.0 V	2.0	5.5	11.0		
Output Current 3 (SEG0 to SEG95) (COM1 to COM32)	I_{OH3}	$V_{OH3} = V_{DD6} – 0.2$ V (V_{DD6} level)		—	—	–4	µA	
	I_{OHM3}	$V_{OHM3} = V_{DD5} + 0.2$ V (V_{DD5} level)		4	—	—		
	I_{OHM3S}	$V_{OHM3S} = V_{DD5} – 0.2$ V (V_{DD5} level)		—	—	–4		
	I_{OMH3}	$V_{OMH3} = V_{DD4} + 0.2$ V (V_{DD4} level)		4	—	—		
	I_{OMH3S}	$V_{OMH3S} = V_{DD4} – 0.2$ V (V_{DD4} level)		—	—	–4		
	I_{OML3}	$V_{OML3} = V_{DD2} + 0.2$ V (V_{DD2} level)		4	—	—		
	I_{OML3S}	$V_{OML3S} = V_{DD2} – 0.2$ V (V_{DD2} level)		—	—	–4		
	I_{OLM3}	$V_{OLM3} = V_{DD1} + 0.2$ V (V_{DD1} level)		4	—	—		
	I_{OLM3S}	$V_{OLM3S} = V_{DD1} – 0.2$ V (V_{DD1} level)		—	—	–4		
	I_{OL3}	$V_{OL3} = V_{SS} + 0.2$ V (V_{SS} level)		4	—	—		
Output Current 4 (OSC1)	I_{OH4R}	$V_{OH4R} = V_{DDE} – 0.5$ V (RC oscillation)	V_{DDE} = 3.0 V	–2.50	–1.30	–0.25	mA	
	I_{OL4R}	V_{OL4R} = 0.5 V (RC oscillation)	V_{DDE} = 3.0 V	0.25	1.50	2.50		
	I_{OH4C}	$V_{OH4C} = V_{DDE} – 0.5$ V (ceramic oscillation)	V_{DDE} = 3.0 V	–300	–120	–60	µA	
	I_{OL4C}	V_{OL4C} = 0.5 V (ceramic oscillation)	V_{DDE} = 3.0 V	60	120	300		
Output Leakage Current (P2.0 to P2.3) ⋮ (PC.0 to PC.3) (PE.0 to PE.3)	I_{OOH}	$V_{OH} = V_{DDI}$		—	—	0.3		
	I_{OOL}	$V_{OL} = V_{SS}$		–0.3	—	—		

DC Characteristics (continued)

(V_{DD} = 6.0 V, V_{DDI} = V_{DDE} = 3.0 V, V_{DD1} = 1.0 V, V_{DD2} = 2.0 V, V_{DD3} = 3.0 V, V_{DD4} = 4.0 V, V_{DD5} = 5.0 V, V_{DD6} = 6.0 V, Ta = –20 to +70°C unless otherwise specified)

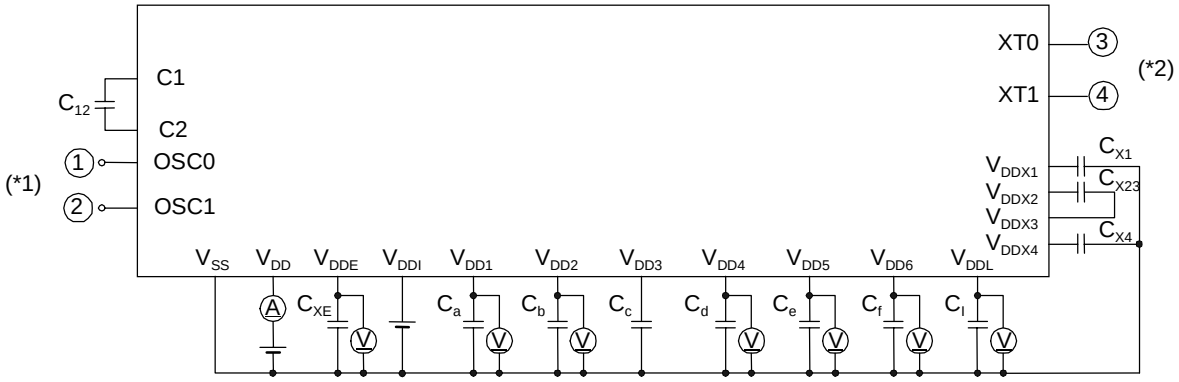
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) ⋮ (PC.0 to PC.3) (PE.0 to PE.3)	I_{IH1}	V_{IH1} = V_{DDI} (when pulled down)	V_{DDI} = 3.0 V	10	20	40	µA	3
			V_{DDI} = 5.0 V	20	60	120		
	I_{IL1}	V_{IL1} = V_{SS} (when pulled up)	V_{DDI} = 3.0 V	–40	–20	–10		
			V_{DDI} = 5.0 V	–120	–60	–20		
	I_{IH1Z}	V_{IH1} = V_{DDI} (in a high impedance state)		0	—	1.0		
	I_{IL1Z}	V_{IL1} = V_{SS} (in a high impedance state)		–1.0	—	0		
Input Current 2 (OSC0)	I_{IL2}	V_{IL2} = V_{SS} (when pulled up)	V_{DDE} = 3.0 V	–350	–170	–30		
	I_{IH2R}	V_{IH2R} = V_{DDE} (RC oscillation)		0	—	1.0		
	I_{IL2R}	V_{IL2R} = V_{SS} (RC oscillation)		–1.0	—	0		
	I_{IH2C}	V_{IH2R} = V_{DDE} (ceramic oscillation)		0.1	0.5	1.0		
	I_{IL2C}	V_{IL2R} = V_{SS} (ceramic oscillation)		–1.0	–0.5	–0.1		
Input Current 3 (RESET)	I_{IH3}	V_{IH3} = V_{DD}	V_{DD} = 6.0 V	40	60	150		
	I_{IL3}	V_{IL3} = V_{SS}		–1.0	—	0		
Input Current 4 (TST1, TST2)	I_{IH4}	V_{IH4} = V_{DD}	V_{DD} = 6.0 V	4.0	12.0	16.0	mA	
	I_{IL4}	V_{IL4} = V_{SS}		–1.0	—	0	µA	

DC Characteristics (continued)

(V_{DD} = 6.0 V, V_{DDI} = V_{DDE} = 3.0 V, V_{DD1} = 1.0 V, V_{DD2} = 2.0 V, V_{DD3} = 3.0 V, V_{DD4} = 4.0 V, V_{DD5} = 5.0 V, V_{DD6} = 6.0 V, Ta = –20 to +70°C unless otherwise specified)

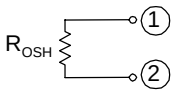
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) ⋮ (PC.0 to PC.3) (PE.0 to PE.3)	V_{IH1}	V_{DDI} = 3.0 V	2.3	—	3.0	V	4
		V_{DDI} = 5.0 V	3.8	—	5.0		
	V_{IL1}	V_{DDI} = 3.0 V	0	—	0.7		
		V_{DDI} = 5.0 V	0	—	1.2		
Input Voltage 2 (OSC0)	V_{IH2}	V_{DDE} = 3.0 V	2.4	—	3.0		
	V_{IL2}		0	—	0.6		
Input Voltage 3 (RESET, TST1, TST2)	V_{IH3}	V_{DD} = 6.0 V	4.8	—	6.0		
	V_{IL3}		0	—	1.2		
Hysteresis Width 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) ⋮ (PC.0 to PC.3) (PE.0 to PE.3)	ΔV_{T1}	V_{DDI} = 3.0 V	0.2	0.5	1.0		
		V_{DDI} = 5.0 V	0.25	1.00	1.50		
Hysteresis Width 2 (RESET, TST1, TST2)	ΔV_{T2}	V_{DD} = 5.0 V	0.25	1.00	1.50		
Input Pin Capacitance (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) ⋮ (PC.0 to PC.3) (PE.0 to PE.3)	C_{IN}	—	—	—	5	pF	—

Measuring circuit 1

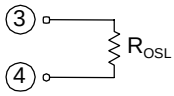


C_{X1}, C_{X23}, C_{X4}, C_{XE}	: 1.0 µF
C_a, C_b, C_c, C_d, C_e, C_f, C_{12}	: 1.0 µF
C_l	: 0.1 µF
C_G	: 15 pF
C_{L0}	: 30 pF
C_{L1}	: 30 pF
Ceramic resonator	: CSA2.00MG (2 MHz) : CSB1000J (1 MHz) (Murata MFG.-make)

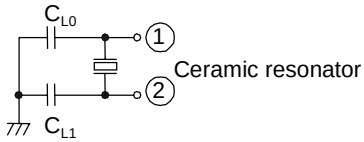
*1 RC Oscillator



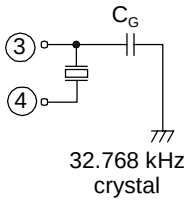
*2 RC Oscillator



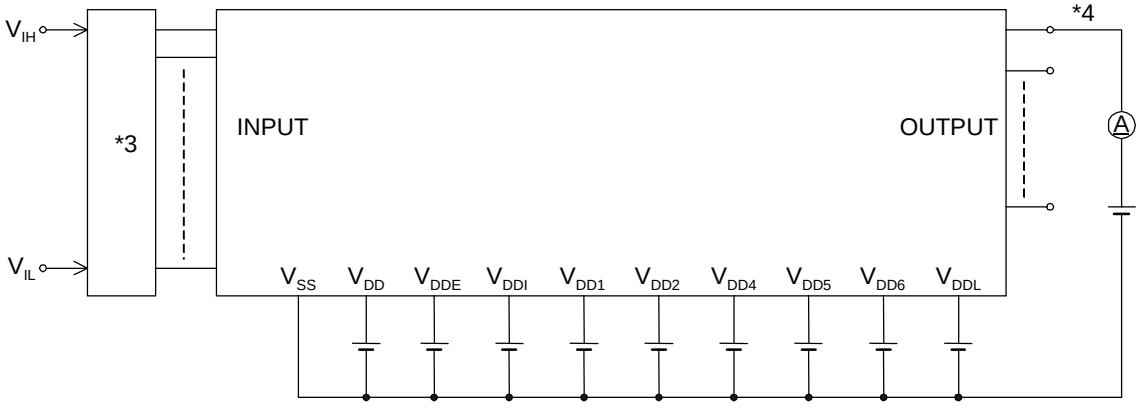
Ceramic Oscillator



Crystal Oscillator



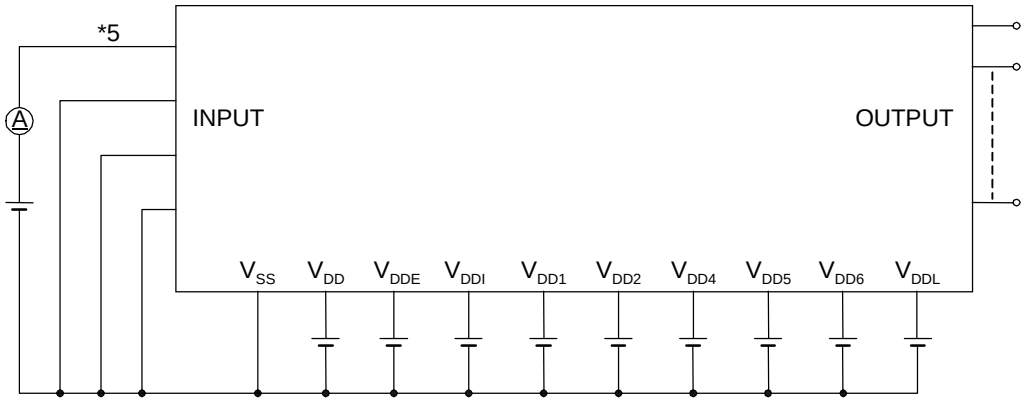
Measuring circuit 2



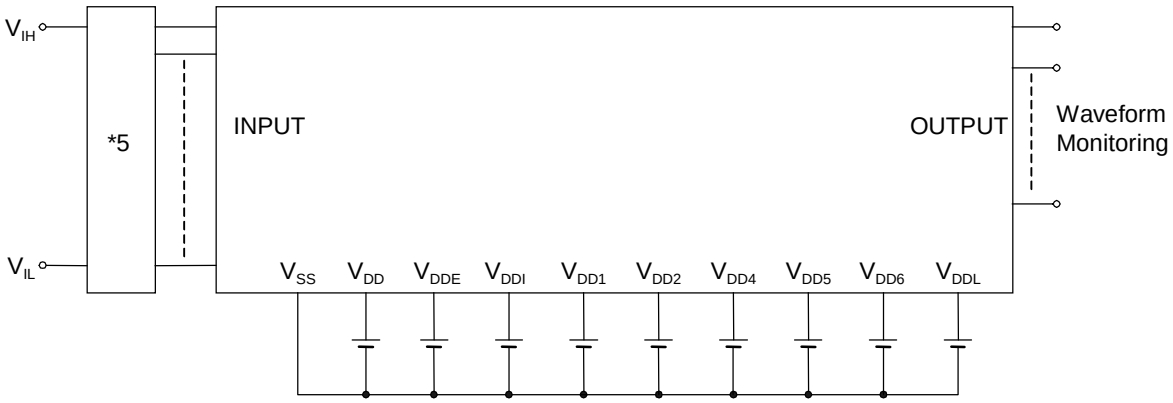
*3 Input logic circuit to determine the specified measuring conditions.

*4 Measured at the specified output pins.

Measuring circuit 3



Measuring circuit 4



*5 Measured at the specified input pins.

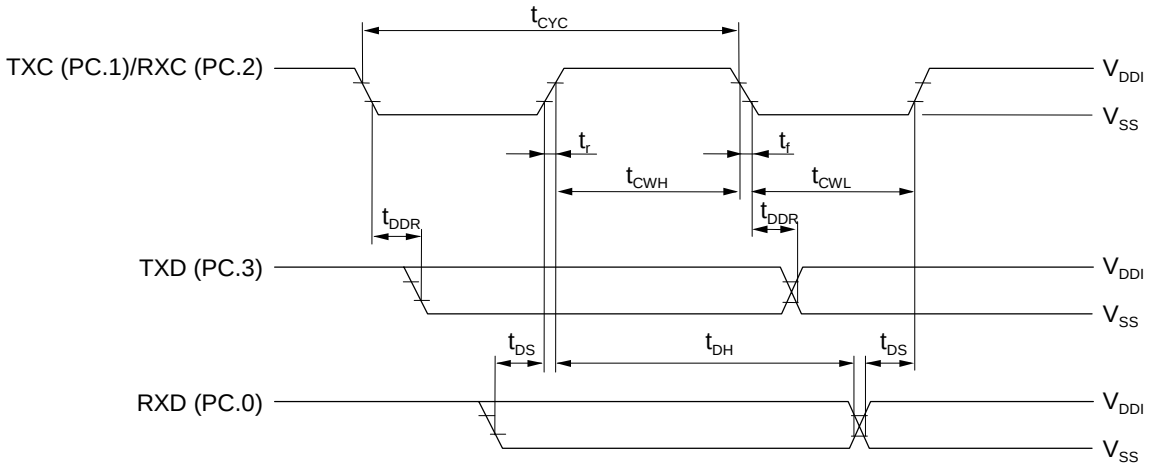
AC Characteristics (Serial Interface, Serial Port)

(V_{DD} = 3.5 to 7.2 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

(1) Synchronous Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TXC/RXC Input Fall Time	t_f	—	—	—	1.0	µs
TXC/RXC Input Rise Time	t_r	—	—	—	1.0	µs
TXC/RXC Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	µs
TXC/RXC Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	µs
TXC/RXC Input Cycle Time	t_{CYC}	—	2.0	—	—	µs
TXC/RXC Output Cycle Time	$t_{CYC1(O)}$	CPU operating at 32.768 kHz	—	30.5	—	µs
	$t_{CYC2(O)}$	CPU operating at 2 MHz	—	0.5	—	µs
TXD Output Delay Time	t_{DDR}	Output load capacitance 10 pF	—	—	0.4	µs
RXD Input Setup Time	t_{DS}	—	0.5	—	—	µs
RXD Input Hold Time	t_{DH}	—	0.8	—	—	µs

Synchronous communication timing waveforms
("H" level = 4.0 V, "L" level = 1.0 V)

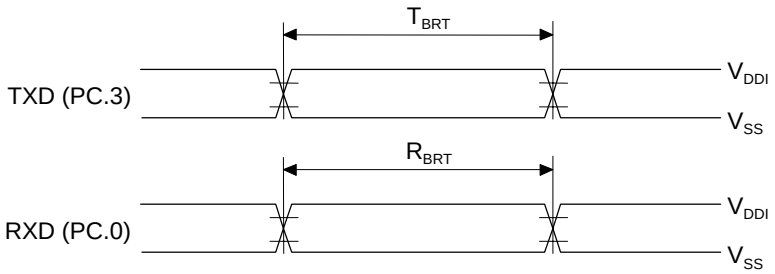


(2) UART Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Baud Rate	T_{BRT}	$T_{BRT} = 1/f_{BRT}$ $T_{CR} = 1/f_{OSC}$	$T_{BRT} - T_{CR}$	T_{BRT}	$T_{BRT} + T_{CR}$	s
Receive Baud Rate	R_{BRT}	$R_{BRT} = 1/f_{BRT}$	$R_{BRT} \times 0.97$	R_{BRT}	$R_{BRT} \times 1.03$	s

f_{BRT}: Baud rates (1200, 2400, 4800, 9600 bps)

UART communication timing waveforms
("H" level = 4.0 V, "L" level = 1.0 V)

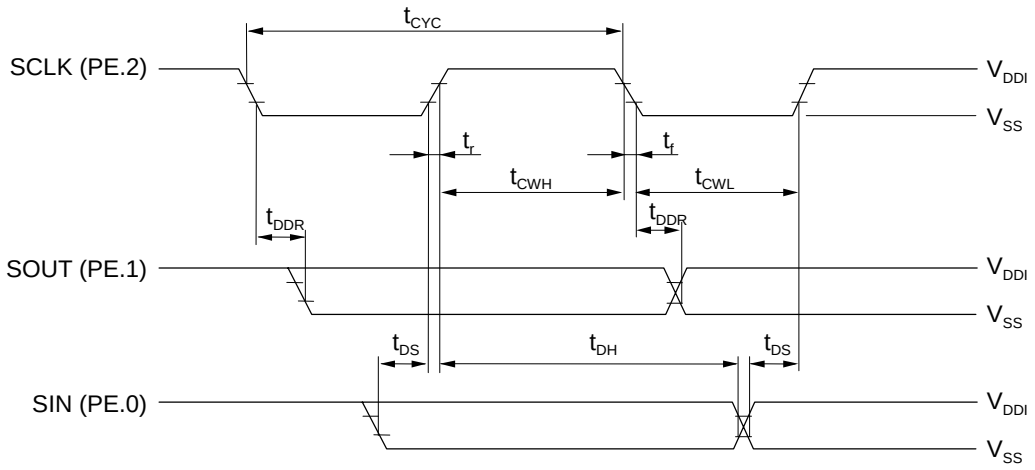


AC Characteristics (Serial Interface, Shift Register)

(V_{DD} = 3.5 to 7.2 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK Input Fall Time	t_f	—	—	—	1.0	µs
SCLK Input Rise Time	t_r	—	—	—	1.0	µs
SCLK Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	µs
SCLK Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	µs
SCLK Input Cycle Time	t_{CYC}	V_{DDI} = V_{DDE} to 5.5 V	1.8	—	—	µs
SCLK Output Cycle Time	$t_{CYC1(O)}$	CPU operating at 32.768 kHz	—	30.5	—	µs
	$t_{CYC2(O)}$	CPU operating at 2 MHz	—	0.5	—	µs
SOUT Output Delay Time	t_{DDR}	Output load capacitance 10 pF	—	—	0.4	µs
SIN Input Setup Time	t_{DS}	—	0.5	—	—	µs
SIN Input Hold Time	t_{DH}	—	0.8	—	—	µs

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)



AC Characteristics (External Memory Interface)

(V_{DD} = 3.5 to 7.2 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

(1) For Reading from External Memory

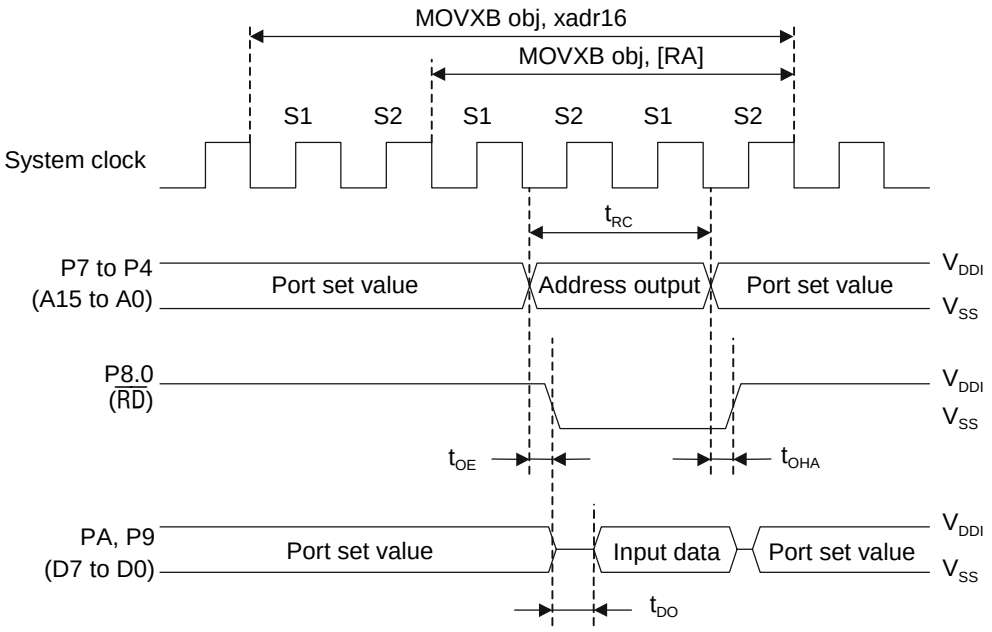
(a) When the CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	—	61.0	—	µs
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	5.0	
Output Enable Time	t_{OHA}	—	—	—	5.0	
External Memory Output Delay Time	t_{DO}	—	—	—	5.0	

(b) When the CPU operates at 2 MHz (V_{DD} = 3.5 to 7.2 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	1.0	—	—	µs
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	100	ns
Output Enable Time	t_{OHA}	—	—	—	100	
External Memory Output Delay Time	t_{DO}	—	—	—	150	

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)



(2) For Writing to External Memory

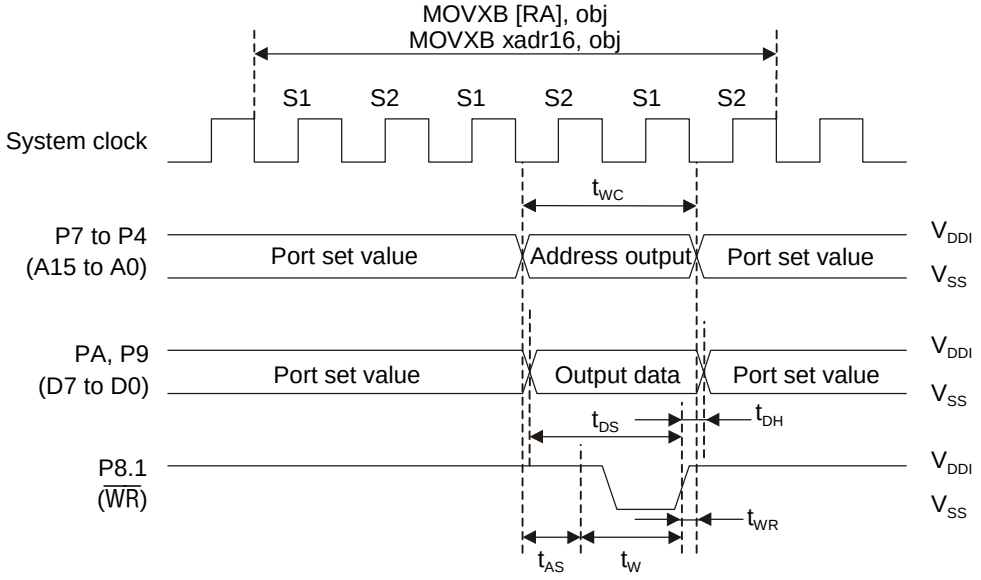
(a) When the CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	—	61.0	—	µs
Address Setup Time	t_{AS}	—	—	30.5	—	
Write Time	t_{W}	—	—	15.3	—	
Write Recovery Time	t_{WR}	—	—	15.3	—	
Data Setup Time	t_{DS}	—	—	45.8	—	
Data Hold Time	t_{DH}	—	—	15.3	—	

(b) When the CPU operates at 2 MHz (V_{DD} = 3.5 to 7.2 V)

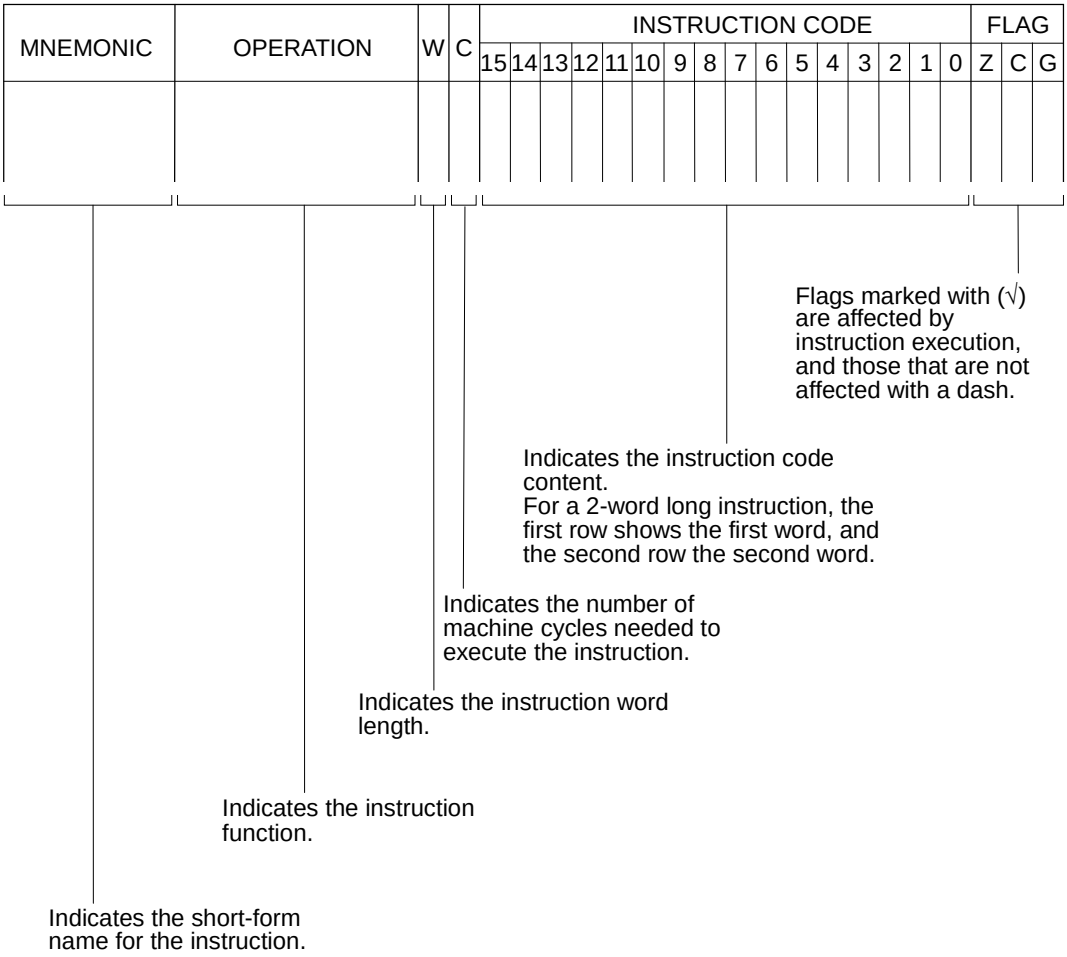
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	1.0	—	—	µs
Address Setup Time	t_{AS}	—	0.4	—	—	
Write Time	t_{W}	—	0.2	—	—	
Write Recovery Time	t_{WR}	—	0.2	—	—	
Data Setup Time	t_{DS}	—	0.7	—	—	
Data Hold Time	t_{DH}	—	0.2	—	—	

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)



Appendix F Instruction List

The format used in the list of instructions is indicated below.



Transfer Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOV direct,A	direct ← A	1	1	1	1	0	0	r_{11}	r_{10}	r_9	r_8	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	—	—	—
MOV [HL],A	[HL] ← A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	—	—	—
MOV [XY],A	[XY] ← A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	—	—	—
MOV E:[HL],A	E:[HL] ← A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	—	—	—
MOV E:[XY],A	E:[XY] ← A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	—	—	—
MOV [HL+],A	[HL] ← A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	—	—	√
MOV [XY+],A	[XY] ← A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	—	—	√
MOV E:[HL+],A	E:[HL] ← A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	—	—	√
MOV E:[XY+],A	E:[XY] ← A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	—	—	√
MOV \cur,#i4	cur,A ← i4	1	1	0	1	0	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MOV [HL],#i4	[HL],A ← i4	1	1	0	0	0	0	0	1	1	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
MOV [XY],#i4	[XY],A ← i4	1	1	0	0	0	0	0	1	1	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
MOV E:[HL],#i4	E:[HL],A ← i4	1	1	0	0	0	0	0	1	1	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
MOV E:[XY],#i4	E:[XY],A ← i4	1	1	0	0	0	0	0	1	1	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
MOV [HL+],#i4	[HL],A ← i4, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
MOV [XY+],#i4	[XY],A ← i4, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
MOV E:[HL+],#i4	E:[HL],A ← i4, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
MOV E:[XY+],#i4	E:[XY],A ← i4, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√
MOV A,#i4	A ← i4	1	1	0	0	0	0	0	0	0	1	1	1	0	0	i_3	i_2	i_1	i_0	√	—	—
MOV A,direct	A ← direct	1	1	1	1	0	1	r_{11}	r_{10}	r_9	r_8	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MOV A,[HL]	A ← [HL]	1	1	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	√	—	—
MOV A,[XY]	A ← [XY]	1	1	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	√	—	—
MOV A,E:[HL]	A ← E:[HL]	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	√	—	—
MOV A,E:[XY]	A ← E:[XY]	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	√	—	—
MOV A,[HL+]	A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	√	—	√
MOV A,[XY+]	A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	0	√	—	√
MOV A,E:[HL+]	A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	√	—	√
MOV A,E:[XY+]	A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	√	—	√
XCH A,sfr	A ↔ sfr	1	1	0	0	1	0	1	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	—	—	—
XCH A,\cur	A ↔ cur	1	1	0	0	1	1	1	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	—	—	—
XCH A,[HL]	A ↔ [HL]	1	1	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	—	—	—
XCH A,[XY]	A ↔ [XY]	1	1	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	1	—	—	—
XCH A,E:[HL]	A ↔ E:[HL]	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	—	—	—
XCH A,E:[XY]	A ↔ E:[XY]	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	1	—	—	—
XCH A,[HL+]	A ↔ [HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	1	—	—	√
XCH A,[XY+]	A ↔ [XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	1	—	—	√
XCH A,E:[HL+]	A ↔ E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1	—	—	√
XCH A,E:[XY+]	A ↔ E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	—	—	√

Rotate Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
ROL sfr	C ← {$_3$sfr$_0$} ← C, A ← sfr	1	1	0	0	1	0	0	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ROL \cur	C ← {$_3$cur$_0$} ← C, A ← cur	1	1	0	0	1	1	0	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ROL [HL]	C ← {$_3$[HL]$_0$} ← C, A ← [HL]	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0	√	√	—
ROL [XY]	C ← {$_3$[XY]$_0$} ← C, A ← [XY]	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	0	√	√	—
ROL E:[HL]	C ← {$_3$E:[HL]$_0$} ← C, A ← E:[HL]	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	√	√	—
ROL E:[XY]	C ← {$_3$E:[XY]$_0$} ← C, A ← E:[XY]	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	√	√	—
ROL [HL+]	C ← {$_3$[HL]$_0$} ← C, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1	0	√	√	√
ROL [XY+]	C ← {$_3$[XY]$_0$} ← C, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	√	√	√
ROL E:[HL+]	C ← {$_3$E:[HL]$_0$} ← C, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	√	√	√
ROL E:[XY+]	C ← {$_3$E:[XY]$_0$} ← C, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0	√	√	√
ROR sfr	C → {$_3$sfr$_0$} → C, A ← sfr	1	1	0	0	1	0	0	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ROR \cur	C → {$_3$cur$_0$} → C, A ← cur	1	1	0	0	1	1	0	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ROR [HL]	C → {$_3$[HL]$_0$} → C, A ← [HL]	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	1	√	√	—
ROR [XY]	C → {$_3$[XY]$_0$} → C, A ← [XY]	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	√	√	—
ROR E:[HL]	C → {$_3$E:[HL]$_0$} → C, A ← E:[HL]	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	√	√	—
ROR E:[XY]	C → {$_3$E:[XY]$_0$} → C, A ← E:[XY]	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	1	√	√	—
ROR [HL+]	C → {$_3$[HL]$_0$} → C, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1	1	√	√	√
ROR [XY+]	C → {$_3$[XY]$_0$} → C, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	√	√	√
ROR E:[HL+]	C → {$_3$E:[HL]$_0$} → C, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	√	√	√
ROR E:[XY+]	C → {$_3$E:[XY]$_0$} → C, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	√	√	√

Increment/Decrement Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
INC sfr	sfr,A ← sfr + 1	1	1	0	0	1	0	0	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
INC \cur	cur,A ← cur + 1	1	1	0	0	1	1	0	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
INC [HL]	[HL],A ← [HL] + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0	√	√	—
INC [XY]	[XY],A ← [XY] + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0	√	√	—
INC E:[HL]	E:[HL],A ← E:[HL] + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	√	√	—
INC E:[XY]	E:[XY],A ← E:[XY] + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	√	√	—
INC [HL+]	[HL],A ← [HL] + 1, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	0	√	√	√
INC [XY+]	[XY],A ← [XY] + 1, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0	0	√	√	√
INC E:[HL+]	E:[HL],A ← E:[HL] + 1, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	√	√	√
INC E:[XY+]	E:[XY],A ← E:[XY] + 1, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	√	√	√
DEC sfr	sfr,A ← sfr – 1	1	1	0	0	1	0	0	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
DEC \cur	cur,A ← cur – 1	1	1	0	0	1	1	0	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
DEC [HL]	[HL],A ← [HL] – 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	1	√	√	—
DEC [XY]	[XY],A ← [XY] – 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	√	√	—
DEC E:[HL]	E:[HL],A ← E:[HL] – 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	√	√	—
DEC E:[XY]	E:[XY],A ← E:[XY] – 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1	√	√	—
DEC [HL+]	[HL],A ← [HL] – 1, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	1	√	√	√
DEC [XY+]	[XY],A ← [XY] – 1, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	√	√	√
DEC E:[HL+]	E:[HL],A ← E:[HL] – 1, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	1	√	√	√
DEC E:[XY+]	E:[XY],A ← E:[XY] – 1, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	1	√	√	√

Arithmetic Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
ADD sfr,A	sfr,A ← sfr + A	1	1	0	0	1	0	0	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADD \cur,A	cur,A ← cur + A	1	1	0	0	1	1	0	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADD [HL],A	[HL],A ← [HL] + A	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	0	√	√	—
ADD [XY],A	[XY],A ← [XY] + A	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	1	0	√	√	—
ADD E:[HL],A	E:[HL],A ← E:[HL] + A	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	√	√	—
ADD E:[XY],A	E:[XY],A ← E:[XY] + A	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	√	√	—
ADD [HL+],A	[HL],A ← [HL] + A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	1	0	√	√	√
ADD [XY+],A	[XY],A ← [XY] + A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	1	0	√	√	√
ADD E:[HL+],A	E:[HL],A ← E:[HL] + A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	0	√	√	√
ADD E:[XY+],A	E:[XY],A ← E:[XY] + A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	1	0	√	√	√
ADD \cur,#i4	cur,A ← cur + i4	1	1	1	0	0	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADD [HL],#i4	[HL],A ← [HL] + i4	1	1	0	0	0	0	0	0	0	0	1	0	1	0	i_3	i_2	i_1	i_0	√	√	—
ADD [XY],#i4	[XY],A ← [XY] + i4	1	1	0	0	0	0	0	0	0	0	1	0	1	1	i_3	i_2	i_1	i_0	√	√	—
ADD E:[HL],#i4	E:[HL],A ← E:[HL] + i4	1	1	0	0	0	0	0	0	0	0	1	0	0	0	i_3	i_2	i_1	i_0	√	√	—
ADD E:[XY],#i4	E:[XY],A ← E:[XY] + i4	1	1	0	0	0	0	0	0	0	0	1	0	0	1	i_3	i_2	i_1	i_0	√	√	—
ADD [HL+],#i4	[HL],A ← [HL] + i4, HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	1	0	1	0	i_3	i_2	i_1	i_0	√	√	√
ADD [XY+],#i4	[XY],A ← [XY] + i4, XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	1	0	1	1	i_3	i_2	i_1	i_0	√	√	√
ADD E:[HL+],#i4	E:[HL],A ← E:[HL] + i4, HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	1	0	0	0	i_3	i_2	i_1	i_0	√	√	√
ADD E:[XY+],#i4	E:[XY],A ← E:[XY] + i4, XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	1	0	0	1	i_3	i_2	i_1	i_0	√	√	√
ADC sfr,A	sfr,A ← sfr + A + C	1	1	0	0	1	0	0	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADC \cur,A	cur,A ← cur + A + C	1	1	0	0	1	1	0	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADC [HL],A	[HL],A ← [HL] + A + C	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	1	√	√	—
ADC [XY],A	[XY],A ← [XY] + A + C	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	1	1	√	√	—
ADC E:[HL],A	E:[HL],A ← E:[HL] + A + C	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	√	√	—
ADC E:[XY],A	E:[XY],A ← E:[XY] + A + C	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	1	√	√	—
ADC [HL+],A	[HL],A ← [HL] + A + C, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	1	1	√	√	√
ADC [XY+],A	[XY],A ← [XY] + A + C, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	1	1	√	√	√
ADC E:[HL+],A	E:[HL],A ← E:[HL] + A + C, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	1	√	√	√
ADC E:[XY+],A	E:[XY],A ← E:[XY] + A + C, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	1	1	√	√	√

Arithmetic Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
ADCD sfr,A	sfr,A ← decimal adjustment {sfr + A + C}	1	1	0	0	1	0	0	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADCD \cur,A	cur,A ← decimal adjustment {cur + A + C}	1	1	0	0	1	1	0	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADCD [HL],A	[HL],A ← decimal adjustment {[HL] + A + C}	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	0	√	√	—
ADCD [XY],A	[XY],A ← decimal adjustment {[XY] + A + C}	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0	0	√	√	—
ADCD E:[HL],A	E:[HL],A ← decimal adjustment {E:[HL] + A + C}	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	√	√	—
ADCD E:[XY],A	E:[XY],A ← decimal adjustment {E:[XY] + A + C}	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0	√	√	—
ADCD [HL+],A	[HL],A ← decimal adjustment {[HL] + A + C}, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	0	√	√	√
ADCD [XY+],A	[XY],A ← decimal adjustment {[XY] + A + C}, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	0	0	√	√	√
ADCD E:[HL+],A	E:[HL],A ← decimal adjustment {E:[HL] + A + C}, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	0	√	√	√
ADCD E:[XY+],A	E:[XY],A ← decimal adjustment {E:[XY] + A + C}, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	0	√	√	√
ADCJ \cur,n	cur,A ← n-ary adjustment {cur + C}	1	1	0	0	0	1	0	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADCJ [HL],n	[HL],A ← n-ary adjustment {[HL] + C}	1	1	0	0	0	0	0	1	1	0	0	0	1	0	0	n_2	n_1	n_0	√	√	—
ADCJ [XY],n	[XY],A ← n-ary adjustment {[XY] + C}	1	1	0	0	0	0	0	1	1	0	0	0	1	1	0	n_2	n_1	n_0	√	√	—
ADCJ E:[HL],n	E:[HL],A ← n-ary adjustment {E:[HL] + C}	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	n_2	n_1	n_0	√	√	—
ADCJ E:[XY],n	E:[XY],A ← n-ary adjustment {E:[XY] + C}	1	1	0	0	0	0	0	1	1	0	0	0	0	1	0	n_2	n_1	n_0	√	√	—
ADCJ [HL+],n	[HL],A ← n-ary adjustment {[HL] + C}, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	0	0	1	0	0	n_2	n_1	n_0	√	√	√
ADCJ [XY+],n	[XY],A ← n-ary adjustment {[XY] + C}, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	0	0	1	1	0	n_2	n_1	n_0	√	√	√
ADCJ E:[HL+],n	E:[HL],A ← n-ary adjustment {E:[HL] + C}, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	n_2	n_1	n_0	√	√	√
ADCJ E:[XY+],n	E:[XY],A ← n-ary adjustment {E:[XY] + C}, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	0	0	0	1	0	n_2	n_1	n_0	√	√	√

Arithmetic Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
SUB sfr,A	sfr,A ← sfr – A	1	1	0	0	1	0	0	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SUB \cur,A	cur,A ← cur – A	1	1	0	0	1	1	0	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SUB [HL],A	[HL],A ← [HL] – A	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	1	√	√	—
SUB [XY],A	[XY],A ← [XY] – A	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0	1	√	√	—
SUB E:[HL],A	E:[HL],A ← E:[HL] – A	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	√	√	—
SUB E:[XY],A	E:[XY],A ← E:[XY] – A	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	√	√	—
SUB [HL+],A	[HL],A ← [HL] – A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1	√	√	√
SUB [XY+],A	[XY],A ← [XY] – A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	0	1	√	√	√
SUB E:[HL+],A	E:[HL],A ← E:[HL] – A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	√	√	√
SUB E:[XY+],A	E:[XY],A ← E:[XY] – A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	1	√	√	√
SUB \cur,#i4	cur,A ← cur – i4	1	1	1	0	0	1	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SUB [HL],#i4	[HL],A ← [HL] – i4	1	1	0	0	0	0	0	0	1	0	1	0	1	0	i_3	i_2	i_1	i_0	√	√	—
SUB [XY],#i4	[XY],A ← [XY] – i4	1	1	0	0	0	0	0	0	1	0	1	0	1	1	i_3	i_2	i_1	i_0	√	√	—
SUB E:[HL],#i4	E:[HL],A ← E:[HL] – i4	1	1	0	0	0	0	0	0	1	0	1	0	0	0	i_3	i_2	i_1	i_0	√	√	—
SUB E:[XY],#i4	E:[XY],A ← E:[XY] – i4	1	1	0	0	0	0	0	0	1	0	1	0	0	1	i_3	i_2	i_1	i_0	√	√	—
SUB [HL+],#i4	[HL],A ← [HL] – i4, HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	1	0	1	0	i_3	i_2	i_1	i_0	√	√	√
SUB [XY+],#i4	[XY],A ← [XY] – i4, XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	1	0	1	1	i_3	i_2	i_1	i_0	√	√	√
SUB E:[HL+],#i4	E:[HL],A ← E:[HL] – i4, HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	i_3	i_2	i_1	i_0	√	√	√
SUB E:[XY+],#i4	E:[XY],A ← E:[XY] – i4, XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	1	0	0	1	i_3	i_2	i_1	i_0	√	√	√
SBC sfr,A	sfr,A ← sfr – A – C	1	1	0	0	1	0	1	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBC \cur,A	cur,A ← cur – A – C	1	1	0	0	1	1	1	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBC [HL],A	[HL],A ← [HL] – A – C	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	0	√	√	—
SBC [XY],A	[XY],A ← [XY] – A – C	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	1	0	√	√	—
SBC E:[HL],A	E:[HL],A ← E:[HL] – A – C	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	√	√	—
SBC E:[XY],A	E:[XY],A ← E:[XY] – A – C	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	0	√	√	—
SBC [HL+],A	[HL],A ← [HL] – A – C, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	1	0	√	√	√
SBC [XY+],A	[XY],A ← [XY] – A – C, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	0	√	√	√
SBC E:[HL+],A	E:[HL],A ← E:[HL] – A – C, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	1	0	√	√	√
SBC E:[XY+],A	E:[XY],A ← E:[XY] – A – C, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	1	0	√	√	√

Arithmetic Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
SBCD sfr,A	sfr,A ← decimal adjustment {sfr – A – C}	1	1	0	0	1	0	1	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBCD \cur,A	cur,A ← decimal adjustment {cur – A – C}	1	1	0	0	1	1	1	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBCD [HL],A	[HL],A ← decimal adjustment {[HL] – A – C}	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	1	√	√	—
SBCD [XY],A	[XY],A ← decimal adjustment {[XY] – A – C}	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	1	1	√	√	—
SBCD E:[HL],A	E:[HL],A ← decimal adjustment {E:[HL] – A – C}	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	1	√	√	—
SBCD E:[XY],A	E:[XY],A ← decimal adjustment {E:[XY] – A – C}	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	1	√	√	—
SBCD [HL+],A	[HL],A ← decimal adjustment {[HL] – A – C}, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	1	1	√	√	√
SBCD [XY+],A	[XY],A ← decimal adjustment {[XY] – A – C}, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	1	√	√	√
SBCD E:[HL+],A	E:[HL],A ← decimal adjustment {E:[HL] – A – C}, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	1	1	√	√	√
SBCD E:[XY+],A	E:[XY],A ← decimal adjustment {E:[XY] – A – C}, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	1	1	√	√	√
SBCJ \cur,n	cur,A ← n-ary adjustment {cur – C}	1	1	0	0	0	1	1	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBCJ [HL],n	[HL],A ← n-ary adjustment {[HL] – C}	1	1	0	0	0	0	0	1	1	0	0	0	1	0	1	n_2	n_1	n_0	√	√	—
SBCJ [XY],n	[XY],A ← n-ary adjustment {[XY] – C}	1	1	0	0	0	0	0	1	1	0	0	0	1	1	1	n_2	n_1	n_0	√	√	—
SBCJ E:[HL],n	E:[HL],A ← n-ary adjustment {E:[HL] – C}	1	1	0	0	0	0	0	1	1	0	0	0	0	0	1	n_2	n_1	n_0	√	√	—
SBCJ E:[XY],n	E:[XY],A ← n-ary adjustment {E:[XY] – C}	1	1	0	0	0	0	0	1	1	0	0	0	0	1	1	n_2	n_1	n_0	√	√	—
SBCJ [HL+],n	[HL],A ← n-ary adjustment {[HL] – C}, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	0	0	1	0	1	n_2	n_1	n_0	√	√	√
SBCJ [XY+],n	[XY],A ← n-ary adjustment {[XY] – C}, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	0	0	1	1	1	n_2	n_1	n_0	√	√	√
SBCJ E:[HL+],n	E:[HL],A ← n-ary adjustment {E:[HL] – C}, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	n_2	n_1	n_0	√	√	√
SBCJ E:[XY+],n	E:[XY],A ← n-ary adjustment {E:[XY] – C}, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	0	0	0	1	1	n_2	n_1	n_0	√	√	√

Compare Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
CMP sfr,A	sfr – A	1	1	0	0	1	0	1	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
CMP \cur,A	cur – A	1	1	0	0	1	1	1	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
CMP [HL],A	[HL] – A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	√	√	—
CMP [XY],A	[XY] – A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	0	0	√	√	—
CMP E:[HL],A	E:[HL] – A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	√	√	—
CMP E:[XY],A	E:[XY] – A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	√	√	—
CMP [HL+],A	[XY] – A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	0	√	√	√
CMP [XY+],A	[XY] – A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	√	√	√
CMP E:[HL+],A	E:[HL] – A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	√	√	√
CMP E:[XY+],A	E:[XY] – A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	√	√	√
CMP \cur,#i4	cur – i4	1	1	1	0	1	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
CMP [HL],#i4	[HL] – i4	1	1	0	0	0	0	0	1	1	0	1	0	1	0	i_3	i_2	i_1	i_0	√	√	—
CMP [XY],#i4	[XY] – i4	1	1	0	0	0	0	0	1	1	0	1	0	1	1	i_3	i_2	i_1	i_0	√	√	—
CMP E:[HL],#i4	E:[HL] – i4	1	1	0	0	0	0	0	1	1	0	1	0	0	0	i_3	i_2	i_1	i_0	√	√	—
CMP E:[XY],#i4	E:[XY] – i4	1	1	0	0	0	0	0	1	1	0	1	0	0	1	i_3	i_2	i_1	i_0	√	√	—
CMP [HL+],#i4	[HL] – i4, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	1	0	1	0	i_3	i_2	i_1	i_0	√	√	√
CMP [XY+],#i4	[XY] – i4, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	1	0	1	1	i_3	i_2	i_1	i_0	√	√	√
CMP E:[HL+],#i4	E:[HL] – i4, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	1	0	0	0	i_3	i_2	i_1	i_0	√	√	√
CMP E:[XY+],#i4	E:[XY] – i4, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	1	0	0	1	i_3	i_2	i_1	i_0	√	√	√

Logic Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
AND sfr,A	sfr,A ← sfr ∧ A	1	1	0	0	1	0	1	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
AND \cur,A	cur,A ← cur ∧ A	1	1	0	0	1	1	1	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
AND [HL],A	[HL],A ← [HL] ∧ A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	√	—	—
AND [XY],A	[XY],A ← [XY] ∧ A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	1	√	—	—
AND E:[HL],A	E:[HL],A ← E:[HL] ∧ A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	√	—	—
AND E:[XY],A	E:[XY],A ← E:[XY] ∧ A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	√	—	—
AND [HL+],A	[HL],A ← [HL] ∧ A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	1	√	—	√
AND [XY+],A	[XY],A ← [XY] ∧ A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	1	√	—	√
AND E:[HL+],A	E:[HL],A ← E:[HL] ∧ A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	√	—	√
AND E:[XY+],A	E:[XY],A ← E:[XY] ∧ A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	1	√	—	√
AND \cur,#i4	cur,A ← cur ∧ i4	1	1	0	1	0	1	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
AND [HL],#i4	[HL],A ← [HL] ∧ i4	1	1	0	0	0	0	0	1	0	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
AND [XY],#i4	[XY],A ← [XY] ∧ i4	1	1	0	0	0	0	0	1	0	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
AND E:[HL],#i4	E:[HL],A ← E:[HL] ∧ i4	1	1	0	0	0	0	0	1	0	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
AND E:[XY],#i4	E:[XY],A ← E:[XY] ∧ i4	1	1	0	0	0	0	0	1	0	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
AND [HL+],#i4	[HL],A ← [HL] ∧ i4, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
AND [XY+],#i4	[XY],A ← [XY] ∧ i4, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
AND E:[HL+],#i4	E:[HL],A ← E:[HL] ∧ i4, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
AND E:[XY+],#i4	E:[XY],A ← E:[XY] ∧ i4, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√
OR sfr,A	sfr,A ← sfr ∨ A	1	1	0	0	1	0	1	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
OR \cur,A	cur,A ← cur ∨ A	1	1	0	0	1	1	1	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
OR [HL],A	[HL],A ← [HL] ∨ A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	√	—	—
OR [XY],A	[XY],A ← [XY] ∨ A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0	√	—	—
OR E:[HL],A	E:[HL],A ← E:[HL] ∨ A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	√	—	—
OR E:[XY],A	E:[XY],A ← E:[XY] ∨ A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	√	—	—
OR [HL+],A	[HL],A ← [HL] ∨ A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	1	0	√	—	√
OR [XY+],A	[XY],A ← [XY] ∨ A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	1	0	√	—	√
OR E:[HL+],A	E:[HL],A ← E:[HL] ∨ A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	√	—	√
OR E:[XY+],A	E:[XY],A ← E:[XY] ∨ A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	0	√	—	√

Logic Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
OR \cur,#i4	cur,A ← cur ∨ i4	1	1	0	1	1	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
OR [HL],#i4	[HL],A ← [HL] ∨ i4	1	1	0	0	0	0	0	0	1	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
OR [XY],#i4	[XY],A ← [XY] ∨ i4	1	1	0	0	0	0	0	0	1	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
OR E:[HL],#i4	E:[HL],A ← E:[HL] ∨ i4	1	1	0	0	0	0	0	0	1	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
OR E:[XY],#i4	E:[XY],A ← E:[XY] ∨ i4	1	1	0	0	0	0	0	0	1	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
OR [HL+],#i4	[HL],A ← [HL] ∨ i4, HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
OR [XY+],#i4	[XY],A ← [XY] ∨ i4, XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
OR E:[HL+],#i4	E:[HL],A ← E:[HL] ∨ i4, HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
OR E:[XY+],#i4	E:[XY],A ← E:[XY] ∨ i4, XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√
XOR sfr,A	sfr,A ← sfr ∀ A	1	1	0	0	1	0	1	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
XOR \cur,A	cur,A ← cur ∀ A	1	1	0	0	1	1	1	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
XOR [HL],A	[HL],A ← [HL] ∀ A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	1	√	—	—
XOR [XY],A	[XY],A ← [XY] ∀ A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	1	√	—	—
XOR E:[HL],A	E:[HL],A ← E:[HL] ∀ A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	√	—	—
XOR E:[XY],A	E:[XY],A ← E:[XY] ∀ A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	√	—	—
XOR [HL+],A	[HL],A ← [HL] ∀ A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	1	1	√	—	√
XOR [XY+],A	[XY],A ← [XY] ∀ A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	1	1	√	—	√
XOR E:[HL+],A	E:[HL],A ← E:[HL] ∀ A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1	√	—	√
XOR E:[XY+],A	E:[XY],A ← E:[XY] ∀ A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	√	—	√
XOR \cur,#i4	cur,A ← cur ∀ i4	1	1	0	1	1	1	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
XOR [HL],#i4	[HL],A ← [HL] ∀ i4	1	1	0	0	0	0	0	0	0	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
XOR [XY],#i4	[XY],A ← [XY] ∀ i4	1	1	0	0	0	0	0	0	0	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
XOR E:[HL],#i4	E:[HL],A ← E:[HL] ∀ i4	1	1	0	0	0	0	0	0	0	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
XOR E:[XY],#i4	E:[XY],A ← E:[XY] ∀ i4	1	1	0	0	0	0	0	0	0	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
XOR [HL+],#i4	[HL],A ← [HL] ∀ i4, HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
XOR [XY+],#i4	[XY],A ← [XY] ∀ i4, XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
XOR E:[HL+],#i4	E:[HL],A ← E:[HL] ∀ i4, HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
XOR E:[XY+],#i4	E:[XY],A ← E:[XY] ∀ i4, XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√

Mask Operation Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MTST sfr,A	Testing of all bits in sfr not masked by A	1	1	0	0	1	0	1	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MTST \cur,A	Testing of all bits in cur not masked by A	1	1	0	0	1	1	1	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MTST [HL],A	Testing of all bits in [HL] not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	1	√	—	—
MTST [XY],A	Testing of all bits in [XY] not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	0	1	√	—	—
MTST E:[HL],A	Testing of all bits in E:[HL] not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	√	—	—
MTST E:[XY],A	Testing of all bits in E:[XY] not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	√	—	—
MTST [HL+],A	Testing of all bits in [HL] not masked by A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	1	√	—	√
MTST [XY+],A	Testing of all bits in [XY] not masked by A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	1	√	—	√
MTST E:[HL+],A	Testing of all bits in E:[HL] not masked by A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	√	—	√
MTST E:[XY+],A	Testing of all bits in E:[XY] not masked by A, XY← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	1	√	—	√
MTST \cur,#m	Testing of all bits in cur not masked by #m	1	1	1	0	1	1	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MTST [HL],#m	Testing of all bits in [HL] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	1	0	m_3	m_2	m_1	m_0	√	—	—
MTST [XY],#m	Testing of all bits in [XY] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	1	1	m_3	m_2	m_1	m_0	√	—	—
MTST E:[HL],#m	Testing of all bits in E:[HL] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	0	0	m_3	m_2	m_1	m_0	√	—	—
MTST E:[XY],#m	Testing of all bits in E:[XY] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	0	1	m_3	m_2	m_1	m_0	√	—	—
MTST [HL+],#m	Testing of all bits in [HL] not masked by #m, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	1	0	1	0	m_3	m_2	m_1	m_0	√	—	√
MTST [XY+],#m	Testing of all bits in [XY] not masked by #m, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	1	0	1	1	m_3	m_2	m_1	m_0	√	—	√
MTST E:[HL+],#m	Testing of all bits in E:[HL] not masked by #m, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	1	0	0	0	m_3	m_2	m_1	m_0	√	—	√
MTST E:[XY+],#m	Testing of all bits in E:[XY] not masked by #m, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	1	0	0	1	m_3	m_2	m_1	m_0	√	—	√

Mask Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MCLR \cur,#m	Clearing of all bits in cur not masked by #m, A ← cur	1	1	0	1	0	1	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MCLR [HL],#m	Clearing of all bits in [HL] not masked by #m, A ← [HL]	1	1	0	0	0	0	0	1	0	0	0	1	1	0	m_3	m_2	m_1	m_0	√	—	—
MCLR [XY],#m	Clearing of all bits in [XY] not masked by #m, A ← [XY]	1	1	0	0	0	0	0	1	0	0	0	1	1	1	m_3	m_2	m_1	m_0	√	—	—
MCLR E:[HL],#m	Clearing of all bits in E:[HL] not masked by #m, A ← E:[HL]	1	1	0	0	0	0	0	1	0	0	0	1	0	0	m_3	m_2	m_1	m_0	√	—	—
MCLR E:[XY],#m	Clearing of all bits in E:[XY] not masked by #m, A ← E:[XY]	1	1	0	0	0	0	0	1	0	0	0	1	0	1	m_3	m_2	m_1	m_0	√	—	—
MCLR [HL+],#m	Clearing of all bits in [HL] not masked by #m, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	1	1	0	m_3	m_2	m_1	m_0	√	—	√
MCLR [XY+],#m	Clearing of all bits in [XY] not masked by #m, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	1	1	1	m_3	m_2	m_1	m_0	√	—	√
MCLR E:[HL+],#m	Clearing of all bits in E:[HL] not masked by #m, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	1	0	0	m_3	m_2	m_1	m_0	√	—	√
MCLR E:[XY+],#m	Clearing of all bits in E:[XY] not masked by #m, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	1	0	1	m_3	m_2	m_1	m_0	√	—	√

Mask Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MSET \cur,#m	Setting of all bits in cur not masked by #m, A ← cur	1	1	0	1	1	0	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MSET [HL],#m	Setting of all bits in [HL] not masked by #m, A ← [HL]	1	1	0	0	0	0	0	0	1	0	0	1	1	0	m_3	m_2	m_1	m_0	√	—	—
MSET [XY],#m	Setting of all bits in [XY] not masked by #m, A ← [XY]	1	1	0	0	0	0	0	0	1	0	0	1	1	1	m_3	m_2	m_1	m_0	√	—	—
MSET E:[HL],#m	Setting of all bits in E:[HL] not masked by #m, A ← E:[HL]	1	1	0	0	0	0	0	0	1	0	0	1	0	0	m_3	m_2	m_1	m_0	√	—	—
MSET E:[XY],#m	Setting of all bits in E:[XY] not masked by #m, A ← E:[XY]	1	1	0	0	0	0	0	0	1	0	0	1	0	1	m_3	m_2	m_1	m_0	√	—	—
MSET [HL+],#m	Setting of all bits in [HL] not masked by #m, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	m_3	m_2	m_1	m_0	√	—	√
MSET [XY+],#m	Setting of all bits in [XY] not masked by #m, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	1	1	1	m_3	m_2	m_1	m_0	√	—	√
MSET E:[HL+],#m	Setting of all bits in E:[HL] not masked by #m, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	m_3	m_2	m_1	m_0	√	—	√
MSET E:[XY+],#m	Setting of all bits in E:[XY] not masked by #m, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	1	0	1	m_3	m_2	m_1	m_0	√	—	√

Mask Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MNOT \cur,#m	Inverting of all bits in cur not masked by #m, A ← cur	1	1	0	1	1	1	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MNOT [HL],#m	Inverting of all bits in [HL] not masked by #m, A ← [HL]	1	1	0	0	0	0	0	0	0	0	0	1	1	0	m_3	m_2	m_1	m_0	√	—	—
MNOT [XY],#m	Inverting of all bits in [XY] not masked by #m, A ← [XY]	1	1	0	0	0	0	0	0	0	0	0	1	1	1	m_3	m_2	m_1	m_0	√	—	—
MNOT E:[HL],#m	Inverting of all bits in E:[HL] not masked by #m, A ← E:[HL]	1	1	0	0	0	0	0	0	0	0	0	1	0	0	m_3	m_2	m_1	m_0	√	—	—
MNOT E:[XY],#m	Inverting of all bits in E:[XY] not masked by #m, A ← E:[XY]	1	1	0	0	0	0	0	0	0	0	0	1	0	1	m_3	m_2	m_1	m_0	√	—	—
MNOT [HL+],#m	Inverting of all bits in [HL] not masked by #m, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	m_3	m_2	m_1	m_0	√	—	√
MNOT [XY+],#m	Inverting of all bits in [XY] not masked by #m, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	m_3	m_2	m_1	m_0	√	—	√
MNOT E:[HL+],#m	Inverting of all bits in E:[HL] not masked by #m, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	m_3	m_2	m_1	m_0	√	—	√
MNOT E:[XY+],#m	Inverting of all bits in E:[XY] not masked by #m, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	m_3	m_2	m_1	m_0	√	—	√

Bit Operation Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
BTST \cur.n	Bit testing of cur.n	1	1	1	0	1	1	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BTST [HL].n	Bit testing of [HL].n	1	1	0	0	0	0	0	1	0	0	1	0	1	0	n_3	n_2	n_1	n_0	√	—	—
BTST [XY].n	Bit testing of [XY].n	1	1	0	0	0	0	0	1	0	0	1	0	1	1	n_3	n_2	n_1	n_0	√	—	—
BTST E:[HL].n	Bit testing of E:[HL].n	1	1	0	0	0	0	0	1	0	0	1	0	0	0	n_3	n_2	n_1	n_0	√	—	—
BTST E:[XY].n	Bit testing of E:[XY].n	1	1	0	0	0	0	0	1	0	0	1	0	0	1	n_3	n_2	n_1	n_0	√	—	—
BTST [HL+].n	Bit testing of [HL].n, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	1	0	1	0	n_3	n_2	n_1	n_0	√	—	√
BTST [XY+].n	Bit testing of [XY].n, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	1	0	1	1	n_3	n_2	n_1	n_0	√	—	√
BTST E:[HL+].n	Bit testing of E:[HL].n, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	1	0	0	0	n_3	n_2	n_1	n_0	√	—	√
BTST E:[XY+].n	Bit testing of E:[XY].n, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	1	0	0	1	n_3	n_2	n_1	n_0	√	—	√
BCLR \cur.n	cur.n ← 0, A ← cur	1	1	0	1	0	1	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BCLR [HL].n	[HL].n ← 0, A ← [HL]	1	1	0	0	0	0	0	1	0	0	0	1	1	0	n_3	n_2	n_1	n_0	√	—	—
BCLR [XY].n	[XY].n ← 0, A ← [XY]	1	1	0	0	0	0	0	1	0	0	0	1	1	1	n_3	n_2	n_1	n_0	√	—	—
BCLR E:[HL].n	E:[HL].n ← 0, A ← E:[HL]	1	1	0	0	0	0	0	1	0	0	0	1	0	0	n_3	n_2	n_1	n_0	√	—	—
BCLR E:[XY].n	E:[XY].n ← 0, A ← E:[XY]	1	1	0	0	0	0	0	1	0	0	0	1	0	1	n_3	n_2	n_1	n_0	√	—	—
BCLR [HL+].n	[HL].n ← 0, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	1	1	0	n_3	n_2	n_1	n_0	√	—	√
BCLR [XY+].n	[XY].n ← 0, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	1	1	1	n_3	n_2	n_1	n_0	√	—	√
BCLR E:[HL+].n	E:[HL].n ← 0, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	1	0	0	n_3	n_2	n_1	n_0	√	—	√
BCLR E:[XY+].n	E:[XY].n ← 0, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	1	0	1	n_3	n_2	n_1	n_0	√	—	√
BSET \cur.n	cur.n ← 1, A ← cur	1	1	0	1	1	0	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BSET [HL].n	[HL].n ← 1, A ← [HL]	1	1	0	0	0	0	0	0	1	0	0	1	1	0	n_3	n_2	n_1	n_0	√	—	—
BSET [XY].n	[XY].n ← 1, A ← [XY]	1	1	0	0	0	0	0	0	1	0	0	1	1	1	n_3	n_2	n_1	n_0	√	—	—
BSET E:[HL].n	E:[HL].n ← 1, A ← E:[HL]	1	1	0	0	0	0	0	0	1	0	0	1	0	0	n_3	n_2	n_1	n_0	√	—	—
BSET E:[XY].n	E:[XY].n ← 1, A ← E:[XY]	1	1	0	0	0	0	0	0	1	0	0	1	0	1	n_3	n_2	n_1	n_0	√	—	—
BSET [HL+].n	[HL].n ← 1, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	n_3	n_2	n_1	n_0	√	—	√
BSET [XY+].n	[XY].n ← 1, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	1	1	1	n_3	n_2	n_1	n_0	√	—	√
BSET E:[HL+].n	E:[HL].n ← 1, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	n_3	n_2	n_1	n_0	√	—	√
BSET E:[XY+].n	E:[XY].n ← 1, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	1	0	1	n_3	n_2	n_1	n_0	√	—	√

Bit Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
BNOT \cur.n	cur.n ← $\overline{\text{cur.n}}$, A ← cur	1	1	0	1	1	1	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BNOT [HL].n	[HL].n ← $\overline{\text{[HL].n}}$, A ← [HL]	1	1	0	0	0	0	0	0	0	0	0	1	1	0	n_3	n_2	n_1	n_0	√	—	—
BNOT [XY].n	[XY].n ← $\overline{\text{[XY].n}}$, A ← [XY]	1	1	0	0	0	0	0	0	0	0	0	1	1	1	n_3	n_2	n_1	n_0	√	—	—
BNOT E:[HL].n	E:[HL].n ← $\overline{\text{E:[HL].n}}$, A ← E:[HL]	1	1	0	0	0	0	0	0	0	0	0	1	0	0	n_3	n_2	n_1	n_0	√	—	—
BNOT E:[XY].n	E:[XY].n ← $\overline{\text{E:[XY].n}}$, A ← E:[XY]	1	1	0	0	0	0	0	0	0	0	0	1	0	1	n_3	n_2	n_1	n_0	√	—	—
BNOT [HL+].n	[HL].n ← $\overline{\text{[HL].n}}$, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	n_3	n_2	n_1	n_0	√	—	√
BNOT [XY+].n	[XY].n ← $\overline{\text{[XY].n}}$, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	n_3	n_2	n_1	n_0	√	—	√
BNOT E:[HL+].n	E:[HL].n ← $\overline{\text{E:[HL].n}}$, A ←E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	n_3	n_2	n_1	n_0	√	—	√
BNOT E:[XY+].n	E:[XY].n ← $\overline{\text{E:[XY].n}}$, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	n_3	n_2	n_1	n_0	√	—	√

ROM Table Reference Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOVHB [HL],[RA]	[HL],[HL + 1] ← $(RA)_{15–8}$	1	2	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	—	—	—
MOVHB [XY],[RA]	[XY],[XY + 1] ← $(RA)_{15–8}$	1	2	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	0	—	—	—
MOVHB E:[HL],[RA]	E:[HL],E:[HL + 1] ← $(RA)_{15–8}$	1	2	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	—	—	—
MOVHB E:[XY],[RA]	E:[XY],E:[XY + 1] ← $(RA)_{15–8}$	1	2	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	—	—	—
MOVHB [HL+],[RA]	[HL],[HL + 1] ← $(RA)_{15–8}$, HL ← HL + 2	1	2	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	0	—	—	√
MOVHB [XY+],[RA]	[XY],[XY + 1] ← $(RA)_{15–8}$, XY ← XY + 2	1	2	0	0	0	0	0	0	1	1	0	0	1	1	1	0	1	0	—	—	√
MOVHB E:[HL+],[RA]	E:[HL],E:[HL + 1] ← $(RA)_{15–8}$, HL ← HL + 2	1	2	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	—	—	√
MOVHB E:[XY+],[RA]	E:[XY],E:[XY + 1] ← $(RA)_{15–8}$, XY ← XY + 2	1	2	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1	0	—	—	√
MOVHB [HL],cadr16	[HL],[HL + 1] ← $(cadr16)_{15–8}$	2	3	0	0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB [XY],cadr16	[XY],[XY + 1] ← $(cadr16)_{15–8}$	2	3	0	0	0	0	0	0	1	1	0	0	1	1	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[HL],cadr16	E:[HL],E:[HL + 1] ← $(cadr16)_{15–8}$	2	3	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[XY],cadr16	E:[XY],E:[XY + 1] ← $(cadr16)_{15–8}$	2	3	0	0	0	0	0	0	1	1	0	0	0	1	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB [HL+],cadr16	[HL],[HL + 1] ← $(cadr16)_{15–8}$, HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB [XY+],cadr16	[XY],[XY + 1] ← $(cadr16)_{15–8}$, XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[HL+],cadr16	E:[HL],E:[HL + 1] ← $(cadr16)_{15–8}$, HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[XY+],cadr16	E:[XY],E:[XY + 1] ← $(cadr16)_{15–8}$, XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

ROM Table Reference Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOVLB [HL],[RA]	[HL],[HL + 1] ← $(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	1	—	—	—
MOVLB [XY],[RA]	[XY],[XY + 1] ← $(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	—	—	—
MOVLB E:[HL],[RA]	E:[HL],E:[HL + 1] ← $(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	—	—	—
MOVLB E:[XY],[RA]	E:[XY],E:[XY + 1] ← $(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	—	—	—
MOVLB [HL+],[RA]	[HL],[HL + 1] ← $(RA)_{7-0}$, HL ← HL + 2	1	2	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	1	—	—	√
MOVLB [XY+],[RA]	[XY],[XY + 1] ← $(RA)_{7-0}$, XY ← XY + 2	1	2	0	0	0	0	0	0	1	1	0	0	1	1	1	0	1	1	—	—	√
MOVLB E:[HL+],[RA]	E:[HL],E:[HL + 1] ← $(RA)_{7-0}$, HL ← HL + 2	1	2	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	1	—	—	√
MOVLB E:[XY+],[RA]	E:[XY],E:[XY + 1] ← $(RA)_{7-0}$, XY ← XY + 2	1	2	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1	1	—	—	√
MOVLB [HL],cadr16	[HL],[HL + 1] ← $(cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	1	0	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB [XY],cadr16	[XY],[XY + 1] ← $(cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	1	1	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[HL],cadr16	E:[HL],E:[HL + 1] ← $(cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[XY],cadr16	E:[XY],E:[XY + 1] ← $(cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	0	1	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB [HL+],cadr16	[HL],[HL + 1] ← $(cadr16)_{7-0}$, HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	0	0	1	0	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB [XY+],cadr16	[XY],[XY + 1] ← $(cadr16)_{7-0}$, XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[HL+],cadr16	E:[HL],E:[HL + 1] ← $(cadr16)_{7-0}$, HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[XY+],cadr16	E:[XY],E:[XY + 1] ← $(cadr16)_{7-0}$, XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

External Memory Transfer Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOVXB [HL],[RA]	[HL],[HL + 1] ← (RA)	1	2	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	0	—	—	—
MOVXB [XY],[RA]	[XY],[XY + 1] ← (RA)	1	2	0	0	0	0	0	0	1	1	0	0	1	1	0	1	1	0	—	—	—
MOVXB E:[HL],[RA]	E:[HL],E:[HL + 1] ← (RA)	1	2	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	—	—	—
MOVXB E:[XY],[RA]	E:[XY],E:[XY + 1] ← (RA)	1	2	0	0	0	0	0	0	1	1	0	0	0	1	0	1	1	0	—	—	—
MOVXB [HL+],[RA]	[HL],[HL + 1] ← (RA), HL ← HL + 2	1	2	0	0	0	0	0	0	1	1	0	0	1	0	1	1	1	0	—	—	√
MOVXB [XY+],[RA]	[XY],[XY + 1] ← (RA), XY ← XY + 2	1	2	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	0	—	—	√
MOVXB E:[HL+],[RA]	E:[HL],E:[HL + 1] ← (RA), HL ← HL + 2	1	2	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	0	—	—	√
MOVXB E:[XY+],[RA]	E:[XY],E:[XY + 1] ← (RA), XY ← XY + 2	1	2	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	0	—	—	√
MOVXB [RA],[HL]	(RA) ← [HL],[HL + 1]	1	3	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	—	—	—
MOVXB [RA],[XY]	(RA) ← [XY],[XY + 1]	1	3	0	0	0	0	0	0	1	1	0	0	1	1	0	1	1	1	—	—	—
MOVXB [RA],E:[HL]	(RA) ← E:[HL],E:[HL + 1]	1	3	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	—	—	—
MOVXB [RA],E:[XY]	(RA) ← E:[XY],E:[XY + 1]	1	3	0	0	0	0	0	0	1	1	0	0	0	1	0	1	1	1	—	—	—
MOVXB [RA],[HL+]	(RA) ← [HL],[HL + 1], HL ← HL + 2	1	3	0	0	0	0	0	0	1	1	0	0	1	0	1	1	1	1	—	—	√
MOVXB [RA],[XY+]	(RA) ← [XY],[XY + 1], XY ← XY + 2	1	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	—	—	√
MOVXB [RA],E:[HL+]	(RA) ← E:[HL],E:[HL + 1], HL ← HL + 2	1	3	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	1	—	—	√
MOVXB [RA],E:[XY+]	(RA) ← E:[XY],E:[XY + 1], XY ← XY + 2	1	3	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1	—	—	√

External Memory Transfer Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOVXB [HL],xadr16	[HL],[HL + 1] ← (xadr16)	2	3	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB [XY],xadr16	[XY],[XY + 1] ← (xadr16)	2	3	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB E:[HL],xadr16	E:[HL],E:[HL + 1] ← (xadr16)	2	3	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB E:[XY],xadr16	E:[XY],E:[XY + 1] ← (xadr16)	2	3	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB [HL+],xadr16	[HL],[HL + 1] ← (xadr16), HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB [XY+],xadr16	[XY],[XY + 1] ← (xadr16), XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB E:[HL+],xadr16	E:[HL],E:[HL + 1] ← (xadr16), HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB E:[XY+],xadr16	E:[XY],E:[XY + 1] ← (xadr16), XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	1	1	0	1	1	0	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,[HL]	(xadr16) ← [HL],[HL + 1]	2	3	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,[XY]	(xadr16) ← [XY],[XY + 1]	2	3	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,E:[HL]	(xadr16) ← E:[HL],E:[HL + 1]	2	3	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,E:[XY]	(xadr16) ← E:[XY],E:[XY + 1]	2	3	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,[HL+]	(xadr16) ← [HL],[HL + 1], HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,[XY+]	(xadr16) ← [XY],[XY + 1], XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,E:[HL+]	(xadr16) ← E:[HL],E: [HL + 1], HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,E:[XY+]	(xadr16) ← E:[XY],E: [XY + 1], XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	1	1	0	1	1	0	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

Stack Operation Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
PUSH HL	(RSP) ← {FLAG, A, HL}, RSP ← RSP + 1	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	—	—	—
PUSH XY	(RSP) ← {CBR, EBR, XY}, RSP ← RSP + 1	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	—	—	—
POP HL	RSP ← RSP – 1, {FLAG, A, HL} ← (RSP)	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	√	√	√
POP XY	RSP ← RSP – 1, {CBR, EBR, XY} ← (RSP)	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	—	—	—

Flag Operation Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
FCLR G	G ← 0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	—	—	√
FCLR C	C ← 0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	—	√	—
FCLR Z	Z ← 0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	√	—	—
FSET G	G ← 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	—	—	√
FSET C	C ← 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	—	√	—
FSET Z	Z ← 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	√	—	—

Jump Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
LJMP cadr15	PC ← cadr15	2	2	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	—	—	—
				0	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
JMP cadr12	$PC_{11–0}$ ← cadr12	1	1	1	1	1	0	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
SJMP radr8	PC ← Next PC + radr8	1	1	0	0	0	0	1	0	0	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
JMP PC + A	PC ← PC + A + 1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	—	—	—

Conditional Branch Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
BC radr8 BLT radr8	if C = 1 then PC ← Next PC + radr8 (<)	1	1	0	0	0	0	1	0	1	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BNC radr8 BGE radr8	if C = 0 then PC ← Next PC + radr8 (≥)	1	1	0	0	0	0	1	0	1	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BZ radr8 BEQ radr8	If Z = 1 then PC ← Next PC + radr8 (=)	1	1	0	0	0	0	1	1	0	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BNZ radr8 BNE radr8	If Z = 0 then PC ← Next PC + radr8 (≠)	1	1	0	0	0	0	1	1	0	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BLE radr8	If (C = 1) ∨ (Z = 1) then PC ← Next PC + radr8 (≤)	1	1	0	0	0	0	1	1	1	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BGT radr8	If (C = 0) ∧ (Z =0) then PC ← Next PC + radr8 (>)	1	1	0	0	0	0	1	1	1	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BNG radr8	if G = 0 then PC ← Next PC + radr8	1	1	0	0	0	0	1	0	0	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—

Call/Return Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
LCAL cadr15	(SP) ← PC, PC ← cadr15, SP ← SP + 1	2	2	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	—	—	—
				0	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
CAL cadr12	(SP) ← PC, $PC_{11–0}$ ← cadr12, SP ← SP + 1	1	1	1	1	1	1	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
RT	PC ← (SP) + 1, SP ← SP – 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	—	—	—
RTI	PC ← (SP) + 1, SP ← SP – 1, MIE ← 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	—	—	—
RTNMI	PC ← (SP) + 1, SP ← SP – 1 MIE ← status of MIE before an interrupt occurs	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	—	—	—

Control Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
NOP	NO OPERATION	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—
HALT	HALT CPU	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	—	—	—
EI	MIE ← 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	—	—	—
DI	MIE ← 0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	—	—	—
INCB HL	HL ← HL + 1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	—	—	√
INCB XY	XY ← XY + 1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	—	—	√
INCW RA	RA ← RA + 1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	—	—	√
MOV CBR,#i4	CBR ← i4	1	1	0	0	0	0	0	0	0	0	0	0	1	1	i_3	i_2	i_1	i_0	—	—	—
MOV EBR,#i4	EBR ← i4	1	1	0	0	0	0	0	0	0	0	0	0	1	0	i_3	i_2	i_1	i_0	—	—	—
MOV RA0,#i4	RA0 ← i4	1	1	0	0	0	0	0	0	1	0	0	0	0	0	i_3	i_2	i_1	i_0	—	—	—
MOV RA1,#i4	RA1 ← i4	1	1	0	0	0	0	0	0	1	0	0	0	0	1	i_3	i_2	i_1	i_0	—	—	—
MOV RA2,#i4	RA2 ← i4	1	1	0	0	0	0	0	0	1	0	0	0	1	0	i_3	i_2	i_1	i_0	—	—	—
MOV RA3,#i4	RA3 ← i4	1	1	0	0	0	0	0	0	1	0	0	0	1	1	i_3	i_2	i_1	i_0	—	—	—
MOV H,#i4	H ← i4	1	1	0	0	0	0	0	0	0	1	0	0	1	1	i_3	i_2	i_1	i_0	—	—	—
MOV L,#i4	L ← i4	1	1	0	0	0	0	0	0	0	1	0	0	1	0	i_3	i_2	i_1	i_0	—	—	—
MOV X,#i4	X ← i4	1	1	0	0	0	0	0	0	0	1	0	0	0	1	i_3	i_2	i_1	i_0	—	—	—
MOV Y,#i4	Y ← i4	1	1	0	0	0	0	0	0	0	1	0	0	0	0	i_3	i_2	i_1	i_0	—	—	—
MSA cadr15	Melody output starts	2	3	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	—	—	—
				0	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

Appendix G Mask Option

The ML63295A can select the crystal oscillation circuit or the RC oscillation circuit as the oscillation circuit of the low-speed clock generator circuit by mask option.

To use the mask option, assign mask option data in the application program in accordance with the format below.

Assignment of the mask option data does not affect the application program execution area, because the areas for data assignment for each device are out of the program memory area.

- Data assignment area for ML63295A: address 7FE0H

ML63295A Mask Option Data Assignment Format

Address	Function	Contents	Data	
7FE0H	Low-speed oscillation clock	Crystal oscillation/ RC oscillation	0: Crystal oscillation	1: RC oscillation

Example of mask option data generation

- When the RC oscillation circuit is specified for the low-speed clock oscillation circuit in the ML63295A

```
ORG     7FE0H   ← Use an assembler pseudo-instruction to set the address of option data to 7FE0H.
DW      0001H   :  Low-speed oscillation clock, RC oscillation
```

ML63295A

User's Manual

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