OKI

OKI ML670100 CPU BOARD

User's Guide (Preliminary)

Oki ARM7TDMI Emulation Kit

First Edition, February 2000

Oki Electric Industry Co., Ltd.

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Chapter 1 Read Me First

This chapter describes the procedures to be followed upon receipt of the ML670100 CPU Board. Verify the items described in this chapter before applying power to the ML670100 CPU Board.

1.1 Precaution for Safe and Proper Use

This User's Guide uses various labels and icons that serve as your guides to operating this product safely and properly so as to prevent death, personal injury, and property damage. The following table lists these labels and their definitions.

Labels

Warning	This label indicates precautions that, if ignored or otherwise not completely followed, could lead to death or serious personal injury.
Caution	This label indicates precautions that, if ignored or otherwise not completely followed, could lead to personal injury or property damage.

Icons

A triangular icon draws your attention to the presence of a hazard. The illustration inside the triangular frame indicates the nature of the hazard—in this example, an electrical shock hazard.

A circular icon with a solid background illustrates an action to be performed. The illustration inside this circle indicates this action—in this example, unplugging the power cord.

A circular icon with a crossbar indicates a prohibition. The illustration inside this circle indicates the prohibited action—in this example, disassembly.

1.2 Important Safety Notes

Please read this page before using the product.

⚠ Warning	
Use only the specified voltage. Using the wrong voltage risks fire and electrical shock.	
At the first signs of smoke, an unusual smell, or other problems, unplug the emulator and disconnect all external power cords. Continued use risks fire and electrical shock.	
Do not use the product in an environment exposing it to moisture or high humidity. Such exposure risks fire and electrical shock	
Do not pile objects on top of the product. Such pressure risks fore and electrical shock.	
At the first signs of breakdown, immediately stop using the product, unplug the emulator, and disconnect all external power cords. Continued use risks fire and electrical shock.	

Please read this page before using the product.

⚠ Caution	
Do not use this product on an unstable or inclined base as it can fall or overturn, producing injury.	
Do not use this product in an environment exposing it to excessive vibration, strong magnetic fields, or corrosive gases. Such factors can loosen or even disconnect cable connectors, producing a breakdown.	
Do not use this product in an environment exposing it to temperatures outside the specified range, direct sunlight, or excessive dust. Such factors risk fire and breakdown.	
Use only the cables and other accessories provided. Using non-compatible parts risks fire and breakdown.	
Always observe the specified order for turning equipment on and off. Using the incorrect order risks fire and breakdown.	
Do not use the cables and other accessories provided with other systems. Such improper usage risks fire.	
Before connecting or disconnecting the cables and the accessories, the power source for the emulator must be turned OFF. Connections or disconnections performed while the power source is ON risk fire and damage to the system.	

1.3 Notation

This manual utilizes the following notational conventions for convenience.

■ Caution ■	A “caution” indicates a section of the manual that requires special attention.
■ Reference ■	A “reference” provides information related to the current topic and indicates the page number of a related section of the manual.
■ Application Example ■	An “application example” indicates an example related to the current topic.
(note ×)	“(note ×)” is a reference to a numbered note that provides supplementary information lower on the same page.
■ Note x ■	“Note ×:” provides supplementary information related to the passage marked with “(note ×).”

1.4 For Further Information

Thank you for purchasing the Oki ML670100 CPU Board.

Please direct any questions or comments regarding this product to your Oki distributor or the nearest Oki Electric Sales Office.

1.5 Verify Package Contents

Upon receiving the OKI ML670100 CPU Board, verify that the package contains all the components listed in Table 1.

Although every effort has been made to minimize damage and eliminate mistakes, please report any damaged or missing parts to your Oki distributor or the nearest Oki Electric Sales Office.

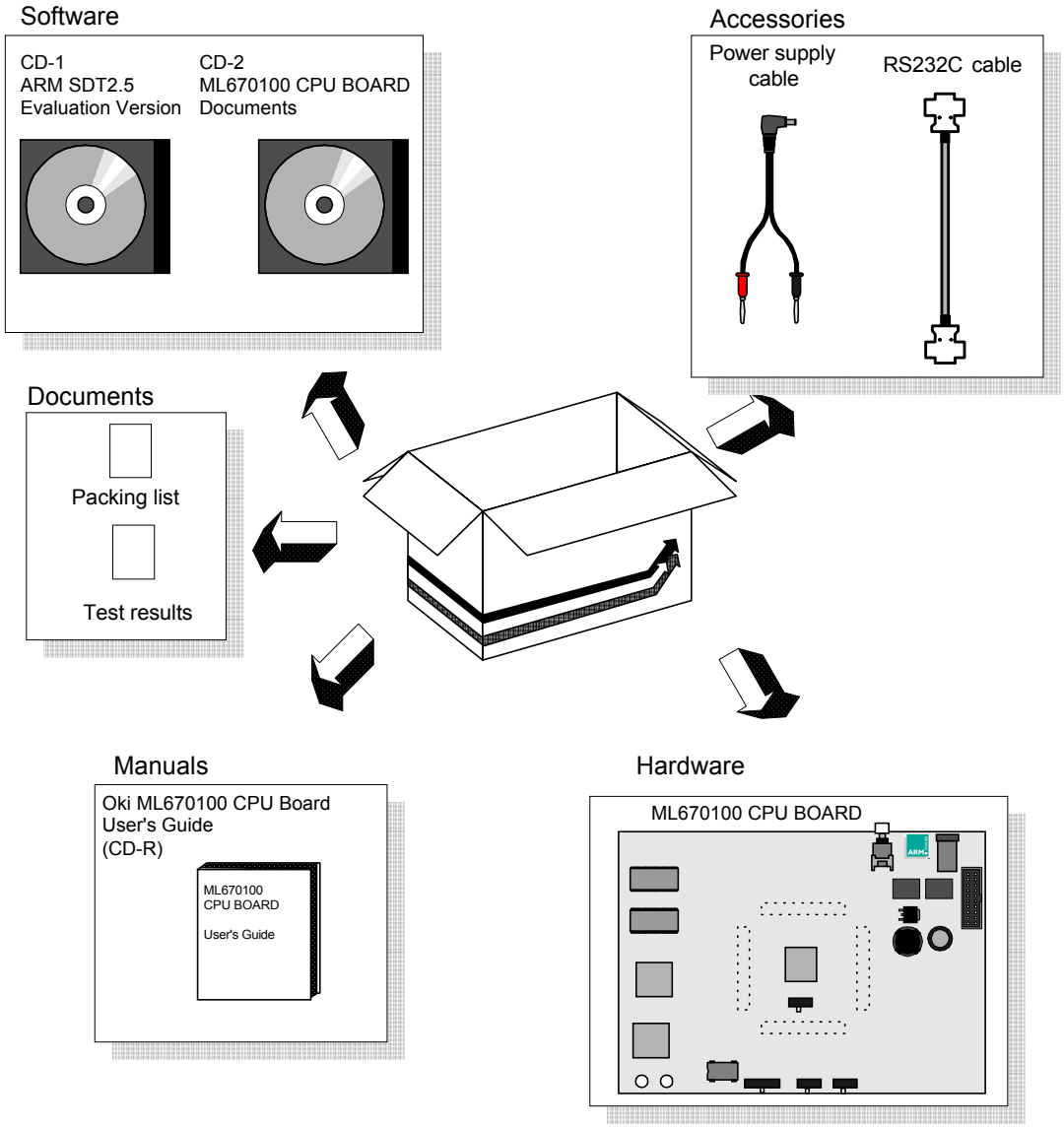


Figure 1.1. Package Contents

Option

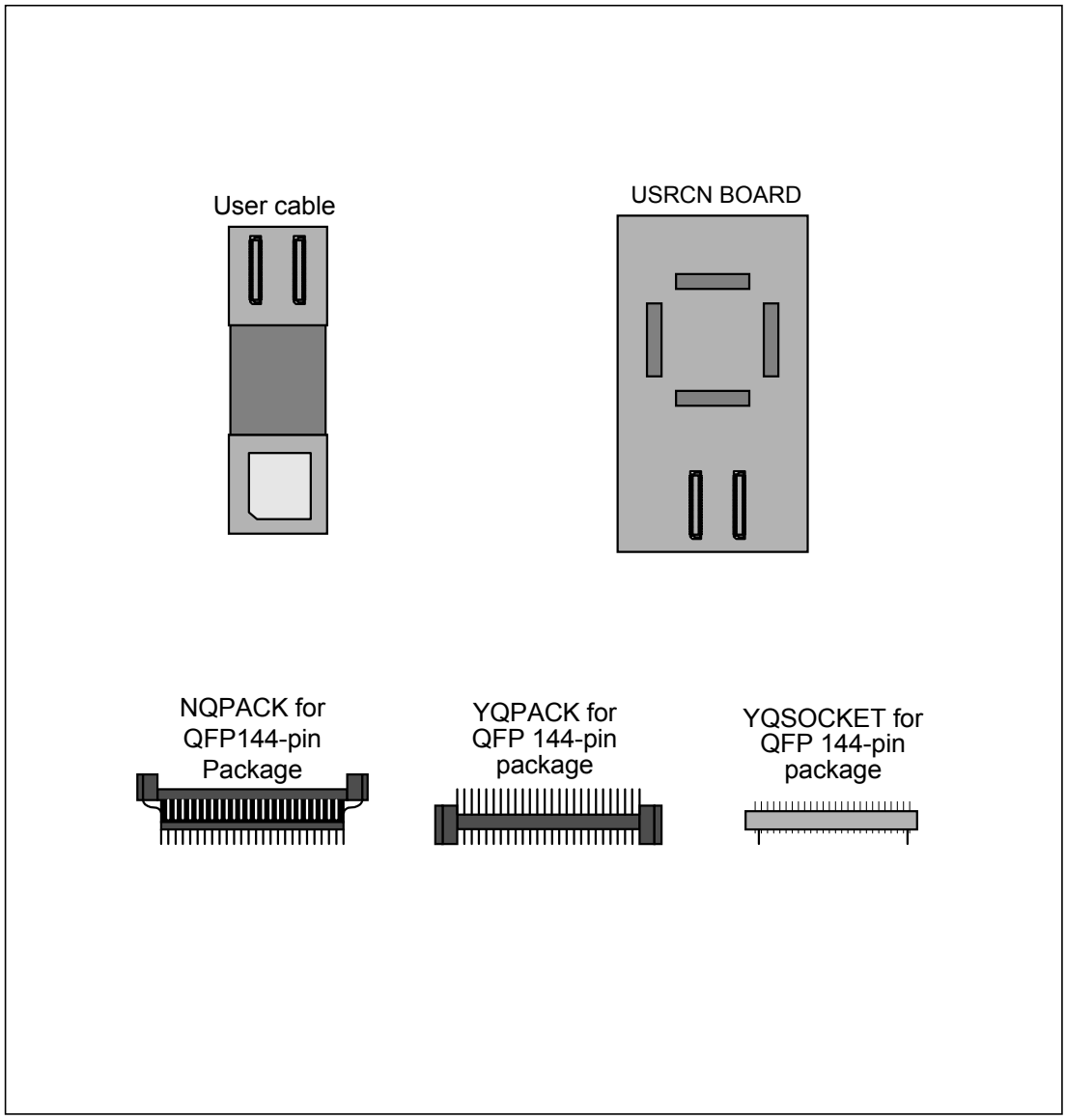
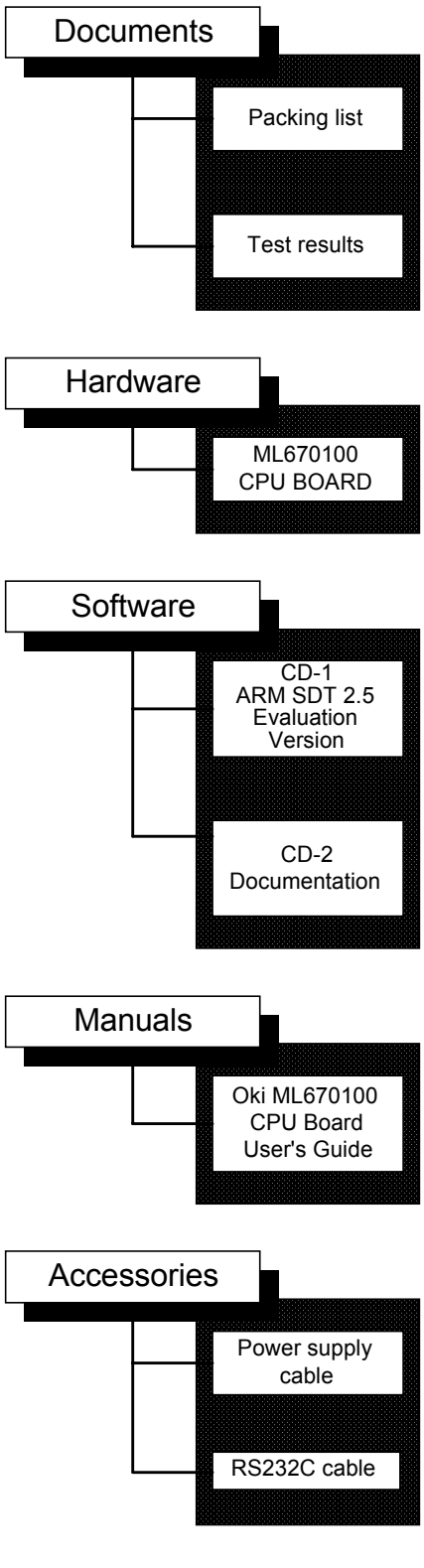


Figure 1.2. Oki ML670100 CPU Board Options



This lists the contents of the Oki ML670100 CPU board package. Check the contents against this list when you first open the package.

This lists the results of testing the Oki ML670100 CPU board at the factory.

This is the board itself.

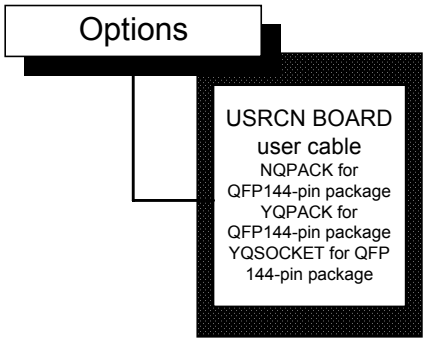
This CD-ROM contains a 60-day trial version of a complete program development and debugging environment, from Advanced RISC Machines Limited (ARM), for the Oki ML670100 CPU board.

This CD-ROM contains such documentation for the Oki ML670100 CPU board as the circuit diagrams, parts list, User's Guide (this document), and configuration file for the Oki ICE Server.

This CD-R contains the manual (this document) for the Oki ML670100 CPU board.

This cable is for connecting the Oki ML670100 CPU board to the system power supply (5 V DC ±5%).

This cable provides a communications link between the Oki ML670100 CPU Board and a development host with an IBM PC/AT-compatible serial port.



These optional components are for connecting the Oki ML670100 CPU Board to the user application system.Ord from the nearest Oki Electric Sales Office.

Figure 1.3. Oki ML670100 CPU Board

Chapter 2 OVERVIEW

This Chapter provides an overview of the Oki ML670100 CPU Board, its components, and its functions.

2.1 What is it?

The Oki ML670100 CPU Board is part of an emulation kit for developers debugging and evaluating embedded user application systems to run on the ML670100, Oki Electric's high-performance 32-bit single-chip microcontroller.

This document distinguishes two setups for debugging user application programs.

Angel mode (Note 1): Debugging with a direct link to the ARM Software Development Toolkit (SDT) from Advanced RISC Machines Limited (ARM)

Normal embedded mode: Debugging with a link to the SDT through a JTAG communications interface unit (Oki Electric ADI Board or ARM Multi-ICE^{TM})

The Oki ML670100 CPU Board contains an ML670100 emulating the target device. It replaces, however, the internal program ROM with rewritable emulation memory (SRAM).

Figure 2.1 shows the general Board layout.

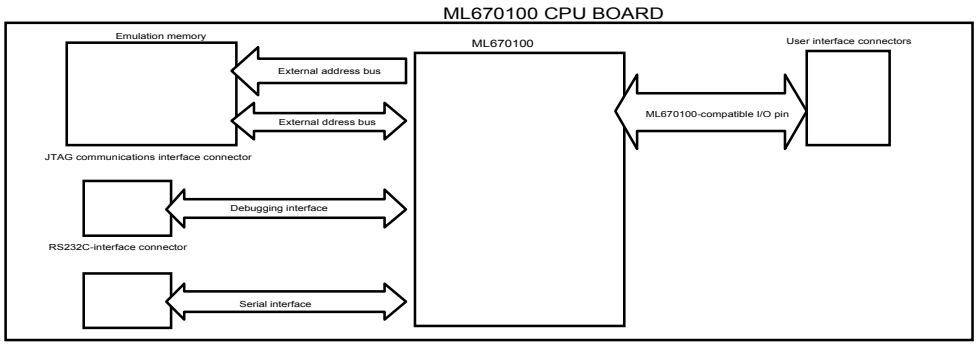


Figure 2.1. Oki ML670100 CPU Board Layout

As Figure 2.1 indicates, the user interface connectors provide access to most (See Note 1) of the evaluation chip's I/O pins (Note 2). Connecting them to the user application program with the optional user connector Board (USRCN) and user cable permits in-place debugging.

■ Note 1 ■

The Oki ML670100 CPU Board's Flash memory contains the Angel debugging monitor, for use in developing applications based on the ARM CPU. For further details on this program, refer to the ARM Software Development Toolkit User Guide and ARM Software Development Toolkit Reference Guide.

■ Note 2 ■

The Oki ML670100 CPU Board sometimes handles the following ML670100 built-in peripheral ports and pins differently: PIO0, PIO1, PIO2.5, PIO2.6, PIO5.6, PIO5.7, and PIO8. For further details, see Chapter 5 "Notes on Debugging."

2.2 System Components

Figure 2.2 lists the components making up a program development support system using the Oki ARM7TDMI Interface Unit (ADI Board).

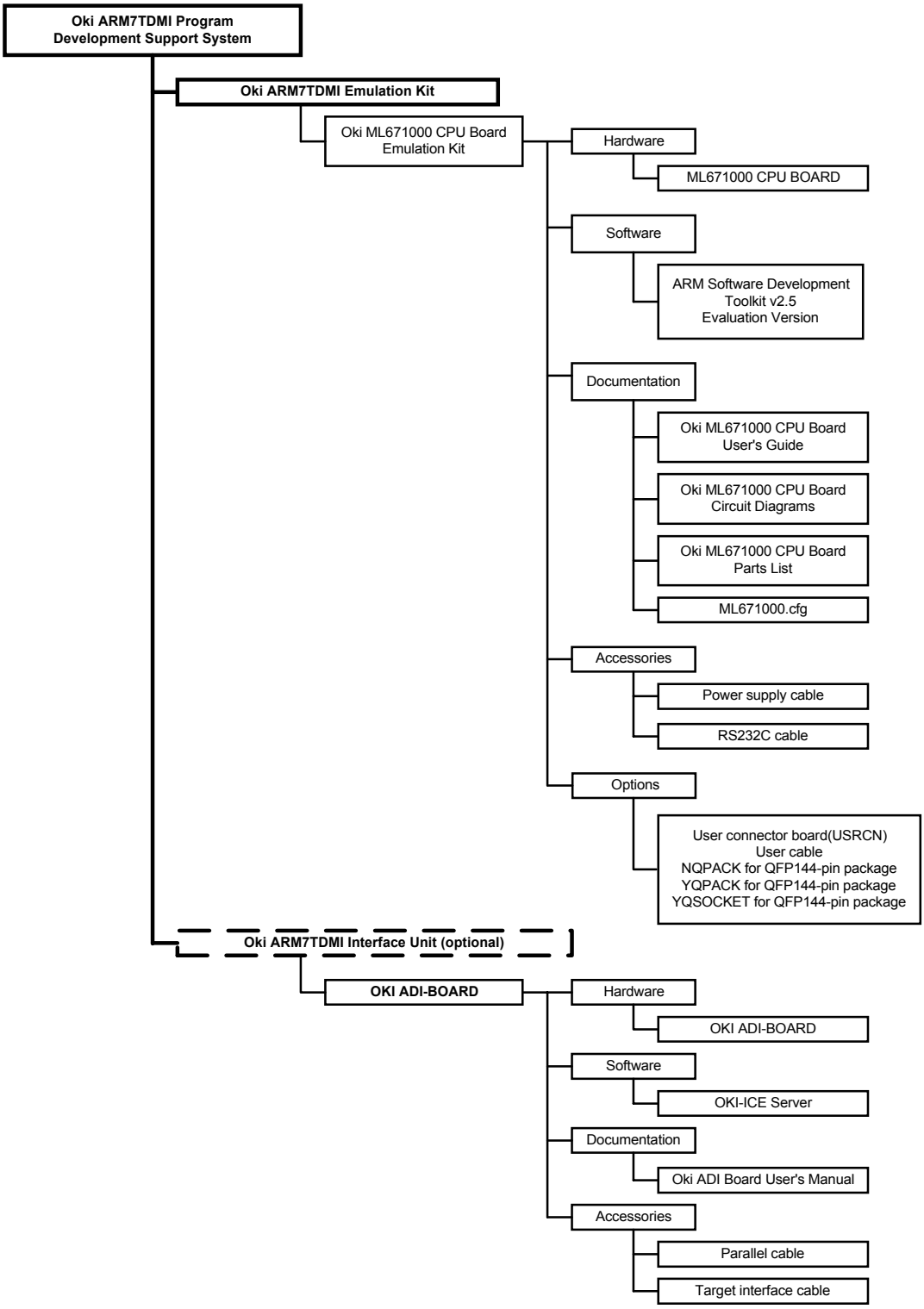


Figure 2.2. ARM7TDMI Program Development Support System Components

Oki ARM7TDMI Program Development Support System

This term covers all hardware and software provided by Oki Electric and Advanced RISC Machines.

Oki ARM7TDMI Emulation Kit

This term covers all Oki Electric support hardware and software used in program development for the ARM7TDMI core. The Oki ML670100 CPU Board falls into this category.

Oki ML670100 CPU Board Emulation Kit

This term covers all Oki Electric hardware, manuals, and accessories used in program development for the ML670100, Oki Electric's high-performance 32-bit single-chip microcontroller.

Oki ML670100 CPU Board

This term covers all Oki Electric hardware used in program development for the ML670100, Oki Electric's high-performance 32-bit single-chip microcontroller. This User's Guide sometimes refers to it simply as the Board.

ARM Software Development Toolkit 2.5 Evaluation Version

This CD-ROM contains a 60-day trial version of the ARM Software Development Toolkit 2.5 from Advanced RISC Machines Limited (ARM). This software provides a complete program development and debugging environment for the Oki ML670100 CPU board.
This User's Guide and other documentation sometimes abbreviates the Software Development Toolkit portion to ARM SDT or ARM Software Development Toolkit.

Oki ML670100 CPU Board User's Guide

This is the User's Guide (this document) for the Oki ML670100 CPU board.

Oki ML670100 CPU Board Circuit Diagrams

These are the circuit diagrams for the Oki ML670100 CPU board.

Oki ML670100 CPU Board Parts List

This is the parts list for the Oki ML670100 CPU board.

ML670100.cfg

This file configures Oki ICE Server for remote debugging of the Oki ML670100 CPU board via the Oki ADI board. Oki ICE Server initializes the JTAG port using the contents of this file.

Power Supply Cable

This cable is for connecting the Oki ML670100 CPU Board to the system power supply (5 V DC ± 5%).

RS232C Cable

This cable provides a communications link between the Oki ML670100 CPU Board and a development host with an IBM PC/AT-compatible serial port.

USRCN Board, User Cable, NQPACK, YQPACK, and YQSOCKET

These optional components are for connecting the Oki ML670100 CPU Board to the user application system.
It is also possible to connect the Oki ML670100 CPU Board directly to the user application system with the user cable.

Oki ADI Board

This hardware provides a JTAG communications interface between the Oki ML670100 CPU Board and the development host.

Oki ICE Server

This software communicates between the Oki ADI Board and the ARM multiprocessor debugger. It is supplied on a CD-ROM.

Parallel Cable

This cable connects the Oki ML670100 CPU Board to the development host.

2.3 Main Components

This Section shows the layout of the Oki ML670100 CPU Board and describes the main components.

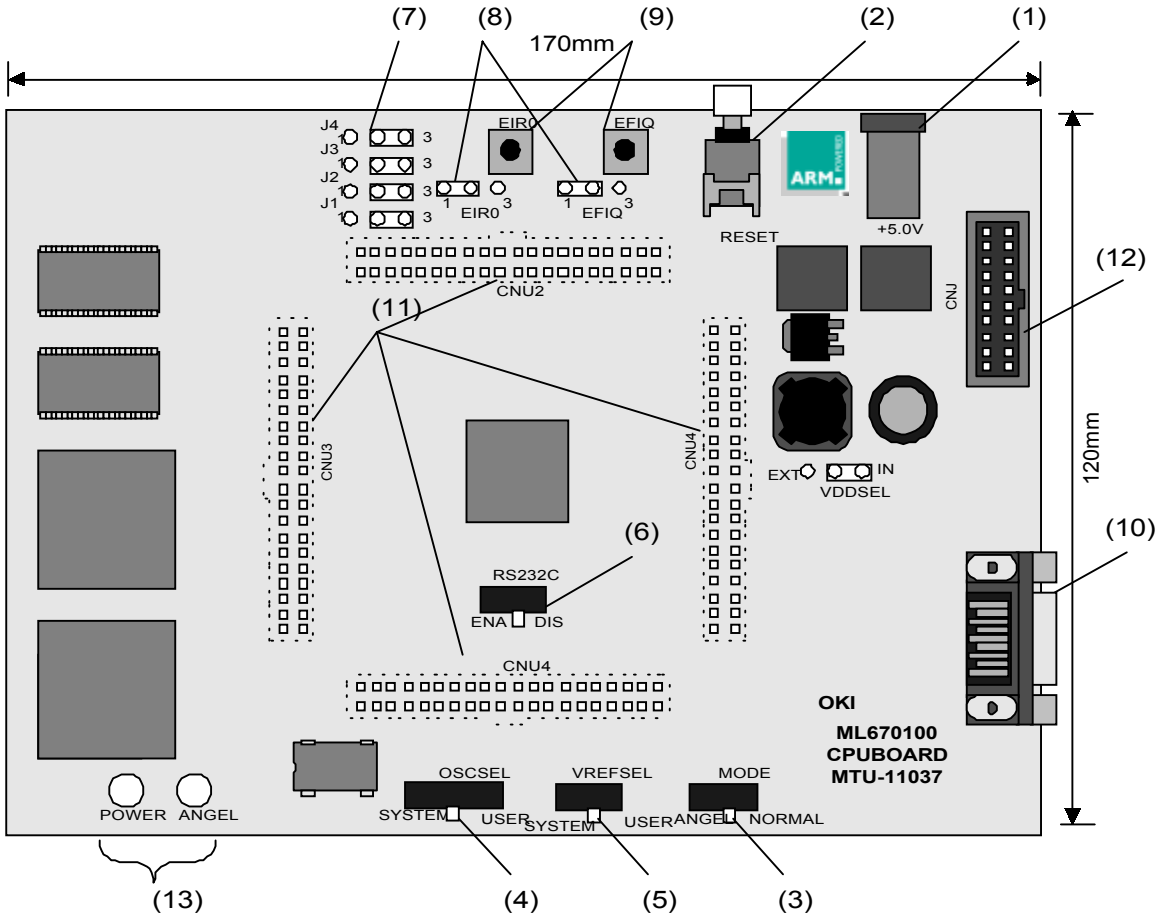


Figure 2.3. Oki ML670100 CPU Board Layout

(1) DC connector — This connector supplies the Board with its system power supply. Connect it to the specified power supply (5 V DC ± 5%, 1 A) with the supplied power supply cable.

(2) System reset switch (RESET) — Pushing this switch resets the Board.

(3) Operating mode switch (MODE) — This switch specifies the Board's operating mode: Angel or normal.

(4) Clock selection switch (OSCSEL) This switch specifies the source for the ML670100 operating clock, supplied to the OSC0 pin: the built-in oscillator circuit or the user application system.

(5) V_{ref} selection switch (VREFSEL) This switch specifies the reference voltage source for the Board's analog-to-digital converter: the internal +3.3-volt power supply or the user application system.

(6) Serial interface switch (RS232C) This switch specifies the connections for the ML670100 serial port pins PIO5.6 and PIO5.7: to theRS232C driver IC (ENA) or to the user interface connectors (DIS).

(7) Memory mask jumpers (J1 to J4) These jumpers control ML670100 read/write access to external memory (SRAM and Flash) on the Board.

(8) EIR0 and EFIQ input selection jumpers (EIR0 and EFIQ)

These jumpers specify the sources for the ML670100 EIR0 and EFIQ pin inputs: the switches on the Board or external signals from the user application system.

(9) EIR0 and EFIQ switches (EIR0 and EFIQ)

These switches are for generating external interrupt request signals to the ML670100 EIR0 and EFIQ pins.

(10)RS232C interface connector (RS232C)

This connects the Oki ML670100 CPU Board to the development host for debugging in Angel mode.

(11) User interface connectors (CNU1 to CNU4)

This connects ML670100 pins to the user application system.

(12) ICE interface connector (CNJ)

This connects to a JTAG communications interface unit (Oki Electric ADI Board or ARM Multi-ICE™) for debugging in normal mode.

(13) Indicators

These LEDs give the Board's operating status.

2.4 Main Components

This Section describes the main functions of the Oki ML670100 CPU Board.

2.4.1 Angel Debugging

This configuration provides remote debugging and emulation of the user application program with the ARM Software Development Toolkit over a direct serial (RS232C) link to the development host.

Figure 2.4 shows this configuration.

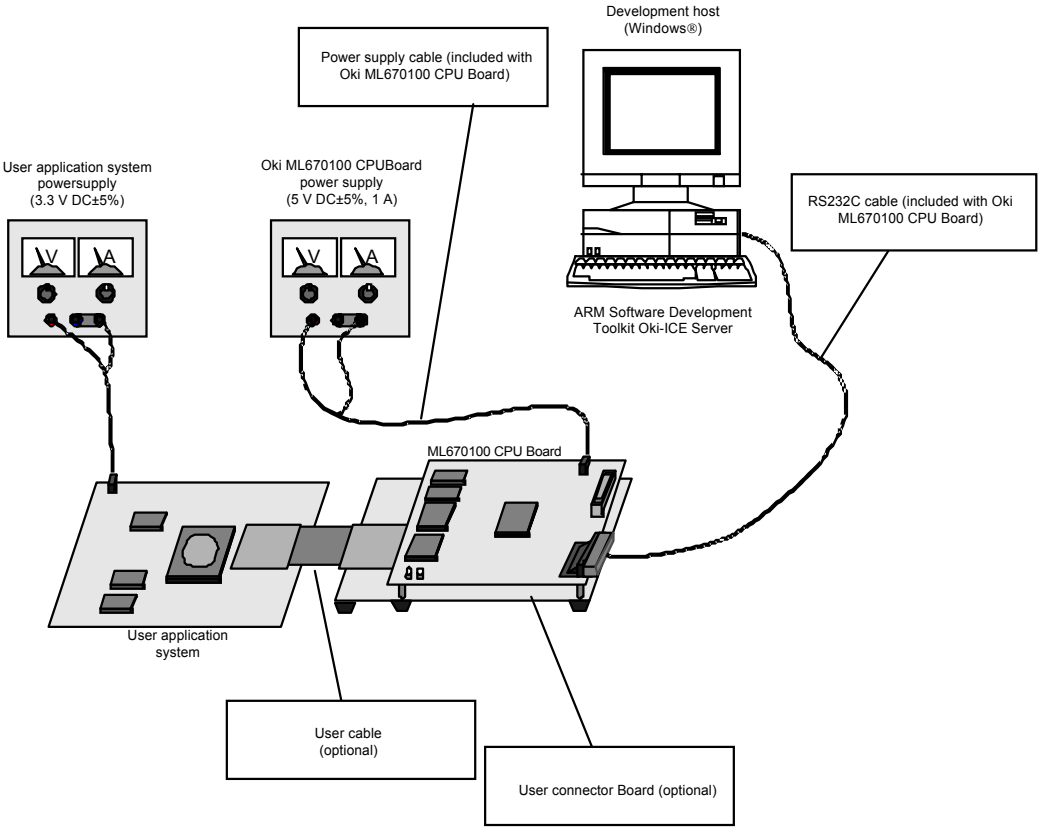


Figure 2.4. Angel Debugging Configuration

For the related procedures, see Section 3.6 "Procedures."

2.4.2 Normal Debugging

This configuration provides remote debugging and emulation of the user application program with the ARM Software Development Toolkit through a JTAG communications interface unit (Oki Electric ADI Board or ARM Multi-ICE™).

Figure 2.5 shows this configuration.

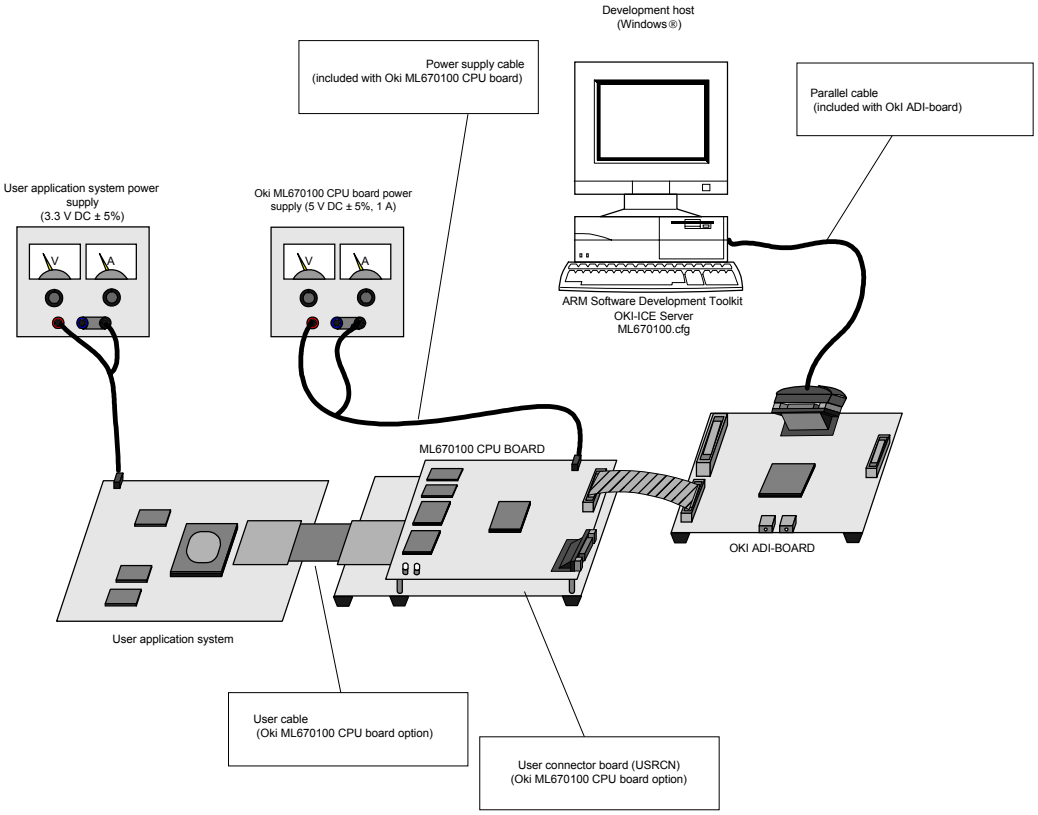


Figure 2.5. Normal Debugging Configuration

For the related procedures, see Section 3.5 "Procedures."

2.4.3 Indicators (POWER & ANGEL)

The Oki ML670100 CPU Board has two LEDs that give the system's operating status. For the locations, see Figure 2.3 in Section 2.3 above.

These LEDs have the following meanings.

POWER (green): **This LED indicates the status of the Oki ML670100 CPU Board's power supply. It lights when the Board is receiving the proper voltage.**

ANGEL (orange): **This LED indicates the debugging mode. It lights during Angel mode operation.**

2.5 Hardware Specifications

The Oki ML670100 CPU Board has the following specifications.

Target microcontroller:	ML670100
System power supply input:	5 V DC ± 5%
ML670100 operating voltage:	3.3 V DC ± 5%
ML670100 operating frequency:	24 MHz (multiplied fourfold from 6 MHz input)
External program memory:	928K bytes (Angel mode) 1 megabyte (Normal mode)
External Flash memory:	192K bytes
Internal data memory:	4K bytes
Built-in peripherals:	Most ML670100 pins (See Note 2)
RS232C interface:	One (connectorRS232C)
User interface:	One (connectors CNU1 to CNU4)
JTAG communications interface:	One (connecting to Oki Electric ADI Board or ARM Multi-ICE™)
EIR0 and EFIQ switches:	One each (with enable/disable switches)
Other:	Operating mode switch (MODE), clock selection switch (OSCSEL), serial interface switch (RS232C), V_{ref} selection switch (VREFSEL), two indicators (POWER and ANGEL)

■ Note 2 ■

The Oki ML670100 CPU Board sometimes handles the following ML670100 built-in peripheral ports and pins PIO0, PIO1, PIO2.5, PIO2.6, PIO5.6, PIO5.7 and PIO8. For further details, see Chapter 5"Notes on Debugging."

2.6 Operating Conditions

Use the Oki ML670100 CPU Board only in environments satisfying the following conditions.

Oki ML670100 CPU Board Operating Conditions

Item	Description
System input power voltage [rating]	DC +5V±5%[DC +5V]
Maximum current drain	0.8 A
Environmental conditions	Operating temperature: 5 to 35°C Operating humidity: 40 to 60%

Note that the Board has the following dimensions and weight.

Oki ML670100 CPU Board Dimensions and Weight

Item	Description
Dimensions	170 (W) × 120 (D) × 30 (H) [mm]
Weight	approximately 0.2 kg

Chapter 3 Setup and Operation

This Chapter describes the procedures for setting up and operating the Oki ML670100 CPU Board.

3.1 Switches and Settings

Figure 3.1 shows the switches and jumpers controlling Oki ML670100 CPU Board operation. This Section describes their uses.

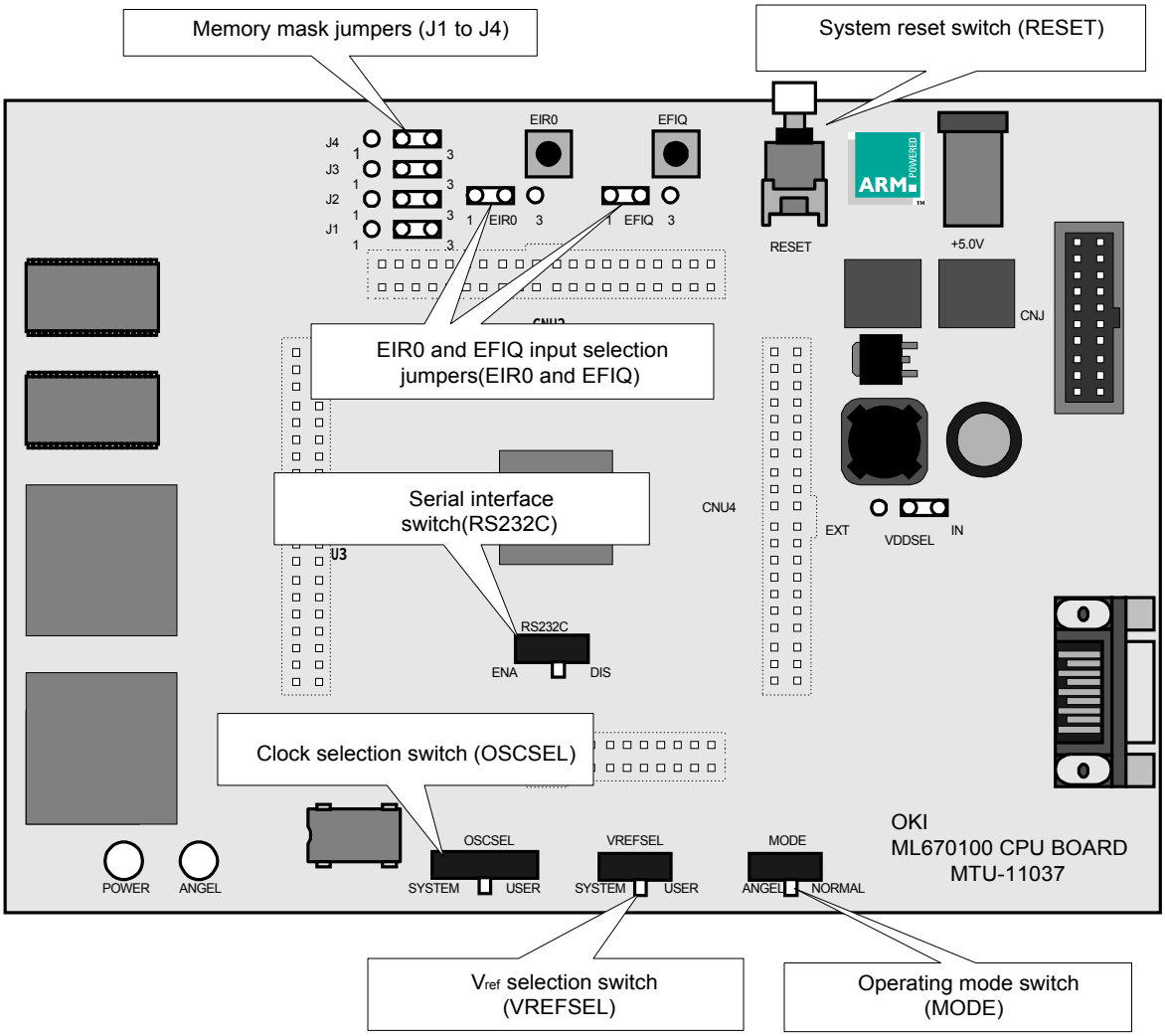


Figure 3.1. Oki ML670100 CPU Board Switches

3.1.1 System Reset Switch (RESET)

Pushing this switch resets the Oki ML670100 CPU Board.

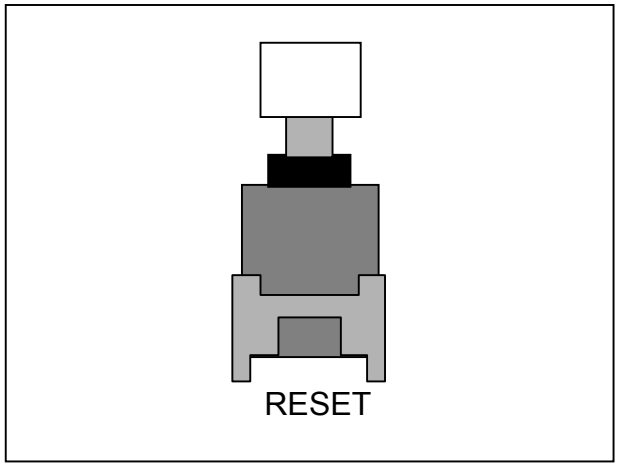


Figure 3.2. System Reset Switch (RESET)

The Board has two types of reset:

- A power on reset produced by applying the power for the first time
- A system reset produced by pressing this push-button switch

Either type initializes the ML670100 on the Board.

Do not press this switch during normal operation, however, as it also resets the JTAG communications interface unit (Oki Electric ADI Board or ARM Multi-ICE^{TM}) joining the Board to the host computer.

To change to the Angel mode, set the MODE switch to the ANGEL position and press this button.

■ Note ■

Pressing this button during remote debugging in either Angel or normal mode can break the communications link to the development host.

3.1.2 Operating Mode Switch (MODE)

This switch specifies the Board's operating mode: Angel or normal.

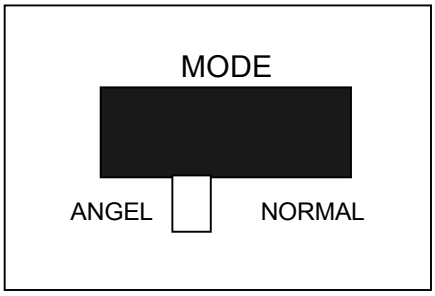


Figure 3.3. Operating Mode Switch (MODE)

Setting this switch to its ANGEL position debugs with a direct link to the development host; the NORMAL position, with a link through a JTAG communications interface unit (Oki Electric ADI Board or ARM Multi-ICE™).

Figure 3.4 shows the related circuitry.

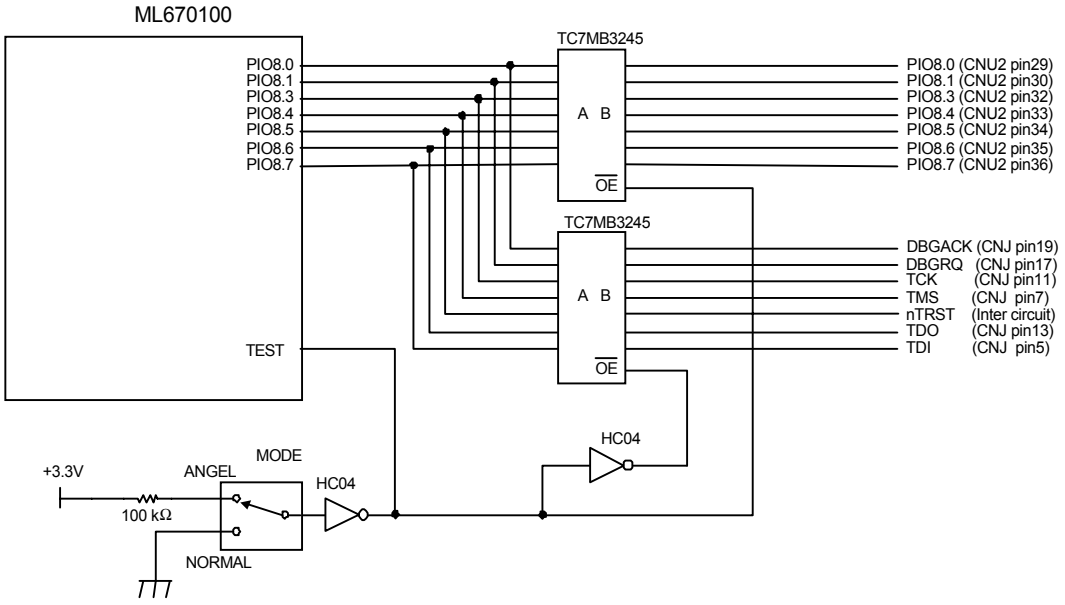


Figure 3.4. Operating Mode Switch (MODE) Circuits

■ Note ■

The NORMAL position of this switch disconnects all PIO8 pins except PIO8.2 from the user interface connectors.

3.1.3 Clock Selection Switch (OSCSEL)

This switch specifies the source for the ML670100 operating clock, supplied to the OSC0 pin: the built-in oscillator circuit or the user application system.

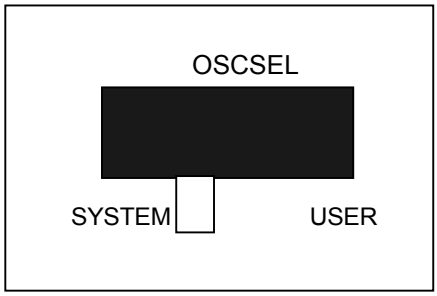


Figure 3.5. Clock Selection Switch (OSCSEL)

Setting this switch to its SYSTEM position connects the ML670100 OSC0 pin to the 6-MHz clock signal from the built-in oscillator circuit. It also drives the ML670100 FSEL and PLLEN pins at "H" level to quadruple the internal frequency to 24 MHz.
The USER position, in contrast, connects all three pins to the corresponding user interface connector pins.
Figure 3.6 shows the related circuitry.

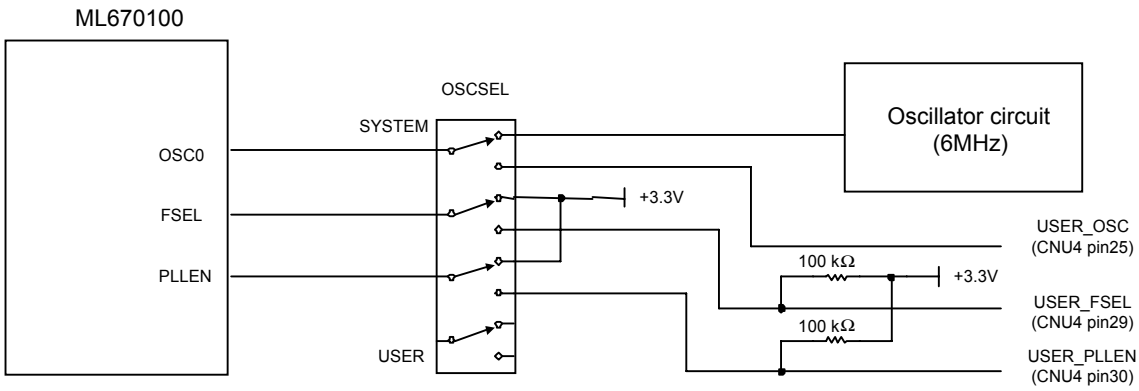


Figure 3.6. Clock Selection Switch (OSCSEL) Circuits

Note the 100-kΩ pull-up resistances on the user interface connector pins USER_FSEL and USER_PLLEN connecting to the corresponding ML670100 pins FSEL and PLLEN. Note that the ML670100 internal oscillator circuit is not available. For the USER position, the user application system must supply a clock signal with guaranteed duty to the interface connector pin USER_OSC0 connecting to the corresponding ML670100 pin OSC0.

3.1.4 V_{ref} Selection Switch (VREFSEL)

This switch specifies the reference voltage source for the Board's analog-to-digital converter: the internal +3.3-volt power supply or the user application system. (GND < $V_{ref} \leq$ VDD)

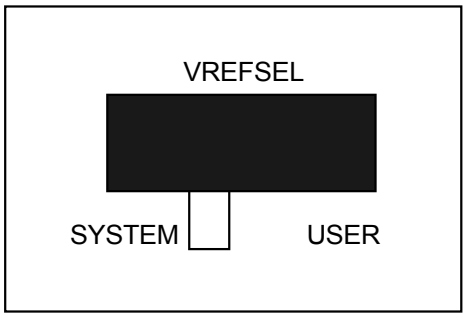


Figure 3.7. V_{ref} Selection Switch (VREFSEL)

Setting this switch to its SYSTEM position connects the ML670100 V_{ref} pin to the internal +3.3-volt power supply; the USER position, to the corresponding user interface connector pin.

Figure 3.8 shows the related circuitry.

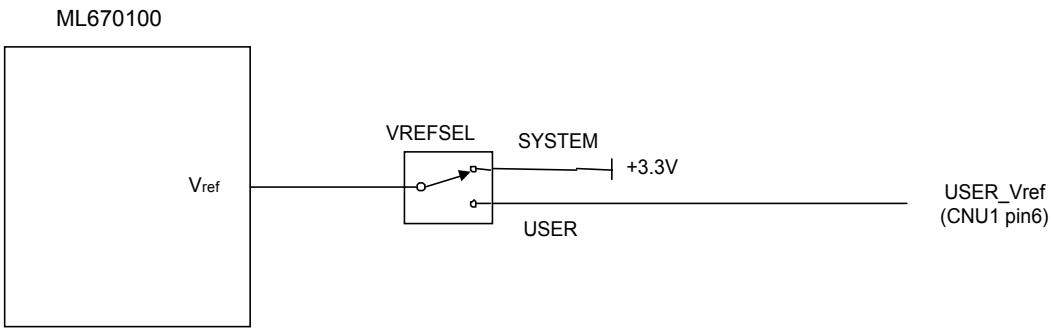


Figure 3.8. V_{ref} Selection Switch (VREFSEL) Circuits

3.1.5 Serial Interface Switch (RS232C)

This switch specifies the connections for the ML670100 serial port pins PIO5.6 and PIO5.7: to the RS232C driver IC (ENA) or to the corresponding user interface connector pins (DIS).

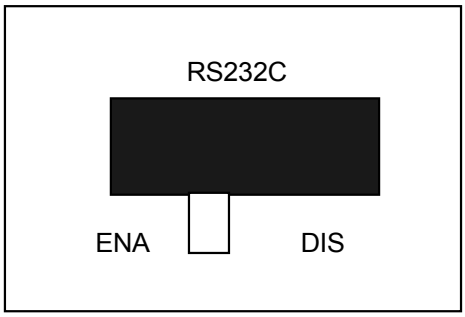


Figure 3.9. Serial Interface Switch (RS232C)

Setting this switch to its ENA position connects the ML670100 serial port pins PIO5.6 and PIO5.7 to the RS232C driver IC; the DIS position, to the corresponding user interface connector pins.

Figure 3.10 shows the related circuitry.

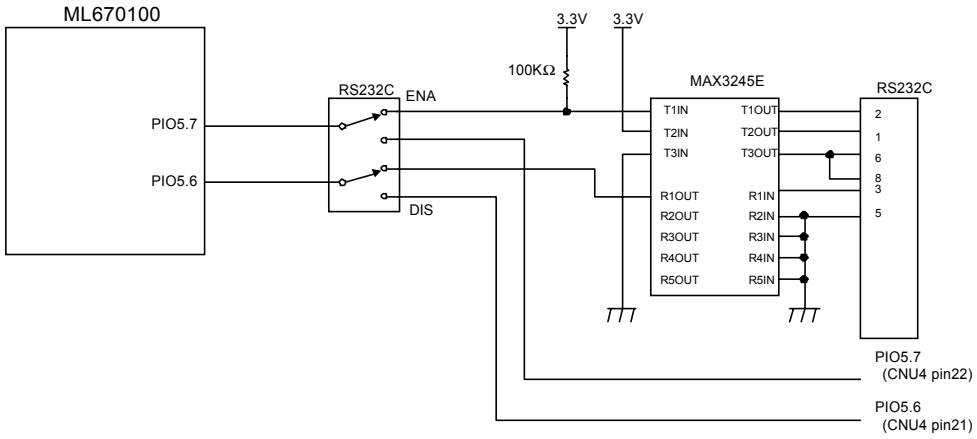


Figure 3.10. Serial Interface Switch (RS232C) Circuits

■ Note ■

The Angel mode requires that this switch be in its ENA position so that the Board can use the ML670100 serial port pins PIO5.6 and PIO5.7 to communicate with the development host. As result, the user application system does not have access to these two pins.

3.1.6 Memory Mask Jumpers (J1 to J4)

These jumpers control ML670100 read/write access to external memory (SRAM and Flash) on the Board.

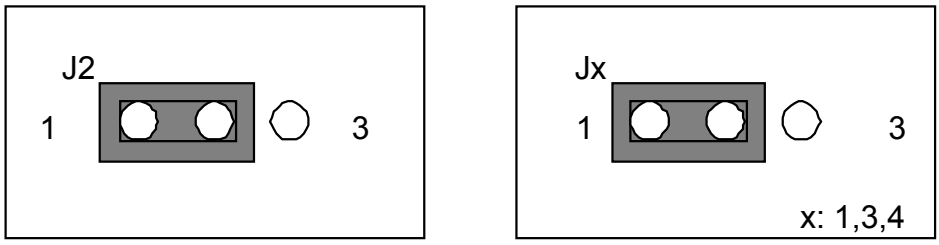


Figure 3.11. Memory Mask Jumpers (J1 to J4)

These jumpers have the following settings.

Memory Mask Jumper J2

The 1 position enables the mask, blocking write access to Flash memory addresses 0x00800000 to 0x0080ffff. The 3 position disables the mask, permitting access.
The normal setting is 1 to prevent accidental overwrites of the boot and Angel portions of the Flash memory.

Memory Mask Jumper J1

The 3 position enables the mask, blocking write access to Flash memory addresses 0x00800000 to 0x0083ffff. The 1 position disables the mask, permitting access.
Memory mask jumper J2 controls access to the first quarter of the Flash memory (0x00800000 to 0x0080ffff).

Memory Mask Jumper J3

The 3 position enables the mask, blocking read/write access to external memory 1, the SRAM at addresses 0x00000000 to 0x0007ffff. The 1 position disables the mask, permitting access.

Memory Mask Jumper J4

The 3 position enables the mask, blocking read/write access to external memory 2, the SRAM at addresses 0x00100000 to 0x0017ffff. The 1 position disables the mask, permitting access.
Figure 3.12 shows the related circuitry.

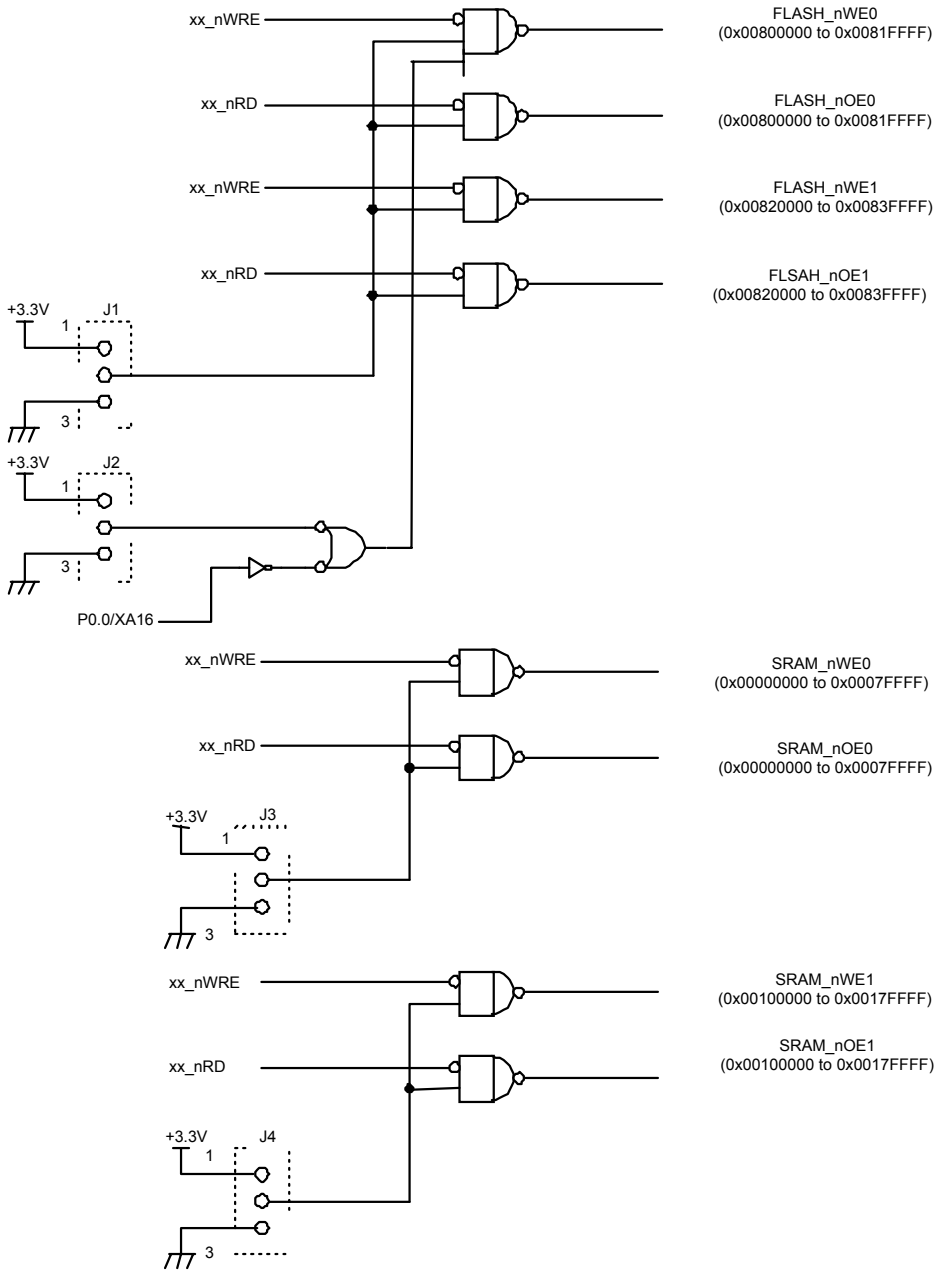


Figure 3.12. Memory Mask Jumpers (J1 to J4) Circuits

3.1.7 EIR0 and EFIQ Input Selection Jumpers (EIR0 and EFIQ)

These jumpers specify the sources for the ML670100 EIR0 and EFIQ pin inputs: the switches on the Board or external signals from the user application system.

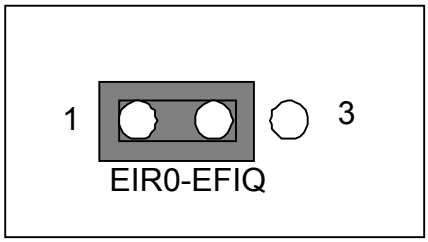


Figure 3.13. EIR0 and EFIQ Input Selection Jumpers (EIR0 and EFIQ)

Connecting a jumper to the IN side enables use of the buttons; the EXT position connects the corresponding ML670100 pin to the corresponding user interface connector pin.

Figure 3.14 shows the related circuitry.

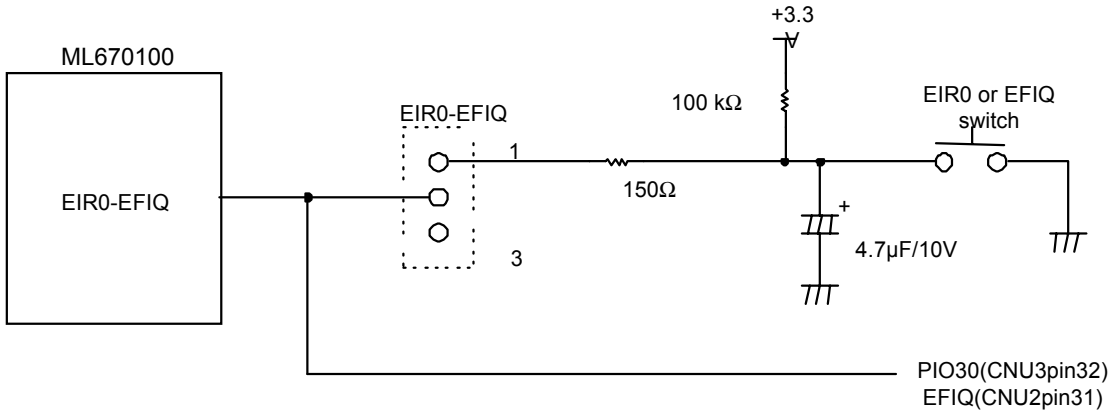


Figure 3.14. EIR0 and EFIQ Input Selection Jumpers (EIR0 and EFIQ) Circuits

■ Note ■

If the EIR0-EFIQ jumper is connected to the 1 side, the signals from the user application system remain connected to the corresponding user interface connector pins through a capacitance and a resistance.

3.2 Connecting Power Supply Cable

The Oki ML670100 CPU Board ships with the power cable shown in Figure 3.15.

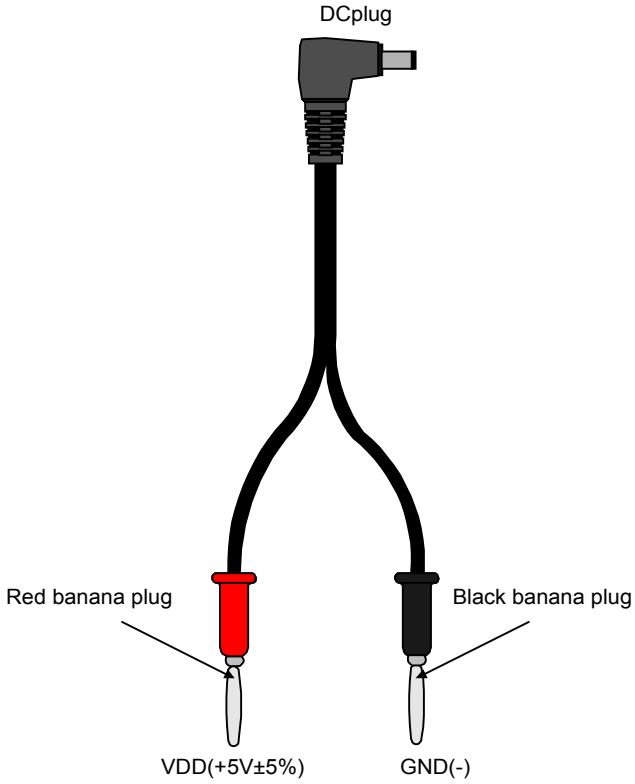


Figure 3.15. Oki ML670100 CPU Board Power Supply Cable

Supply power to the Board by connecting it with this cable to a stabilized DC power supply (5 V DC ± 5%).

Below are the procedures for connecting both ends of this cable.

(1) Connect the cable to the Board's DC connector.

Fit the plug end of the power supply cable into the DC connector in the upper right corner of the Board.

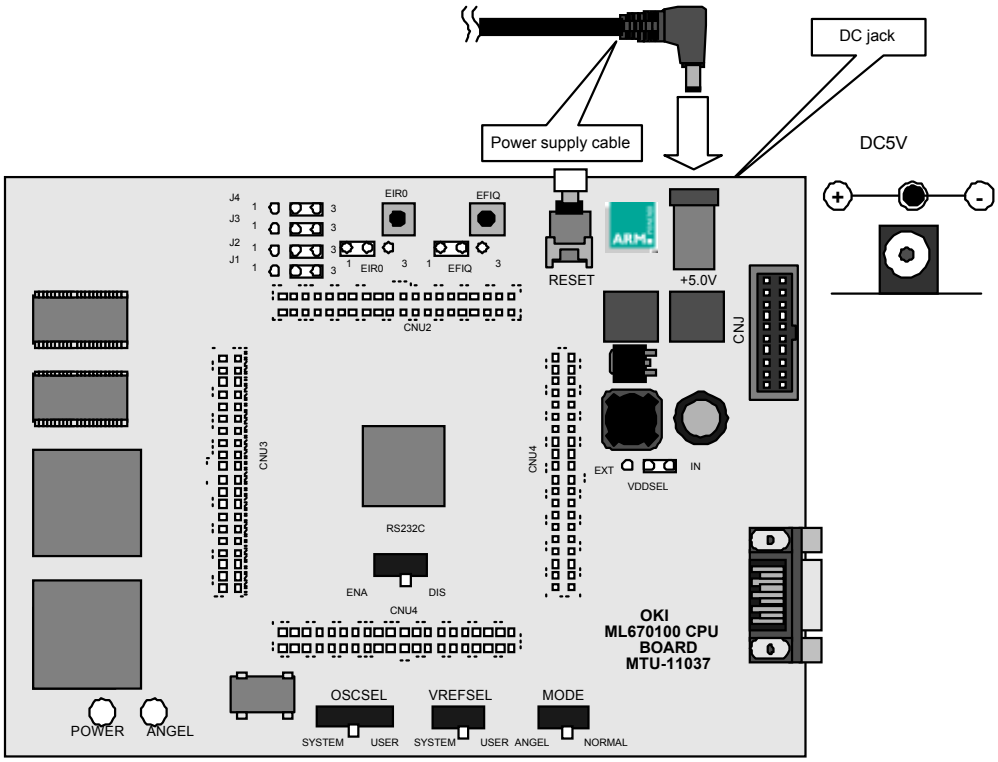


Figure 3.16. Power Supply Cable Connections (1/2)

(2) Connect the banana plugs to a stabilized DC power supply.

Connect the red banana plug to the stabilized DC power supply's plus outlet and the black one to the minus outlet. Double-check to make sure that the connections are not reversed.

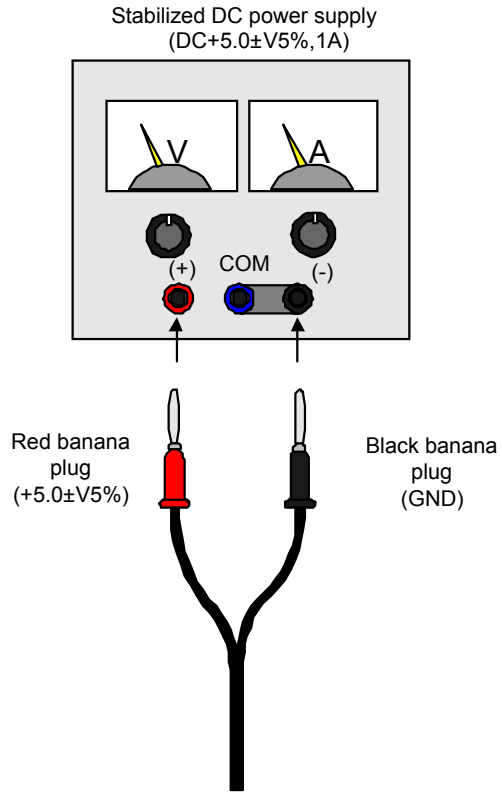


Figure 3.17. Power Supply Cable Connections (2/2)

Warning

Make sure that the banana plugs go into the correct outlets. Reversing the polarity leads to breakdown or fire and risks electrical shock.

3.3 Connecting to User Application System

These connectors provide access to the I/O pins forming the ML670100 user interface. The Oki ML670100 CPU Board provides two ways to connect them to the user application system.

- Directly with the user interface connectors (CNU1 to CNU4)
- Indirectly with the optional user connector Board (USRCN) and the user cable

Figures 3.18 and 3.19 show the optional user connector Board (USRCN) and the user cable.

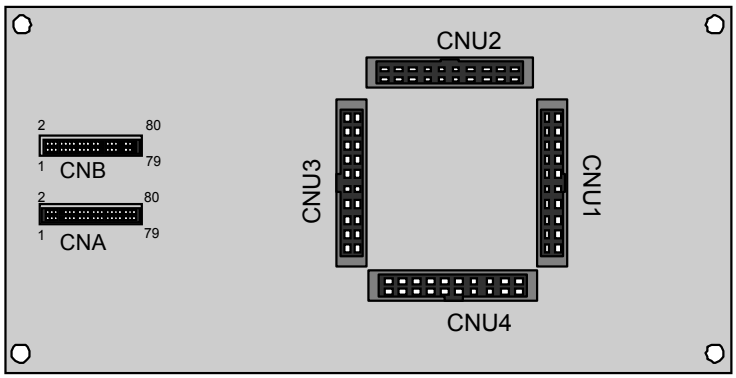


Figure 3.18. Optional User Connector Board (USRCN)

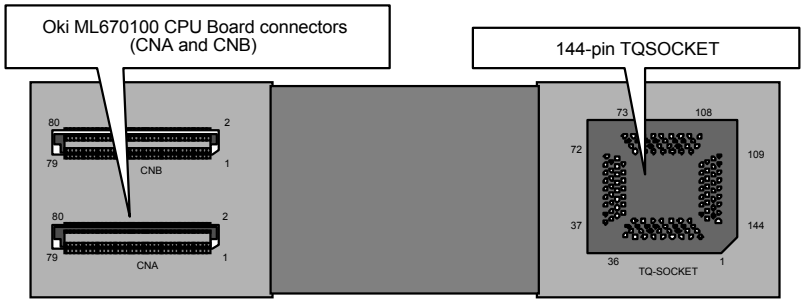


Figure 3.19. User Cable

The user connector Board (USRCN) has four connectors, labeled CNU1 to CNU4, that plug into their counterparts on the Oki ML670100 CPU Board and two, labeled CNA and CNB, for connecting the user cable.

The user cable has two connectors, labeled CNA and CNB, that plug into their counterparts on the user connector Board (USRCN) and a 144-pinTQSOCKET for connecting the user application system.

Below are the procedures for connecting both ends of this cable.

(1) Plug user connector Board (USRCN) connectors CNU1 to CNU4 into their counterparts on the Oki ML670100 CPU Board.

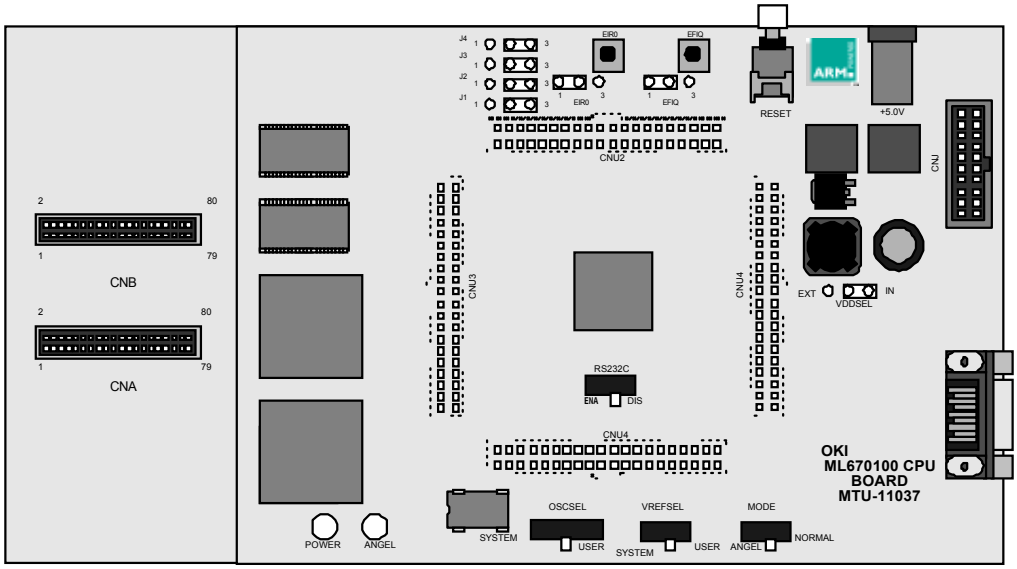


Figure 3.20. Connecting to User Application System (1/2)

(2) Connect the TQSOCKET to the user application system.

Plug the user cable 144-pinTQSOCKET into a suitable connector provided in the user application system.

Figure 3.21 shows one such connection.

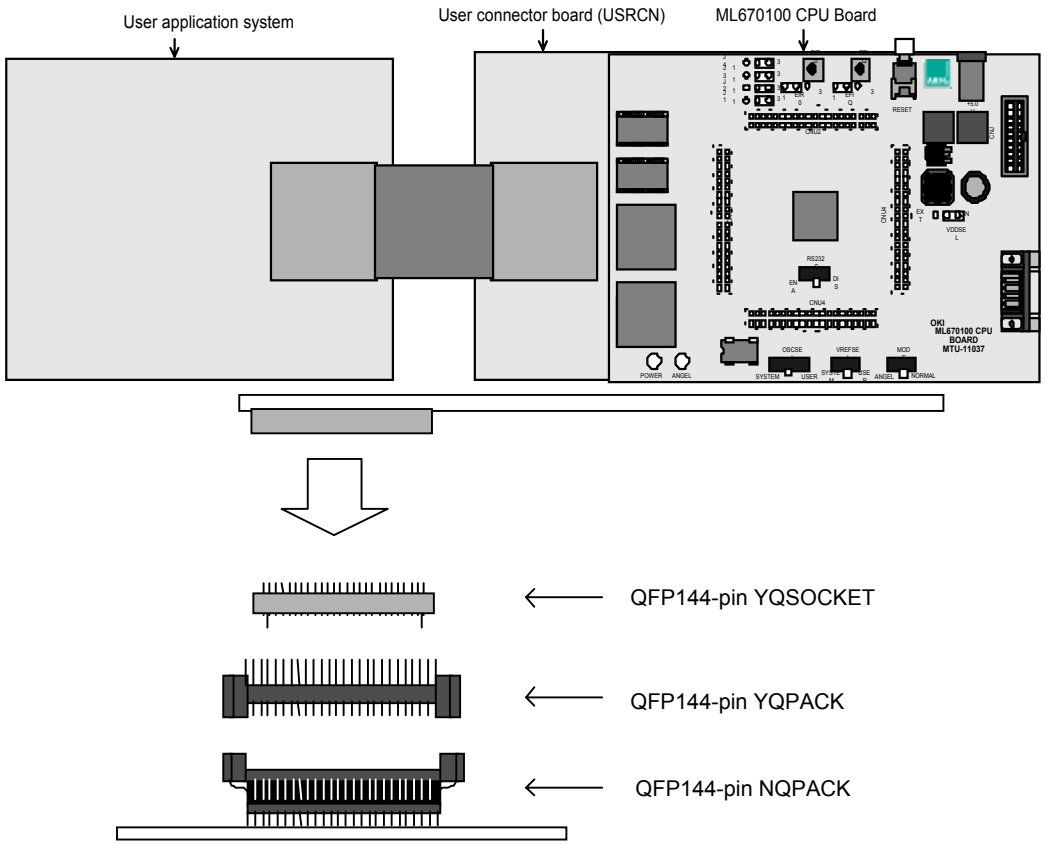


Figure 3.21. Connecting User Cable

The pin assignments for the ML670100 and the user application system connector appear in Chapter 6 "Appendices."

3.4 Connecting to Host

3.4.1 Angel Mode

The mode connects the Oki ML670100 CPU Board directly to the development host with the provided RS232C cable plugged into the RS232C interface connector (RS232C) in the lower left corner of the Board.

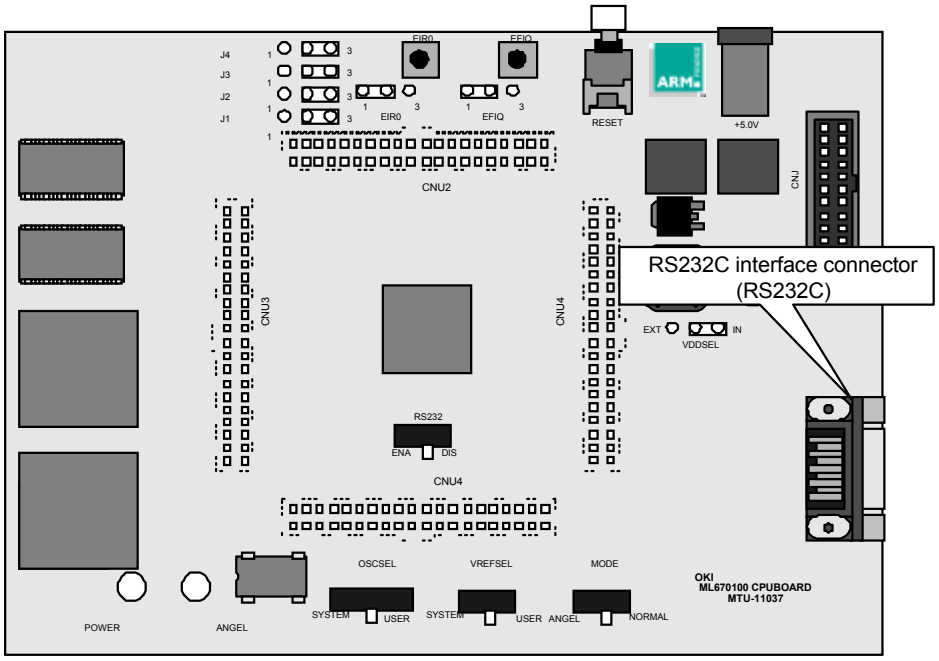


Figure 3.22. RS232C Interface Connector (RS232C)

3.4.2 Normal Mode

The mode connects the Oki ML670100 CPU Board to the development host through a JTAG communications interface unit (Oki Electric ADI Board or ARM Multi-ICE™) connected to the ICE interface connector (CNJ) in the upper right corner of the Board.

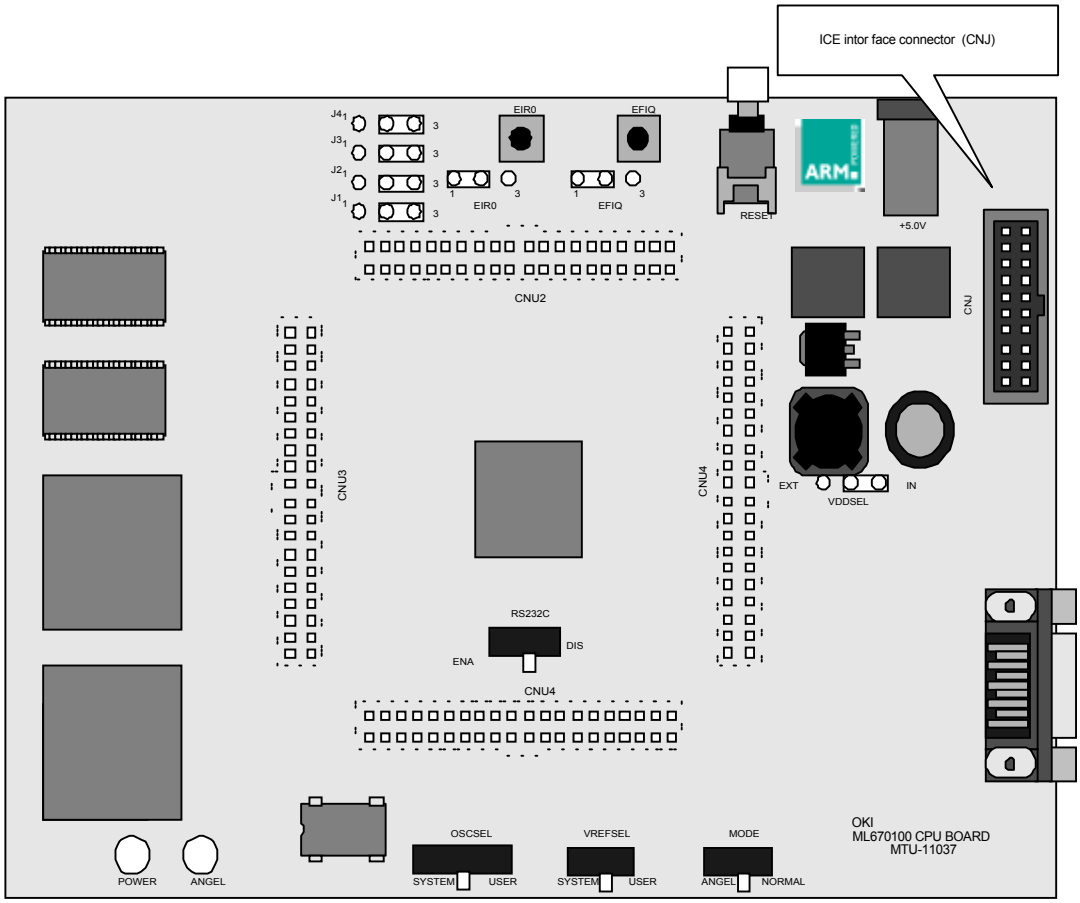


Figure 3.23. ICE Interface Connector (CNJ)

Below are the procedures for connecting the components.

(1) Plug the 20-pin cable provided with the interface unit into the ICE interface connector (CNJ) in the upper right corner of the Board.

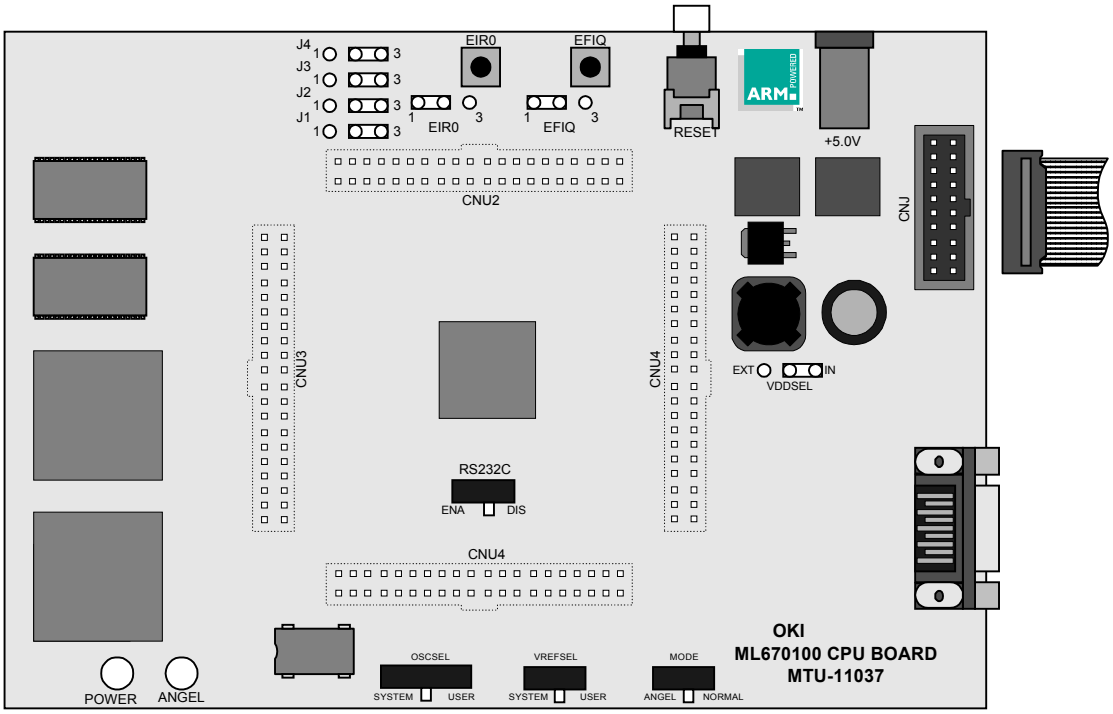


Figure 3.24. Connecting Interface Unit (1/2)

(2) Plug the other end of the cable into the interface unit.

Figure 3.25 shows the connector location for the Oki Electric ADI Board.

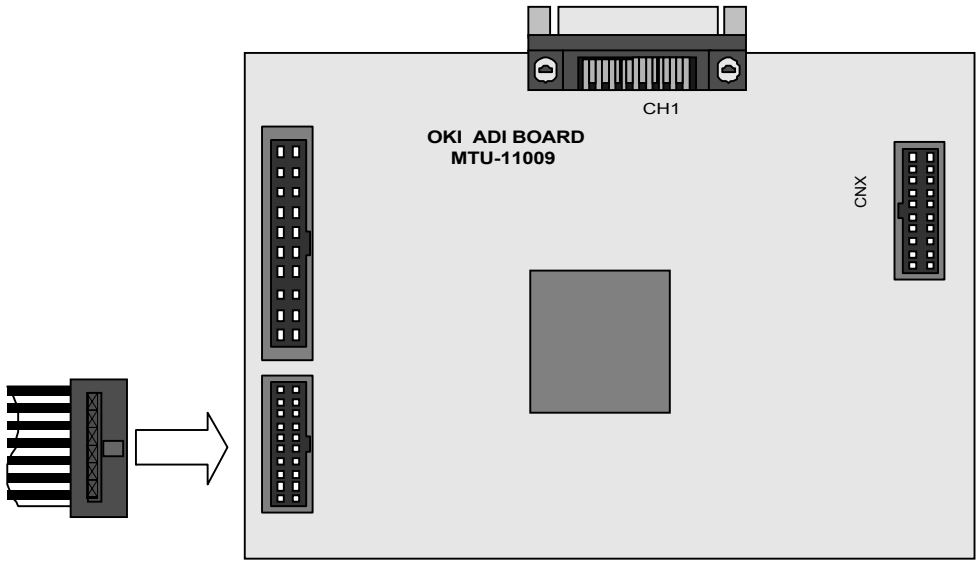


Figure 3.25. Connecting Interface Unit (2/2)

For further details on connecting to the Oki Electric ADI Board or ARM Multi-ICE™, refer to the User's Manual included with the interface unit.

(3) Plug the parallel cable into the parallel interface connector on the interface unit.

(4) Connect the other end of the parallel cable to the development host.

3.5 Procedures

This Section gives the procedures for setting up and using the Oki ML670100 CPU Board. It assumes that the ARM Software Development Toolkit has already been installed.

If the ARM Software Development Toolkit has not been installed, insert the ARM Software Development Toolkit 2.50 CD-ROM in the drive and follow the automatic installation procedure. For further details, refer to the Toolkit package.

3.5.1 Angel Debugging

Double-check all connections shown in Figure 3.26. For further details, see the preceding Section.

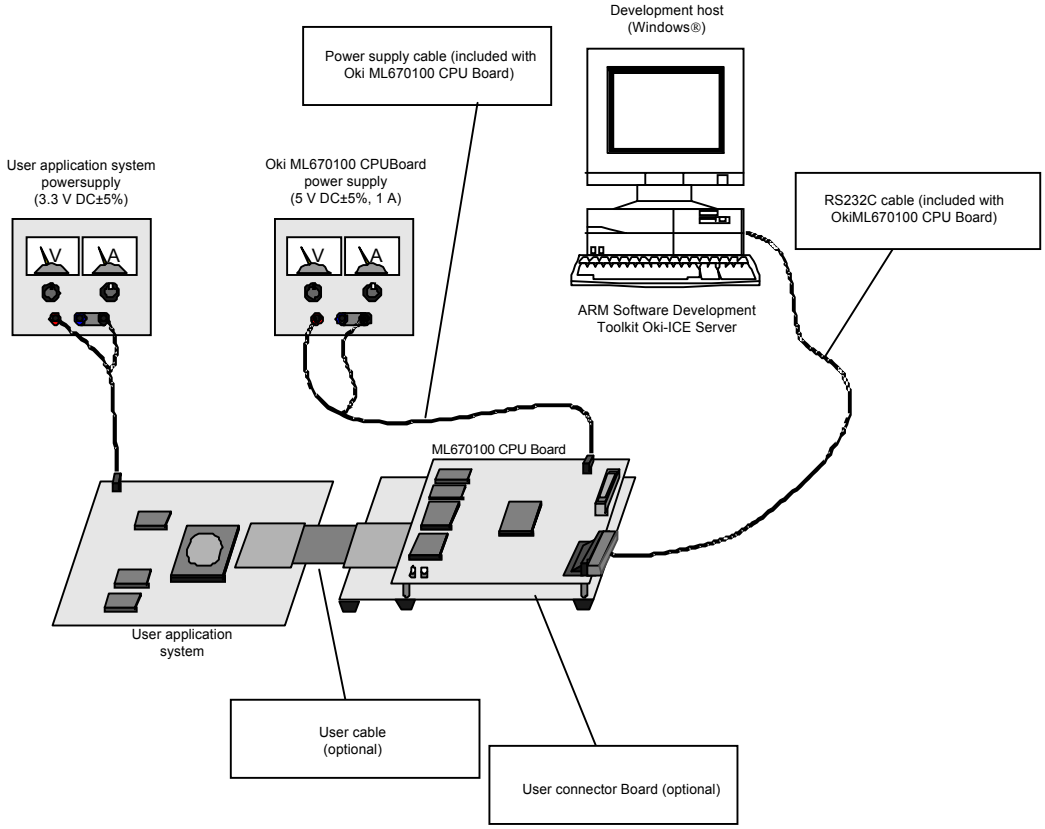


Figure 3.26. Angel Debugging Configuration

Necessary Parts

- Oki ML670100 CPU Board
- RS232C cable
- ARM Software Development Toolkit
- Stabilized DC power supply (5 V DC ± 5%, 1 A)
- Development host (Windows® or Unix®)

3.5.1.1 Switch Setting

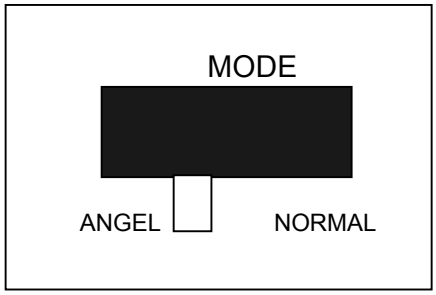


Figure 3.27 Operating Mode Switch (MODE)

Set the MODE switch to its ANGEL setting.

3.5.2 Normal Debugging

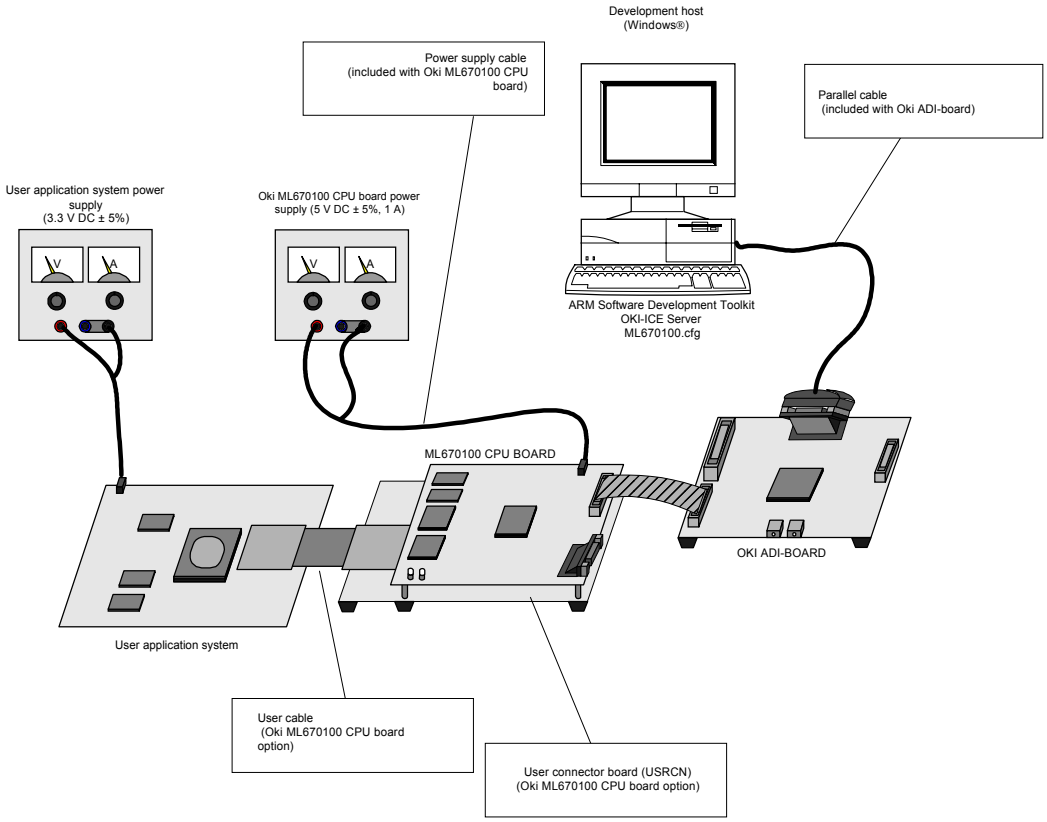


Figure 3.28. Normal Debugging Configuration

ADI Board Necessary Parts

- Oki ML670100 CPU Board
- Parallel cable
- JTAG communications interface unit (Oki Electric ADI Board or ARM Multi-ICE™)
- ARM Software Development Toolkit
- Stabilized DC power supply (5 V DC ± 5%, 1 A)
- Development host (Windows® or Unix®)
- User application system

3.5.2.1 Switch Setting

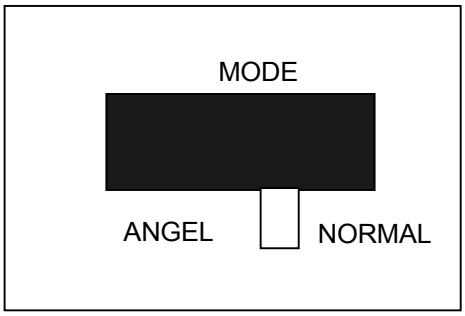


Figure 3.29. Operating Mode Switch (MODE)

Set the MODE switch to its NORMAL setting.

3.5.3 Checking Switch Settings

Before applying the power, make sure that the following switches and jumpers are in the proper positions. Starting up the Board with incorrect settings can lead to faulty operation or breakdown.

- Operating mode switch (MODE)
- Clock selection switch (OSCSEL)
- V_{ref} selection switch (VREFSEL)
- Serial interface switch (RS232C)
- Memory mask jumpers (J1 to J4)
- EIR0 and EFIQ input selection jumpers (EIR0 and EFIQ)

3.5.4 Applying Power

Apply the power to the Oki ML670100 CPU Board and, if present, the user application system.

■ **Note** ■

Always apply the power in the order given: Oki ML670100 CPU Board and then the user application system.

The normal mode powers the JTAG communications interface unit (Oki Electric ADI Board or ARM Multi-ICE^{TM}) connected to the ICE interface connector (CNJ) through the cable joining it to the Oki ML670100 CPU Board.

3.5.5 Angel Debugging

The following are the procedures for Angel debugging.

3.5.6 Loading Debugger

On the development host, load the debugger.

The first time, it starts in ARMulator (software emulation) mode.

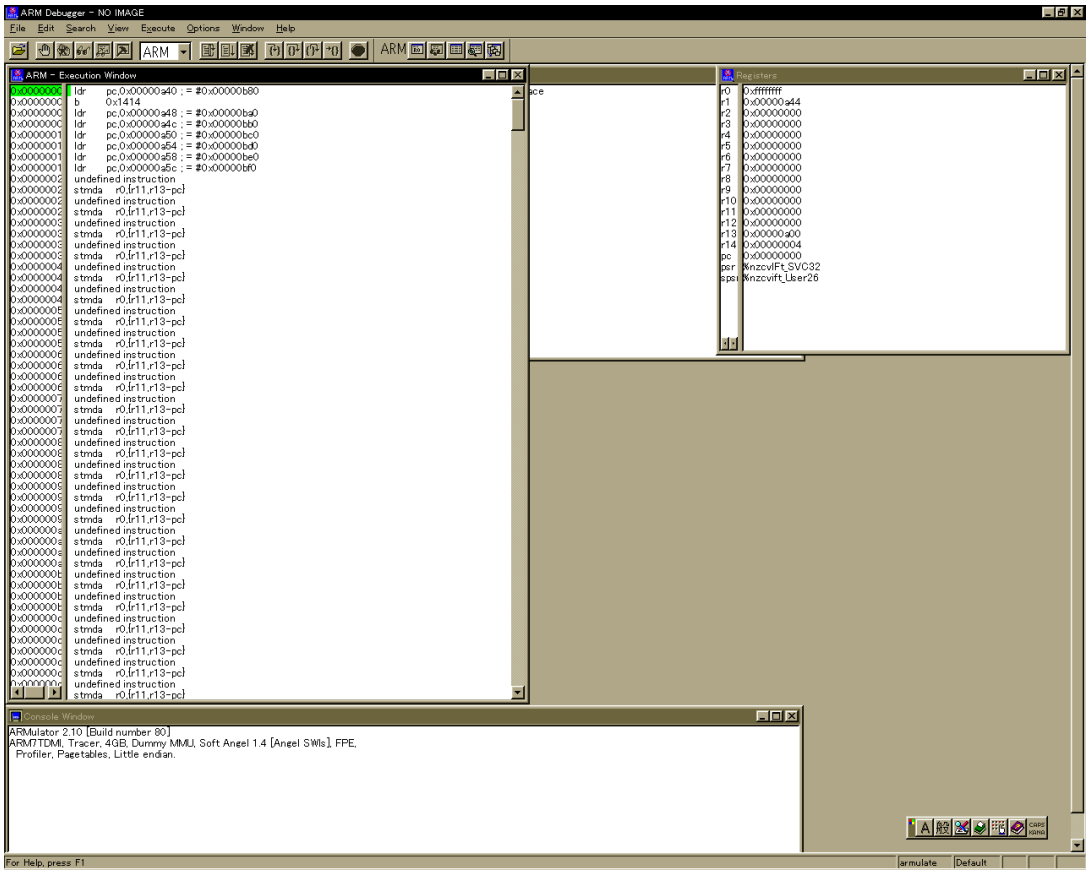


Figure 3.30. ARM Multiprocessor Debugger for Windows® Starting Screen

To change the debugger from ARMulator mode to remote debugging mode, choose "Configure debugger" on the "Options" menu.

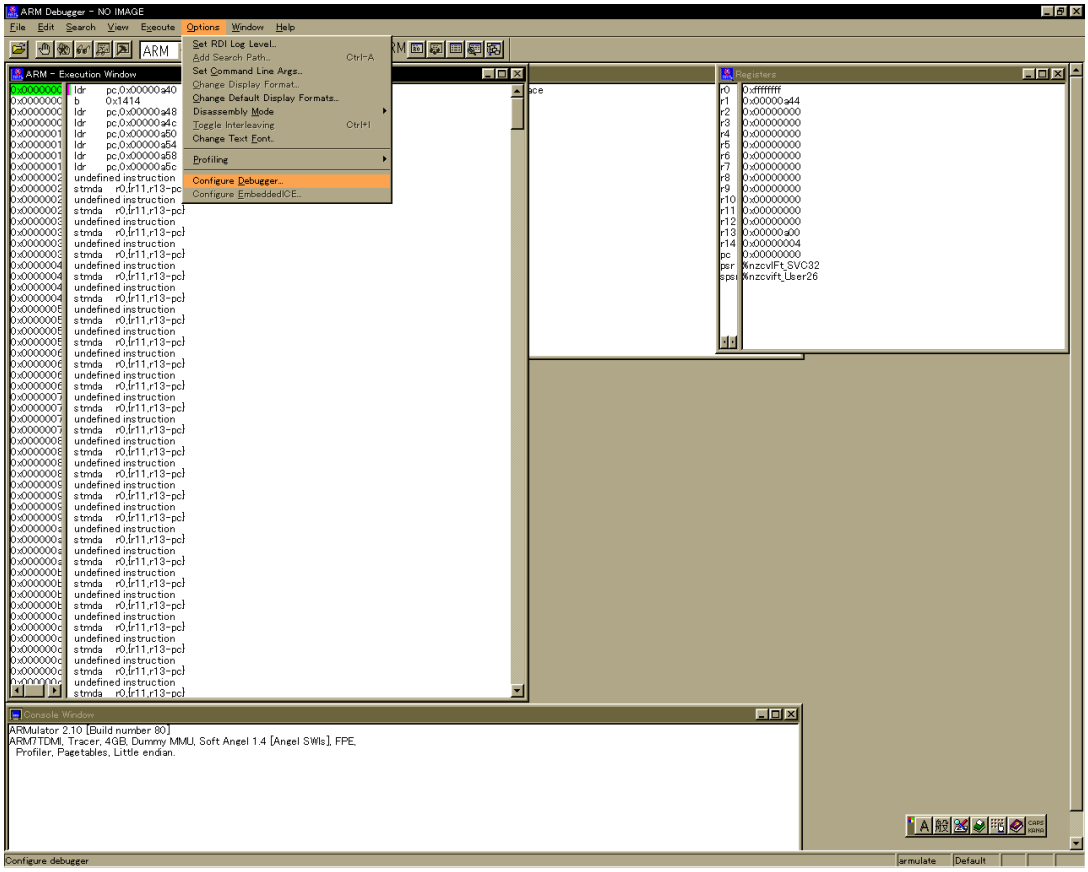


Figure 3.31. Configuring Debugger

In the "Debugger configuration" dialog box that appears, choose "remote_a" as the target and push the "Configure" button.

In the "Remote connection" dialog box that appears, select "Serial" and then specify the port and baud rate (9600or 19200).

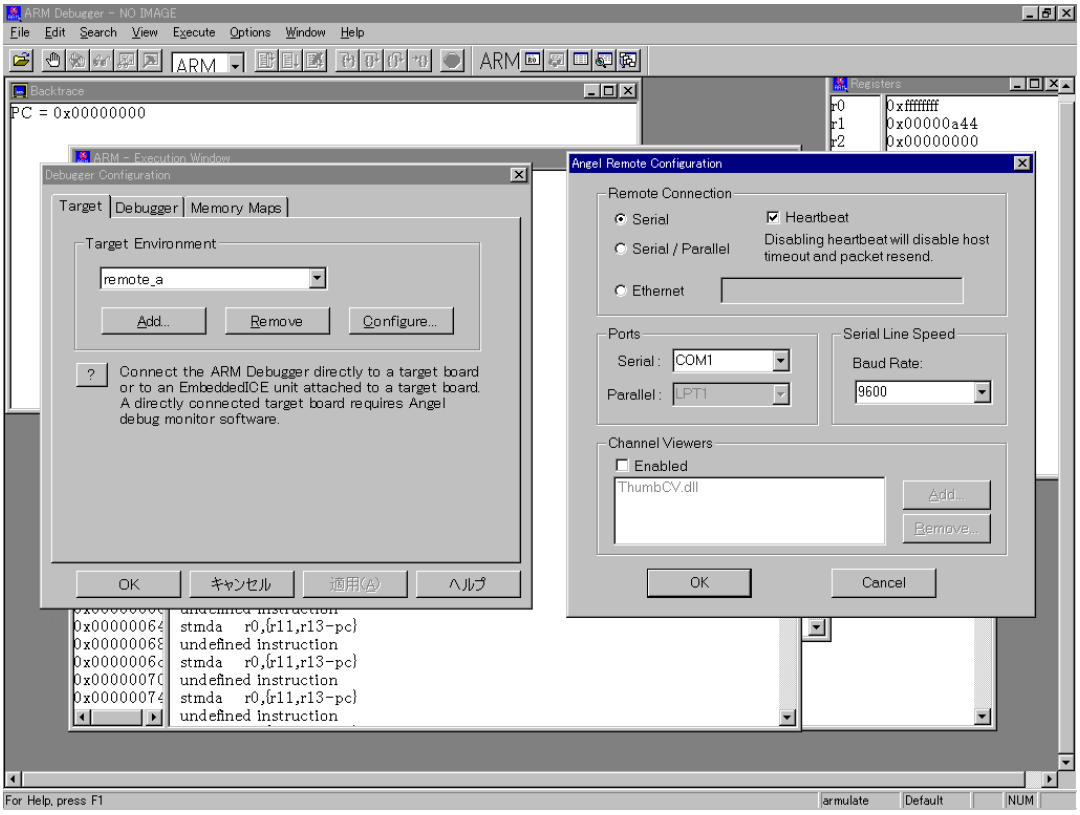


Figure 3.32. Configuring for Remote Debugging

Push the "OK" button to return to the "Debugger configuration" dialog box.

Push the "OK" button to restart the debugger and establish the link to the Angel debugging monitor. If communications are properly established, a boot message similar to the following appears in debugger's console window.

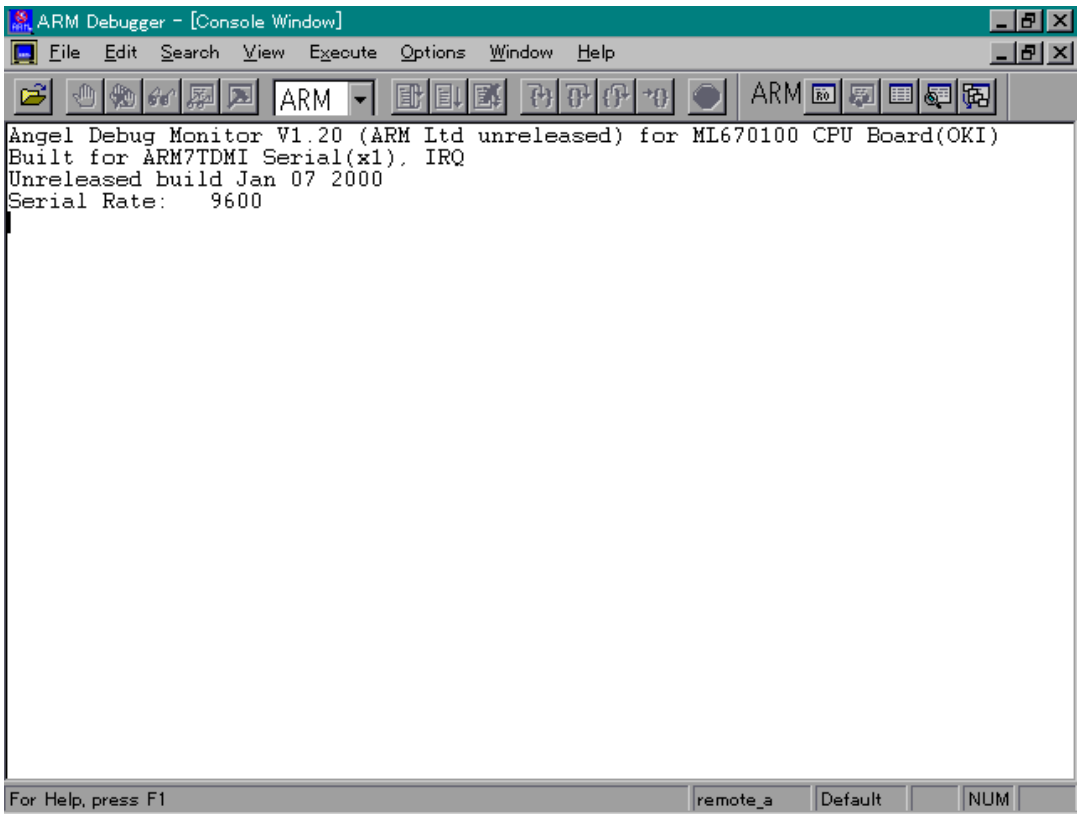


Figure 3.33. Angel Debugger Start-Up Display

*1. The fast interrupt request (FIQ) pin is available to the user application system.

*2. The Angel debugging monitor does not support profiling.

3.5.7 Normal Debugging

The following are the procedures for Normal debugging.

The first step is to run Portmap.exe on the development host running Windows®.

Open an MS-DOS box, change to the directory containing the Oki ICE server software, and type Portmap.

Figure 3.34 shows the Portmap starting screen.

Figure 3.34. Portmap.exe Starting Screen

3.5.8 Loading Oki ICE Server

The next step is to run Oki ICE Server on the development host.

Note that the power to both the user application system and the Oki ADI board must be on. Otherwise, the software simply aborts when it cannot find the latter.

Choose "Load configuration" on the "File" menu and select the ML670100.cfg file from the second CD-ROM to display the following screen.

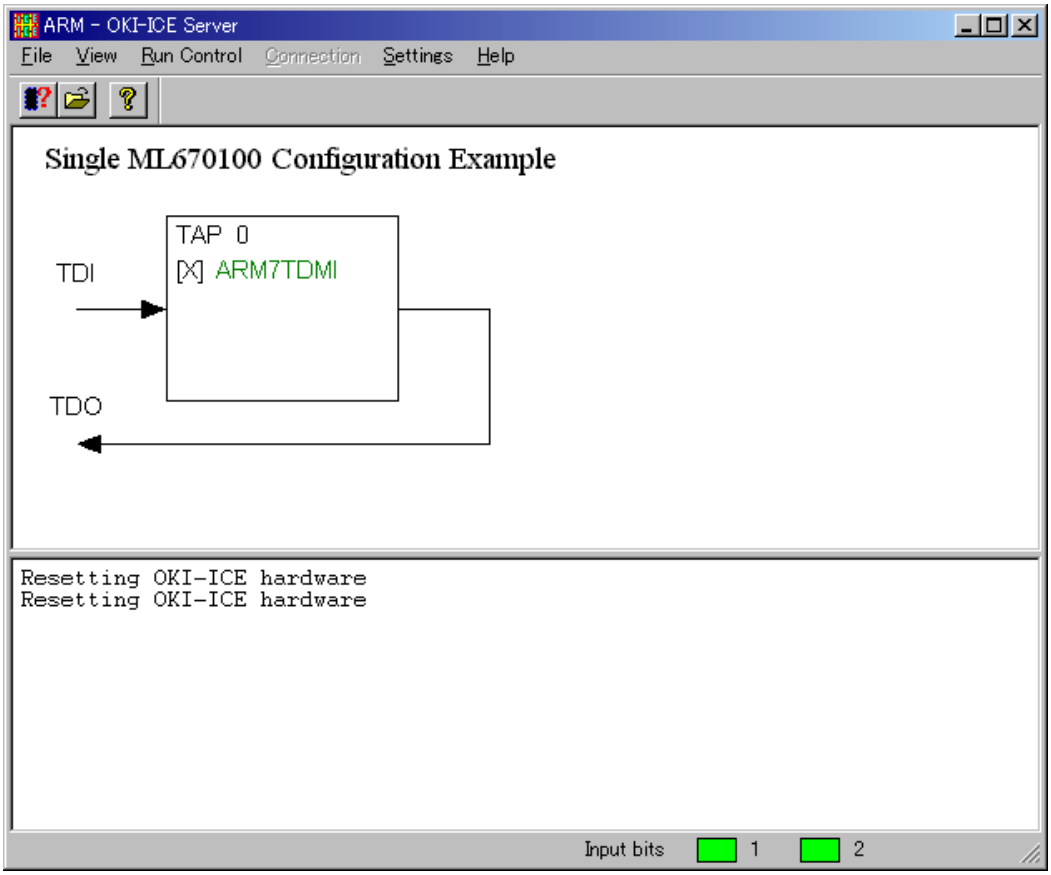


Figure 3.35. Oki ICE Server for Windows®

To have the Oki ICE Server automatically run Portmap.exe and load the configuration file the next time, choose "Start-up settings" on the "Settings" menu to display the following dialog box, select both the "Start port map service" and "Load configuration check boxes, and specify the complete path to the configuration file.

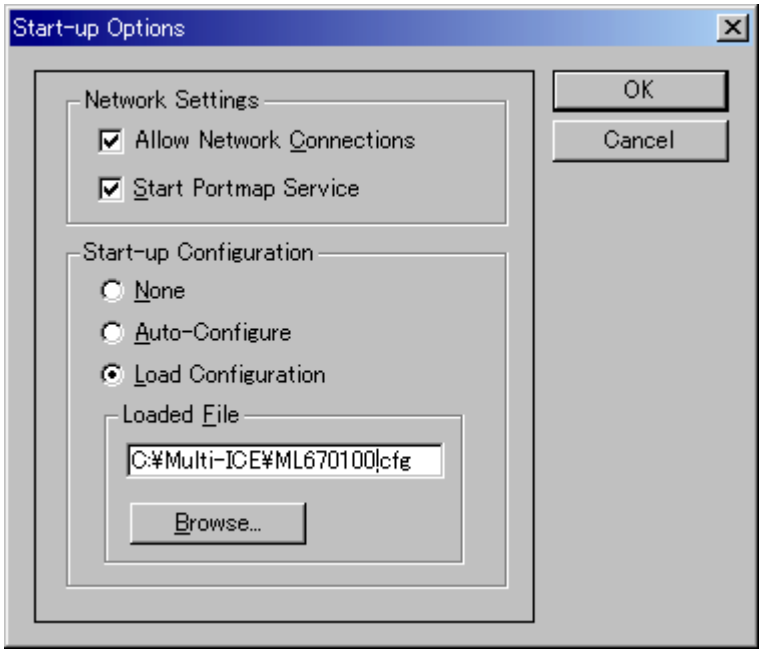


Figure 3.36. Start-Up Settings Dialog Box

3.5.9 Loading Debugger

On the development host, load the debugger.

The first time, it starts in ARMulator (software emulation) mode.

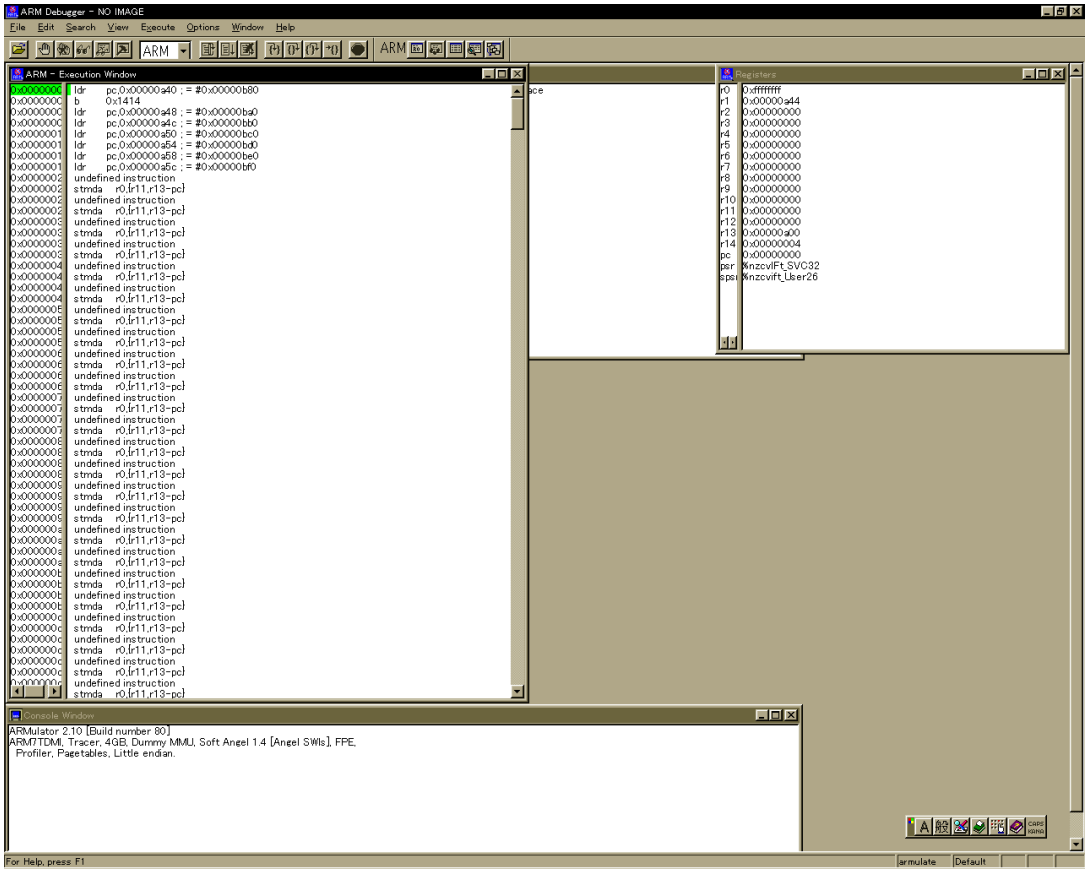


Figure 3.37. ARM Multiprocessor Debugger for Windows®

To change the debugger from ARMulator mode to remote debugging mode, choose "Configure debugger" on the "Options" menu.

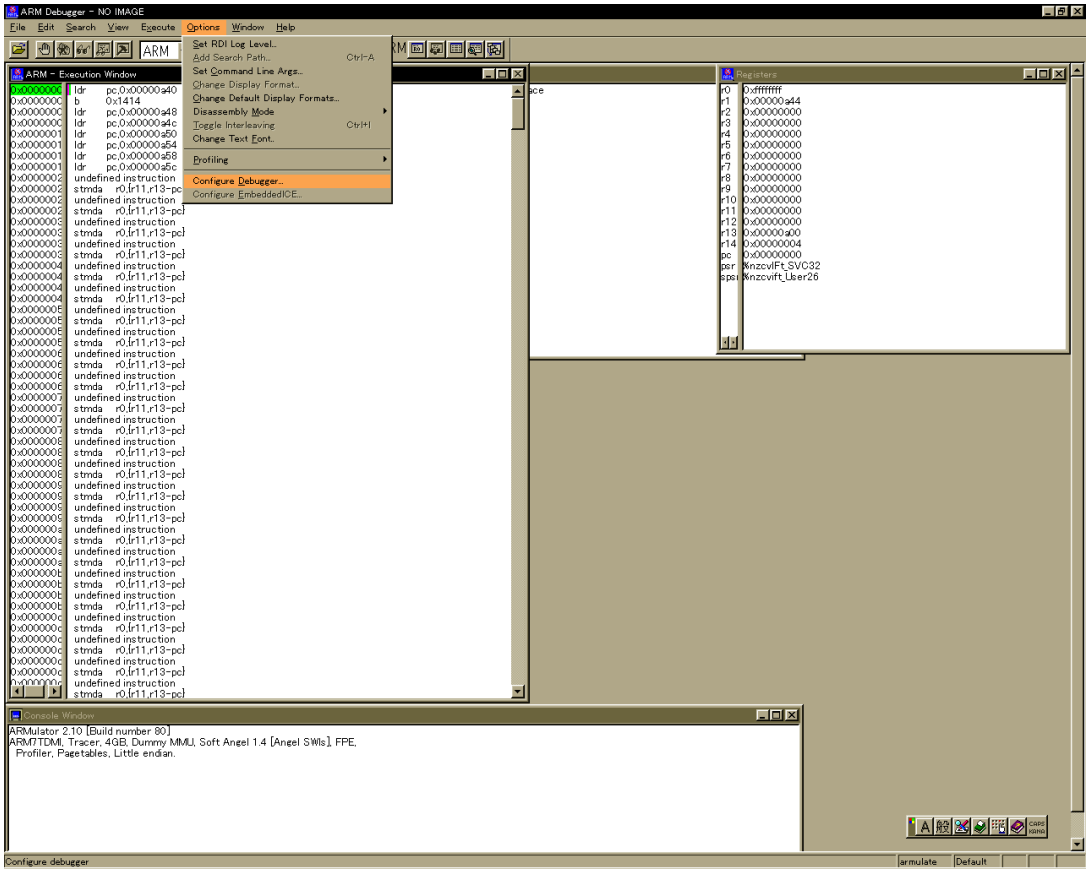


Figure 3.38. Configuring Debugger

In the "Debugger configuration" dialog box that appears, specify the target JTAG communications interface unit: Oki Electric ADI Board or ARM Multi-ICE™.

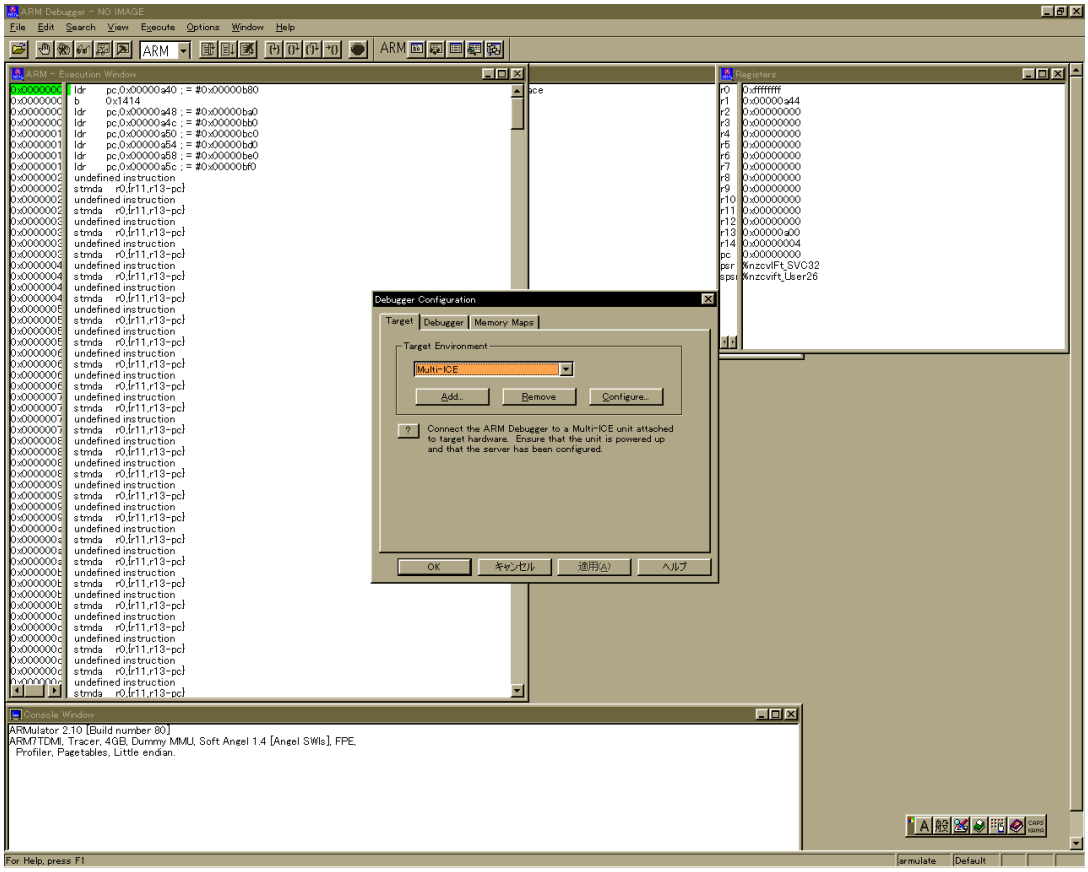


Figure 3.39. Setting Up for Remote Debugging

Once the debugger has established a link with the target JTAG communications interface unit, the following screen appears.

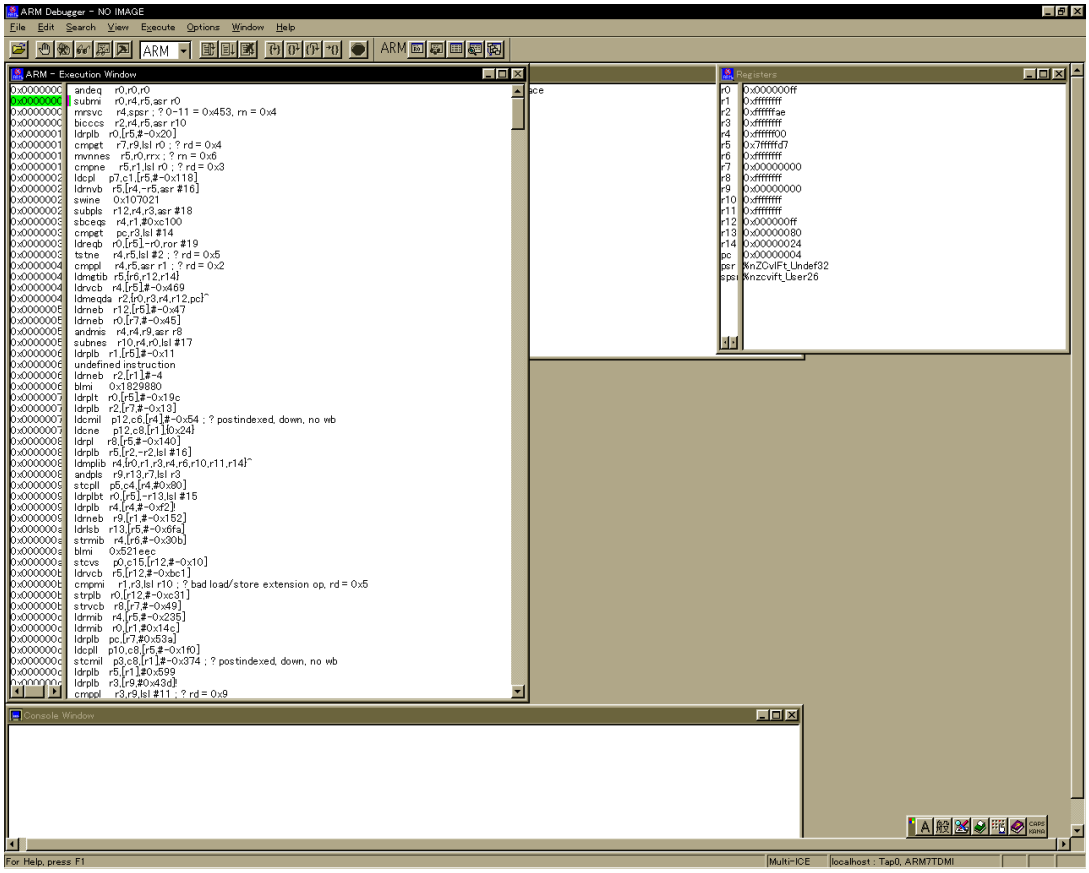


Figure 3.40. ARM Multiprocessor Debugger for Windows®

The Oki ML670100 CPU Board is now ready for remote debugging.

For further details on remote debugging with the ARM Software Development Toolkit, see the ARM Software Development Toolkit User Guide.

Chapter 4 User Interface

This Chapter contains the procedures for connecting the Oki ML670100 CPU Board to the user application system for in-place debugging of the user application program.

4.1 Overview

The evaluation chip on the Oki ML670100 CPU Board features the same memory spaces, peripherals, and I/O pins (See Note 1) as the target ML670100.

Connecting the I/O pins available on the Oki ML670100 CPU Board to the user application system with the user interface connectors and optional user cable permits in-place debugging.

Figure 4.1 outlines this relationship.

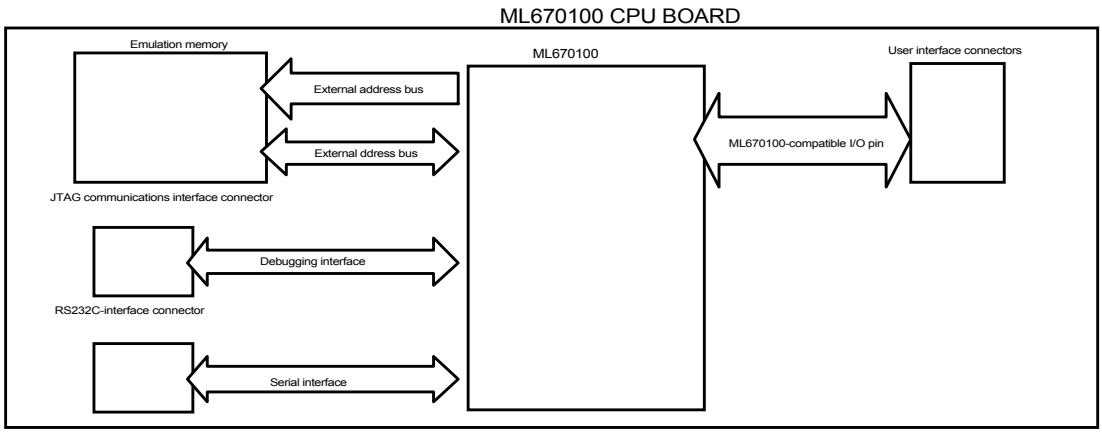


Figure 4.1. User Interface Equivalence

■ Note 1 ■

The Oki ML670100 CPU Board sometimes handles the following ML670100 built-in peripheral ports and pins differently: PIO0, PIO1, PIO2.5, PIO2.6, PIO5.6, PIO5.7, and PIO8. For further details, see Chapter 5 "Notes on Debugging."

4.2 User Interface

4.2.1 User Interface Connectors (CNU1 to CNU4)

These four connectors are for directly connecting the Oki ML670100 CPU Board to the user application system for in-place debugging.

Figure 4.2 shows the location; Table 4.1, the pin assignments.

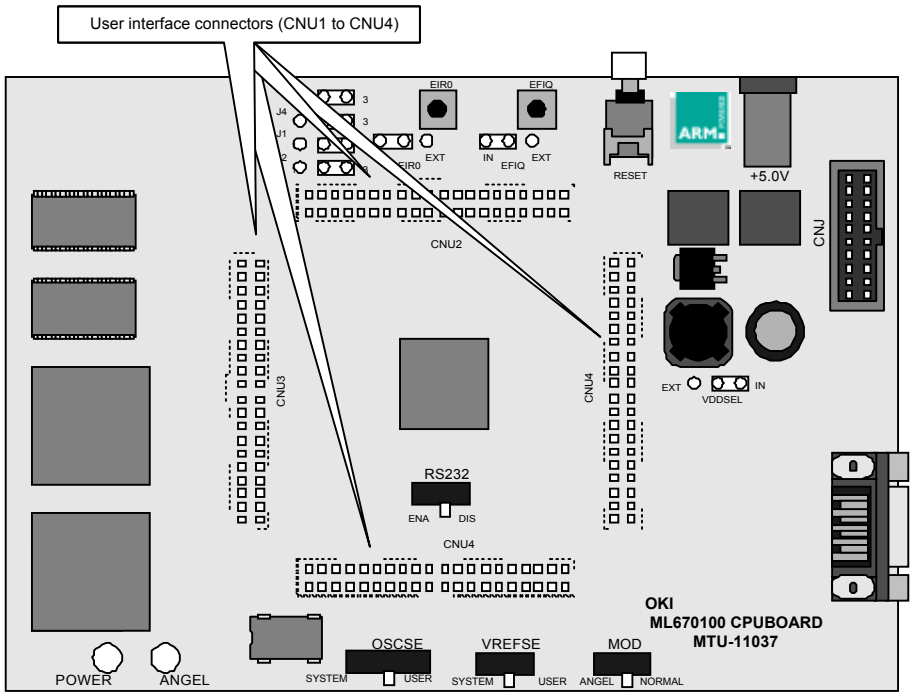


Figure 4.2. User Interface Connectors (CNU1 to CNU4)

Table 4.1. CNU1 and CNU2 Pin Assignments

CNU1No.	Pin Name	I/O	CNU2No.	Pin Name	I/O
1	AI4	I	1	GND	O
2	AI3	I	2	VDD	I
3	AI2	I	3	XA0	O
4	AI1	I	4	XA1	O
5	AI0	I	5	XA2	O
6	VREF	I	6	XA3	O
7	N.C.	-	7	XA4	O
8	VDD	I	8	XA5	O
9	N.C.	-	9	XA6	O
10	DBSEL *1	I	10	XA7	O
11	PIO6.0	I/O	11	GND	O
12	PIO6.1	I/O	12	VDD	I
13	PIO6.2	I/O	13	XA8	O
14	PIO6.3	I/O	14	XA9	O
15	PIO6.4	I/O	15	XA10	O
16	PIO6.5	I/O	16	XA11	O
17	PIO6.6	I/O	17	XA12	O
18	PIO6.7	I/O	18	XA13	O
19	PIO7.0	I/O	19	XA14	O
20	PIO7.1	I/O	20	XA15	O
21	PIO7.2	I/O	21	GND	O
22	GND	O	22	VDD	I
23	VDD	I	23	PIO0.0 *3	I/O
24	PIO7.3	I/O	24	PIO0.1 *3	I/O
25	PIO7.4	I/O	25	PIO0.2 *3	I/O
26	PIO7.5	I/O	26	PIO0.3 *3	I/O
27	PIO7.6	I/O	27	PIO0.4 *3	I/O
28	PIO7.7	I/O	28	PIO0.5 *3	I/O
29	PIO8.0 *2	I/O	29	PIO0.6 *3	I/O
30	PIO8.1 *2	I/O	30	PIO0.7 *3	I/O
31	PIO8.2 *2	I/O	31	EFIQ/	I
32	PIO8.3 *2	I/O	32	EA/ *3	I
33	PIO8.4 *2	I/O	33	GND	O
34	PIO8.5 *2	I/O	34	VDD	I
35	PIO8.6 *2	I/O	35	XD0	I/O
36	PIO8.7 *2	I/O	36	XD1	I/O
37	N.C	-	37	N.C	-
38	N.C	-	38	N.C	-
39	GND	O	39	GND	O
40	GND	O	40	GND	O

*1 These pins have 100-kΩ pull-up resistances.

*2 The NORMAL position of the MODE switch disconnects all but one of these pins. It adds a 10-kΩ pull-up resistance to the PIO8.2 pin.

*3 These pins are used for their secondary functions, so are not available for use as port pins.

*4 This pin has a 100-kΩ pull-down resistance.

Table 4.2. CNU3 and CNU4 Pin Assignments

CNU1No.	Pin Name	I/O	CNU2No.	Pin Name	I/O
1	XD2	I/O	1	PIO3.5	I/O
2	XD3	I/O	2	PIO3.6	I/O
3	XD4	I/O	3	PIO3.7	I/O
4	XD5	I/O	4	GND	O
5	XD6	I/O	5	PIO4.0	I/O
6	XD7	I/O	6	PIO4.1	I/O
7	GND	O	7	PIO4.2	I/O
8	VDD	I	8	PIO4.3	I/O
9	PIO1.0 *5	I/O	9	PIO4.4	I/O
10	PIO1.1 *5	I/O	10	PIO4.5	I/O
11	PIO1.2 *5	I/O	11	PIO4.6	I/O
12	PIO1.3 *5	I/O	12	PIO4.7	I/O
13	PIO1.4 *5	I/O	13	GND	O
14	PIO1.5 *5	I/O	14	VDD	I
15	PIO1.6 *5	I/O	15	PIO5.0	I/O
16	PIO1.7 *5	I/O	16	PIO5.1	I/O
17	CS0/	O	17	PIO5.2	I/O
18	RD/	O	18	PIO5.3	I/O
19	WRE_WRL/	O	19	PIO5.4	I/O
20	GND	O	20	PIO5.5	I/O
21	VDD	I	21	PIO5.6 *6	I/O
22	PIO2.0	I/O	22	PIO5.7 *6	I/O
23	PIO2.1	I/O	23	CLKOUT	O
24	PIO2.2	I/O	24	GND	I/O
25	PIO2.3	I/O	25	OSC0	I
26	PIO2.4	I/O	26	N.C.	-
27	PIO2.5 *5	I/O	27	VDD	I
28	PIO2.6 *5	I/O	28	N.C.	-
29	PIO2.7	I/O	29	FSEL	I
30	GND	O	30	PLLEN	I
31	VDD	I	31	RESETB/ *7	I
32	PIO3.0	I/O	32	GND	O
33	PIO3.1	I/O	33	GND	O
34	PIO3.2	I/O	34	AI7	I
35	PIO3.3	I/O	35	AI6	I
36	PIO3.4	I/O	36	AI5	I
37	N.C	-	37	N.C	-
38	N.C	-	38	N.C	-
39	GND	O	39	GND	O
40	GND	O	40	GND	O

*5 These pins are used for their secondary functions, so are not available for use as port pins.

*6 The ENA position of theRS232C-SEL switch disconnects all these pins.

*7 This pin has a 10-kΩ pull-up resistance.

4.2.2 User Connector Board (USRCN)

This optional Board fits between the Oki ML670100 CPU Board and the user cable leading to the user application system.

Tables 4.3 and 4.4 show the pin assignments for the CNA and CNB connectors.

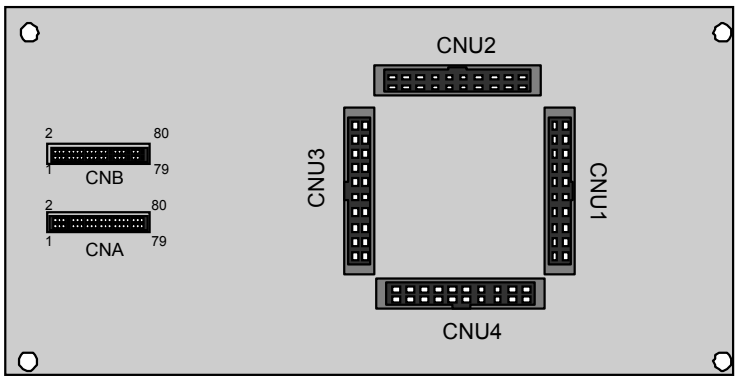


Figure 4.3. User Connector Board (USRCN)

Table 4.3. CNUA Pin Assignments

CNU1No.	Pin Name	I/O	CNU2No.	Pin Name	I/O
1	AI4	I	41	XA2	O
2	AI3	I	42	XA3	O
3	AI2	I	43	XA4	O
4	AI1	I	44	XA5	O
5	AI0	I	45	XA6	O
6	VREF	I	46	XA7	O
7	N.C.	-	47	GND	O
8	VDD	I	48	VDD	I
9	N.C.	-	49	XA8	O
10	DBSEL *1	I	50	XA9	O
11	PIO6.0	I/O	51	XA10	O
12	PIO6.1	I/O	52	XA11	O
13	PIO6.2	I/O	53	XA12	O
14	PIO6.3	I/O	54	XA13	O
15	PIO6.4	I/O	55	XA14	O
16	PIO6.5	I/O	56	XA15	O
17	PIO6.6	I/O	57	GND	O
18	PIO6.7	I/O	58	VDD	I
19	PIO7.0	I/O	59	PIO0.0 *3	I/O
20	PIO7.1	I/O	60	PIO0.1 *3	I/O
21	PIO7.2	I/O	61	PIO0.2 *3	I/O
22	GND	O	62	PIO0.3 *3	I/O
23	VDD	I	63	PIO0.4 *3	I/O
24	PIO7.3	I/O	64	PIO0.5 *3	I/O
25	PIO7.4	I/O	65	PIO0.6 *3	I/O
26	PIO7.5	I/O	66	PIO0.7 *3	I/O
27	PIO7.6	I/O	67	EFIQ/	I
28	PIO7.7	I/O	68	EA/ *4	I
29	PIO8.0 *2	I/O	69	GND	O
30	PIO8.1 *2	I/O	70	VDD	I
31	PIO8.2 *2	I/O	71	XD0	I/O
32	PIO8.3 *2	I/O	72	XD1	I/O
33	PIO8.4 *2	I/O	73	N.C.	-
34	PIO8.5 *2	I/O	74	N.C.	-
35	PIO8.6 *2	I/O	75	N.C.	-
36	PIO8.7 *2	I/O	76	N.C.	-
37	GND	O	77	GND	O
38	VDD	I	78	GND	O
39	XA0	O	79	GND	O
40	XA1	O	80	GND	O

*1 This pin has a 100-kΩ pull-up resistance.

*2 The NORMAL position of the MODE switch disconnects all but one of these pins. It adds a 10-kΩ pull-up resistance to the PIO8.2 pin.

*3 These pins are used for their secondary functions, so are not available for use as port pins.

*4 This pin has a 100-kΩ pull-down resistance.

Table 4.4. CNUB Pin Assignments

CNU1No.	Pin Name	I/O	CNU2No.	Pin Name	I/O
1	XD2	I/O	41	PIO4.0	I/O
2	XD3	I/O	42	PIO4.1	I/O
3	XD4	I/O	43	PIO4.2	I/O
4	XD5	I/O	44	PIO4.3	I/O
5	XD6	I/O	45	PIO4.4	I/O
6	XD7	I/O	46	PIO4.5	I/O
7	GND	O	47	PIO4.6	I/O
8	VDD	I	48	PIO4.7	I/O
9	PIO1.0 *5	I/O	49	GND	O
10	PIO1.1 *5	I/O	50	VDD	I
11	PIO1.2 *5	I/O	51	PIO5.0	I/O
12	PIO1.3 *5	I/O	52	PIO5.1	I/O
13	PIO1.4 *5	I/O	53	PIO5.2	I/O
14	PIO1.5 *5	I/O	54	PIO5.3	I/O
15	PIO1.6 *5	I/O	55	PIO5.4	I/O
16	PIO1.7 *5	I/O	56	PIO5.5	I/O
17	CS0/	O	57	PIO5.6 *6	I/O
18	RD/	O	58	PIO5.7 *6	I/O
19	WRE_WRL/	O	59	CLKOUT	O
20	GND	O	60	GND	I/O
21	VDD	I	61	OSC0	I
22	PIO2.0	I/O	62	N.C.	-
23	PIO2.1	I/O	63	VDD	I
24	PIO2.2	I/O	64	N.C.	-
25	PIO2.3	I/O	65	FSEL	I
26	PIO2.4	I/O	66	PLLEN	I
27	PIO2.5 *5	I/O	67	RESET/ *7	I
28	PIO2.6 *5	I/O	68	GND	O
29	PIO2.7	I/O	69	GND	O
30	GND	O	70	AI7	I
31	VDD	I	71	AI6	I
32	PIO3.0	I/O	72	AI5	I
33	PIO3.1	I/O	73	N.C.	-
34	PIO3.2	I/O	74	N.C.	-
35	PIO3.3	I/O	75	N.C.	-
36	PIO3.4	I/O	76	N.C.	-
37	PIO3.5	I/O	77	GND	O
38	PIO3.6	I/O	78	GND	O
39	PIO3.7	I/O	79	GND	O
40	GND	O	80	GND	O

*5 These pins are used for their secondary functions, so are not available for use as port pins.

*6 The ENA position of theRS232C-SEL switch disconnects all these pins.

*7 This pin has a 10-kΩpull-up resistance.

The user connectors do not provide access to the following ML670100 pins: PIO8[7:0], AVDD, AGND, VCOM, OSC1, and TEST.

Access to the following ML670100 pins is via control circuits on the Oki ML670100 CPU Board: OSC0, FSEL, PLLEN, VREF, DBSEL, EA/, EFIQ/ and RESET/.

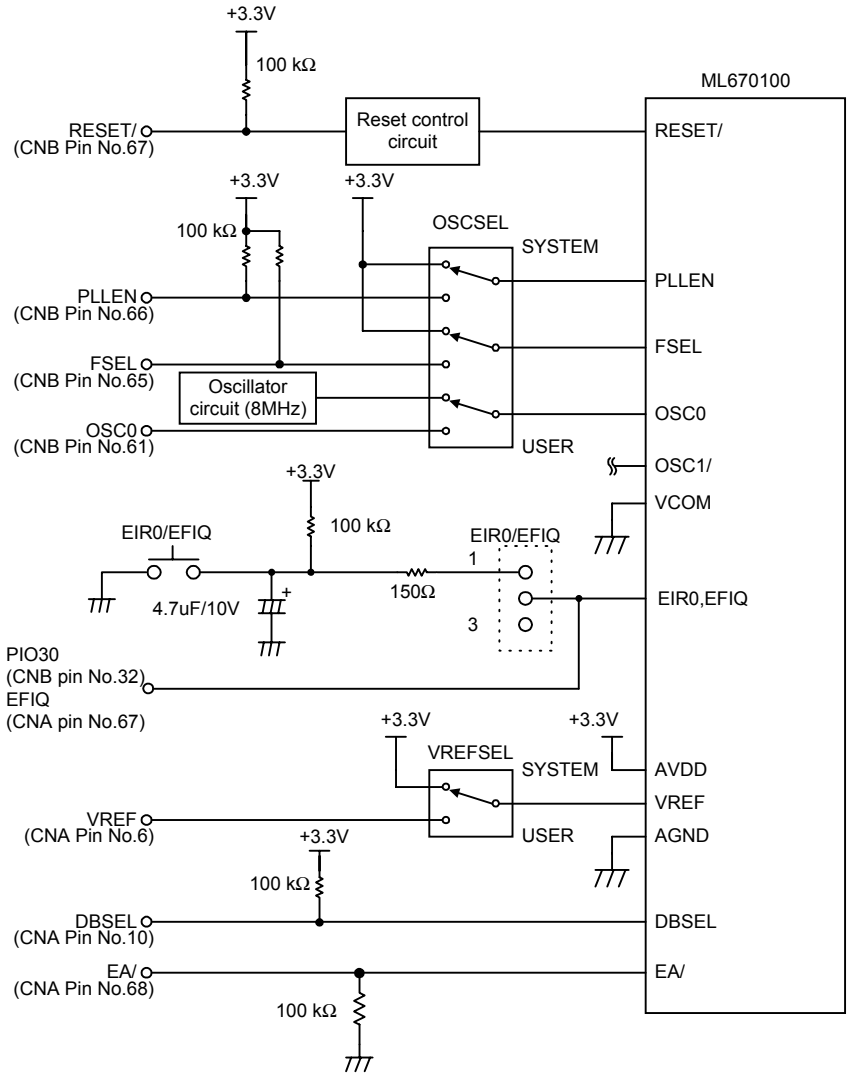


Figure 4.4 shows the connections for these two sets of pins.

Figure 4.4. User Interface Connector Peripheral Circuits

As Figure 4.4 shows, the Oki ML670100 CPU Board connects the AVDD pin to VDD (+3.3 V), connects AGND and VCOM to GND, and pulls RESET/, PLLEN, FSEL, and DBSEL, up to +3.3 V with 100-kΩ resistances, and . pull nEA down to GND with 100-kΩ resistances

If the EIR0-EFIQ jumper is connected to the IN side, the signals from the user application system remain connected to the corresponding user interface connector pins through a capacitance and a resistance.

4.3 User Cable

The user cable connects the user application system to the Oki ML670100 CPU Board and user connector Board (USRCN).

Figure 4.5 shows this cable.

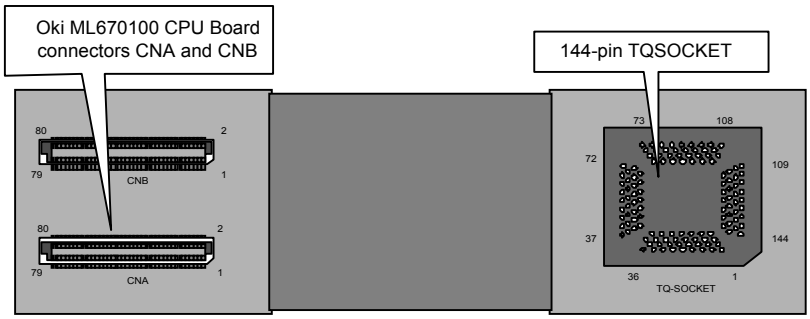


Figure 4.5. User Cable

4.4 User Application System Connector Layout

The Oki ML670100 CPU Board provides two ways to connect the I/O pins forming the ML670100 user interface to the user application system.

- Direct connection to the user interface connectors (CNU1 to CNU4)
- Indirect connection via the optional user connector Board (USRCN) and user cable.

Figure 4.6 shows the connector layout and dimensions for the former approach.

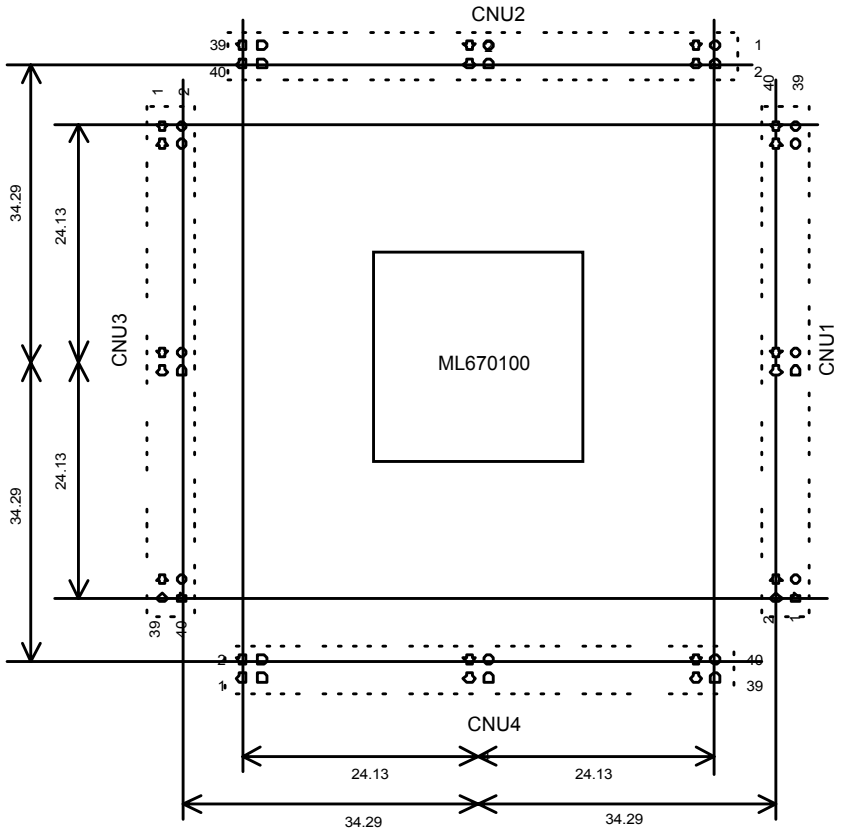


Figure 4.6. User Application System Connector Layout 1

The following are the specifications for this connector.

Manufacturer:	Hirose
Model:	HIF3F-40P-2.54DSA

The connector specifications for indirect connection depends on the ML670100 package. For further details, see Chapter 6 "Appendices."

Chapter 5 Notes on Debugging

This Chapter contains important notes on debugging application programs with the Oki ML670100 CPU Board.

5.1 Chip Differences

The chip at the core of the Oki ML670100 CPU Board differs from the target ML670100 in the following areas.

5.1.1 User Interface

The Oki ML670100 CPU Board treats certain I/O pins differently from the target ML670100.

Neither the Angel nor Normal mode supports the primary functions for the following I/O pins: all PIO0 pins, all PIO1 pins, PIO2.5, and PIO2.6.

The Angel mode supports neither the primary nor secondary functions for the following I/O pins: PIO5.6 and PIO5.7.

The Normal mode supports neither the primary nor secondary functions for all PIO8 pins except PIO8.2. It also pulls up PIO8.2 with a 100-kΩ resistance.

The Oki ML670100 CPU Board also provides additional circuitry for the following ML670100 pins: AVDD, AGND, VCOM, OSC1, TEST, OSC0, FSEL, PLLEN, VREF, DBSEL, EA/, EFIQ/ and RESET/.

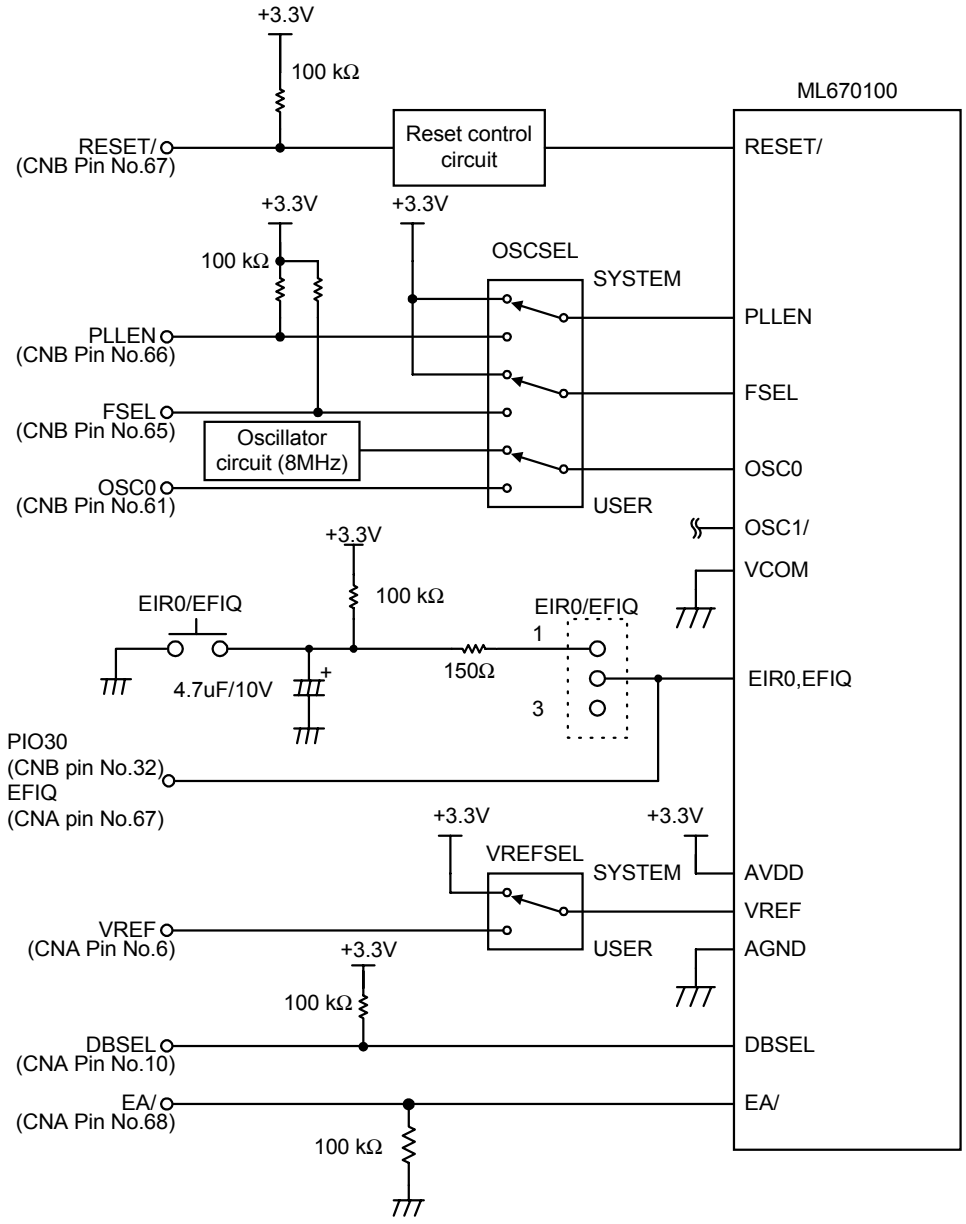


Figure 5.1. User Interface Connector Peripheral Circuits

The main purpose of this additional circuitry is to pull the I/O pins up to appropriate levels. Note, however, that the USER positions of configuration switches disconnect this protection, making it the responsibility of the user application system to ensure appropriate levels.

The RESET/ pin only supports input from the user application system during emulation.

Not shown in Figure 5.1 are the PIO8 port pins (PIO8[7:0]). These are not available for debugging with the Oki ML670100 CPU Board.

5.1.2 Memory Maps

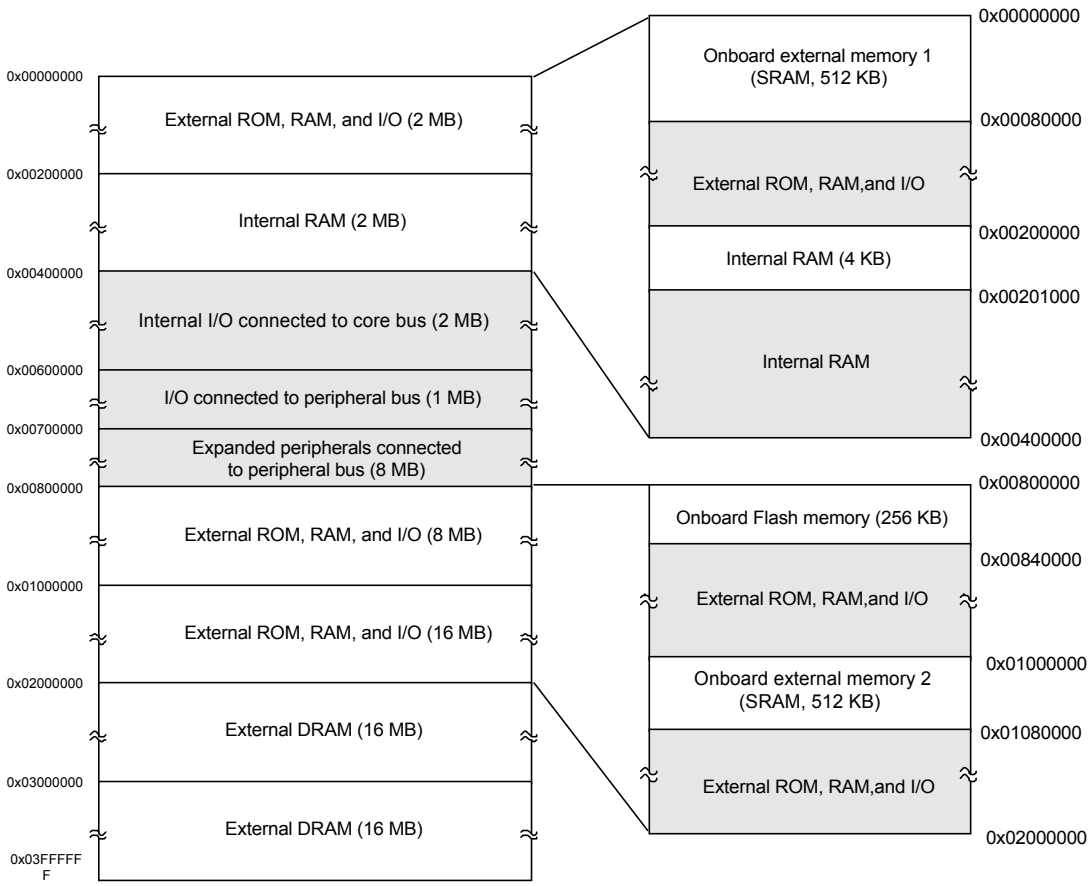


Figure 5.2. Oki ML670100 CPU Board Memory Map

Figure 5.2 shows how the two memory maps are equivalent. Because the 128-KB ML670100 on-chip ROM area (0x000000 to 0x01ffff) is unavailable, however, the Oki ML670100 CPU Board substitutes two 512-KB SRAM emulation areas (0x000000 to 0x07ffff and 0x1000000 to 0x107ffff). Note that the Angle mode reserves the top 96 KB in the second one for the Angel debugging monitor.

The Oki ML670100 CPU Board also adds 256 KB of Flash memory (0x800000 to 0x80ffff). Note that the Angle mode uses software stored in the first quarter (0x800000 to 0x80ffff), so protect this area.

Note that this use of SRAM in place of ROM allows runaway programs and errant pointers to overwrite the user application program being debugged.

5.2 Other Notes

This Section covers other things to keep in mind when debugging user application programs with the Oki ML670100 CPU Board.

5.2.1 System Reset Switch (RESET)

Do not press the system reset switch (RESET) on the Oki ML670100 CPU Board during normal operation as it also resets the JTAG communications interface unit (Oki Electric ADI Board or ARM Multi-ICE™) joining the Board to the host computer and can thus break the communications link to the ARM Software Development Toolkit running on the development host.

5.2.2 User Cable

Do not crimp the user cable. Flexing it with excessive force can damage not only the cable, but also the Oki ML670100 CPU Board itself.

5.2.3 External Clock

Do not change the OSCSEL switch to its external clock position unless the user application system can provide an external clock signal matching the following specifications.

Frequency: See table below.

Duty: 50%

Level: 3.3 V DC ± 5%

Oki ML670100 CPU Board External Clock Specifications		
FSEL pin input level	PLLEN pin input level	OSC0 pin input clock frequency
“H”	“H”	4 to 6 MHz
“L”	“H”	4 to 12 MHz
X	“L”	4 to 24 MHz

X: Don’t Care

Failure to match these specifications can lead to unpredictable CPU behavior and even damage the Oki ML670100 CPU Board.

5.3 Angel resources requirements introduce a number of restrictions on application development under Angel.

Programmers developing application programs using the Angel debugging monitor should keep the following in mind.

1. Specify the default (0x8000) as the loader address using the following linker syntax.

   armlink -R0 0x8000

   Do not specify the address 0x0 because the Angel debugging monitor requires addresses 0x0 to 0x3c to load the application program.

2. Do not modify the contents of the following registers with the Angel debugging monitor.

Address	Register Name
0x400004	CKCON
0x600008	IRR0[3],IRR0[4],IRR0[5]
0x600012	ILCON2
0x600300	ASBUF
0x600301	ASIST
0x600302	ASICON
0x600303	ASBCON
0x600304	ASBTMC
0x600305	ASBTMR
0x600306	ASTSCON
0x600635	PFS5[6],PFS5[7]
0x600703	PWCON

   For further details on these registers, refer to the ML670100 User's Manual.

3. Chain IRQ handlers.

   If the application program uses IRQ interrupts, modify it to chain its IRQ handler to the Angel debugging monitor counterpart with a procedure similar to the following.

   Define a function Install_Handler() with two arguments: location, an address for storing the entry address for the Angel debugging monitor's handler, and address, the address for the

application program's handler.

```
unsigned Install_Handler (unsigned *location, unsigned address)
{

    unsigned vec, oldvec;

    oldvec = *location;
    *location = address;

    return (oldvec);

}
```

The return value provides the IRQ handler entry address before calling this function.

Near the beginning of the main() function, place the following code for installing the application program's IRQ handler.

```
    unsigned *irqadder = (unsigned *) 0x38;
    angelHandlerEntry = Install_Handler(irqadder, (unsigned)IRQ_Handler);
```

IRQ_handler is the entry address for the application program's IRQ handler.

This chain allows the application program's IRQ handler to pass all exceptions that it does not know how to handle to the Angel debugging monitor's IRQ handler with the following procedure.

(1) Save registers.
(2) Call the application program's IRQ handler.
(3) Restore registers.
(4) If the application program does not know how to handle the interrupt, branch to the Angel debugging monitor's IRQ handler.
(5) Otherwise, return from the application program's IRQ handler.

Do not, however, use __irq inside the IRQ handler.
See also 5. below for a description of the Angel debugging monitor exception vector table.

4. Note the following with regard to SWI instructions.

* Do not use SWI 0x123456 or SWI 0xab. The Angel debugging monitor uses these SWIs to support C library semihosting requests.
* The application must restore registers to their states before the SWI instruction.
* If the application program uses SWI instructions, modify it to chain its SWI handler to the Angel debugging monitor's SWI handler. The procedure is the same as that under 3. above.

See also 5. below for a description of the Angel debugging monitor exception vector table.

5. The Angel debugging monitor uses the following exception vector table.

Address	Description
0x0	ldr pc, 0x20 ; RESET
0x4	ldr pc, 0x24 ; Undefined opcode
0x8	ldr pc, 0x28 ; SWI
0xc	ldr pc, 0x2c ; Prefetch abort
0x10	ldr pc, 0x30 ; Data abort
0x14	ldr pc, 0x34 ; Reserved
0x18	ldr pc. 0x38 ; IRQ
0x1c	ldr pc, 0x3c ; FIQ
0x20	Reset handler (32-bit) address
0x24	Undefined opcode handler (32-bit) address
0x28	SWI handler (32-bit) address
0x2C	Prefetch abort handler (32-bit) address
0x30	Data abort handler (32-bit) address
0x34	Reserved
0x38	IRQ handler (32-bit) address
0x3c	FIQ handler (32-bit) address

Using this table

Consider the entry for 0x18, for example.
This instruction loads the program counter with the 32-bit address stored at the address 0x38, producing a branch to that handler.

■ Note ■

For further details on chaining exception handlers in 3. and 4. above, refer to the SDT250 User's Manual Section 9.3.2 descriptions for C handlers (p. 9-11) and exception handlers (pp. 9-39 and 9-19).

6. When connecting the ML670100 CPU board to a user application system, we recommend the use of fast interrupts (FIQs) because the Angel debugging monitor does not use them.

Chapter 6 Appendices

6.1 ML670100 Pin Assignments

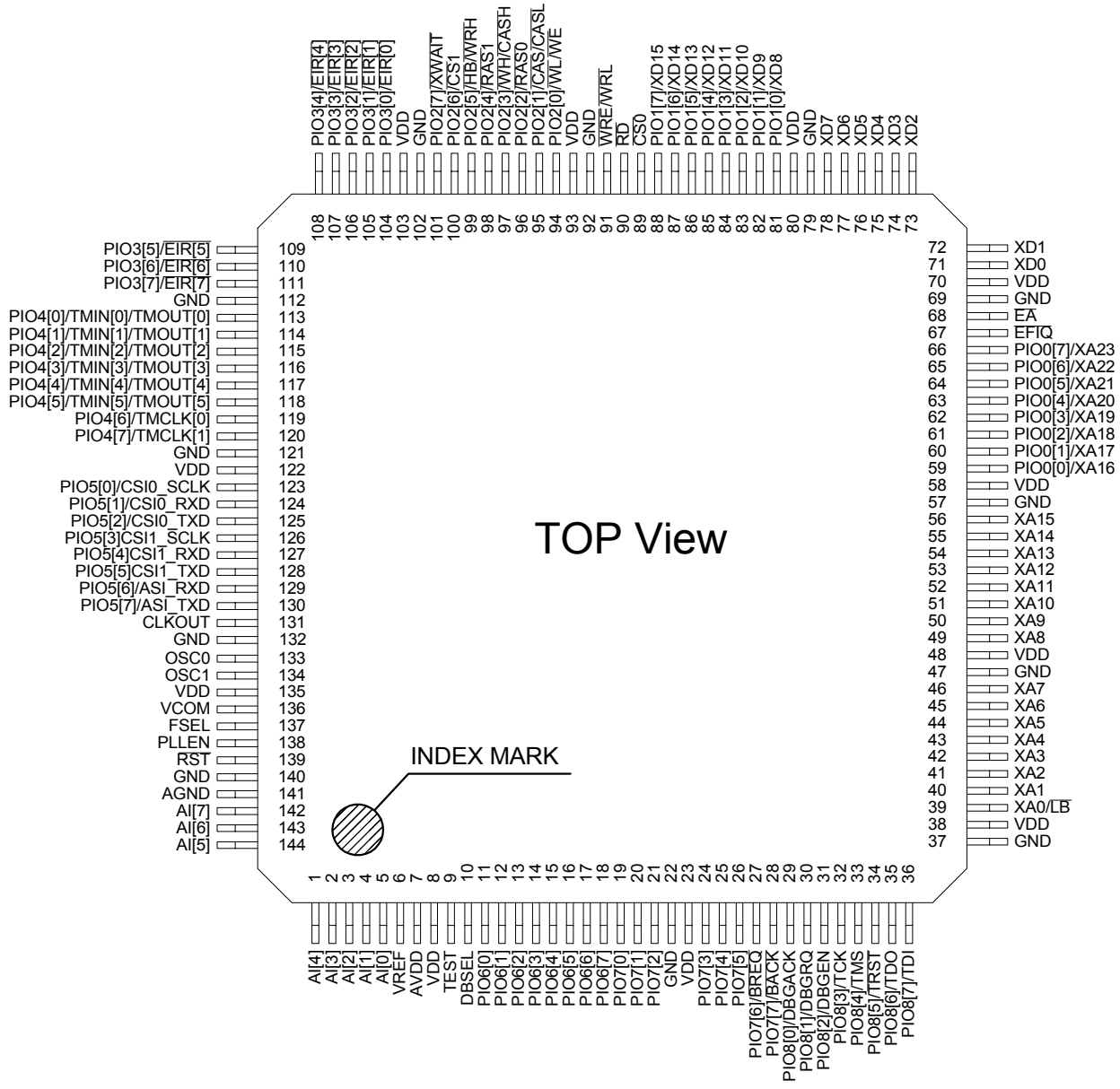


Figure 6.1. ML670100 Pin Assignments

6.2 ML670100 Package Layout

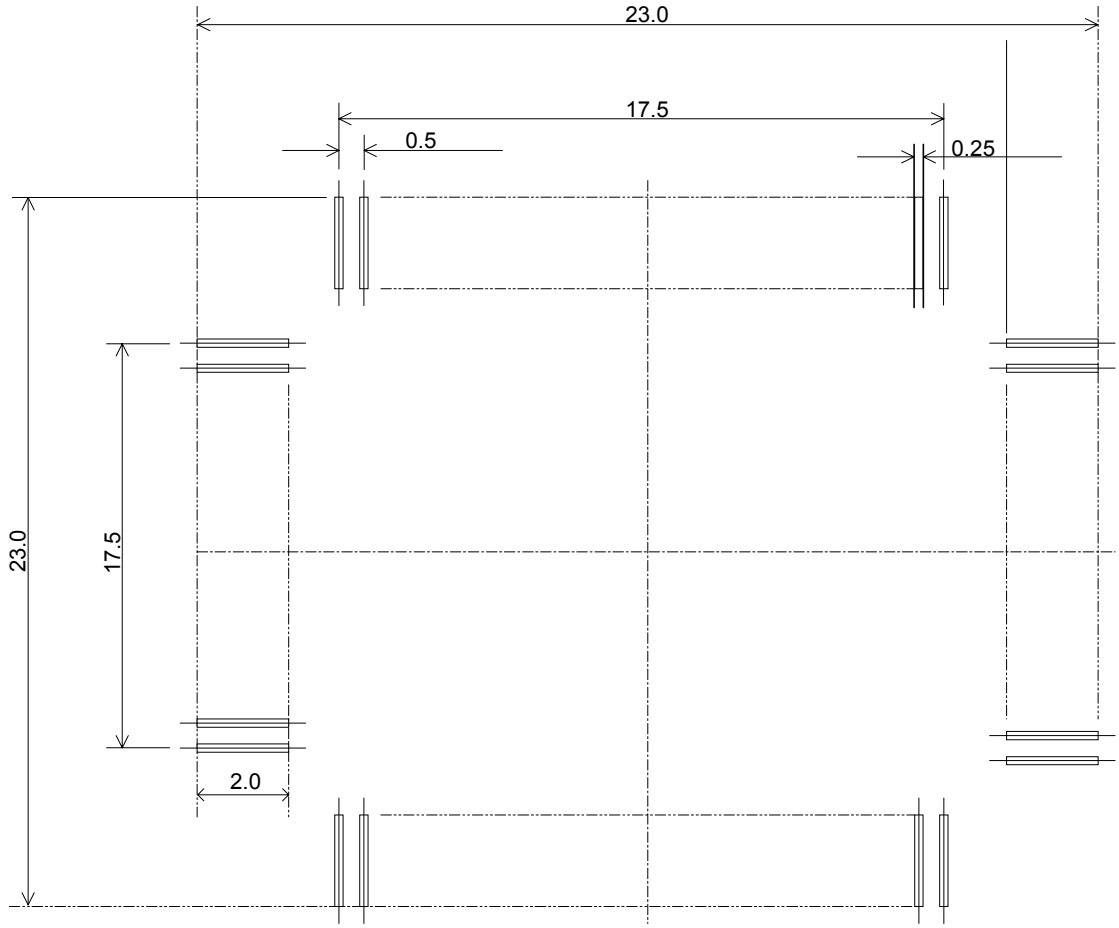


Figure 6.2. ML670100 Package Layout