OKI Semiconductor

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ML7033 Application Note

Dual-Channel Line Card CODEC

GENERAL DESCRIPTION

This application note is intended to help the user understand the broad functionality of the OKI ML7033 2-channel PCM CODEC. Of particular emphasis in this document is the interface between the ML7033 and the SLIC RSLIC™-series device from Intersil Corporation.

1. Architectural Overview

Figure 1 shows a functional block diagram for Channel-n of the ML7033. The ML7033 integrates Channel 1 and Channel 2, and the diagrams for both of the channels are identical. The ML7033 supports the ITU-T G.711 specification μ-law/A-law PCM companding laws and 14-bit linear PCM, and is compatible with the ITU-T G.714 specification in its transmission characteristics.

In addition to the PCM CODEC functionality, the ML7033 provides various tone generation and gain control options. All of the functions are programmable with built-in control registers accessed through the serial interface. Figure 1 shows a block diagram of Channel-n. Generally, a 'n' in a small letter in the pin name indicates the connection for Channel-n. For example, AINnN would be the negative analog input for Channel-n. Table 1 shows a list of the control registers corresponding to the switches and gain controllers shown in Figure 1. For more details, please refer to the ML7033 Data Sheet.

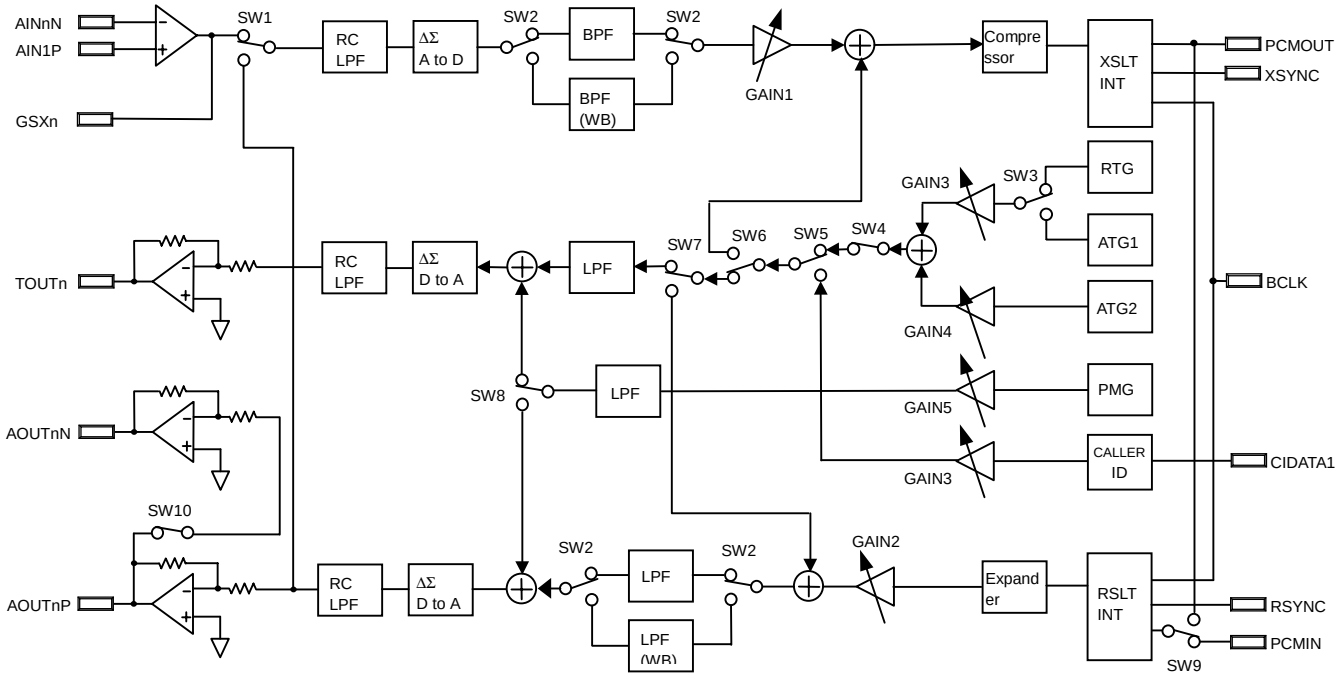


Figure 1. ML7033 Functional Block Diagram

Symbol	Function	Ch-1Control Register	Ch-2 Control Register	Remarks
SW1	Analog loop-back test mode switch	CR18-B5, B4	CR18-B7, B6	(0, 0) (0, 1) : Loop-back OFF (1, 1) : Analog loop-back test mode
SW2	Voice band filter select switch	CR0-B7	CR0-B6	'0' : G.714 filter '1' : V.90 modem performance filter
SW3	Tone (Ring/ATG1) select switch	CR11-B3	CR11-B7	'0' : Normal Tone '1' : Ringing Tone
SW4	Tone generator ON/OFF switch	CR1-B6	CR1-B7	'0' : Tone generator OFF '1' : Tone ON The frequency and the level must be set in advance.
SW5	Caller ID/Tone select switch	CR1-B0	CR1-B1	'0' : Tone '1' : Caller ID In Caller ID mode, mark-tone and space-tone are generated dependent upon CIDATA.
SW6	Tx/Rx select switch for tone generation	CR7-B6	CR14-B6	'0' : Rx-side (D/A) '1' : Tx-side (A/D)
SW7	TOUT/AOUT select switch for tone generator output pin	CR7-B5	CR14-B5	'0' : AOUT '1' : TOUT
SW8	TOUT/AOUT select switch for PMG output pin	CR2-B0	CR2-B4	'0' : AOUT '1' : TOUT
SW9	Digital loop-back test mode switch	CR18-B5, B4	CR18-B7, B6	(0, 0) (0, 1) : Loop-back OFF (1, 0) : Digital loop-back mode
SW10	AOUTN on/OFF switch	CR7-B7	CR14-B7	'0' : AOUTN OFF (single-ended output) '1' : AOUTN ON (differential output)
GAIN1	Tx (A/D) GAIN setting	CR5-B3~B0	CR12-B3~B0	0dB to -14 dB (1 dB intervals) and OFF
GAIN2	Rx (D/A) GAIN setting	CR5-B7~B4	CR12-B7~B4	0dB to -14 dB (1 dB intervals) and OFF
GAIN3	Tone1 GAIN setting	CR9-B7~B1	CR16-B7~B1	+0.5dB~-12.1dB (0.1dB intervals) and OFF
GAIN4	Tone2 GAIN setting	CR7-B4~B1	CR14-B4~B1	+2.0~-12.0dB (1dB intervals) and OFF
GAIN5	Pulse Metering Tone GAIN setting	CR2-B2, B1	CR2-B6, B5	OFF / 0.5Vpp / 1.0Vpp / 1.5Vpp select

Table 1. Correspondence Between ML7033 Switch/Gain Controller and Control Registers Register

The ML7033 contains two channels that work independently of one another. However, the following functions are common between the channels:

- Settings for the PCM and Caller ID formats are common to both channels. Different formats cannot be selected for each channel.
- Both channels share a common PCMIN pin as the time-division multiplexed PCM data input pin.
- Both channels share a common PCMOUT pin as the time-division multiplexed PCM data output pin.

Refer to the section on Time Slot Assignments for more information on the time-division multiplexed PCM data interface.

The ML7033 is a general purpose 2-channel PCM CODEC. However, when designing line cards, using the ML7033 in conjunction with the Intersil SLIC RSLIC™-series device is recommended for ease of design and system configuration. The following sections in this documentation mainly explain the use of ML7033 in a combination with HC55185 that is among the Intersil SLIC RSLIC™-series devices.

2. Interfaces between ML7033 and HC55185 (Voice Transmission)

Figure 2 illustrates an example of interfacing the ML7033 and the HC55185 to establish a voice signal path.

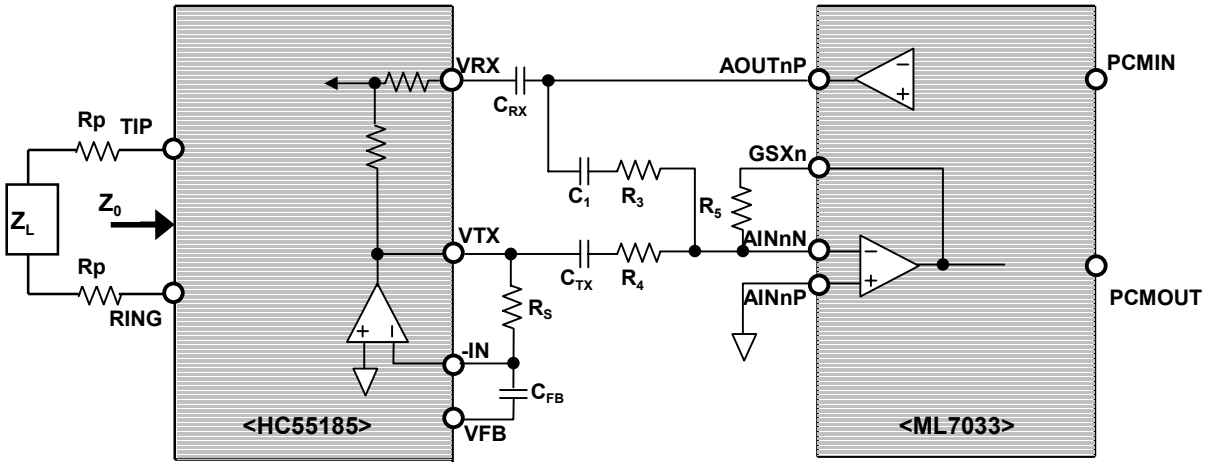


Figure 2. Interfaces between ML7033 and HC55185 (Voice signals)

2-(a) Impedance Matching

Impedance can be matched when the following formula is satisfied: $Z_L = 2R_P + Z_0$

Where :

Z_L impedance of the line side

Z_0 input impedance of the HC55185

R_P protective resistance connected to the TIP pin and RING pin to protect the ML7033 from excess current

The resistance value for the RP should typically be greater than 49 Ω. However, the value for the RP should be chosen to match the 2-wire analog line is determined by the external resistance of the HC55185, or R_S, as shown in the following formula:

$$R_S=133.3\ (Z_L-2R_P) \quad \ldots(2\text{-}1)$$

For more details, please refer to the HC55185 Data Sheet.

2-(b) GAIN from 4W to 2W

The voice signals from the AOUTnP pin of the ML7033 are input to the VRX pin of the HC55185 after the DC component of the signal is filtered by the C_{RX} capacitor shown in Figure 2. The conversion gain from 4 W to 2 W in the HC55185, or G_{42}, is expressed by the formula below:

$$G_{42} = - 2Z_L /(Z_0+2R_P+Z_L) \qquad \ldots(2\text{-}2)$$

Assuming the impedance is matched, the formula, $Z_L = 2R_P + Z_0$, is satisfied.
Herein,

$$G_{42} = -1$$

This shows that the output level of the AOUT1P pin is observed at the 2-W line (0 dB transmission). In the ML7033, the output level of the voice signal from the AOUTnP pin for Channel-n is controlled by the CR5 and the CR12 Control registers.
When the CR5 or the CR12 register is set to 0 dB and the PCM values are the maximum (= +3.00 dBm0), 1.7 Vop is output from the AOUTnP pin.

2-(c) GAIN from 2W to 4W

The voice signals from 2 W to 4 W are output from the VTX pin of the HC55185. The conversion gain from 2 W to 4 W in the HC55185 is expressed by the formula below:

$$G_{24} = -Z_0 / (Z_0 + 2R_P + Z_L) \quad \ldots (2\text{-}3)$$

When R_P and Z_L are :

$R_P = 50\ \Omega$

$Z_L = 600\ \Omega$

$$G_{24} = 0.416\ (-7.6\text{dB})$$

When R_P and Z_L are :

$R_P = 0\ \Omega$

$Z_L = 600\ \Omega$

$$G_{24} = 0.5\ (-6\text{dB})$$

The analog full swing at the GSXn pin of the ML7033 (1.113 Vop @ 1 kHz) corresponds to the maximum PCM value (+3.00 dBm0). In this case, the R4 and R5 resistors in Figure 2 should be tuned to take advantage of the full-swing characteristics of the ML7033.

The signal level at the GSXn pin of the ML7033 (V_{GSX}) corresponds to the signal level at the VTX pin (V_{TX}) of the HC55185. This level is determined by the following formula using the R_4 and R_5 resistors.

$$V_{GSX1} = -(R_5 / R_4) * V_{TX} \quad \ldots (2\text{-}3a)$$

The R_4 and R_5 resistors value should be set so that V_{GSX} does not exceed 1.113 Vop.

2-(d) GAIN from 4W to 4W (Trans Hybrid Gain)

The voice signal output from the AOUTnP pin of the ML7033 is transmitted to not only the 2 W side, but is also returned back to the VTX pin of the HC55185 on the 4W side as echo. The gain from 4 W to 4 W is called the Trans Hybrid Gain and is expressed as G_{44} as shown below:

$$G_{44} = -Z_0 / (Z_0 + 2R_P + Z_L) \quad \ldots (2\text{-}4)$$

When R_P and Z_L are :

$R_P = 50\ \Omega$

$Z_L = 600\ \Omega$

$$G_{44} = -0.416\ (-7.6\text{dB})$$

When R_P and Z_L are :

$R_P = 0\ \Omega$

$Z_L = 600\ \Omega$

$$G_{24} = -0.5\ (-6\text{dB})$$

The echo signal is not needed and must be cancelled. Taking it into consideration that the voice signal from the AOUTnP pin is output from the VTX pin with a gain of G_{44} and that the phase at the AOUTnP and VTX pins is 180°, it is known that the echo back to the GSXn pin can be cancelled by setting the resistor R_3 in Figure 2 as follows:

$$R3 = -R4 / G_{44} \quad \ldots (2\text{-}5)$$

This is called as Trans Hybrid Balance Circuit.

2-(e) Example of C & R

An example of C and R is shown below:

Where Z_L = 600 Ω

R_P = 50 Ω

R_S = 66.5 kΩ

R_3 = 141.3 kΩ

R_4 = 58.8 kΩ

R_5 = 100 kΩ

$C_{RX} = C_{TX} = C_1 = C_{FB}$ = 0.47 µF

In the configuration, 0 dBm0 alanog signal input on the 2 W side is output as µ-law codes corresponding to 0 dBm0 on the 4 W side, and 0 dBm0 µ-law PCM codes input on the 4 W side is output as 0.658 dBm analog signals on the 2 W side.

3. Interfaces between ML7033 and HC55185 (Ringing Signal)

The ML7033 includes a generator for various tones, including ringing and DTMF tones. Figure 3 shows an example of how to interface the ML7033 to the HC55185 for ringing signals.

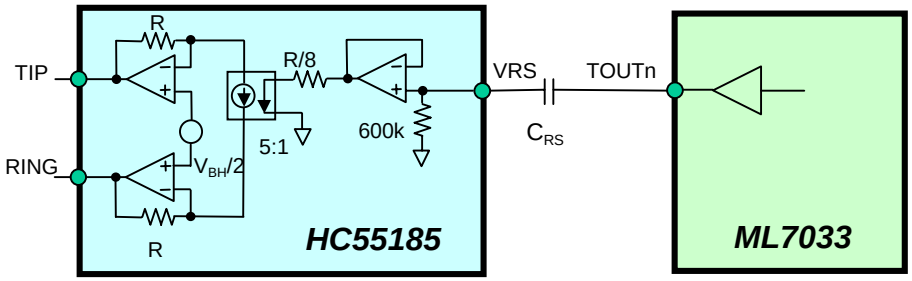


Figure 3. Ringing Signal Interface Circuit

In the ML7033, ringing tones are output by the TOUTn pin for Channel-n. Depending on the control register settings, the ringing tones can also be output to the AOUTnP pin. After the DC component is filtered by C_{RS} in Figure 3, the TOUTn pin is input to the VRS pin of the HC55185. Although the frequency of the ringing signal is low (in some cases in the Hz range), this is acceptable as long as the termination resistance of the HC55185 is ≥ 450 Ω, and C_{RS} ≥ 0.47 µF. The HC55185 outputs the ringing signals input from the VRS pin to the TIP/RING-pin using a 40x gain in a single output mode, and an 80x gain in a differential output mode.

Tone generation is implemented in the RTG block of the ML7033 as shown in Figure 1. Depending on the register settings, the generated tone signals can be sinusoidal or trapezoidal. When a trapezoidal tone is selected, the crest factor can be set. In addition, the frequency could be set arbitrarily from 15 Hz to 50 Hz in 1 Hz increments. The crest factor is defined by the formula in Figure 4.

Figure 4 shows the correspondence between each parameter and the generated tone waveforms in the case of a trapezoidal tone. In the ML7033, the crest factor for a trapezoidal waveform ranges from 1.225 to 1.375 in 0.025 increments. The smaller the crest, the more the generated tone waveform becomes trapezoidal. The greater the crest factor gets, the more the generated tone waveform becomes triangular.

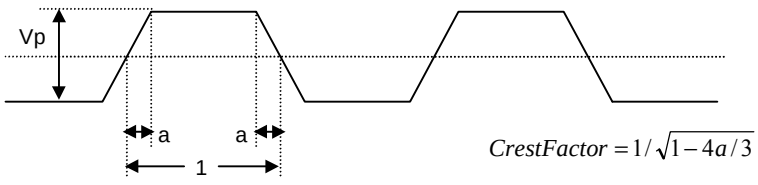


Figure 4. Ringing Tone Waveform

The output level from the ML7033 (Vp) is 2.5 Vpp (max.). The level is adjustable by 127 steps by 0.1 dB/step.

4. Interfaces between ML7033 and HC55185 (SLIC Mode Setting and Indicator Detect)

In this configuration the ML7033 sets the operational mode of the HC55185 and reads the indicator outputs from the HC55185 through its serial MCU. The Figure 5 shows this interface circuit.

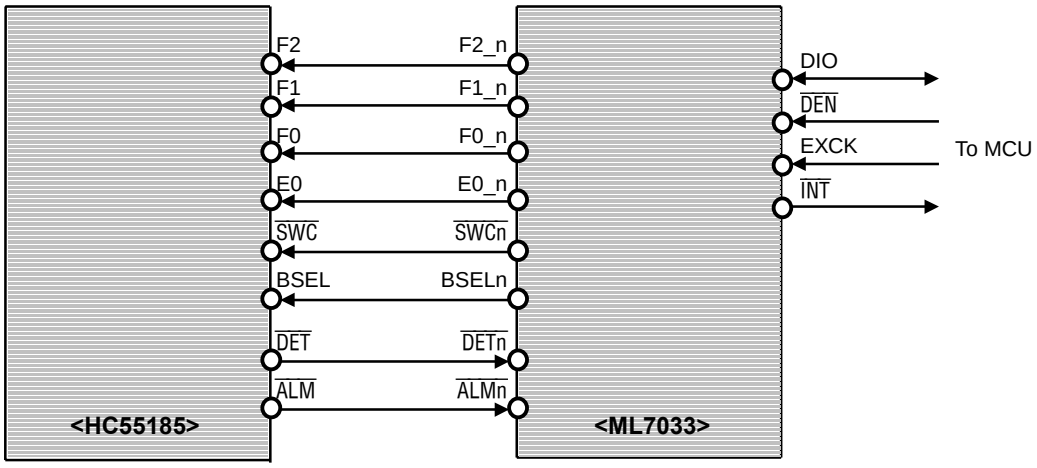


Figure 5. Interface Circuit between ML7033 and HC55185 (SLIC Mode Setting / Indicator Read)

The signals in Figure 5 perform the following functions:

- The F2, F1, F0, and E0 signals are used to select the HC55185's operating mode and to select what event the HC55185 to detect among SHD, RTD and GKD.
- The $\overline{SWC}$ signal controls the On/Off states with the HC55185's uncommitted switches.
- The BSEL signal selects the HC55185 battery operating mode: Low-Battery Mode or High-Battery Mode. For more details, please refer to the HC55185 Data Sheet.
- The $\overline{DET}$ signal is asserted by the HC55185 (driven to a logic '0') when it detects any of the following conditions dependent upon the combination of the F2, F1, F0 and E0 signals:
  - A change of hook state (Switch Hook Detection)
  - Ring trip (Ring Trip Detection)
  - Ground key (Ground Key Detection)
- The $\overline{ALM}$ thermal shutdown alram signal is asserted by the HC55185 when the device temperature exceeds 175ºC typical and automatically goes into the power-down mode.

The ML7033 alerts the change of state to the MCU by deasserting the $\overline{INT}$ pin (high to low) when either the $\overline{DET}$ pin or the $\overline{ALM}$ pin transitions from a logic '1' to a logic '0'. The MCU then reads the ML7033 CR6 and CR13 Control registers, and drives the $\overline{INT}$ pin high when both of the CR6 and the CR13 registers are read.

Even when the HC55185 does not detect an Off-hook condition, or spurious assertions of $\overline{DET}$ could occur. To prevent unnecessary interrupts from occuring due to the glitches on $\overline{DET}$, the ML7033 contains a debounce-timer that can be set beetween 0 and 225 ms in 15 ms increments. For example, if this value is set to 100 ms, the logic '0' $\overline{INT}$ signal is not generated by the ML7033 unless the assetion of $\overline{DET}$ signals continues for 100 ms. The length of the holding time with the debounce timer can be set independently for each channel.

5. Example for Various Tone Generations

In addition to ringing tones explained in Section 3, the ML7033 provides for the generation of the following additional tones.

- DTMF Tones
- Pulse Metering Tones
- Caller ID Signals

5-(a) DTMF Tone

The ATG1 and ATG2 blocks in Figure 1 generate the Dual Tone Multiple Frequency (DTMF) tones. The ML7033 supports DTMF tone frequencies from 300 Hz to 3400 Hz in 10-Hz increments. Table 2 shows the DTMF tone frequencies and their corresponding register settings.

Digit	Target Frequency [Hz]	Set Frequency [Hz]	CH1	CR7	CR8								CR9	CR10						
			CH2	CR14	CR15								CR16	CR17						
				B0	B7	B6	B5	B4	B3	B2	B1	B0	B0	B7	B6	B5	B4	B3	B2	B1	B0
1	697+1209	700+1210		0	0	1	0	0	0	1	1	0	0	0	1	1	1	1	0	0	1
2	697+1336	700+1340		0	0	1	0	0	0	1	1	0	0	1	0	0	0	0	1	1	0
3	697+1477	700+1480		0	0	1	0	0	0	1	1	0	0	1	0	0	1	0	1	0	0
4	770+1209	770+1210		0	0	1	0	0	1	1	0	1	0	0	1	1	1	1	0	0	1
5	770+1336	770+1340		0	0	1	0	0	1	1	0	1	0	1	0	0	0	0	1	1	0
6	770+1477	770+1480		0	0	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	0
7	852+1209	850+1210		0	0	1	0	1	0	1	0	1	0	0	1	1	1	1	0	0	1
8	852+1336	850+1340		0	0	1	0	1	0	1	0	1	0	1	0	0	0	0	1	1	0
9	852+1477	850+1480		0	0	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	0
0	941+1209	940+1210		0	0	1	0	1	1	1	1	0	0	0	1	1	1	1	0	0	1
*	941+1336	940+1340		0	0	1	0	1	1	1	1	0	0	1	0	0	0	0	1	1	0
#	941+1477	940+1480		0	0	1	0	1	1	1	1	0	0	1	0	0	1	0	1	0	0
A	697+1633	700+1630		0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	1
B	770+1633	770+1630		0	0	1	0	0	1	1	0	1	0	1	0	1	0	0	0	1	1
C	852+1633	850+1630		0	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1	1
D	941+1633	940+1630		0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1

Table 2 DTMF Frequency Setting

DTMF tone generation requires the use of both the ATG1 and ATG2 blocks. The GAIN3 block in Figure 1 is used to adjust ATG1 via the CHnTG2LV3 to the CHnTG2LV0 (CR7-B4 to B1/ CR14-B4 to B1) bits. The frequency of ATG1 is set using the CHnTG2_8 to the CHnTG2_0 (CR7-B0, CR8-B7 to B0/ CR14-B0, CR15-B7 to B0) bits.

The GAIN4 block in Figure 1 is used to adjust ATG2 via the CHnTG1LV6 to the CHnTG1LV0 (CR9-B7 to B1/ CR16-B7 to B1) bits. The frequency of ATG2 is set using the CHnTG1_8 to the CHnTG1_0 (CR9-B0, CR10-B7 to B0/ CR16-B0, CR17-B7 to B0) bits.

Once these values are set, switch SW4 in Figure 1 is used to enable and disable tone generation.

For ATG1 and ATG2, the generated DTMF tone frequency is accurate from –3 to +4 Hz in 10 Hz increments and is shown as the difference between Target Frequency and Set Frequency in Table 2 above. The DTMF frequency can be set at 700 Hz, 710 Hz, 720 Hz, etc. through 1630 Hz. For example, if the frequency is set to 720 Hz, the actual frequency is between 717 Hz and 724 Hz.

5-(b) Pulse Metering Tone

Many European countries use a 12 kHz or 16 kHz sinusoidal tone for billing counts such as to time phone calls. The Pulse Metering Tone is used for this purpose. The tone is injected into the voice signal and transmitted to the network. The ML7033 generates the pulse metering tone in the PMG block in Figure 1. There are two options for generating the pulse tone.

- The pulse metering tone is added to the voice signal and output to the AOUTnP pin. When the pulse metering tone is designated to be output to the AOUTnP pin, the tone level should not exceed 1.7 Vop, which is the maximum output of the AOUTnP pin.
- The pulse metering tone is transmitted independently of the voice signal using the TOUTn pin without adding to the voice signals.

The output pulse metering tone waveform is shown below in Figure 6.

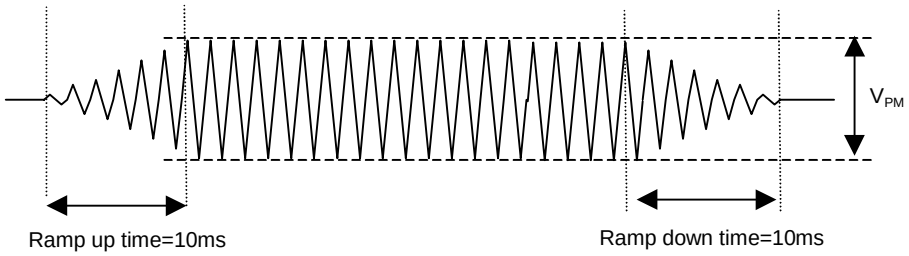


Figure 6. Pulse Metering Tone Waveform

Pulse Metering Tone generation is enabled by writing the appropriate data to the PMGnLV1 to the PMGnLV0 (CR2-B6 to B5/CR2-B2 to B1) bits. The signal level, V_{PM}, can be 0.5Vpp, 1.0 Vpp, or 1.5 Vpp. The PMGnFRQ (CR2-B3/CR2-B7) bit is used to select the frequency of the pulse metering tone. This bit is cleared (logic '0') for 12 kHz and set (logic '1') for 16 kHz. As shown in Figure 6, 10 ms are required for the ramp-up time, and an additional 10 ms for the ramp-down time.

5-(c) Caller ID Signals

For Channel-n, Caller ID generation is enabled using the CIDCHnON (CR1-B0/CR1-B1) bit. When logic '1' is set in the bit, Caller ID is enabled. The serial input from the CIDATAn pin is FSK-modulated in the Caller ID block in Figure 1 and output to the AOUTnP pin.

The set of frequencies to modulate the mark (logic '1') and the space (logic '0') input into the CIDATAn pin is determined by whether the ITU-T V.23 mode (CR1-B2 = 0), or the Bell 202 mode (CR1-B2 = 1) is selected as shown in Table 3 below.

CIDATAn	ITU-T V.23 mode (CR1-B2=0)	Bell 202 mode (CR1-B2=1)
1 (Mark)	1300Hz	1200Hz
0 (Space)	2100Hz	2200Hz

Table 3 FSK Modulation Frequency Set

6. Other Functions

Hereunder, other functions provided with the ML7033 are introduced.

6-(a) PCM Formats

The ML703 supports not only μ-law and A-law PCM formats recommended by the ITU-T G.711 specification, but also 14-bit linear PCM (2's compliment). The required register setting for the selection is shown below:

CR0-(B3,B2) = (0,0) 8-bit μ-law
= (0,1) 8-bit A-law
= (1,0), (1,1) 14-bit linear

6-(b) Time Slot Assignment

Depending on the data written to the CR3 (Time slot assignment) Control register, the PCM data for Channel-n can be assigned to an arbitrary time slot. The default time slot assignment is Channel 1 for Slot 0 and Channel 2 for Slot 2 regardless of a selected PCM data formats (8-bit μ-law, 8-bit A-law, 14-bit linear PCM).
An example when either of 8-bit PCM modes is selected is shown in Figure 7.

1CH : Slot0
2CH : Slot2

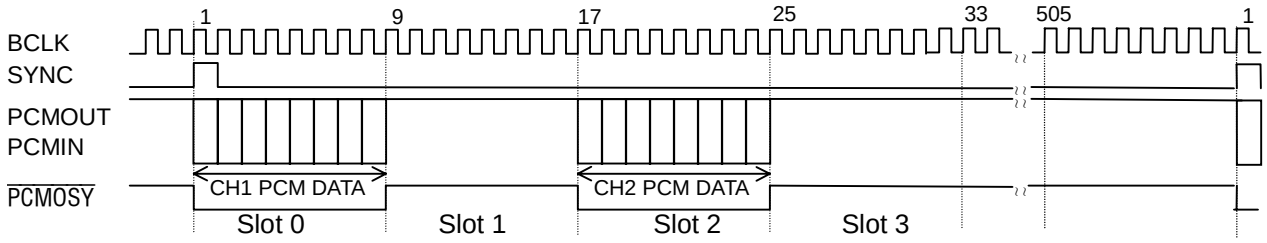


Figure 7. Time Slot Assignment (8-bit PCM)

Each time slot is consists of 8 BCLK cycles. The number of slots available is dependent upon the frequency of the BCLK as examples shown below:

BCLK = 4.096 MHz : 64 slots
BCLK = 256 kHz : 4 slots

As an example, the data written to the CR3 Control register when PCM data on Channel 1 is assigned to Slot 31 and PCM data on Channel 2 are assigned to Slot 63 is shown below:

	B7	B6	B5	B4	B3	B2	B1	B0
	On/Off	Channel Select	Time slot assignment position select					
CR3	1	0	0	1	1	1	1	1
CR3	1	1	1	1	1	1	1	1

CR3-B7 : Time slot assignment customization enable
0 : Default time slot assignment 1 : Customized time slot assignment

CR3-B6 : Time slot assignment channel select
0 : Channel 1 1 : Channel 2

CR3-B5 to B0 : Assigned time slot select

Note: The same register (CR3-B7 to B0) is used for both for Channel 1 and Channel 2. This means that data must be written to register CR3 twice, once for the Channel 1 time slot assignment and the second for the Channel 2 time slot assignment.

Figure 8 illustrates the case when 14-bit linear PCM data format is selected.

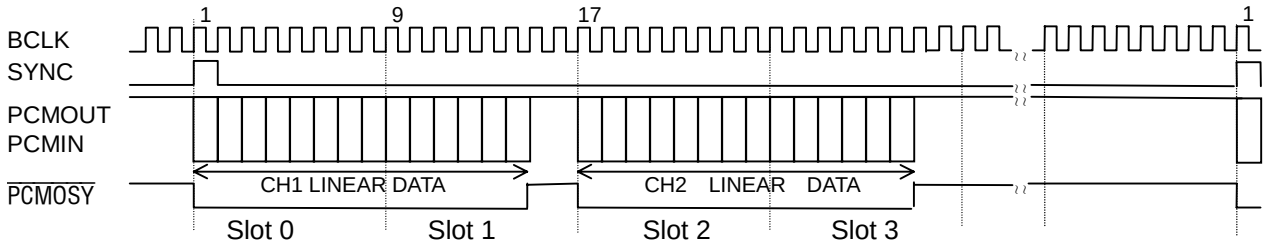


Figure 8. Time Slot Assignment (14-bit Linear PCM)

Because linear PCM data is 14 bits wide, two time slots must be allocated for one channel. It is noted that only an even number of a time slot (0, 2, 4,…, 62) can be assigned to avoid losing PCM data. If the Channel 1 and Channel 2 time slots are adjacent to one another, a portion of the PCM data will be lost.

Note : The CR3 control register is used both for the input (PCMIN) and the output (PCMOUT) of a channel. Therefore, different time slots cannot be assigned for PCMIN and PCMOUT for a given channel.

6-(c) V.90 Filter Mode

The ML7033 includes not only a conventional ITU-T G.714 band-pass filter for 300 to 3400 Hz, but also a wider band-pass filter for 300 to 3700 Hz used for V.90 data communications that require a wider bandwidth. The selection between the two filters is made using switch SW2 in Figure 1. The frequency characteristics of the ITU-T G.714 band-pass filter are shown in Figure 9. The wide-band filter is shown in Figure 10.

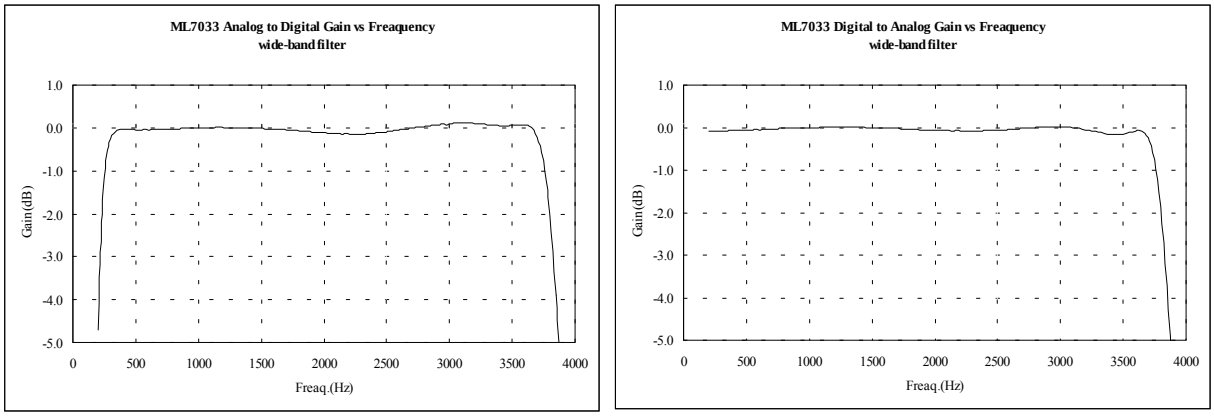
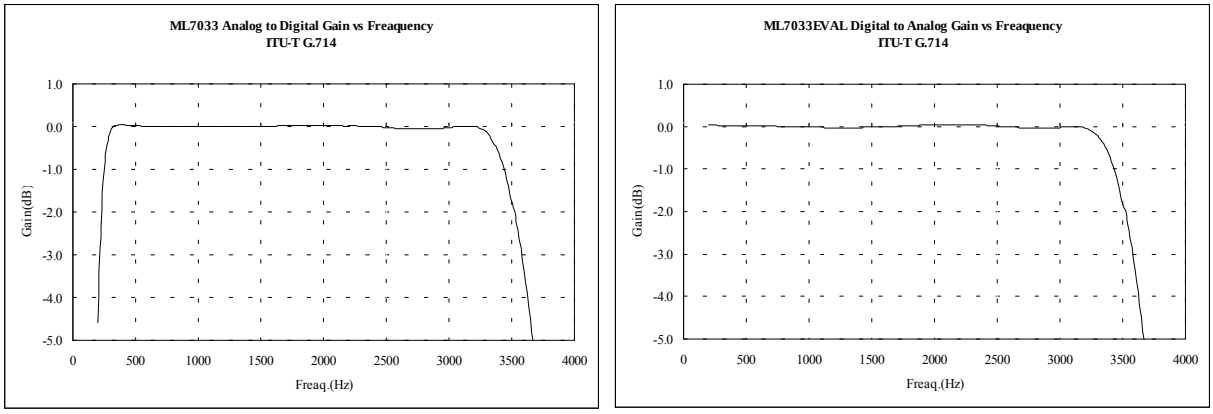


Figure 9. ITU-T G.714 Filter Frequency Characteristics



A/D D/A

Figure 10. Wide-Band Filter Frequency Characteristics

6-(d) Power Down Mode and Power Saving Mode

The power down mode with ML7033 is enabled by the $\overline{PDN}$ pin. Additionally a power saving mode by the MODEn (CR0-B0/CR0-B1) bit is provided. For more details, please refer to the Data Sheet of the ML7033.

7. Other Notes on Usage

- Connect the AG and DG pins as close as possible to each other and connect them to the system ground with as low impedance as possible.
- For the power supply, use bypass capacitors with a good high frequency characteristics, and keep them as close as possible to the device pins.
- The bypass capacitor for the SGC pin should be placed as close as possible to the SGC pin. The SGC pin has a 50 kΩ output impedance and its input is utilized by the ML7033 as the analog signal ground, which must be as free from noise as possible. Therefore, try to keep the SGC pin away from external circuits.
- Keep overshoots and undershoots on the digital input signals minimal so as not to affect the audio characteristics.

Reference Documentation

- ML7033 data sheet
- HC55185 data sheet
- ML7033 Evaluation Board Manual

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

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