FEDL7050LA-02

OKI Semiconductor

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ML7050LA

Bluetooth RF Transceiver IC

GENERAL DESCRIPTION

The Oki ML7050LA is a highly integrated Bluetooth™ radio transceiver designed to operate in the global 2.4 GHz Industrial, Scientific, and Medical (ISM) band. The ML7050LA architecture incorporates vital intermediate frequency (IF) and radio frequency (RF) circuits on a low cost, integration-friendly bulk CMOS process.

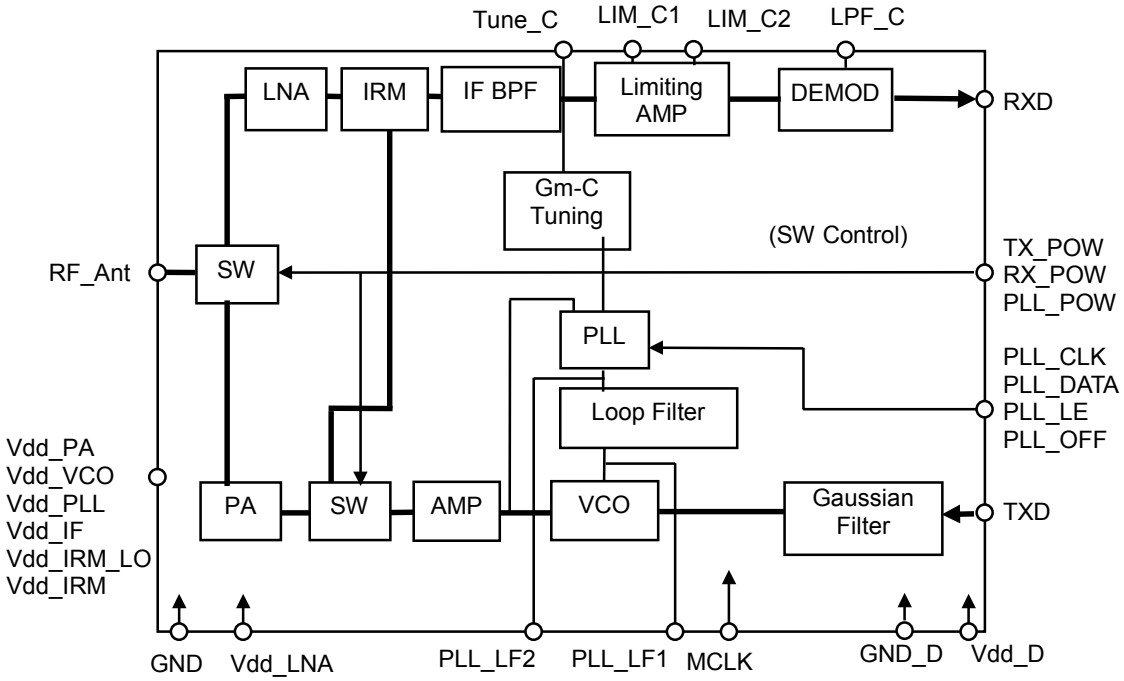
Bluetooth technology directly supports short range, wireless voice and data communications with 1 Mbps throughput performance in the public ISM band across many applications, employing rapid frequency hopping (1.6K hops/s) spread spectrum (FHSS) approach. The ML7050LA highly integrated CMOS Bluetooth RF transceiver LSI will establish a 2.4 to 2.5 GHz communication link compliant with Bluetooth Specification Version 1.1 and is packaged in the Oki 48-pin ball grid array (BGA) package requires only 7 mm x 7 mm of the systems critical board space.

Oki's Bluetooth LSI family includes baseband LSI (ML70511LA), System Development Kit (BT-SDK), firmware and software (BTS Pack1/2/3). Together, the RF LSI (ML7050LA) and baseband (ML70511LA) devices form a complete hardware solution optimized for low system cost, small form factor, and reduced power consumption Bluetooth applications.

FEATURES

- Circuit design based on the Bluetooth Specification Version 1.1.
- CMOS process technology lowers system cost and simplifies future baseband integration
- Fully integrated CMOS RF LSI: TX/RX switch, power amplifier, LNA, image rejection mixer, VCO, PLL, gm-C IF filter, modulator, and demodulator.
- Low IF circuitry eliminates off-chip SAW filter reducing bill-of-material (BOM)
- Class 2 power operation compliant covering a wide range of applications
- Seamless interface with Oki's ML70511LA Bluetooth baseband controller LSI
- Power supply voltage: 2.7 to 3.3 V
- Package: 48-pin BGA (7 mm x 7 mm x 1.41mm)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to 4.5	V
Input voltage	V_I		–0.3 to V_{DD} +0.3	V
Allowable power dissipation	P_D	-	0.5	W
Storage temperature	T_{STG}	-	–55 to +150	°C
Input RF Power		In-Band	TBD	dBm
	-	Out-of-Band	TBD	dBm

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	-	2.7	3.0	3.3	V
Full specification range	Ta	-	0	-	55	
Operating temperature range	Ta	-	–20	-	+85	°C

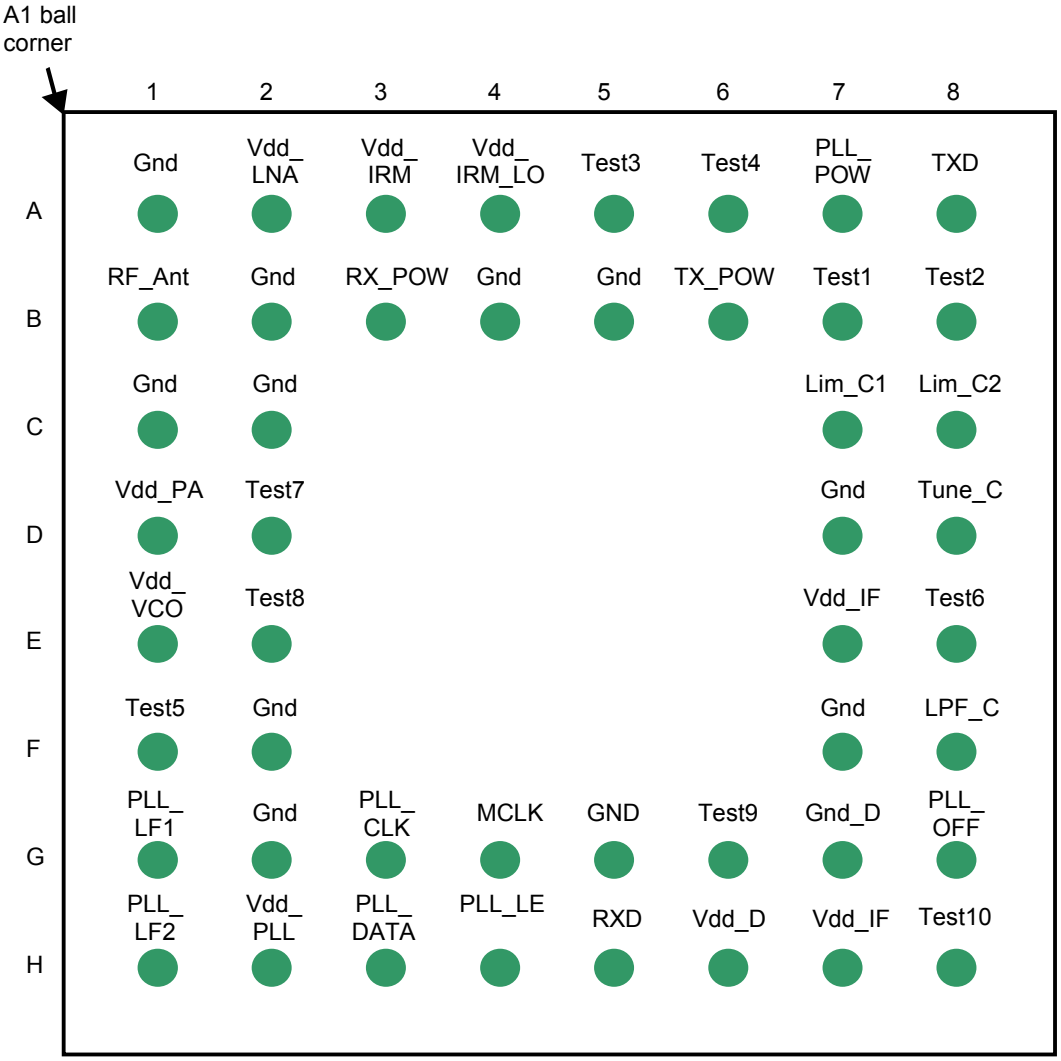
ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, Ta = 0 to +55°C)

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
Digital Inputs						
Vih	Digital input high		2.4		V_{DD}+0.3	V
Vil	Digital input low		-0.3		0.4	V
Digital Outputs						
Voh	Digital output high	Ioh=-2mA	2.2		3.6	V
Vol	Digital output low	Iol=2mA	0		0.8	V
Clock						
MCLK	Master clock frequency		-	12.13, 16	-	MHz
Current Consumption Ta=25°C						
IDDO	Receive Mode		-	55	-	mA
	Transmit Mode		-	34	-	mA
	PLL Mode	TX and RX disabled	-	22	-	mA
IDDS	Standby Mode	V_{DD} applied and power control pins disabled	-	10	-	uA
Receiver						
FRF	RF Frequency		2.4		2.5	GHz
R_{IN}	Reception sensitivity	Includes ANT BPF loss, Note 1		–75		dBm
-	Maximum Received Signal			–20		dBm
-	Spurious level	30 MHz to 1 GHz			–57	dBm
		1 GHz to 12.75 GHz			–47	dBm
-	Input VSWR		-	2:1	-	
Z_{IN}	RF Input impedance	SW in		50		Ω
Transmitter						
f_{RF}	RF Frequency		2.4		2.5	GHz
P_O	RF Output power	f_{RF} = 2.4 to 2.5 GHz,	0	2	4	dBm
—	Carrier frequency tolerance	initial accuracy (static)	-75		75	KHz
f_{stab1}	Frequency drift(1 slot packet)		-25		25	KHz
f_{stab2}	Frequency drift(3 slot packet)		-40		40	KHz
f_{stab3}	Frequency drift(5 slot packet)		-40		40	KHz
	Maximum frequency drift rate				400	Hz/μs
—	Power stability	over temp			TBD	dBm
—	Modulation index		0.28		0.35	-
—	In-band spurious level	±500 kHz			–20	dBm
		Offset = 2 MHz			–20	dBm
		Offset > 3 MHz			–40	dBm

—	Out-of-band spurious level	30 MHz to 1 GHz			–36	dBm
		1 GHz to 12.75 GHz			–30	dBm
		1.8 GHz to 1.9 GHz			–47	dBm
		5.15 GHz to 5.3 GHz			–47	dBm
—	Output VSWR		-	2:1	-	
Z_{OUT}	RF Output impedance	SW out		50		Ω
PLL						
—	Phase noise	@550 kHz		–103		dBc/Hz
		@2 MHz		–120		dBc/Hz
—	PLL lock-up time		-	-	150	μs

PIN LAYOUT (TOP VIEW)



TOP VIEW

PIN DESCRIPTION

Pins for RF Function

No.	Pin Name	I/O	Description
B1	RF_Ant	I/O	RF connection to external BPF (antenna filter)
D8	Tune_C	I	Gm-C tuning components - Connect capacitors and resister between D8 and GND
C7 C8	Lim_C1 Lim_C2	I	Limiting amplifier capacitors - Connect capacitors between pins and GND
F8	LPF_C	I	Low pass filter (LPF) capacitor - Connect capacitor between F8 and GND
G1 H1	PLL_LF1 PLL_LF2	—	External components for loop filter tuning: PLL_LF1 - Connect to VCO PLL_LF2 - Connect to PLL
Pins for TEST Interface, etc.			
G4	MCLK	I	Master clock (12MHz, 13MHz or 16MHz) - CMOS level
B7	Test1	I/O	Test pins - Connect to GND
B8	Test2	I/O	
A5	Test3	I	
A6	Test4	I	
F1	Test5	O	No connect - Open
E8	Test6	O	No connect - Open
D2 E2	Test7 Test8	O	Test pins - Connect to GND
G6	Test9	O	No connect - Open
H8	Test10	I/O	No connect - Open
Pins for Power Supply and Ground			
H6	Vdd_D	—	Power supply (V_{DD})- Digital; 3.0V+/-0.3V (from regulated voltage source)
G7	GND_D	—	Common Ground - Digital
D1	Vdd_PA	—	Power supply (V_{DD}) - Analog; 3.0V+/-0.3V (from regulated voltage source)
E1	Vdd_VCO		
A2	Vdd_LNA		
H2	Vdd_PLL		
A3	Vdd_IRM		
A4	Vdd_IRM_LO		
E7, H7	Vdd_IF		
A1/B2 B4/B5 C1/C2 D7/F2 F7/G2 G5	GND	—	Common ground (GND) - Analog

Pins for the Interface Between the RF LSI and the Baseband LSI

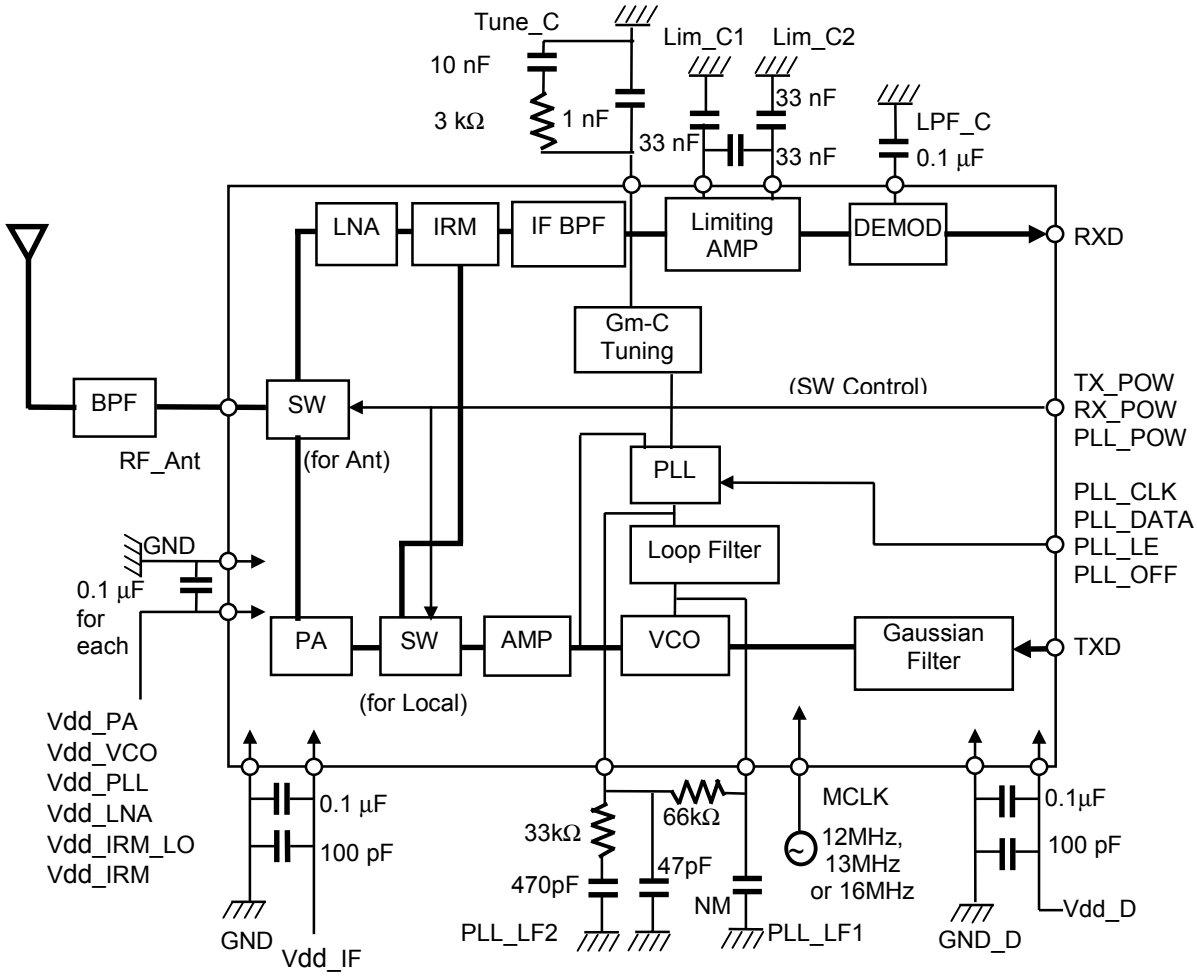
No.	Pin Name	I/O	Description
A8	TXD	I	Transmit (TX) data - CMOS level
H5	RXD	O	Receive (RX) data - CMOS level
H3	PLL_DATA	I	PLL setup data: 6 Mbps <= PLL DATA <= 10 Mbps
G3	PLL_CLK	I	PLL clock setup: 6 MHz <= PLL CLK <= 10 MHz
H4	PLL_LE	I	PLL load enable setup: Data latched : 'High' 100 nsec <= PLL LE
G8	PLL_OFF	I	PLL Open-loop/Closed-loop mode control: Closed loop mode (receive): 'High' Open loop mode (transmit) : 'Low'
A7	PLL_POW	I	PLL power supply control switch: PLL Power ON : 'Low' PLL Power OFF :' High'
B6	TX_POW	I	Transmitter (TX) power supply control switch: TX ON (transmit) : 'Low ' TX OFF(receive) : 'High'
B3	RX_POW	I	Receiver (RX) power supply control switch: RX ON (receive) : 'Low' RX OFF (transmit) : 'High'

Modes of Operation

By setting or transitioning control pins, the device will enter into various modes of operation including receive, transmit, and standby.

Mode	Receive	Transmit	PLL	Standby
PLL_POW	0	0	0	1
TX_POW	1	0	1	1
RX_POW	0	1	1	1

PIN CONNECTION DIAGRAM



The externally connected components shown are tentative (April 2001).

* The circuit is subject to change according to the specific board design.
Please contact Oki Electric Industry Co., Ltd. for detailed information.

The ML7050LA provides a low bill-of-material (BOM) Bluetooth solution by minimizing external components. The design incorporates numerous internal tuning circuits using Gm-C and other leading-edge technologies to reliably control phase lock loop (PLL), VCO, amplifiers, modulator, and demodulator circuits. The TX-POW, RX_POW, PLL_POW, PLL-CLK, PLL_DATA, PLL_LE, PLL_OFF, RXD, and TXD connect directly to the complementary Bluetooth baseband (ML70511LA) device.

DESCRIPTION OF INTERNAL BLOCKS

- Transmit filter (Gaussian filter):
  The input data is converted into a frequency modulation signal by a filter with Gaussian characteristics and is sent to the VCO.

- Frequency control section (VCO, PLL, Loop Filter, AMP and SW):
  Generates a frequency in the 2.4 GHz to 2.5 GHz band (ISM band). During transmission, the VCO oscillator frequency is modulated by the modulation signal output by the Gaussian filter. The PLL frequency is controlled by the signals PLL_DATA, PLL_CLK, and PLL_LE. The switch SW (for Local) distributes the oscillator output to the transmitter circuit and the receiver circuit depending on the control signal (TX_POW/RX_POW).

- Power amplifier (PA):
  This is the power amplifier for the transmitter.

- Transmit/Receive selection switch (SW for Ant)
  Depending on the control signal (TX_POW/RX_POW), this switch feeds the output of the power amplifier to the antenna during transmission. During reception, the received signal of the antenna is fed to the LNA.

- Reception amplifier (LNA):
  This amplifies the weak RF received signal from the antenna.

- Image Rejection Mixer (IRM):
  Converts the output signal from the LNA (2.4 to 2.5 GHz) into an intermediate frequency and also eliminates the image frequency component.

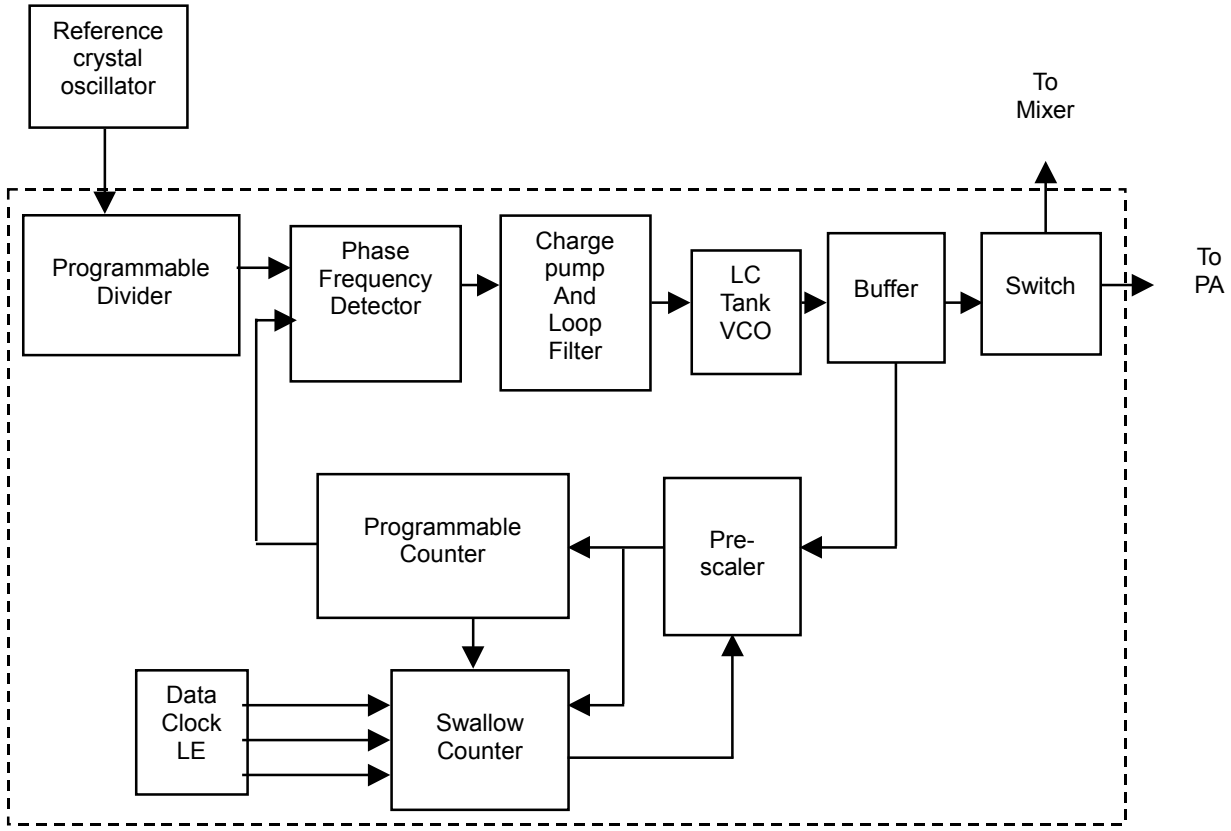
- IF Band pass filter (IF BPF):
  Removes the signal of the nearby bands.

- Limiting amplifier:
  Amplifies the signal converted into the intermediate frequency up to a specific amplitude.

- Demodulator (DEMOD):
  The received signal is demodulated using the delay detector circuit.

- Filter tuning (Gm-C Tuning):
  The reference clock is compared with the oscillator frequency inside the tuning circuit, and the frequency characteristics of the Gm-C filter is adjusted automatically.

PLL METHODOLOGY



PLL Computation Method

$$\frac{Fvco}{MxN+A} \quad \frac{Fosc}{R}$$

(0 <= A<=31)

(M × N + A denotes (M - A) × 32 + A × 33)
R: Reference counter set value
N: Programmable counter set value
A: Swallow counter set value

PLL Reference Counter

Freq	R	R(Bin)				
(MHz)	(Dec)	R4	R3	R2	R1	R0
5	5	0	0	1	0	1
6	6	0	0	1	1	0
7	7	0	0	1	1	1
8	8	0	1	0	0	0
9	9	0	1	0	0	1
10	10	0	1	0	1	0
11	11	0	1	0	1	1
12	12	0	1	1	0	0
13	13	0	1	1	0	1
14	14	0	1	1	1	0
15	15	0	1	1	1	1
16	16	1	0	0	0	0
17	17	1	0	0	0	1
18	18	1	0	0	1	0
19	19	1	0	0	1	1
20	20	1	0	1	0	0

Programmable Counter and Swallow Counter

F.step	1 MHz
M	32 div

(RX PLL Frequency) = (TX PLL Frequency) – 2MHz
* In receive mode, PLL generates local frequency for IRM. Intermediate frequency is 2MHz.

Freq.	N	A	N(Bin)							A(Bin)				
(MHz)	(Dec)	(Dec)	N6	N5	N4	N3	N2	N1	N0	A4	A3	A2	A1	A0
2397	74	29	1	0	0	1	0	1	0	1	1	1	0	1
2398	74	30	1	0	0	1	0	1	0	1	1	1	1	0
2399	74	31	1	0	0	1	0	1	0	1	1	1	1	1
2400	75	0	1	0	0	1	0	1	1	0	0	0	0	0
2401	75	1	1	0	0	1	0	1	1	0	0	0	0	1

2402	75	2	1	0	0	1	0	1	1	0	0	0	1	0
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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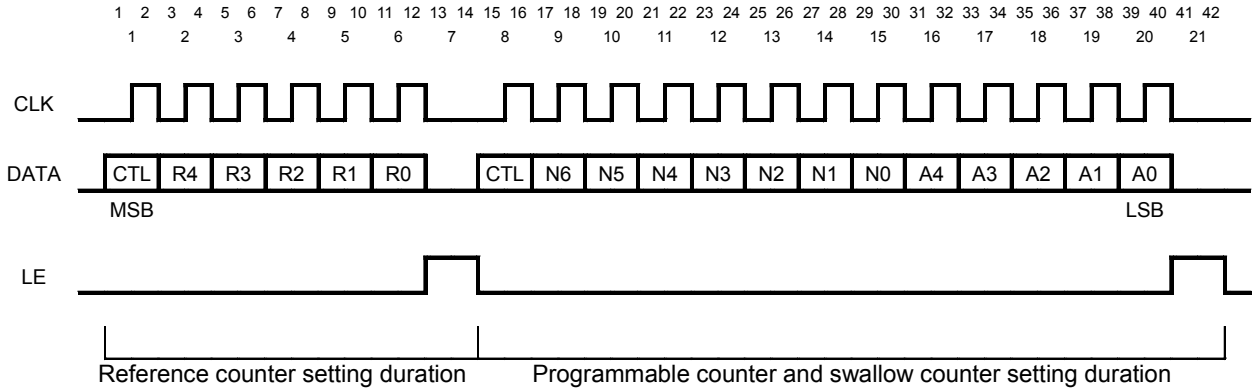
2496	78	0	1	0	0	1	1	1	0	0	0	0	0	0
2497	78	1	1	0	0	1	1	1	0	0	0	0	0	1
2498	78	2	1	0	0	1	1	1	0	0	0	0	1	0
2499	78	3	1	0	0	1	1	1	0	0	0	0	1	1
2500	78	4	1	0	0	1	1	1	0	0	0	1	0	0

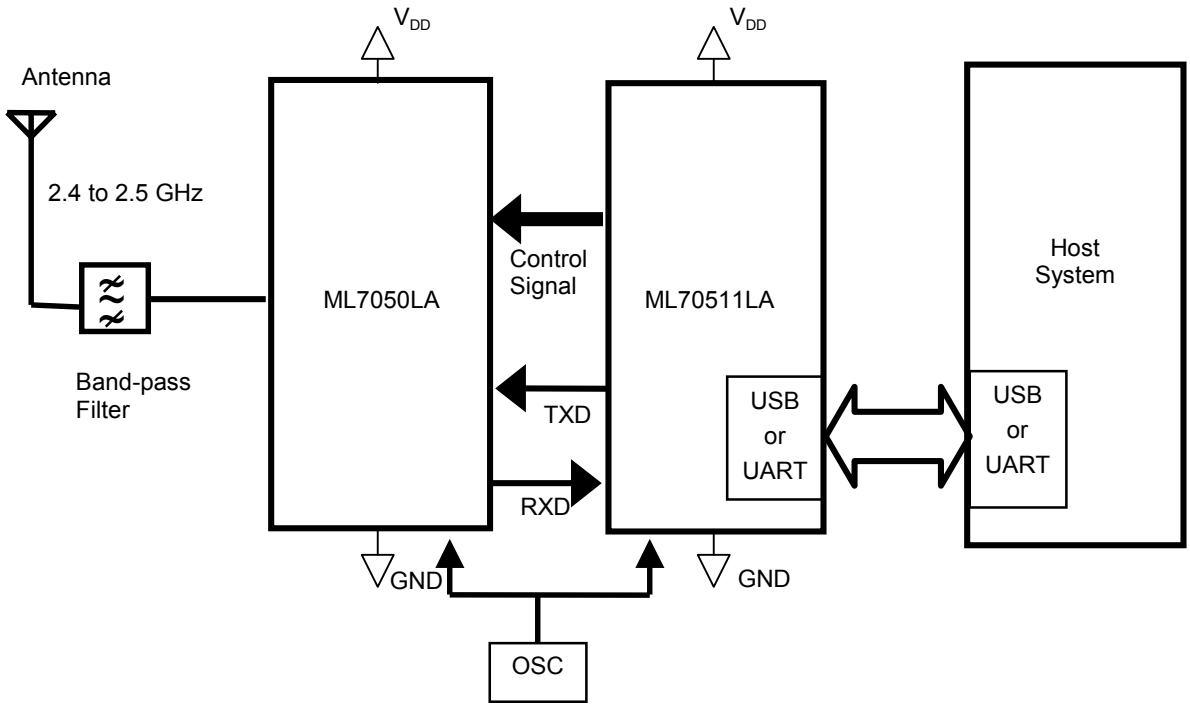
PLL Set-up Time Chart



R4 to R0: Binary 5-bit reference counter (5-20)
N6 to N0: Programmable counter (7 bits)
See "PLL Setting method".
A4 to A0: Swallow counter (0-31) (5 bits)
See "PLL Setting method".
CTL: When CTL is "H", the input data is handed over to the reference counter register.
When CTL is "L", the input data is handed over to the programmable and swallow counter register.

Note: Start data input from the MSB.

SYSTEM OVERVIEW



Together, RF (ML7050LA) and baseband (ML70511LA) devices form a complete hardware solution optimized for low system cost, small form factor, and reduced power consumption wireless applications. The ML70511LA baseband IC controls the ML7050LA frequency selection, tuning characteristics, and control functions through writing to internal registers. ML7050LA can then read-back the register information to ML70511LA insuring proper modes of operation. The communication between the devices occurs on Oki's proprietary, low pin count serial interface. The connection between a host controller or processor and the baseband device is implemented via USB (version 1.1) or UART.

Power Supply

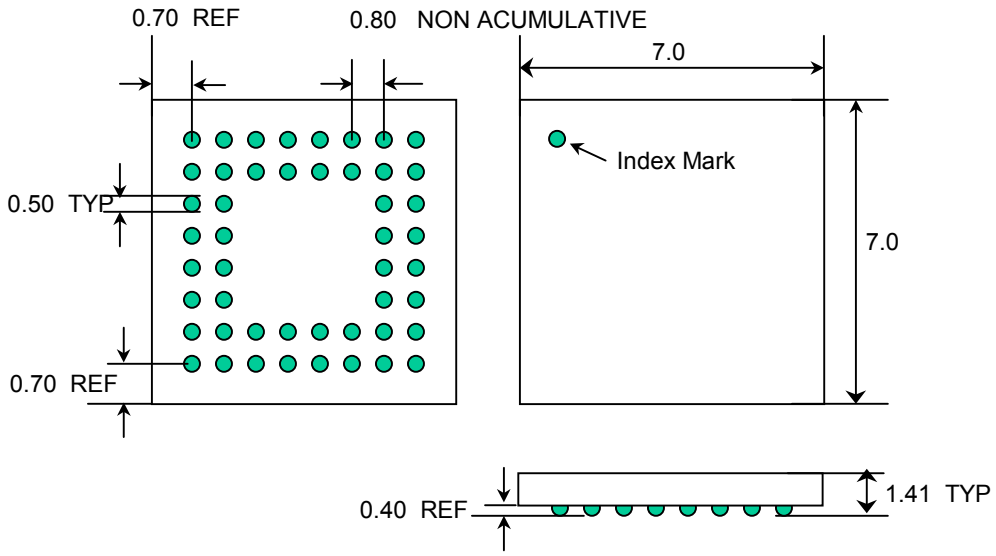
The analog power supply (V_{DD}) voltage is connected to pins serving each analog functional blocks (Vdd_PA, Vdd_LNA, Vdd_VCO, Vdd_PLL, Vdd_IF, Vdd_IRM and Vdd_IRM_LO). A separate digital power supply voltage is required by the digital section. Each of the analog power supply voltage should be supplied from regulated voltage source and should be low-frequency de-coupled by external blocking capacitors.

Ground

In order to minimize electrical noise and other interference, the ground plane should be distributed with low impedance characteristics including underneath the ML7050LA. Connect all GND pins to the ground plane.

PACKAGE DIMENSIONS (48-PIN BGA)

(Unit: mm)



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