# OKI Semiconductor

# MR27V802D

524,288-Word x 16-Bit or 1,048,576-Word x 8-Bit

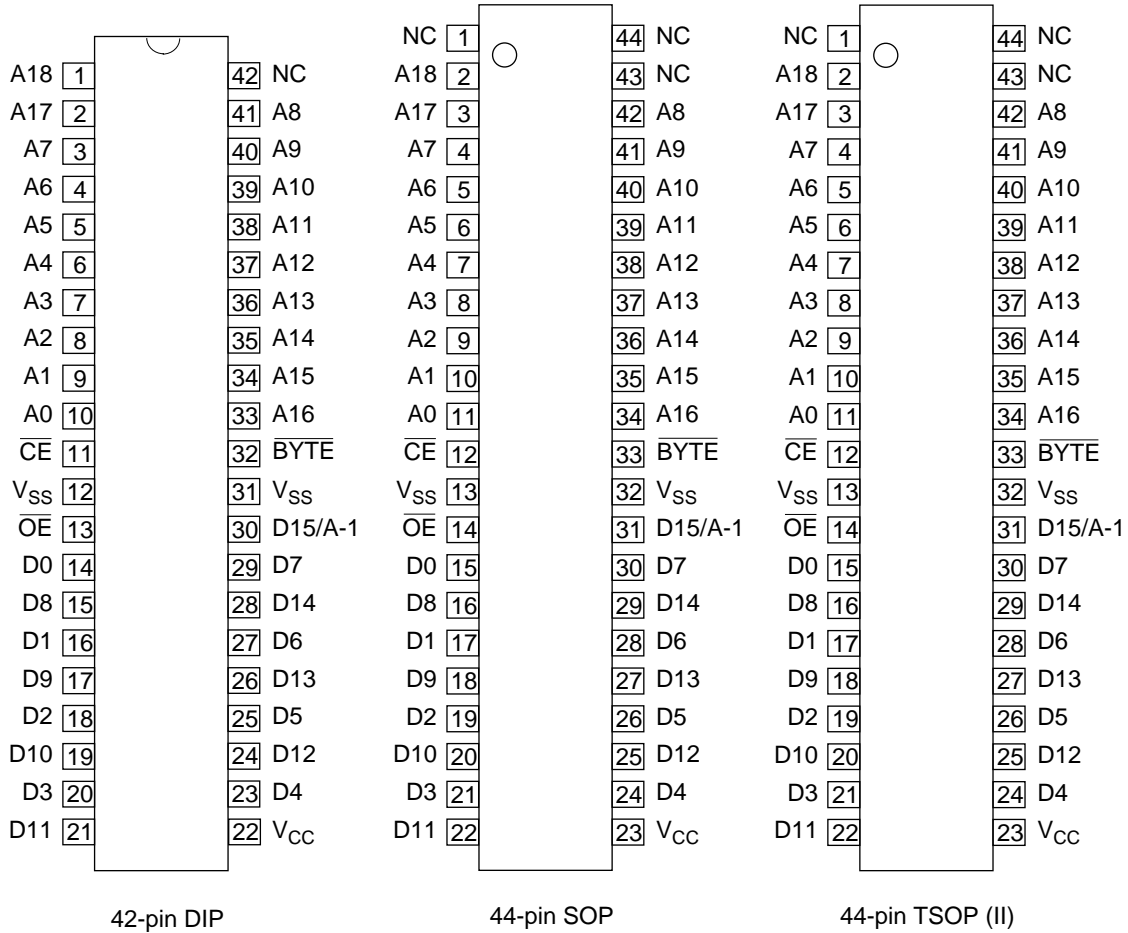Production Programmed Read Only Memory (P2ROM)

## DESCRIPTION

The MR27V802D is a 8Mbit Production Programmed Read-Only Memory (P2ROM) whose configuration can be  electrically switched between 524,288 word x 16bit and 1,048,576 word x 8bit. The MR27V802D operates on a single +3V-3.3V power supply and is TTL compatible. Since the MR27V802D operates asynchronously , external clocks are not required , making this device easy-to-use. The MR27V802D is suitable as large-capacity fixed memory for microcomputers and data terminals. It is manufactured using a CMOS double silicon gate technology and is offered in 42-pin DIP, 44-pin SOP or 44-pin TSOP packages.

## FEATURES

- 524,288 word x 16bit / 1,048,576 word x 8bit electrically switchable configuration
- Single +3V-3.3V power  supply
- Access time          100ns access time (Vcc=+3V)
                        80ns access time (Vcc=+3.3V)
- Input / Output TTL compatible
- Three-state output
- Packages
  - 42-pin plastic DIP (DIP42-P-600-2.54)          (Product name : MR27V802D-xxRA)
  - 44-pin plastic SOP (SOP44-P-600-1.27-K)        (Product name : MR27V802D-xxMA)
  - 44-pin plastic TSOP (TSOP II 44-P-400-0.80-K) (Product name : MR27V802D-xxTP)

## PIN CONFIGURATION  (TOP VIEW)

**42-pin DIP**

| | | |
|---|---|---|
| A18 | 1 | 42 NC |
| A17 | 2 | 41 A8 |
| A7 | 3 | 40 A9 |
| A6 | 4 | 39 A10 |
| A5 | 5 | 38 A11 |
| A4 | 6 | 37 A12 |
| A3 | 7 | 36 A13 |
| A2 | 8 | 35 A14 |
| A1 | 9 | 34 A15 |
| A0 | 10 | 33 A16 |
| $\overline{CE}$ | 11 | 32 $\overline{BYTE}$ |
| $V_{SS}$ | 12 | 31 $V_{SS}$ |
| $\overline{OE}$ | 13 | 30 D15/A-1 |
| D0 | 14 | 29 D7 |
| D8 | 15 | 28 D14 |
| D1 | 16 | 27 D6 |
| D9 | 17 | 26 D13 |
| D2 | 18 | 25 D5 |
| D10 | 19 | 24 D12 |
| D3 | 20 | 23 D4 |
| D11 | 21 | 22 $V_{CC}$ |

**44-pin SOP**

| | | |
|---|---|---|
| NC | 1 | 44 NC |
| A18 | 2 | 43 NC |
| A17 | 3 | 42 A8 |
| A7 | 4 | 41 A9 |
| A6 | 5 | 40 A10 |
| A5 | 6 | 39 A11 |
| A4 | 7 | 38 A12 |
| A3 | 8 | 37 A13 |
| A2 | 9 | 36 A14 |
| A1 | 10 | 35 A15 |
| A0 | 11 | 34 A16 |
| $\overline{CE}$ | 12 | 33 $\overline{BYTE}$ |
| $V_{SS}$ | 13 | 32 $V_{SS}$ |
| $\overline{OE}$ | 14 | 31 D15/A-1 |
| D0 | 15 | 30 D7 |
| D8 | 16 | 29 D14 |
| D1 | 17 | 28 D6 |
| D9 | 18 | 27 D13 |
| D2 | 19 | 26 D5 |
| D10 | 20 | 25 D12 |
| D3 | 21 | 24 D4 |
| D11 | 22 | 23 $V_{CC}$ |

**44-pin TSOP (II)**

| | | |
|---|---|---|
| NC | 1 | 44 NC |
| A18 | 2 | 43 NC |
| A17 | 3 | 42 A8 |
| A7 | 4 | 41 A9 |
| A6 | 5 | 40 A10 |
| A5 | 6 | 39 A11 |
| A4 | 7 | 38 A12 |
| A3 | 8 | 37 A13 |
| A2 | 9 | 36 A14 |
| A1 | 10 | 35 A15 |
| A0 | 11 | 34 A16 |
| $\overline{CE}$ | 12 | 33 $\overline{BYTE}$ |
| $V_{SS}$ | 13 | 32 $V_{SS}$ |
| $\overline{OE}$ | 14 | 31 D15/A-1 |
| D0 | 15 | 30 D7 |
| D8 | 16 | 29 D14 |
| D1 | 17 | 28 D6 |
| D9 | 18 | 27 D13 |
| D2 | 19 | 26 D5 |
| D10 | 20 | 25 D12 |
| D3 | 21 | 24 D4 |
| D11 | 22 | 23 $V_{CC}$ |

| PIN NAMES | FUNCTIONS |
|---|---|
| D15/A-1 | Data output / Address  input |
| A0-A18 | Address input |
| D0-D14 | Data output |
| $\overline{CE}$ | Chip enable |
| $\overline{OE}$ | Output enable |
| $V_{CC}$ | Power supply voltage |
| $V_{SS}$ | GND |
| $\overline{BYTE}$ | Mode switch |
| NC | Non connection |

## BLOCK DIAGRAM
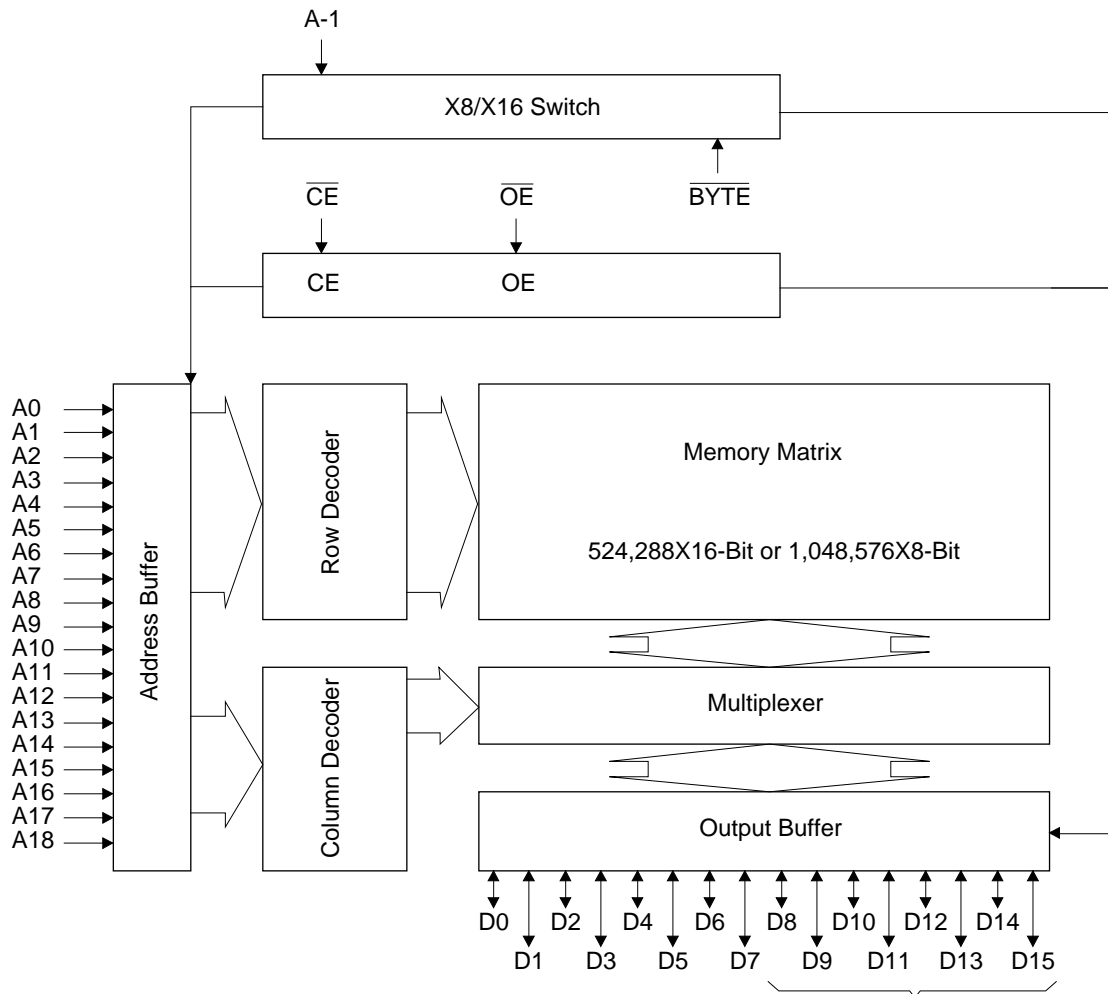


In 8-bit output mode, these pins are three-stated and pin D15 functions as the A-1 address pin.

## FUNCTION TABLE

| MODE | $\overline{CE}$ | $\overline{OE}$ | $\overline{BYTE}$ | $V_{CC}$ | D0 - D7 | D8 - D14 | D15/A-1 |
|---|---|---|---|---|---|---|---|
| READ (16-Bit) | L | L | H | 3.0V to 3.3V | $D_{OUT}$ | | |
| READ (8-Bit) | L | L | L | | $D_{OUT}$ | Hi-Z | L/H |
| OUTPUT DISABLE | L | H | H | | | Hi-Z | |
| | | | L | | | | * |
| STAND-BY | H | * | H | | | Hi-Z | |
| | | | L | | | | * |

*: Don't Care

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Value | Unit |
|---|---|---|---|---|
| Operating temperature under bias | $T_{opr}$ | - | 0 to 70 | °C |
| Storage temperature | $T_{stg}$ | | -55 to 125 | °C |
| Input voltage | $V_I$ | | -0.5 to $V_{CC}$+ 0.5 | V |
| Output voltage | $V_O$ | relative to $V_{SS}$ | -0.5 to $V_{CC}$ +0.5 | V |
| Power supply voltage | $V_{CC}$ | | -0.5 to 5 | V |
| Power dissipation per package | $P_D$ | - | 1.0 | W |

## RECOMMENDED OPERATING CONDITIONS

(Ta=0 to 70°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ power supply voltage | $V_{CC}$ | | 2.7 | - | 3.6 | V |
| Input "H" level | $V_{IH}$ | $V_{CC}$=2.7V-3.6V | 2.2 | - | $V_{CC}$+0.5* | V |
| Input "L"  level | $V_{IL}$ | | -0.5** | - | 0.6 | V |

Voltage is relative to Vss

 * : Vcc+1.5V (Max.) when pulse width of overshoot is less than 10nS.

** : -1.5V (Min.) when pulse width of undershoot is less than 10nS.

## ELECTRICAL CHARACTERISTICS (Read operation)

### DC Characteristics 1

$(V_{CC}=3V\pm0.3V, Ta=0 \text{ to } 70°C)$

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $V_I=0$ to Vcc | - | - | 10 | μA |
| Output leakage current | $I_{LO}$ | $V_O=0$ to Vcc | - | - | 10 | μA |
| $V_{CC}$ power supply current (Standby) | $I_{CCSC}$ | $\overline{CE}=V_{CC}$ | - | - | 50 | μA |
| | $I_{CCST}$ | $\overline{CE}=V_{IH}$ | - | - | 1 | mA |
| $V_{CC}$ power supply current (Read) | $I_{CCA}$ | $\overline{CE}=V_{IL},\overline{OE}=V_{IH}$ tc=100ns | - | - | 35 | mA |
| Input "H" level | $V_{IH}$ | - | 2.2 | - | $V_{CC}+0.5*$ | V |
| Input "L" level | $V_{IL}$ | - | -0.5** | - | 0.6 | V |
| Output "H" level | $V_{OH}$ | $I_{OH}=-400uA$ | 2.4 | - | - | V |
| Output "L" level | $V_{OL}$ | $I_{OL}=2.1mA$ | - | - | 0.4 | V |

Voltage is relative to Vss

 * : Vcc+1.5V (Max.) when pulse width of overshoot is less than 10nS.

** : -1.5V (Min.) when pulse width of undershoot is less than 10nS.

### DC Characteristics 2

$(V_{CC}=3.3V\pm0.3V, Ta=0 \text{ to } 70°C)$

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $V_I=0$ to Vcc | - | - | 10 | μA |
| Output leakage current | $I_{LO}$ | $V_O=0$ to Vcc | - | - | 10 | μA |
| $V_{CC}$ power supply current (Standby) | $I_{CCSC}$ | $\overline{CE}=V_{CC}$ | - | - | 50 | μA |
| | $I_{CCST}$ | $\overline{CE}=V_{IH}$ | - | - | 1 | mA |
| $V_{CC}$ power supply current (Read) | $I_{CCA}$ | $\overline{CE}=V_{IL},\overline{OE}=V_{IH}$ tc=80ns | - | - | 40 | mA |
| Input "H" level | $V_{IH}$ | - | 2.2 | - | $V_{CC}+0.5*$ | V |
| Input "L" level | $V_{IL}$ | - | -0.5** | - | 0.6 | V |
| Output "H" level | $V_{OH}$ | $I_{OH}=-400uA$ | 2.4 | - | - | V |
| Output "L" level | $V_{OL}$ | $I_{OL}=2.1mA$ | - | - | 0.4 | V |

Voltage is relative to Vss

 * : Vcc+1.5V (Max.) when pulse width of overshoot is less than 10nS.

** : -1.5V (Min.) when pulse width of undershoot is less than 10nS.

### AC Characteristics 1

($V_{CC}$=3V±0.3V, Ta=0 to 70°C)

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Address cycle time | $T_C$ | - | 100 | - | ns |
| Address access time | $T_{ACC}$ | $\overline{CE}=\overline{OE}=V_{IL}$ | - | 100 | ns |
| $\overline{CE}$ access time | $T_{CE}$ | $\overline{OE}=V_{IL}$ | - | 100 | ns |
| $\overline{OE}$ access time | $T_{OE}$ | $\overline{CE}=V_{IL}$ | - | 50 | ns |
| Output disable time | $T_{CHZ}$ | $\overline{OE}=V_{IL}$ | 0 | 30 | ns |
| | $T_{OHZ}$ | $\overline{CE}=V_{IL}$ | 0 | 25 | ns |
| Output hold time | $T_{OH}$ | $\overline{CE}=\overline{OE}=V_{IL}$ | 0 | - | ns |

Measurement conditions
- Input signal level --------------------- 0V/3V
- Input timing reference level ----------- 0.8V/2.0V
- Output load ------------------------- 100pF
- Output timing reference level ---------- 0.8V/2.0V

### AC Characteristics 2

($V_{CC}$=3.3V±0.3V, Ta=0 to 70°C)

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Address cycle time | $T_C$ | - | 80 | - | ns |
| Address access time | $T_{ACC}$ | $\overline{CE}=\overline{OE}=V_{IL}$ | - | 80 | ns |
| $\overline{CE}$ access time | $T_{CE}$ | $\overline{OE}=V_{IL}$ | - | 80 | ns |
| $\overline{OE}$ access time | $T_{OE}$ | $\overline{CE}=V_{IL}$ | - | 40 | ns |
| Output disable time | $T_{CHZ}$ | $\overline{OE}=V_{IL}$ | 0 | 30 | ns |
| | $T_{OHZ}$ | $\overline{CE}=V_{IL}$ | 0 | 25 | ns |
| Output hold time | $T_{OH}$ | $\overline{CE}=\overline{OE}=V_{IL}$ | 0 | - | ns |

Measurement conditions
- Input signal level --------------------- 0V/3V
- Input timing reference level ----------- 0.8V/2.0V
- Output load ------------------------- 100pF
- Output timing reference level ---------- 0.8V/2.0V

2.08V

800ohms

Output

100pF

## TIMING CHART (READ CYCLE)

### 16-Bit Read Mode ($\overline{BYTE}=V_{IH}$)
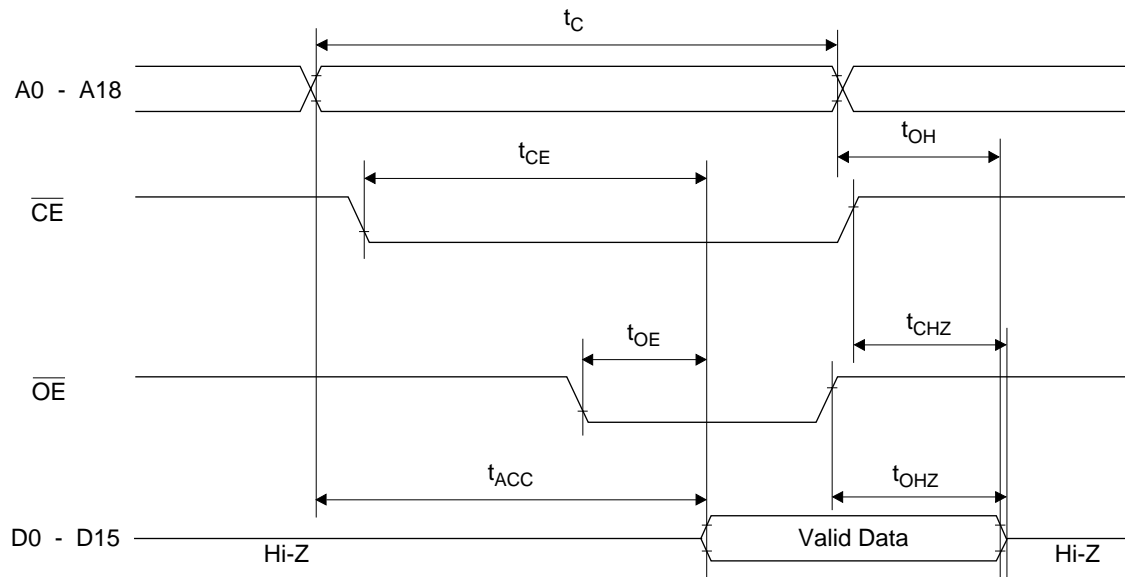


### 8-Bit Read Mode ($\overline{BYTE}=V_{IL}$)
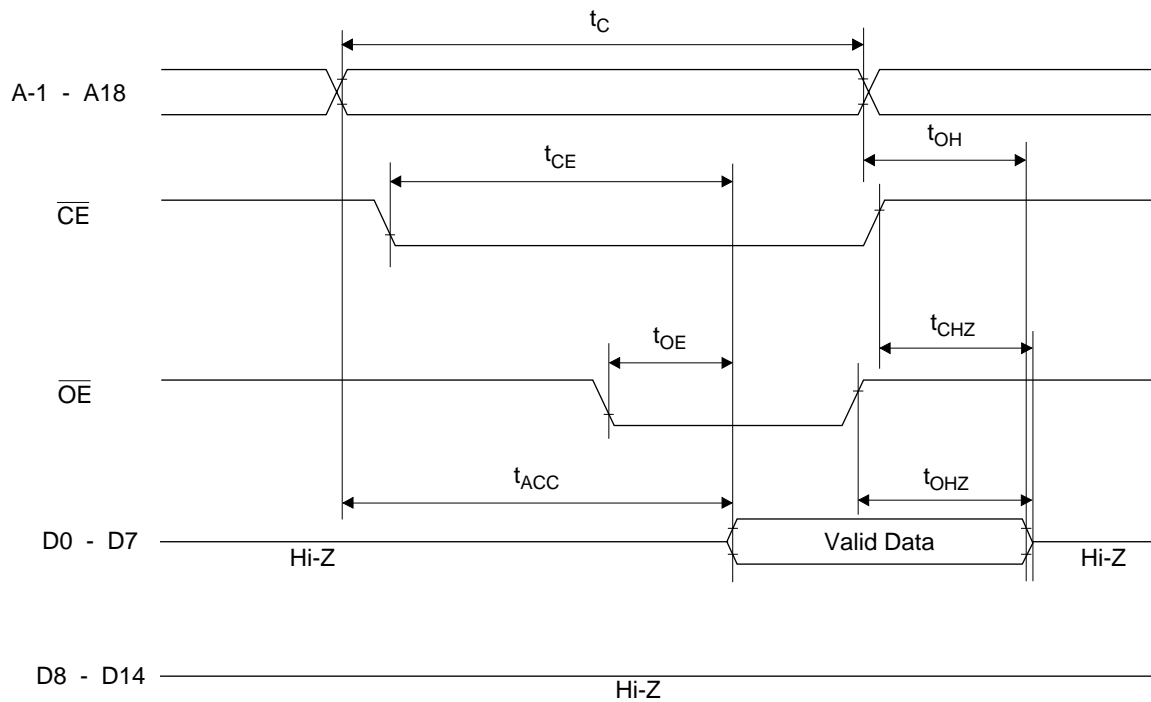
**PIN Capacitance**

$(V_{CC}=3.3V, Ta=25°C, f=1MHz)$

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input | $C_{IN1}$ | $V_I=0V$ | - | - | 8 (10) | pF |
| $\overline{BYTE}$ | $C_{IN2}$ | | - | - | 120 | |
| Output | $C_{OUT}$ | $V_O=0V$ | - | - | 10 (12) | |

( ) : DIP only