
OKI Semiconductor

MR53V1652J

Preliminary

1,048,576-Word X 16-Bit or 2,097,152-Word X 8-Bit

8Word X 16-Bit or 16Word X 8-Bit/Page Mode MASK ROM

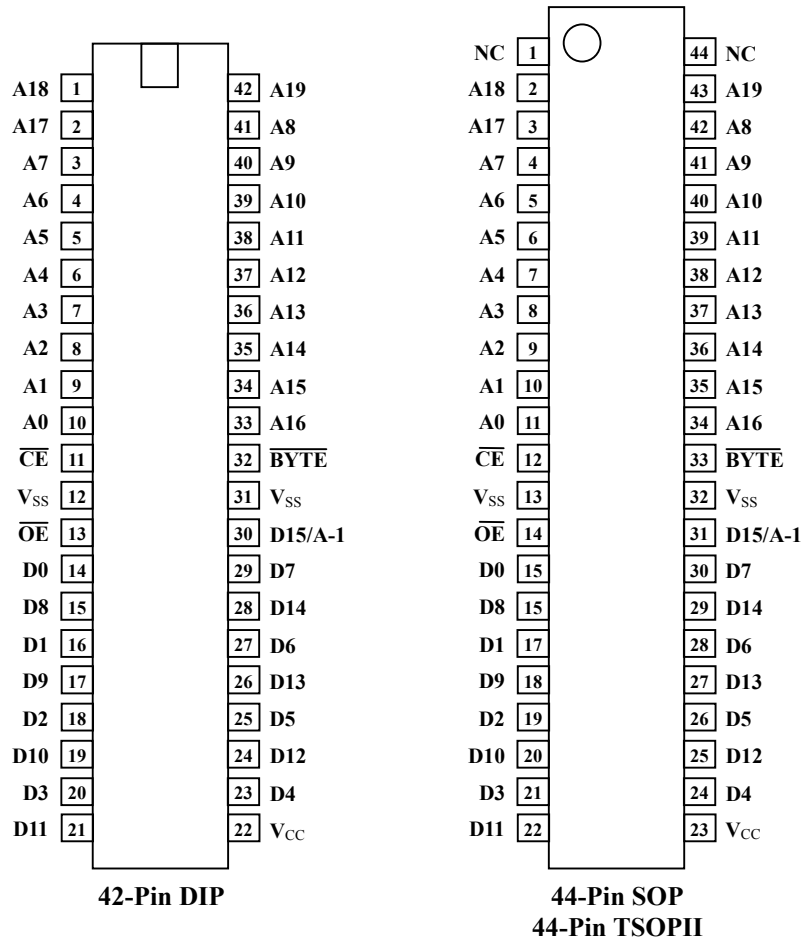
DESCRIPTION

The MR53V1652J is a 16Mbit Read-Only Memory whose configuration can be electrically switched between 1,048,576 word x 16bit and 2,097,152 word x 8bit. The MR53V1652J operates asynchronously, external clocks are not required, making this device easy-to-use. The MR53V1652J is suitable as large-capacity fixed memory for microcomputers and data terminals. It is manufactured using a CMOS silicon gate technology and is offered in 42-pin DIP, 44-pin SOP or 44-pin TSOP packages.

FEATURES

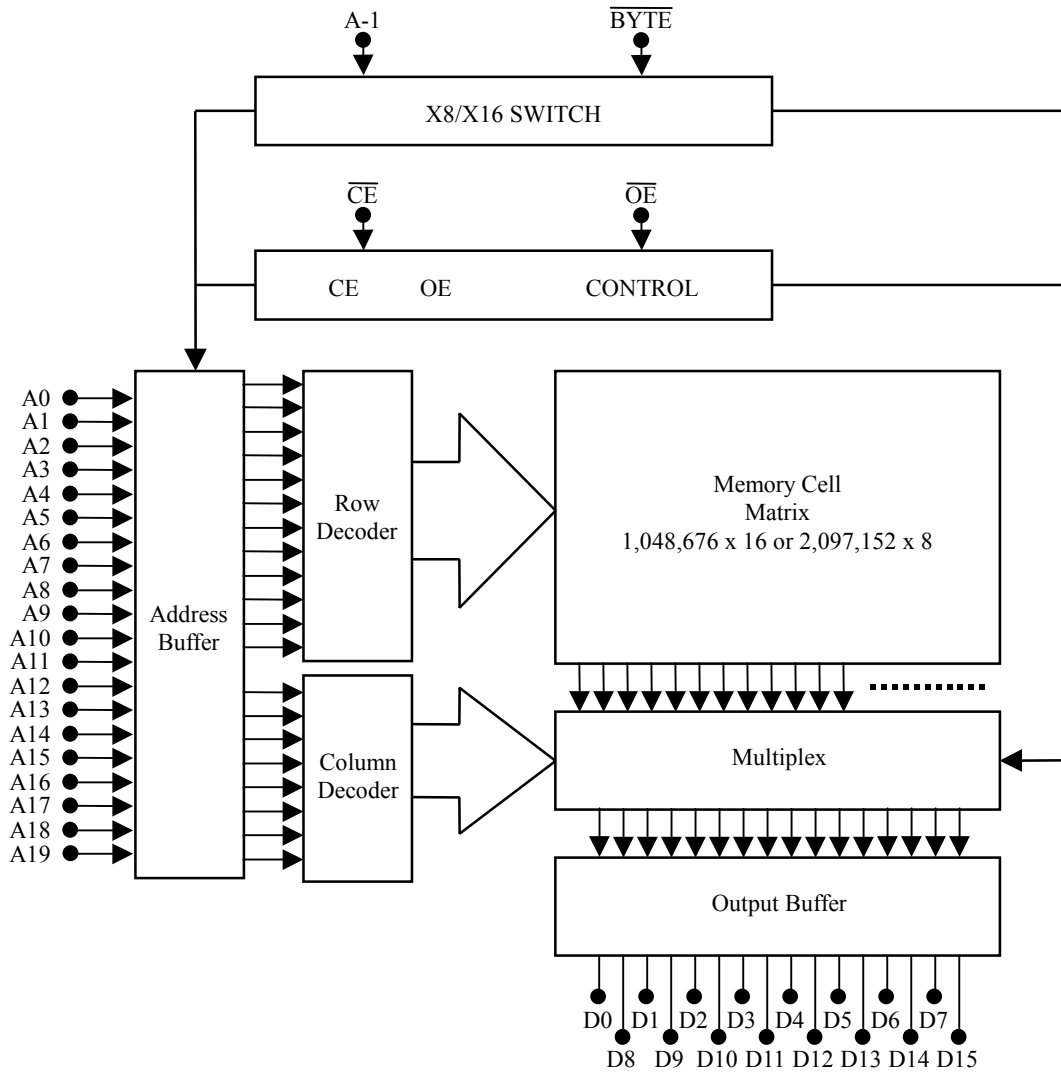
- 1,048,576 word x 16bit / 2,097,152 word x 8bit electrically switchable configuration
- 8word x 16-Bit or 16word x 8-bit / Page read mode
- Single +2.7V~3.6V power supply
- Normal access time 100ns
- Page access time 30ns
- V_{CC} power supply current 80mA
- V_{CC} standby current 10μA
- Input / Output TTL compatible
- Three-state output
- Packages
 - 42-pin plastic DIP (DIP42-P-600-2.54) MR53V1652J-XXRA
 - 44-pin plastic SOP (SOP44-P-600-1.27-K) MR53V1652J-XXMA
 - 44-pin plastic TSOP (TSOP44-P-400-0.80-K) MR53V1652J-XXTP

PIN CONFIGURATION (TOP VIEW)



| PIN NAMES | FUNCTIONS |
|-------------------|-----------------------------|
| D15/A-1 | Data output / Address input |
| A0~A19 | Address input |
| D0~D14 | Data output |
| \overline{CE} | Chip enable |
| \overline{OE} | Output enable |
| \overline{BYTE} | Mode switch |
| V _{CC} | Power supply voltage |
| V _{SS} | GND |
| NC | Non connection |

BLOCK DIAGRAM



FUNCTION TABLE

| MODE | \overline{CE} | \overline{OE} | \overline{BYTE} | D0~D7 | D8~D14 | A-1/D15 |
|----------------|-----------------|-----------------|-------------------|------------------|--------|---------|
| STAND BY | H | X | X | Hi-Z | | |
| OUTPUT DISABLE | L | H | H | Hi-Z | | |
| | L | H | L | L/H | | |
| READ(16-BIT) | L | L | H | D _{OUT} | | |
| READ(8-BIT) | L | L | L | D _{OUT} | Hi-Z | L/H |

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Value | Unit |
|----------------------------------|------------------|-----------------------------|-----------------------------|------|
| Operating temperature under bias | T _{OPR} | - | 0 ~ 70 | °C |
| Storage temperature | T _{STG} | - | -55 ~ 125 | °C |
| Input voltage | V _I | Relative to V _{SS} | -0.5 ~ V _{CC} +0.5 | V |
| Output voltage | V _O | | -0.5 ~ V _{CC} +0.5 | V |
| Power supply voltage | V _{CC} | | -0.5 ~ 5 | V |
| Power dissipation per package | P _D | - | 1.0 | W |

RECOMMENDED OPERATING CONDITIONS FOR READ

(Ta=0 ~ 70°C)

| Parameter | Symbol | Condition | Min. | Typ. | Min. | Unit |
|--------------------------------------|-----------------|------------------------------|------|------|----------------------|------|
| V _{CC} power supply voltage | V _{CC} | V _{CC} =2.7V ~ 3.6V | 2.7 | - | 3.6 | °C |
| Input "H" level | V _{IH} | | 2.2 | - | V _{CC} +0.5 | °C |
| Input "L" level | V _{IL} | | -0.5 | - | 0.8 | V |

Voltage is relative to V_{SS}

PIN Capacitance

(V_{CC}=3.3V, Ta=25°C, f=1MHz)

| Parameter | Symbol | Condition | Min. | Typ. | Min. | Unit |
|-----------|------------------|--------------------|------|------|------|------|
| Input | C _{IN} | V _I =0V | - | - | 12 | pF |
| Output | C _{OUT} | V _O =0V | - | - | 15 | pF |

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC}=2.7V~3.6V, Ta=0~70°C)

| Parameter | Symbol | Condition | Min. | Typ. | Min. | Unit |
|--|-------------------|---|----------------------|------|----------------------|------|
| Input leakage current | C _{IN} | V _I =0V~V _{CC} | - | - | 10 | μA |
| Output leakage current | C _{OUT} | V _O =0V~V _{CC} | - | - | 10 | μA |
| V _{CC} power supply current (Standby) | I _{CCSC} | $\overline{CE}=V_{CC}$ | - | - | 10 | μA |
| | I _{CCST} | $\overline{CE}=V_{IH}$ | - | - | 1 | mA |
| V _{CC} power supply current (Active) | I _{CCA} | $\overline{CE}=V_{IL}, \overline{OE}=V_{IH}$ tc= 100ns | - | - | 80 | mA |
| Input "H" level | V _{IH} | - | 2.0 | - | V _{CC} +0.5 | V |
| Input "L" level | V _{IL} | - | -0.5 | - | 0.8 | V |
| Output "H" level | V _{OH} | I _{OH} =-200 μA | V _{CC} -0.4 | - | - | V |
| Output "L" level | V _{OL} | I _{OL} =1mA | - | - | 0.4 | V |

Voltage is relative to V_{SS}

AC Characteristics

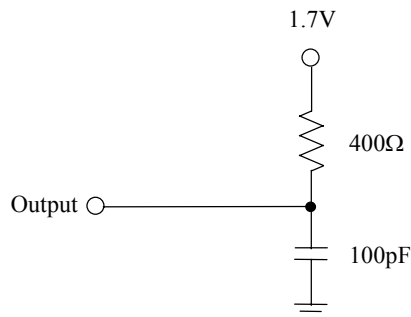
(V_{CC}=2.7V~3.6V, Ta=0~70°C)

| Parameter | Symbol | Condition | Min. | Min. | Unit |
|-----------------------------|-------------------|--------------------------------------|------|------|------|
| Address access cycle time | T _C | - | 100 | - | ns |
| Address access time | T _{ACC} | $\overline{CE}=\overline{OE}=V_{IL}$ | - | 100 | ns |
| Page set up time | T _{PSET} | NOTE.1 | 100 | - | ns |
| Page access cycle time | T _{PC} | - | 30 | - | ns |
| Page access time | T _{PAC} | - | - | 30 | ns |
| \overline{CE} access time | T _{CE} | $\overline{OE}=V_{IL}$ | - | 100 | ns |
| \overline{OE} access time | T _{OE} | $\overline{CE}=V_{IL}$ | - | 30 | ns |
| Output disable time | T _{CHZ} | $\overline{OE}=V_{IL}$ | 0 | 30 | ns |
| | T _{OHZ} | $\overline{CE}=V_{IL}$ | 0 | 25 | ns |
| Output hold time | T _{OH} | $\overline{CE}=\overline{OE}=V_{IL}$ | 0 | - | ns |

NOTE.1 T_{PSET} is defined as the end of either \overline{CE} falling edge or address transition in random access term until the first page address transition.

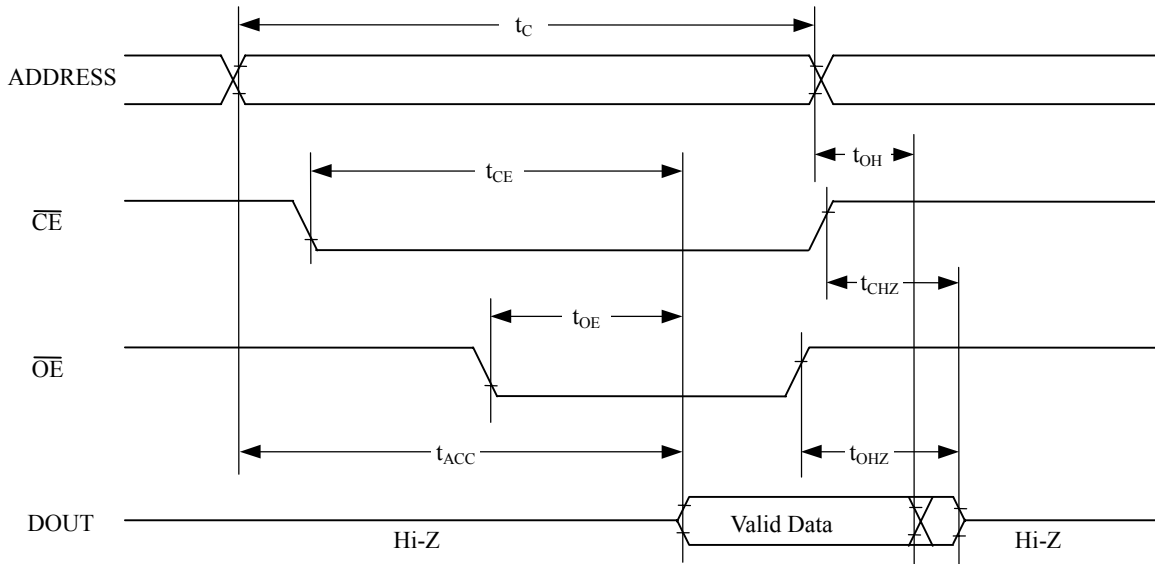
Measurement condition

- Input signal level 0V/3V
- Input timing reference level 0.8V/2.0V
- Output load 100pF
- Output timing reference level 0.8V/2.0V

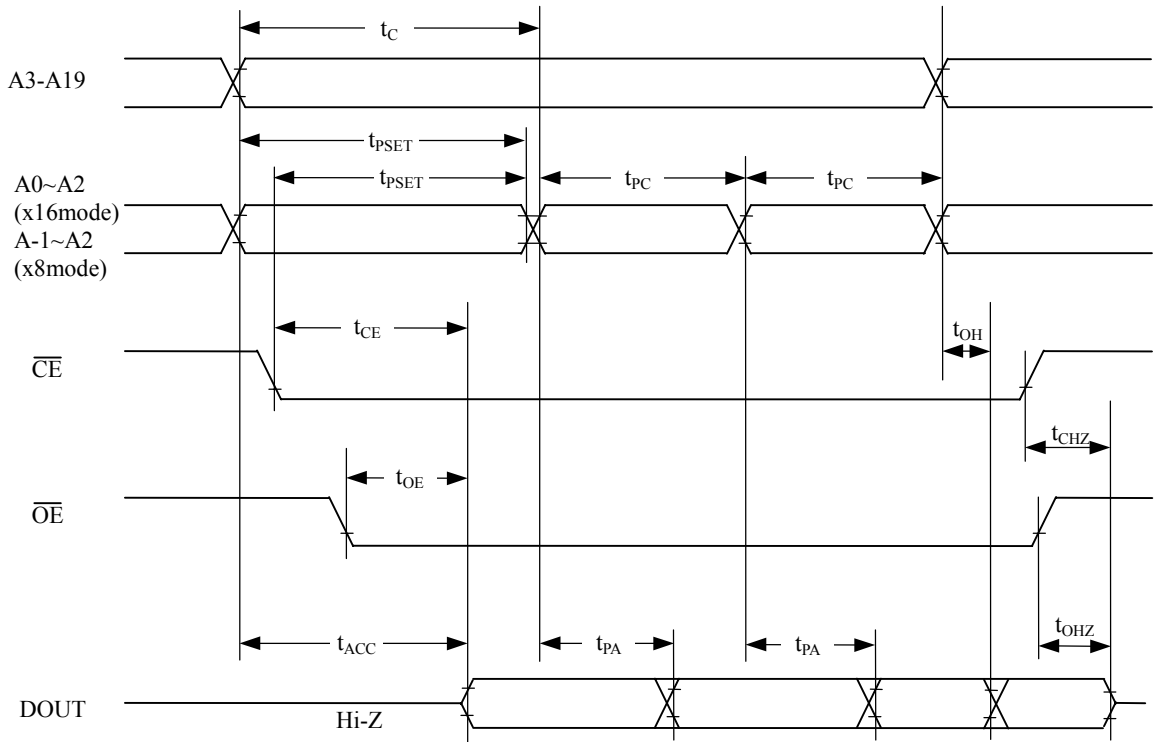


TIMING CHART

NORMAL MODE READ CYCLE



PAGE MODE READ CYCLE



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