

# OKI Semiconductor

## MSM514260E/ESL

Preliminary

**262,144-Word x 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE**

### DESCRIPTION

The MSM514260E/ESL is a 262,144-word × 16-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM514260E/ESL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM514260E/ESL is available in a 40-pin plastic SOJ, 44/40-pin plastic TSOP. The MSM514260ESL (the Self-refresh version) is specially designed for lower-power applications.

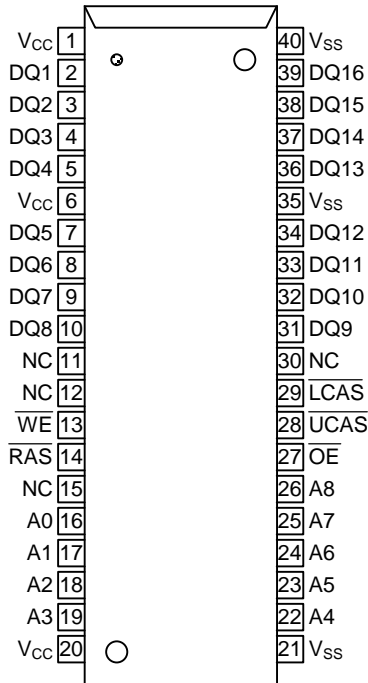
### FEATURES

- 262,144-word × 16-bit configuration
  - Single 5V power supply, ±10% tolerance
  - Input : TTL compatible, low input capacitance
  - Output : TTL compatible, 3-state
  - Refresh : 512 cycles/8 ms, 512 cycles/128 ms (SL version)
  - Fast page mode, read modify write capability
  - $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, hidden refresh,  $\overline{\text{RAS}}$ -only refresh capability
  - $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self-refresh capability (SL version)
  - Package options:
    - 40-pin 400mil plastic SOJ (SOJ40-P-400-1.27) (Product : MSM514260E/ESL-xxJS)
    - 44/40-pin 400mil plastic TSOP (TSOPII44/40-P-400-0.80-K) (Product : MSM514260E/ESL-xxTS-K)
- xx : indicates speed rank.

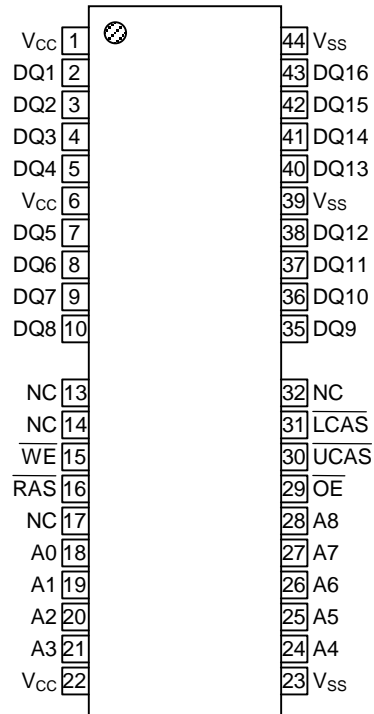
### PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>OEA</sub>		Operating (Max.)	Standby (Max.)
MSM514260E/ESL	60ns	30ns	15ns	15ns	110ns	633mW	5.5mW/
	70ns	35ns	20ns	20ns	130ns	578mW	1.1mW (SL version)

### PIN CONFIGURATION (TOP VIEW)



40-Pin Plastic SOJ

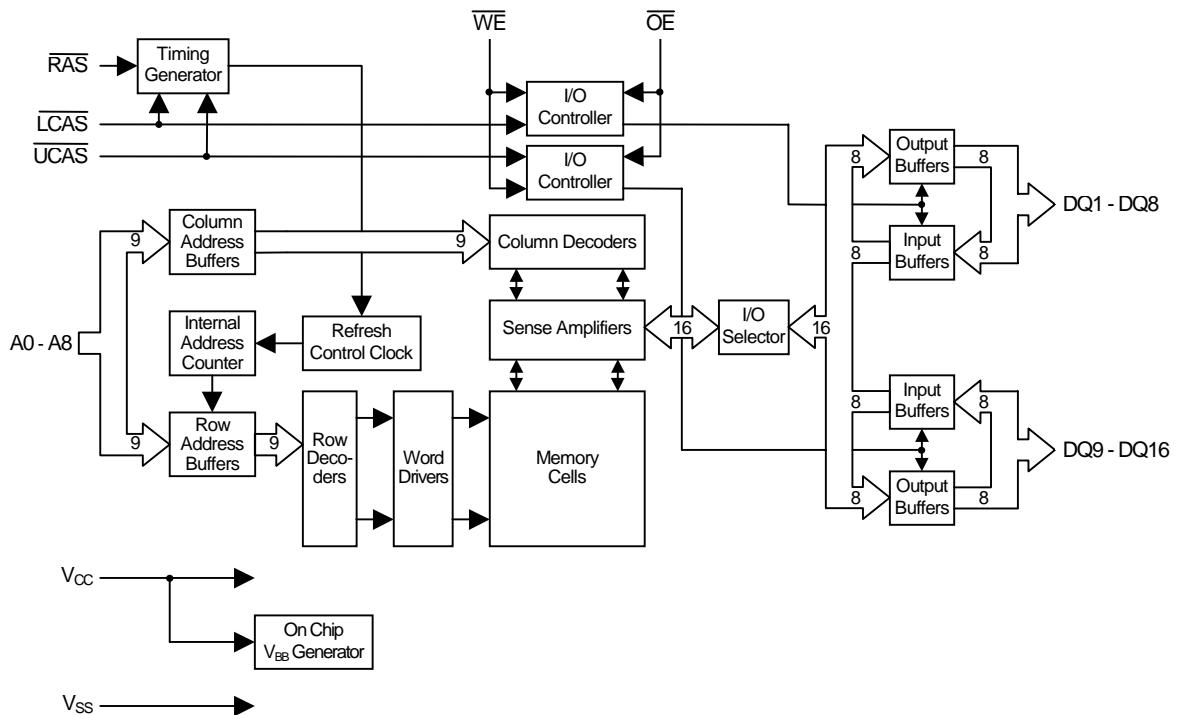


44/40-Pin Plastic TSOP  
(K Type)

Pin Name	Function
A0 – A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$	Lower Byte Column Address Strobe
$\overline{UCAS}$	Upper Byte Column Address Strobe
DQ1 - DQ16	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V <sub>CC</sub>	Power Supply (5V)
V <sub>SS</sub>	Ground (0V)
NC	No Connection

Note : The same power supply voltage must be provided to every V<sub>CC</sub> pin, and the same GND voltage level must be provided to every V<sub>SS</sub> pin.

### BLOCK DIAGRAM



### FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
RAS	LCAS	UCAS	WE	OE	DQ1-DQ8	DQ9-DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D <sub>OUT</sub>	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D <sub>OUT</sub>	Upper Byte Read
L	L	L	H	L	D <sub>OUT</sub>	D <sub>OUT</sub>	Word Read
L	L	H	L	H	D <sub>IN</sub>	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D <sub>IN</sub>	Upper Byte Write
L	L	L	L	H	D <sub>IN</sub>	D <sub>IN</sub>	Word Write
L	L	L	H	H	High-Z	High-Z	—

\* : "H" or "L"

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Voltage $V_{CC}$ supply Relative to $V_{SS}$	$V_{CC}$	-0.5 to 7.0	V
Short Circuit Output Current	$I_{OS}$	50	mA
Power Dissipation	$P_D^*$	1	W
Operating Temperature	$T_{opr}$	0 to 70	°C
Storage Temperature	$T_{stg}$	-55 to 150	°C

\*:  $T_a = 25^\circ\text{C}$

### Recommended Operating Conditions

( $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.4	—	$V_{CC} + 0.5^{*1}$	V
Input Low Voltage	$V_{IL}$	$-0.5^{*2}$	—	0.8	V

Notes: \*1. The input voltage is  $V_{CC} + 2.0\text{V}$  when the pulse width is less than 20ns (the pulse width is with respect to the point at which  $V_{CC}$  is applied).

\*2. The input voltage is  $V_{SS} - 2.0\text{V}$  when the pulse width is less than 20ns (the pulse width respect to the point at which  $V_{SS}$  is applied).

### Capacitance

( $V_{CC} = 5\text{V} \pm 10\%$ ,  $T_a = 25^\circ\text{C}$ ,  $f=1\text{MHz}$ )

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 – A8)	$C_{IN1}$	—	5	pF
Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{LCAS}}$ , $\overline{\text{UCAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	$C_{IN2}$	—	7	pF
Output Capacitance (DQ1 – DQ16)	$C_{I/O}$	—	7	pF

## DC Characteristics

( $V_{CC} = 5V \pm 10\%$ ,  $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Condition	MSM514260 E/ESL-60		MSM514260 E/ESL-70		Unit	Note
			Min.	Max	Min.	Max		
Output High Voltage	$V_{OH}$	$I_{OH} = -5.0\text{mA}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 4.2\text{mA}$	0	0.4	0	0.4	V	
Input Leakage Current	$I_{LI}$	$0V \leq V_I \leq V_{CC} + 0.5V$ ; All other pins not under test = $0V$	-10	10	-10	10	$\mu\text{A}$	
Output Leakage Current	$I_{LO}$	DQ disable $0V \leq V_O \leq V_{CC}$	-10	10	-10	10	$\mu\text{A}$	
Average Power Supply Current (Operating)	$I_{CC1}$	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ cycling, $t_{RC} = \text{Min.}$	—	115	—	105	mA	1,2
Power Supply Current (Standby)	$I_{CC2}$	$\overline{\text{RAS}}$ , $\overline{\text{CAS}} = V_{IH}$	—	2	—	2	mA	1
		$\overline{\text{RAS}}$ , $\overline{\text{CAS}} \geq$ $V_{CC} - 0.2V$	—	1	—	1	$\mu\text{A}$	1,5
Average Power Supply Current ( $\overline{\text{RAS}}$ -only Refresh)	$I_{CC3}$	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$ , $t_{RC} = \text{Min.}$	—	115	—	105	mA	1,2
Power Supply Current (Standby)	$I_{CC5}$	$\overline{\text{RAS}} = V_{IH}$ , $\overline{\text{CAS}} = V_{IL}$ , DQ = enable	—	5	—	5	mA	1
Average Power Supply Current ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	$I_{CC6}$	$\overline{\text{RAS}} = \text{cycling}$ , $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	115	—	105	mA	1,2
Average Power Supply Current (Fast Page Mode)	$I_{CC7}$	$\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ cycling, $t_{PC} = \text{Min.}$	—	115	—	105	mA	1,3
Average Power Supply Current (Battery Backup)	$I_{CC10}$	$t_{RC} = 125\mu\text{s}$ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ $t_{RAS} = 1\mu\text{s}$	—	300	—	300	$\mu\text{A}$	1,4, 5
Average Power Supply Current ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	$I_{CC8}$	$\overline{\text{RAS}} \leq 0.2V$ , $\overline{\text{CAS}} \leq 0.2V$ ,	—	300	—	300	$\mu\text{A}$	1,5

- Notes: 1.  $I_{CC}$  Max. is specified as  $I_{CC}$  for output open condition.  
 2. The address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .  
 3. The address can be changed once or less while  $\overline{\text{CAS}} = V_{IH}$ .  
 4.  $V_{CC} - 0.2V \leq V_{IH} \leq V_{CC} + 0.5V$ ,  $-0.5V \leq V_{IL} \leq 0.2V$ .  
 5. SL version.

**AC Characteristic (1/2)**(V<sub>CC</sub> = 5V ± 10%, Ta = 0°C to 70°C) Note1,2,3

Parameter	Symbol	MSM514260 E/ESL-60		MSM514260 E/ESL-70		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t <sub>RC</sub>	110	—	130	—	ns	
Read Modify Write Cycle Time	t <sub>RWC</sub>	155	—	185	—	ns	
Fast Page Mode Cycle Time	t <sub>PC</sub>	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t <sub>PRWC</sub>	85	—	100	—	ns	
Access Time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	—	60	—	70	ns	4,5,6
Access Time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	—	15	—	20	ns	4,5
Access Time from Column Address	t <sub>AA</sub>	—	30	—	35	ns	4,6
Access Time from $\overline{\text{CAS}}$ Precharge	t <sub>CPA</sub>	—	35	—	40	ns	4,12
Access Time from $\overline{\text{OE}}$	t <sub>OEA</sub>	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t <sub>CLZ</sub>	0	—	0	—	ns	4
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t <sub>OFF</sub>	0	15	0	15	ns	7
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t <sub>OEZ</sub>	0	15	0	15	ns	7
Transition Time	t <sub>T</sub>	3	50	3	50	ns	3
Refresh Period	t <sub>REF</sub>	—	8	—	8	ms	
Refresh Period (SL version)	t <sub>REF</sub>	—	128	—	128	ms	15
$\overline{\text{RAS}}$ Precharge Time	t <sub>RP</sub>	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t <sub>RAS</sub>	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t <sub>RASP</sub>	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t <sub>RSH</sub>	15	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t <sub>ROH</sub>	15	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t <sub>CP</sub>	10	—	10	—	ns	14
$\overline{\text{CAS}}$ Pulse Width	t <sub>CAS</sub>	15	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t <sub>CSH</sub>	60	—	70	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t <sub>CRP</sub>	5	—	5	—	ns	12
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t <sub>RHCP</sub>	35	—	40	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t <sub>RCD</sub>	20	45	20	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t <sub>RAD</sub>	15	30	15	35	ns	6
Row Address Set-up Time	t <sub>ASR</sub>	0	—	0	—	ns	
Row Address Hold Time	t <sub>RAH</sub>	10	—	10	—	ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	—	0	—	ns	11
Column Address Hold Time	t <sub>CAH</sub>	10	—	15	—	ns	11

**AC Characteristic (2/2)**(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0°C to 70°C) Note1,2,3

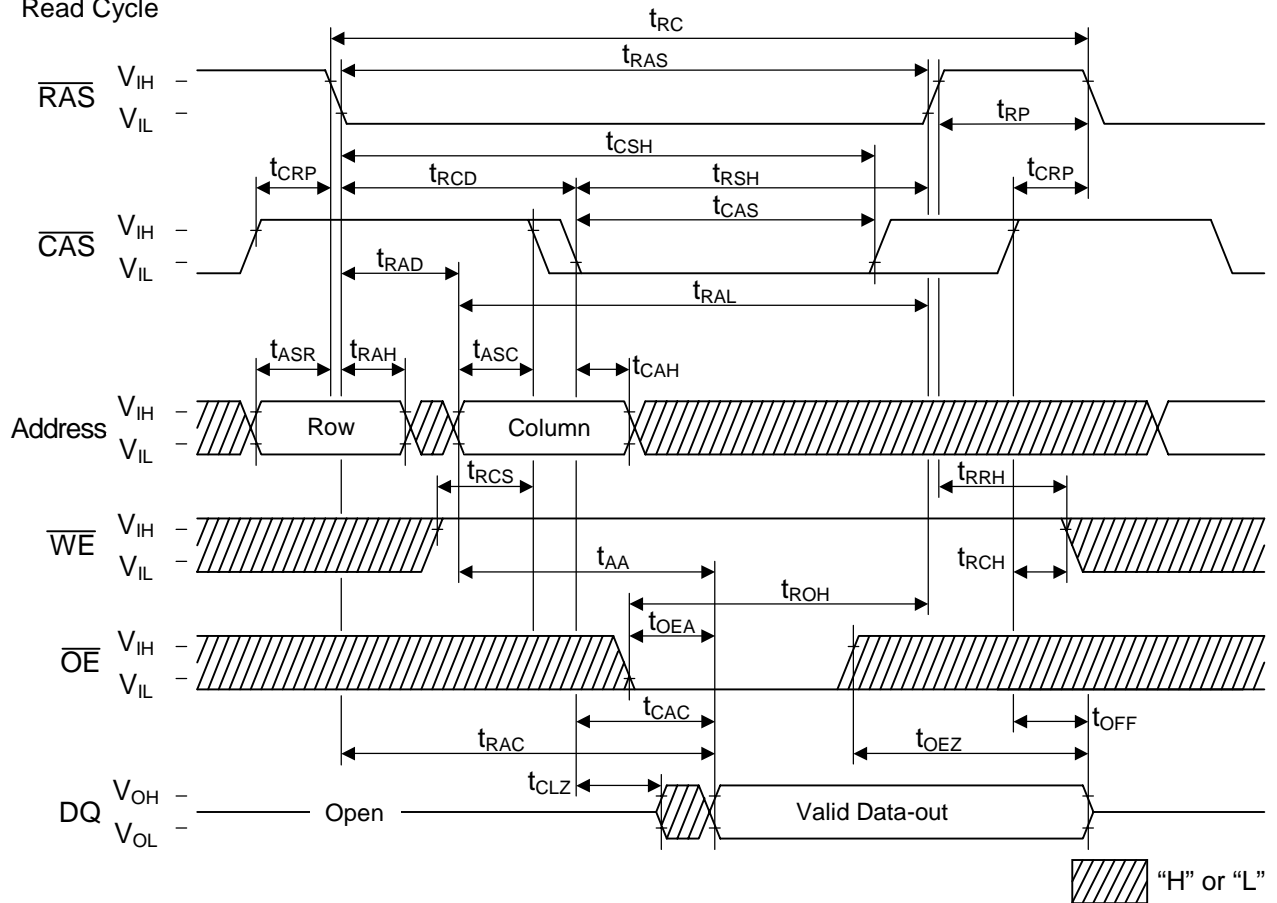
Parameter	Symbol	MSM514260 E/ESL-60		MSM514260 E/ESL-70		Unit	Note
		Min.	Max.	Min.	Max.		
Column Address to $\overline{\text{RAS}}$ Lead Time	t <sub>RAL</sub>	30	—	35	—	ns	
Read Command Set-up Time	t <sub>RCS</sub>	0	—	0	—	ns	11
Read Command Hold Time	t <sub>RCH</sub>	0	—	0	—	ns	8,11
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0	—	0	—	ns	8
Write Command Set-up Time	t <sub>WCS</sub>	0	—	0	—	ns	9,11
Write Command Hold Time	t <sub>WCH</sub>	10	—	15	—	ns	11
Write Command Pulse Width	t <sub>WP</sub>	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t <sub>OEH</sub>	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t <sub>RWL</sub>	15	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t <sub>CWL</sub>	15	—	20	—	ns	13
Data-in Set-up Time	t <sub>DS</sub>	0	—	0	—	ns	10,11
Data-in Hold Time	t <sub>DH</sub>	10	—	15	—	ns	10,11
$\overline{\text{OE}}$ to Data-in Delay Time	t <sub>oED</sub>	15	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>CWD</sub>	40	—	50	—	ns	9
Column Address to $\overline{\text{WE}}$ Delay Time	t <sub>AWD</sub>	55	—	65	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>RWD</sub>	85	—	100	—	ns	9
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t <sub>CPWD</sub>	60	—	70	—	ns	9
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t <sub>RPC</sub>	5	—	5	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CSR</sub>	10	—	10	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CHR</sub>	10	—	10	—	ns	12
$\overline{\text{RAS}}$ Pulse Width ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>RASS</sub>	100	—	100	—	μs	15
$\overline{\text{RAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>RPS</sub>	110	—	130	—	ns	15
$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>CHS</sub>	- 40	—	- 50	—	ns	15

- Notes:
1. A start-up delay of 200 $\mu$ s is required after power-up, followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh) before proper device operation is achieved.
  2. The AC characteristics assume  $t_T = 5\text{ns}$ .
  3.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring input timing signals. Transition times ( $t_T$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. This parameter is measured with a load circuit equivalent to 2 TTL load and 100pF.
  5. Operation within the  $t_{RCD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, then the access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, then the access time is controlled by  $t_{AA}$ .
  7.  $t_{OFF}$  (Max.) and  $t_{OEZ}$  (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.
  8.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  9.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$  (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}$  (Min.),  $t_{RWD} \geq t_{RWD}$  (Min.),  $t_{AWD} \geq t_{AWD}$  (Min.) and  $t_{CPWD} \geq t_{CPWD}$  (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
  10. These parameters are referenced to the  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ , leading edges in an early write cycle, and to the  $\overline{\text{WE}}$  leading edge in an  $\overline{\text{OE}}$  control write cycle, or a read modify write cycle.
  11. These parameters are determined by the falling edge of either  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ , whichever is earlier.
  12. These parameters are determined by the rising edge of either  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ , whichever is later.
  13.  $t_{CWL}$  should be satisfied by both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .
  14.  $t_{CP}$  is determined by the time both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  are high.
  15. Only SL version.

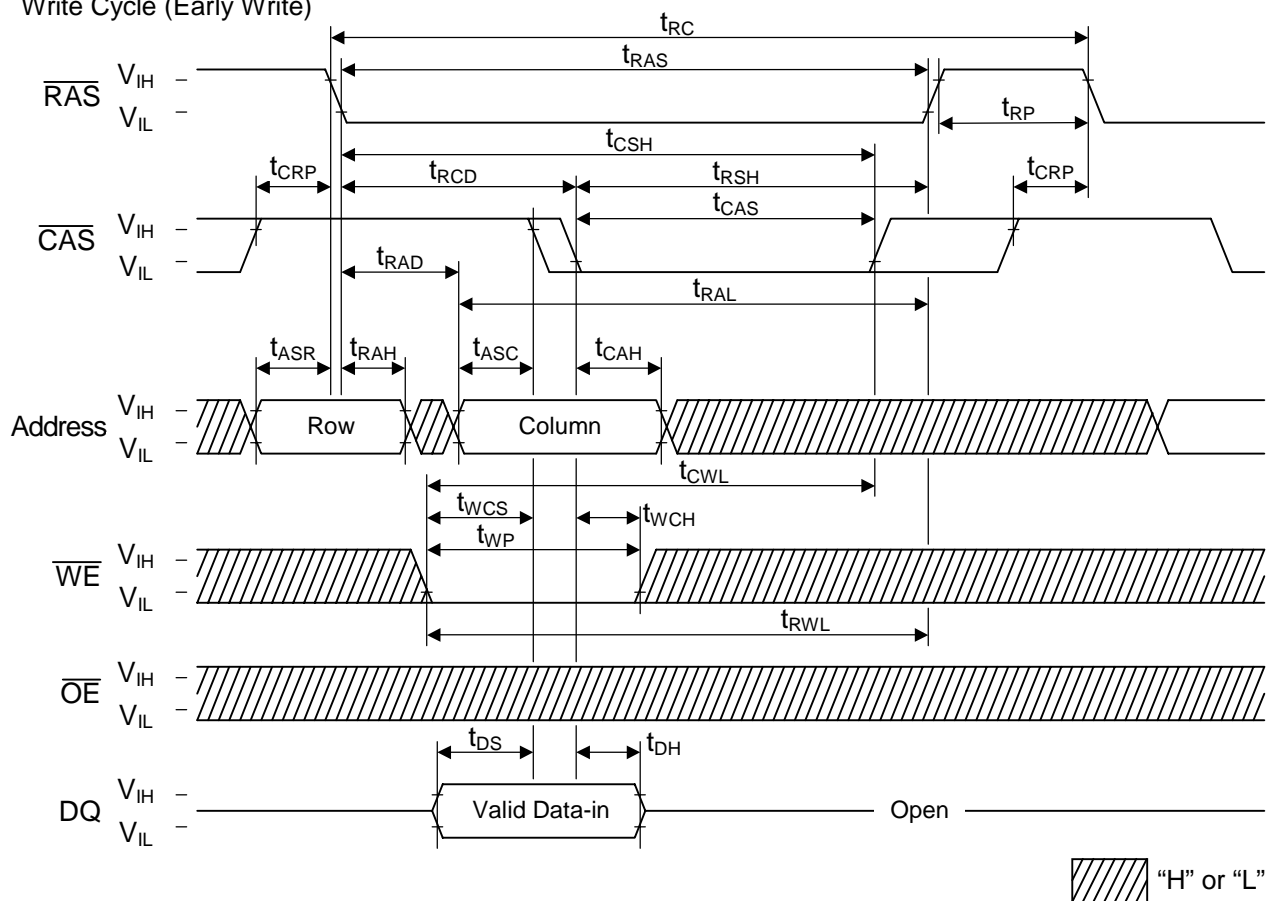


**Timing Chart**

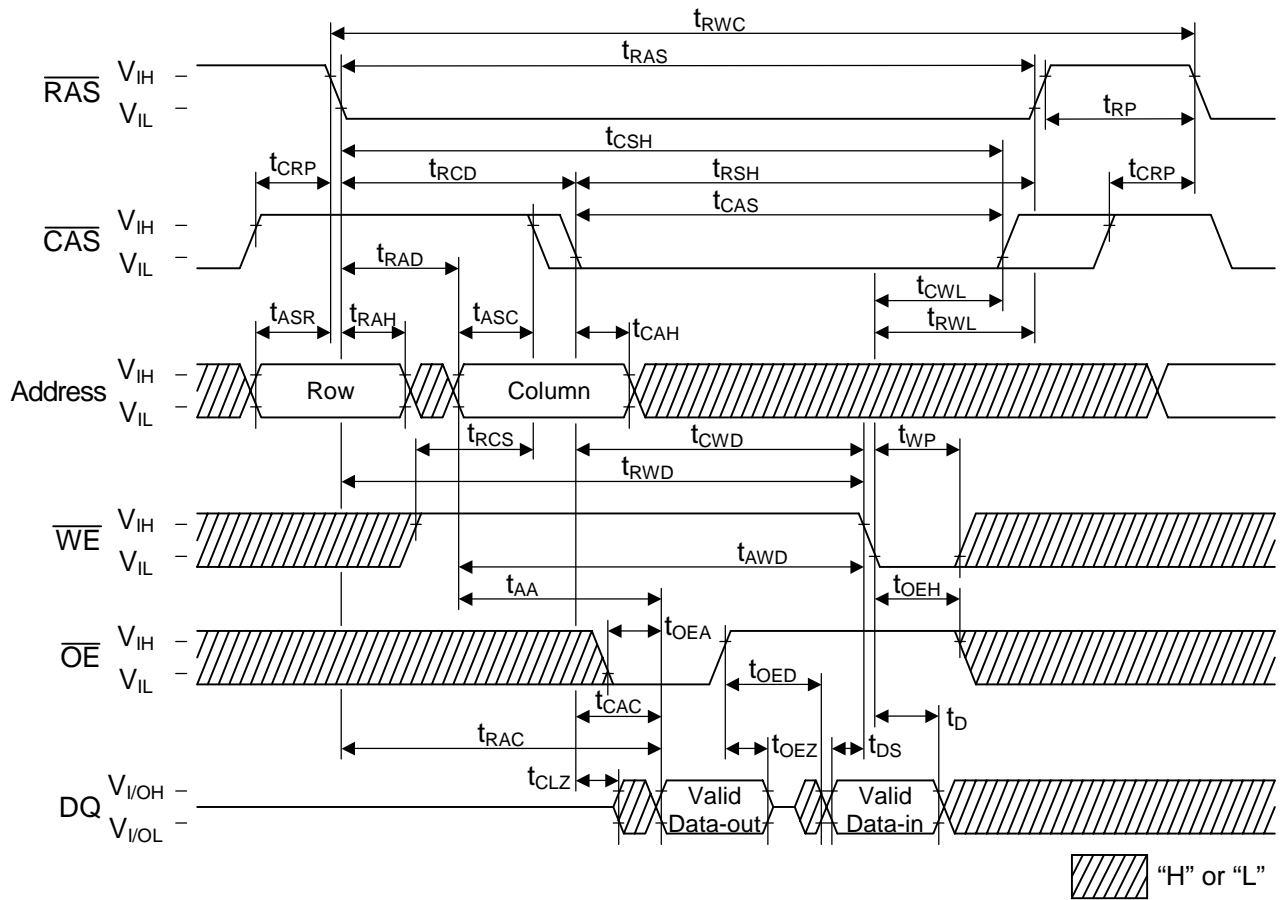
• Read Cycle



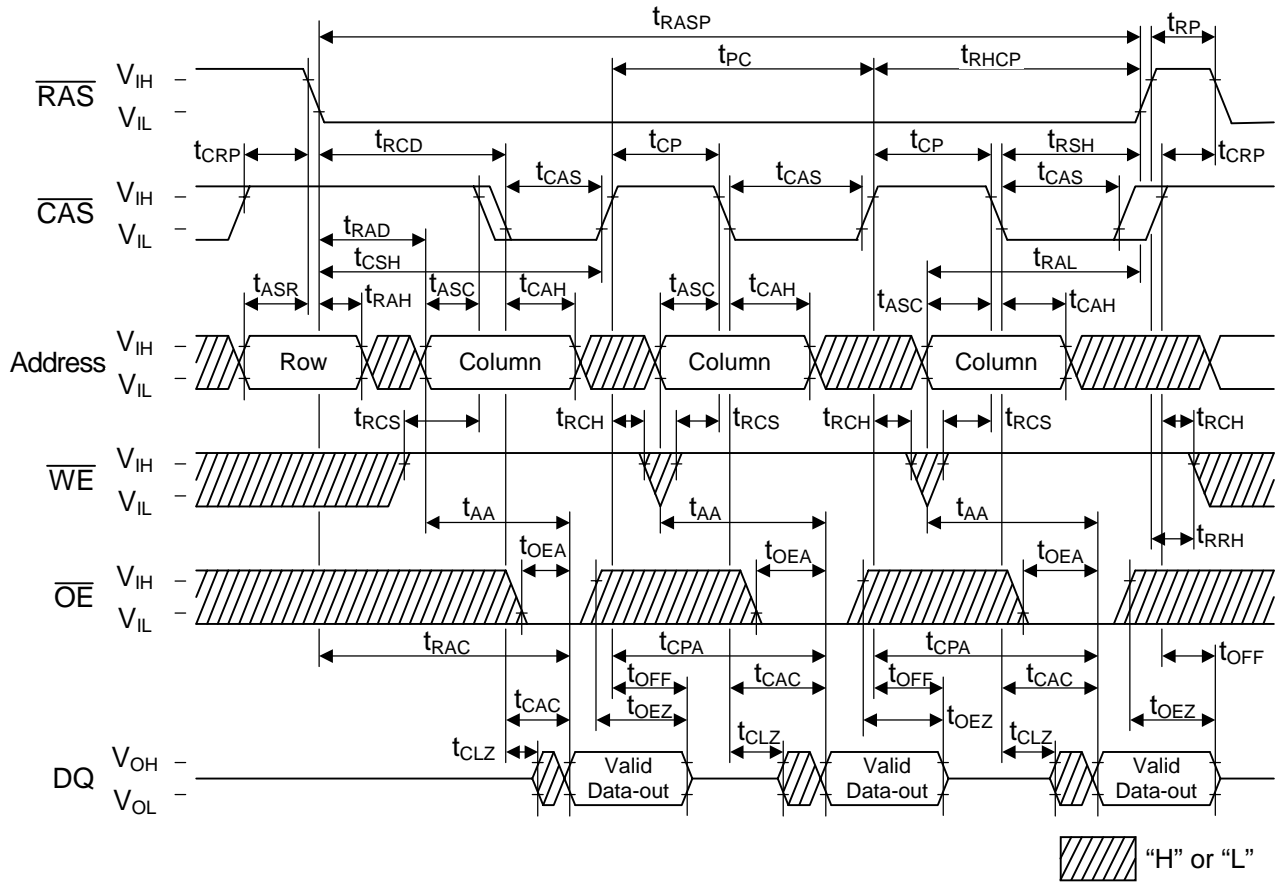
• Write Cycle (Early Write)



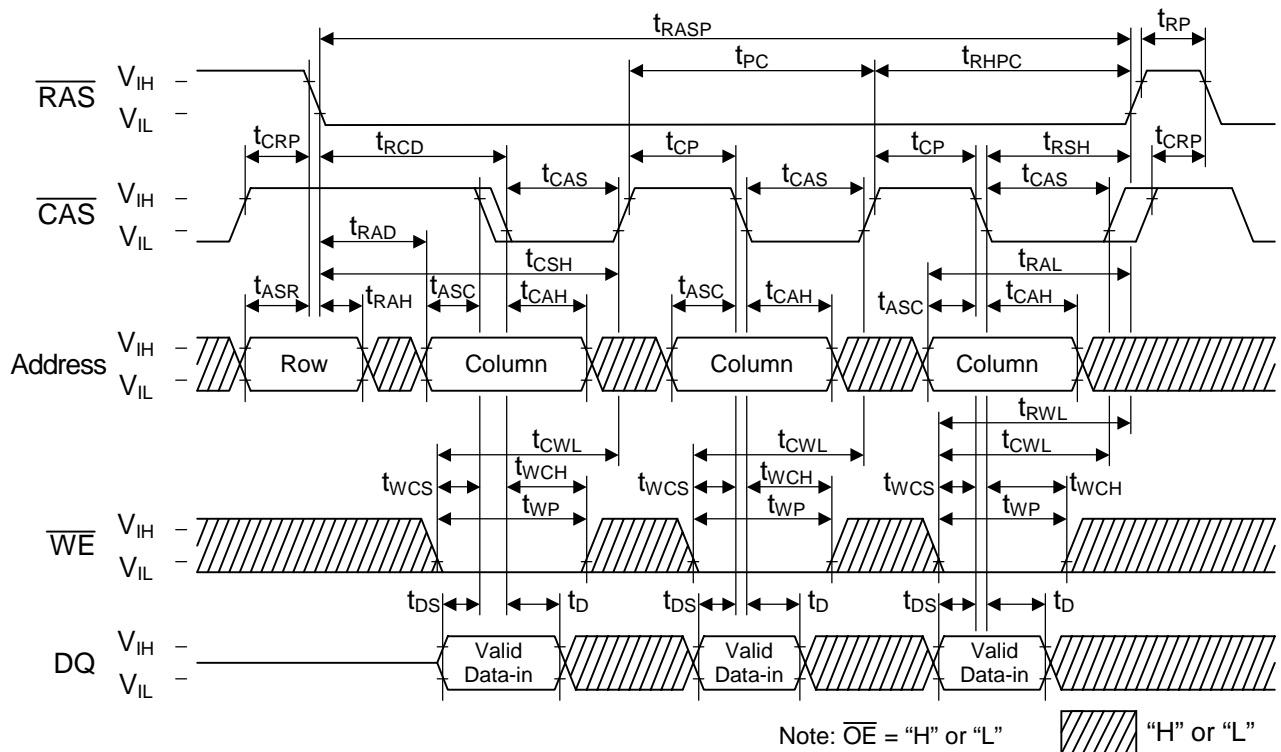
- Read Modify Write Cycle



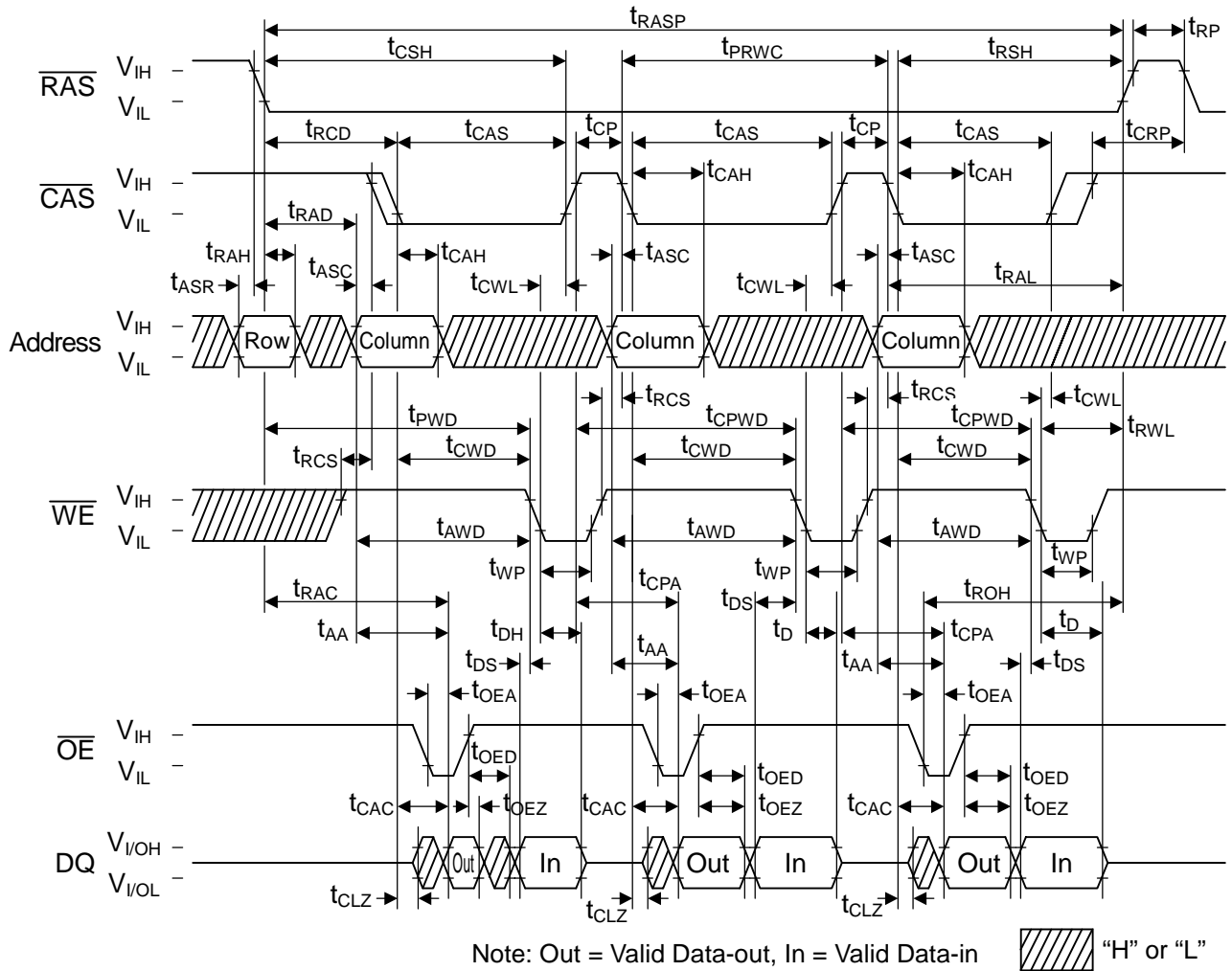
• Fast Page Mode Read Cycle



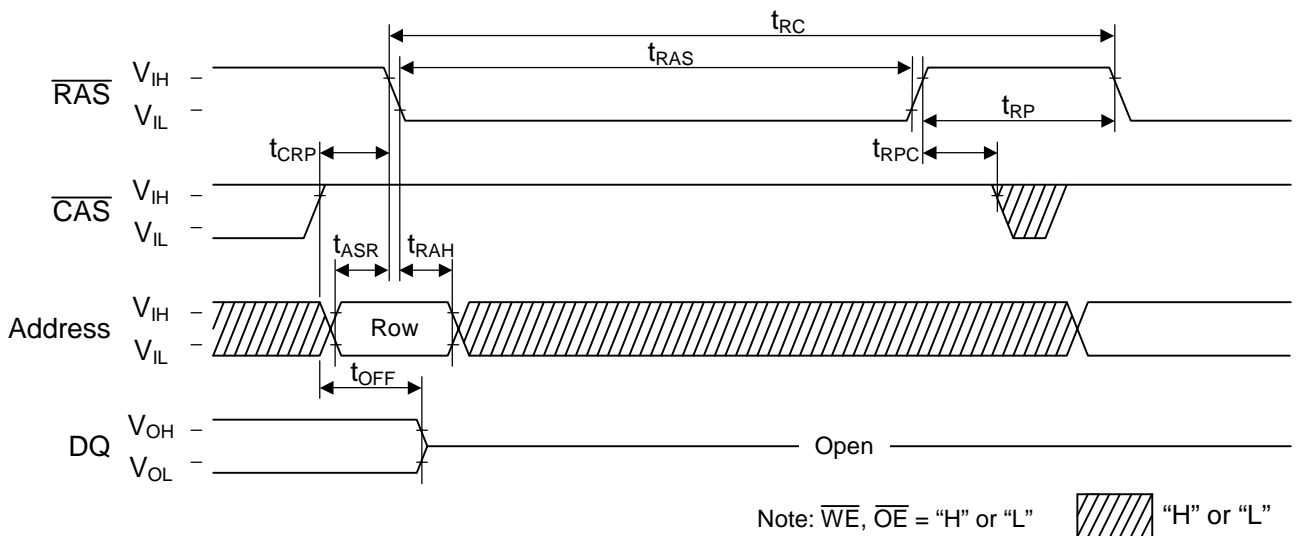
• Fast Page Mode Write Cycle (Early Write)



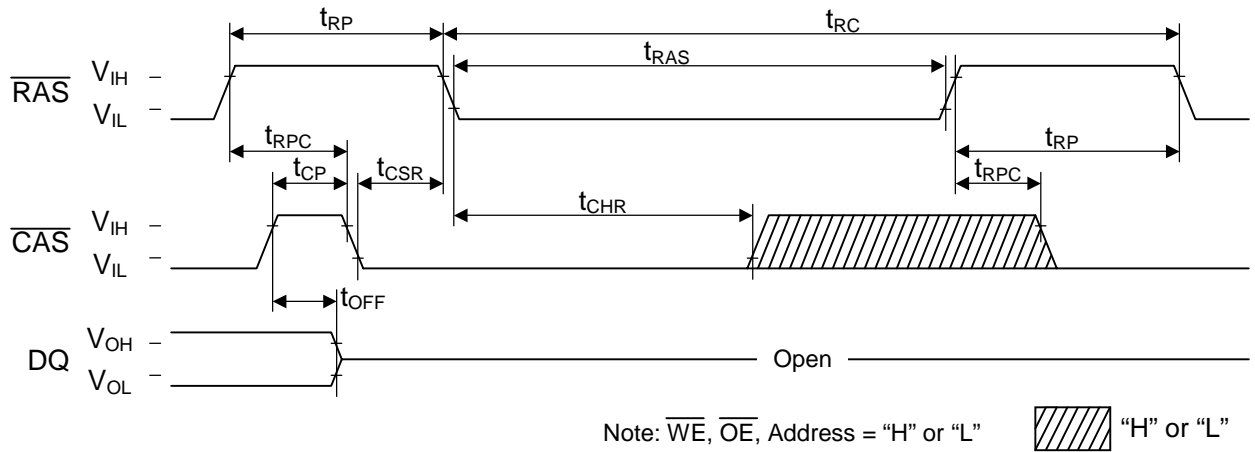
• Fast Page Mode Read Modify Write Cycle



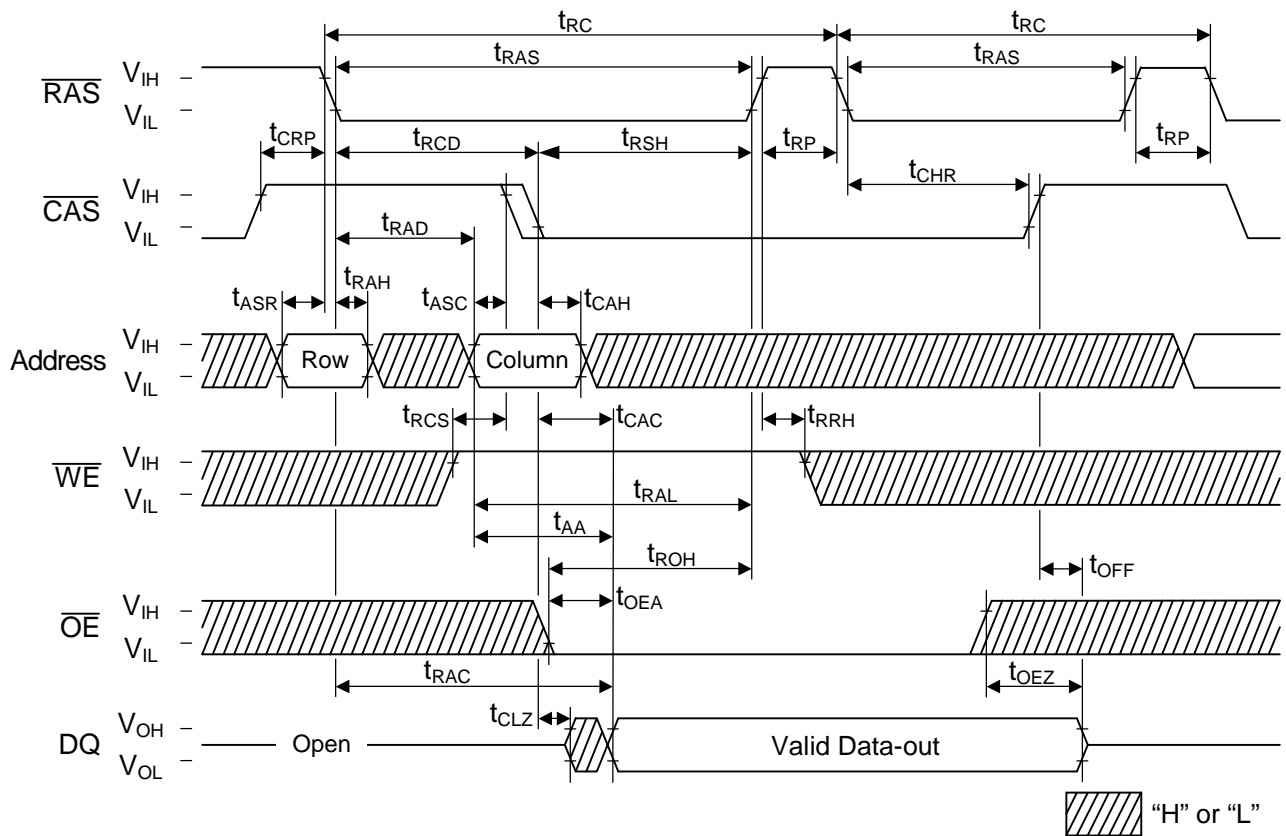
•  $\overline{\text{RAS}}$ -only Refresh Cycle



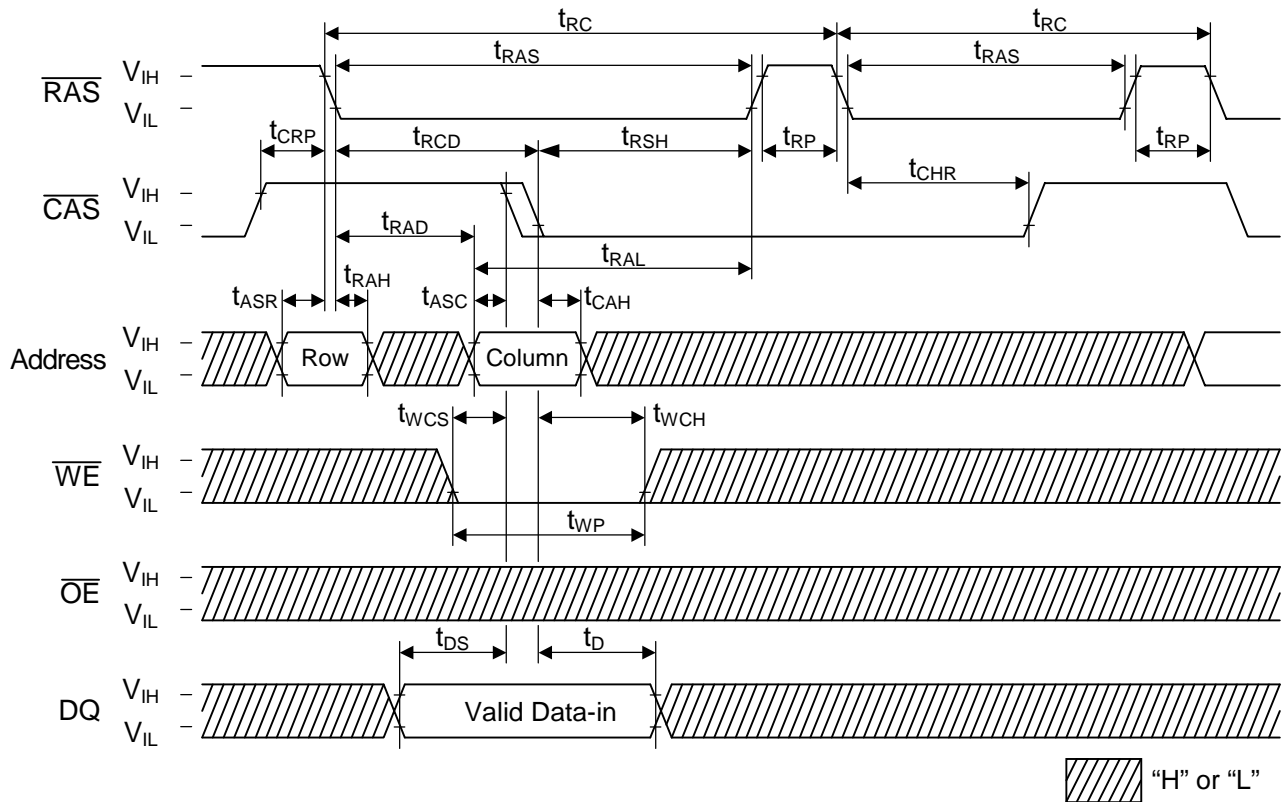
•  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Refresh Cycle



• Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Self-Refresh Cycle

