OKI Semiconductor

This version: Jan. 1998
Previous version: Mar. 1996

MSM6352

Built-in DTMF Generator 4-Bit Microcontroller

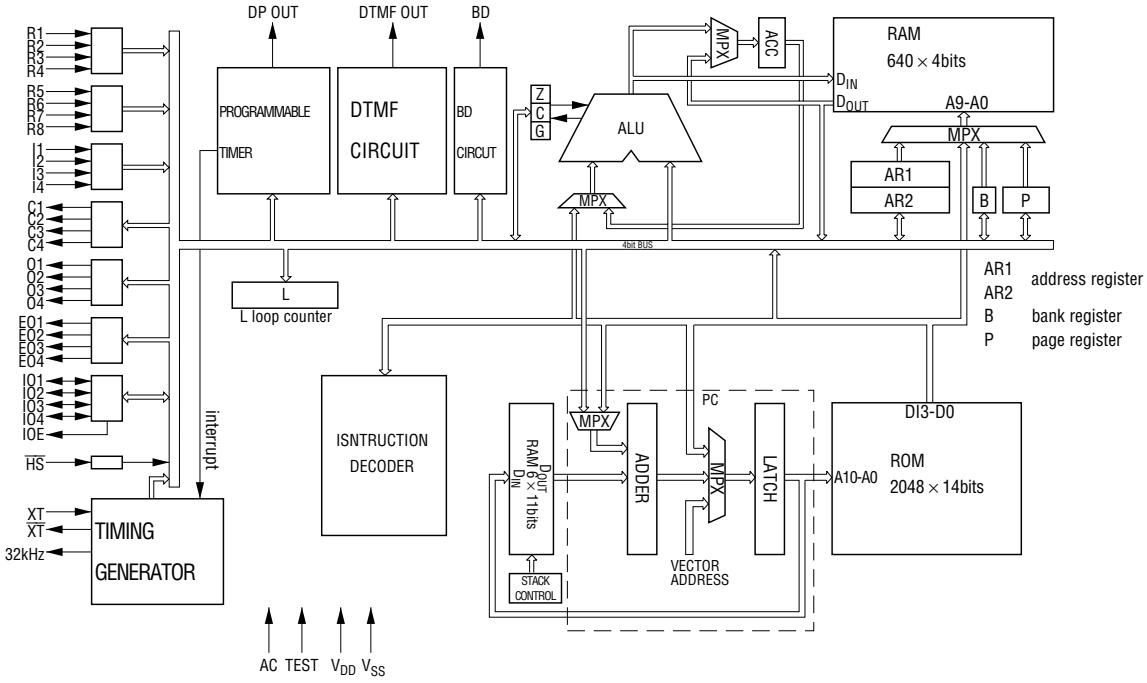
GENERAL DESCRIPTION

The MSM6352 is a high-performance 4-bit microcontroller employing complementary metal oxide semiconductor technology. The use of this device for a repertory telephone, which employed a conventional microcomputer that was difficult to be configured in a single-chip device, allows a compact and high-performance telephone set to be monufactured easily.

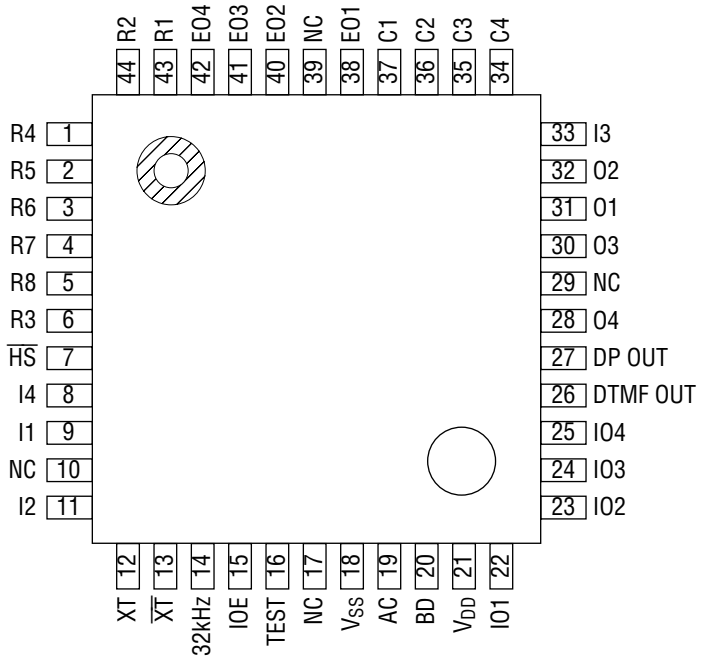
FEATURES

- Lower power consumption
- Mask ROM : 2048 × 14 bits
- ROM : 640 × 4 bits
- I/O port
  Input-output port : 1 port × 4 bits
  Input port : 3 ports × 4 bits
  Output port : 3 ports × 4 bits
- DTMF generator
- Built-in programmable timer
  Applicable for dial pulse output
  (Positive phase/negative phase, 34%/40%, 10 pps/20 pps selectable)
- Watch dog timer
- Stack : 5 Level
- Power down by STOP instruction
- Instructions useful for data management (data search and block data transfer)
- Operating voltage : 2.0 to 5.5V (2.2 to 5.5V in Tone mode)
- 3.58 MHz oscillator
- Instruciton execution time :17.9 µs
- Package options:
  28-pin plastic DIP (DIP28-P-600-2.54) : (Product name: MSM6352-××RS)
  40-pin plastic DIP (DIP40-P-600-2.54) : (Product name: MSM6352-××RS)
  42-pin plastic shrink DIP (SDIP42-P-600-1.78) : (Product name: MSM6352-××SS)
  44-pin plastic QFP (QFP44-P-910-0.80-K) : (Product name: MSM6352-××GS-K)
  44-pin plastic QFP (QFP44-P-910-0.80-2K) : (Product name: MSM6352-××GS-2K)
  ×× indicates the code number.

BLOCK DIAGRAM



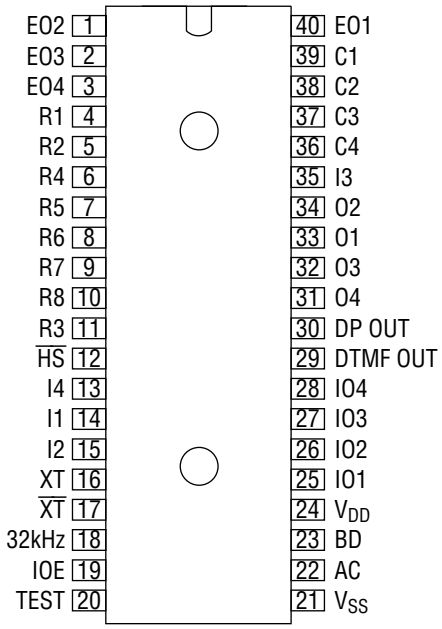
PIN CONFIGURATION (TOP VIEW)



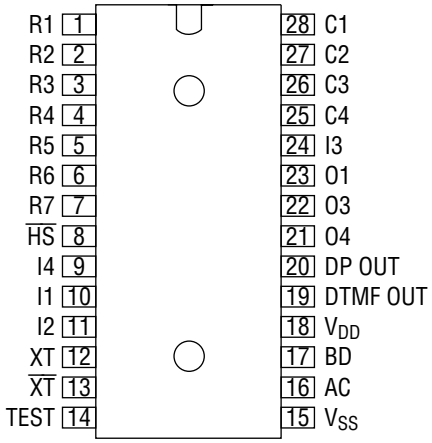
NC : No-connection pin

44-Pin Plastic QFP

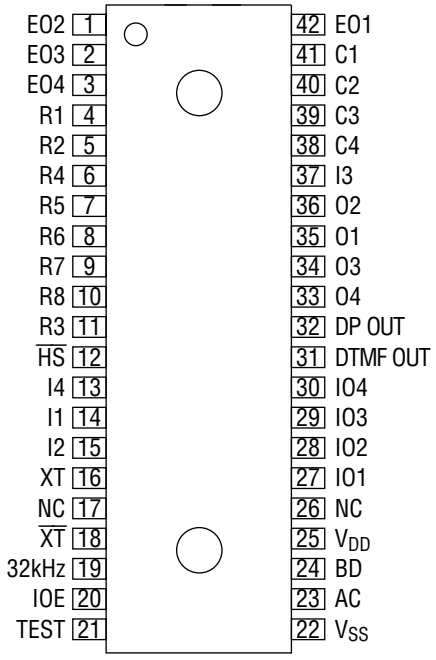
PIN CONFIGURATION (TOP VIEW) (Continued)



40-Pin Plastic DIP



28-Pin Plastic DIP



NC : No-connection pin

42-Pin Plastic Shrink DIP

PIN DESCRIPTIONS

Symbol	Description
V_{DD}	Power source
V_{SS}	Circuit ground potential
AC	Pin to clear internal logic, pulled down to V_{SS}. After power is turned on, the MSM6352 must be reset by this pin.
TEST	Pin to test internal logic, pulled down to V_{SS}. This pin must be open in normal operation.
XT, $\overline{XT}$	Input and output pins of oscillator inverter. 3.58 MHz ceramic resonator and capacitors is connedted to these pins.
$\overline{HS}$	Input pin connected to the hook switch, pulled up to V_{DD}.
DP OUT	Output pin of dial pulse Dial pulse rate (10 pps or 20 pps) and Make Break ratio (40% or 33%) can be selected by software.
DTMF OUT	Output pin of DTMF signal
BD	Output pin of buzzer sound
32 kHz	Output pin of 32 kHz clock
R_1 to R_4 R_5 to R_8	Input port pulled down to V_{SS}
I_1 to I_4	Input port having clocked pull-down resistor to V_{SS} Only when this port is accessed, pull-down resistors are connected to this port.
C_1 to C_4 O_1 to O_4	Output port
IO_1 to IO_4	Tri-state bidirectional port
IOE	Output pin When IO_1-IO_4 is accessed, input completion signal (when read) or load signal (when written) is output from IOE pin.

ABSOLUTE MAXIMUM RATINGS

V_{DD}=0 V (V_{SS1}=Battery Voltage)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	–0.3 to 6	V
Input Voltage	V_I		–0.3 to V_{DD}+0.3	
Output Voltage	V_O		–0.3 to V_{DD}+0.3	
Power Dissipation	P_D		200 max.	mW
Storage Temperature	T_{STG}	—	–55	°C

RECOMMENDED OPERATING CONDITIONS

V_{DD}=0 V (V_{SS1}=Battery Voltage)

Parameter	Symbol	Condition	Range	Unit
Operating Voltage	V_{DD}	Pulse Mode f_{OSC}=3.58 MHz	2.0 to 5.5*	V
Memory Retention Voltage	V_{DDM}	—	1.2 to 5.5	V
Operating Temperature	T_{op}	—	–20 to +75	°C

* During the time that tone sending is stopped.
During tone sending, 2.2 to 5.5 V.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta=–20 to +75°C)

Parameter	Symbol	Condition		Supply Voltage	Min.	Typ.	Max.	Unit	Measuring Circuit
"H" Output Current (1)	I_{OH1}	O_3, O_4	V_{OH}=2.6 V	3.0 V	–0.2	—	—	mA	1
"L" Output Current (1)	I_{OL1}	DP OUT	V_{OL}=0.4 V	3.0 V	0.5	—	—	mA	
"H" Output Current (2)	I_{OH2}		V_{OH}=2.6 V	3.0 V	–1.0	—	—	mA	
"L" Output Current (2)	I_{OL2}	C_1 to C_4	V_{OL}=0.4 V	3.0 V	10	—	—	µA	
"H" Output Current (3)	I_{OH3}	O_1, O_2	V_{OH}=2.6 V	3.0 V	–20	—	—	µA	
"L" Output Current (3)	I_{OL3}	BD	V_{OL}=0.4 V	3.0 V	10	—	—	µA	
"H" Output Current (4)	I_{OH4}	IO_1 to IO_4 IOE EO_1 to EO_4	V_{OH}=2.6 V	3.0 V	–150	—	—	µA	
"L" Output Current (4)	I_{OL4}		V_{OL}=0.4 V	3.0 V	300	—	—	µA	
"H" Output Current (5)	I_{OH5}	32 kHz	V_{OH}=2.6 V	3.0 V	–40	—	—	µA	
"L" Output Current (5)	I_{OL5}		V_{OL}=0.4 V	3.0 V	25	—	—	µA	
"H" Input Voltage	V_{IH}	—		3.0 V	2.2	—	—	V	2
				5.5 V	4.0	—	—		
"L" Input Voltage	V_{IL}	—		3.0 V	—	—	0.8	V	
				5.5 V	—	—	1.4		
"H" Input Current (1)	I_{IH1}	$\overline{HS}$	V_{IH}=5.5 V	5.5 V	—	—	2	µA	3
"L" Input Current (1)	I_{IL1}		V_{IL}=0 V	3.0 V	–20	—	–180	µA	
				5.5 V	–40	—	–360		
"H" Input Current (2)	I_{IH2}	R_1 to R_8	V_{IH}=5.5 V	5.5 V	20	—	180	µA	
			V_{IH}=3.0 V	3.0 V	10	—	90		
"L" Input Current (2)	I_{IL2}		V_{IL}=0 V	5.5 V	—	—	–2	µA	
"H" Input Current (3)	I_{IH3}	I_1 to I_4 AC, TEST	V_{IH}=5.5 V	5.5 V	60	—	600	µA	
			V_{IH}=3.0 V	3.0 V	30	—	300		
"L" Input Current (3)	I_{IL3}		V_{IL}=0 V	5.5 V	—	—	–2	µA	
"H" Input Current (4)	I_{IH4}	IO_1 to IO_4	V_{IH}=5.5 V	5.5 V	—	—	2	µA	
"L" Input Current (4)	I_{IL4}		V_{IL}=0 V	5.5 V	—	—	–2	µA	
Current Consumption (1)	I_{DDP}	While tone sending is stopped with no load		2.5 V	—	0.25	0.5	mA	4
				5.0 V	—	1.5	2.4		
Current Consumption (2)	I_{DDT}	During tone sending, with no load		2.5 V	—	1.3	2.4	mA	
				5.0 V	—	4.2	6.8		
Current Consumption (3)	I_{DDM}	On hook, Ta=25°C With no load		2.5 V	—	—	0.2	µA	

AC Characteristics

(Ta=–20 to +75°C)

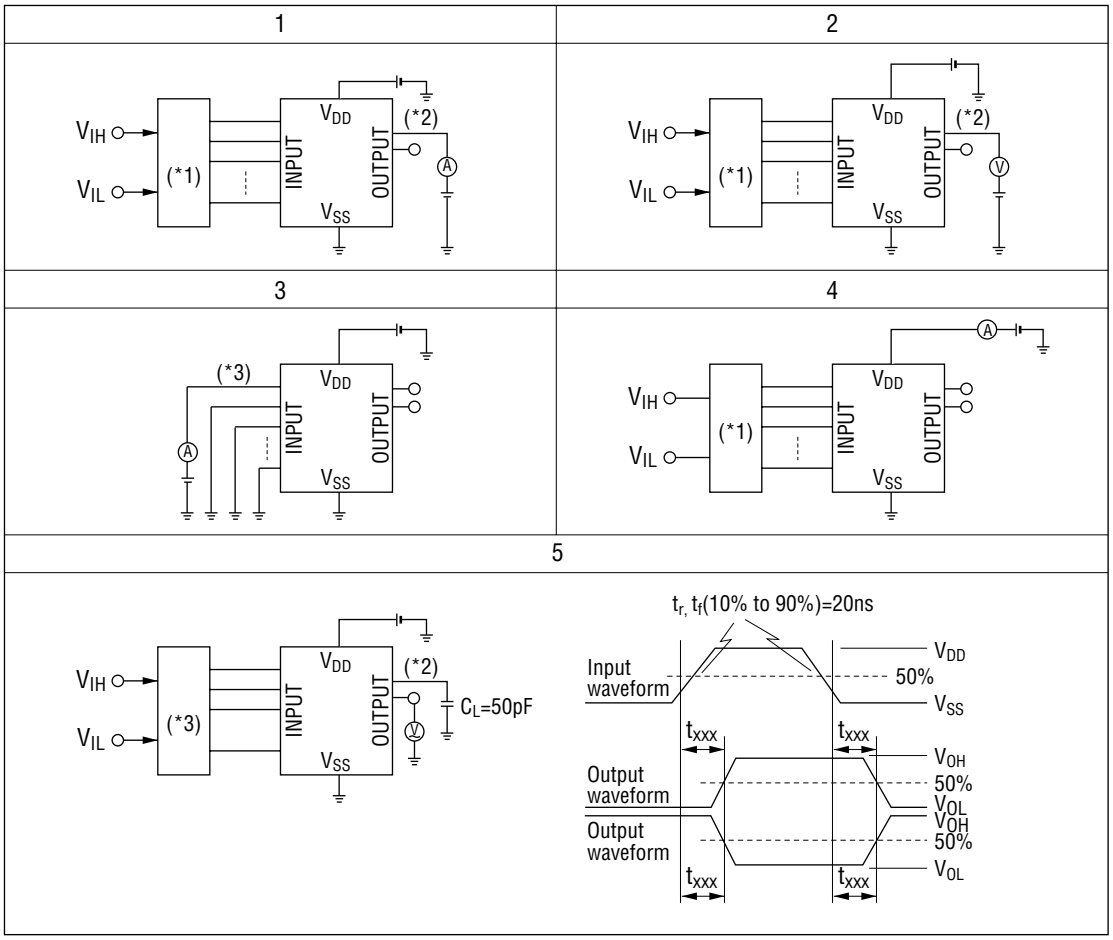
Parameter	Symbol	Conditions	Supply Voltage	Min.	Typ.	Max.	Unit	Measuring Circuit
Cycle Time	t_{CY}	f=3.579545 MHz	3.0 V	—	17.9	—	µs	
Tone Output	V_{OUT}	R_{ow} side only R_L=1 kΩ	2.2 V	—	180	—	mV rms	
			4.0 V	—	260	—		
			5.5 V	—	330	—		
High/Low Level Ratio	dB_{CR}	—	3.0 V	1	2	3	dB	
			5.5 V	1	2	3		
Distortion Ratio	$\%d_{IS}$	R_L=1 kΩ	3.0 V	—	—	5	%	
			5.5 V	—	—	5		
Switch Input Time	t_{KIN}	—	—	16	—	—	ms	5
Rise/Fall Time (1)	t_{TLH1}	O_3, O_4, DP OUT C_L=50 pF	3.0 V	—	—	0.5	µs	
	t_{THL1}		3.0 V	—	—	0.5		
Rise/Fall Time (2)	t_{TLH2}	C_1 to C_4 C_L=50 pF	3.0 V	—	—	0.5	µs	
	t_{THL2}		3.0 V	—	—	10		
Rise/Fall Time (3)	t_{TLH3}	O_1, O_2, BD, 32 kHz C_L=50 pF	3.0 V	—	—	5	µs	
	t_{THL3}		3.0 V	—	—	10		
Rise/Fall Time (4)	t_{TLH4}	IO_1 to IO_4, IOE EO_1 to EO_4, C_L=50 pF	3.0 V	—	—	1	µs	
	t_{THL4}		3.0 V	—	—	1		

DTMF Tone Output Frequency

	Reference Frequency (Hz)	Output Frequency (Hz)	Deviation (%)
R1	697	699.1	+0.30
R2	770	766.2	–0.49
R3	852	847.4	–0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	–0.32
C3	1477	1471.9	–0.35

f_{OSC}=3.579545 MHz

Measuring circuits



*1 Input logic to select a specified state.
*2 To be repeated for the specified output pin.
*3 To be repeated for the specified input pin.

FUNCTIONAL DESCRIPTION

Input Port (R_1-R_4)

Input only port that consists of 4 bits (R_1, R_2, R_3, R_4). The port status is determined by the input instruction. Each input pin, which is pulled down to V_{SS} (low level) through a resistor, can be used as a keyboard input pin.

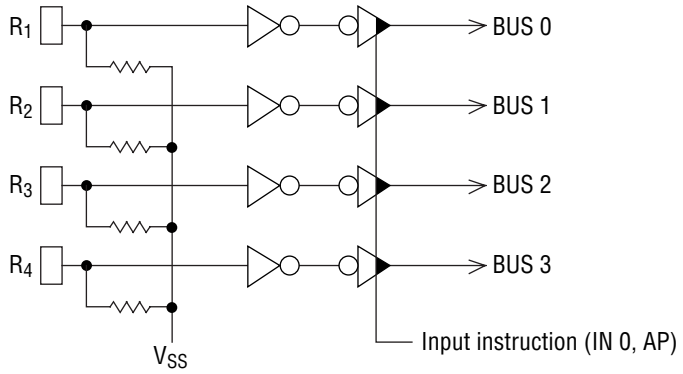


Figure 1. Input Port (R_1-R_4) Configuration

Input Port (R_5-R_8)

Input only port that consists of 4 bits (R_5, R_6, R_7, R_8). The port status is determined by the input instruction.

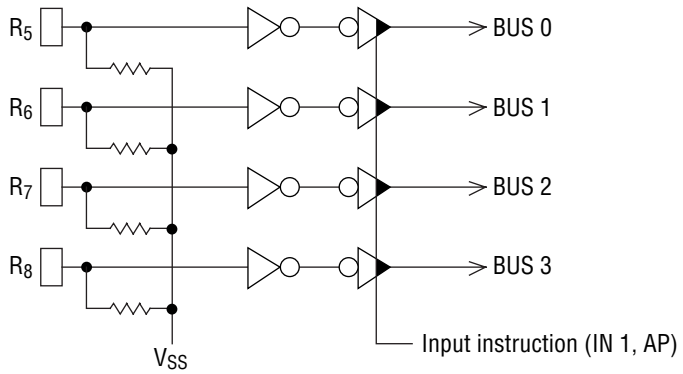


Figure 2. Input Port (R_5-R_8) Configuration

Input Port (I_1-$_4$)

Input only port that consists of 4 bits (I_1, I_2, I_3, I_4). The port status is determined by the input instruction. Each input pin is pulled down to V_{SS} (low level) through a transistor. The resistors are connected only when the port status is determined or a low level signal is input.
Since the input current is limited, this port can be fixed at high level (V_{DD}) for use.

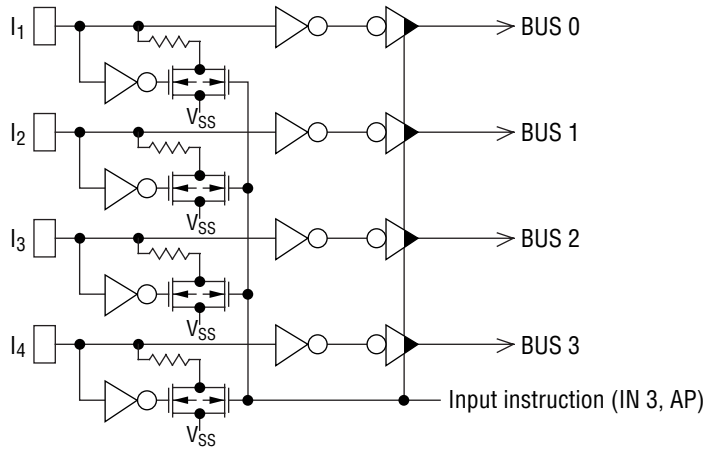


Figure 3. Input port (I_1-I_4) Configuration

$\overline{HS}$ Input Pin

$\overline{HS}$ 1-bit input pin, whose status can be fetched by the input instruction. It is pulled up to high level (V_{DD}) by a resistor and used as a hook switch input pin.

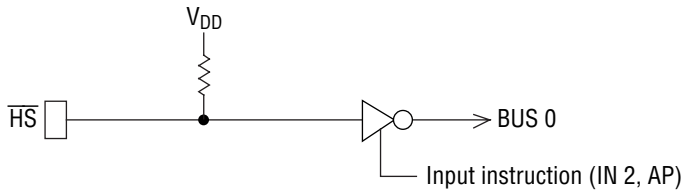


Figure 4. Configuration of $\overline{HS}$ Input Pin

Output Port (C_1-C_4)

Output only port that consists of 4 bits (C_1, C_2, C_3, C_4). The contents of the output latch can be rewritten by the output instruction.

A low level signal is output to each output pin at the time of the system reset.

When the $\overline{HS}$ input pin is open or at high level, a low level signal is output to each output pin irrespective of the contents of the output latch.

By setting this port to the enable state by the EC instruction, the contents of the output latch can be output to each output pin irrespective of the $\overline{HS}$ input pin status. The port goes into the disable state (the output depends on the $\overline{HS}$ input pin status) at the time of the system reset.

C_1 to C_4 are CMOS outputs.

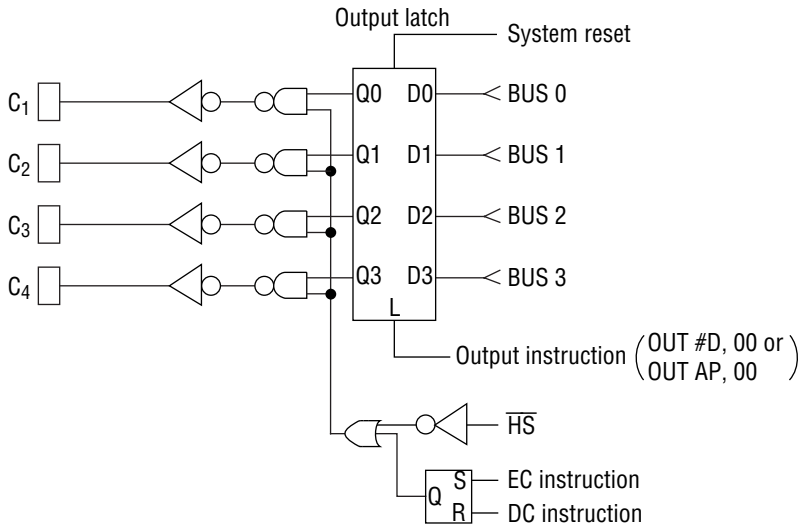


Figure 5. Output Port (C_1-C_4) Configuration

Output Port (O_1-O_4)

Output only port that consists of 4 bits (O_1, O_2, O_3, O_4). The contents of the output latch can be rewritten by the output instruction.

At the time of system reset, the output latch for O_1 and O_2 is reset and that of O_3 and O_4 is set.

When the $\overline{HS}$ input pin is open or at high level, a low level signal is output to the O_3 and O_4 output pins, allowing the contents of the output latch for O_3 and O_4 to be output to each output pin, if EOF, the selection flag for the on-hook dialing and off-hook dialing, is reset.

When EOF is set, the contents of the output latch for O_3 and O_4 can be rewritten irrespective of the $\overline{HS}$ input pin status.

O_1 to O_4 are CMOS outputs.

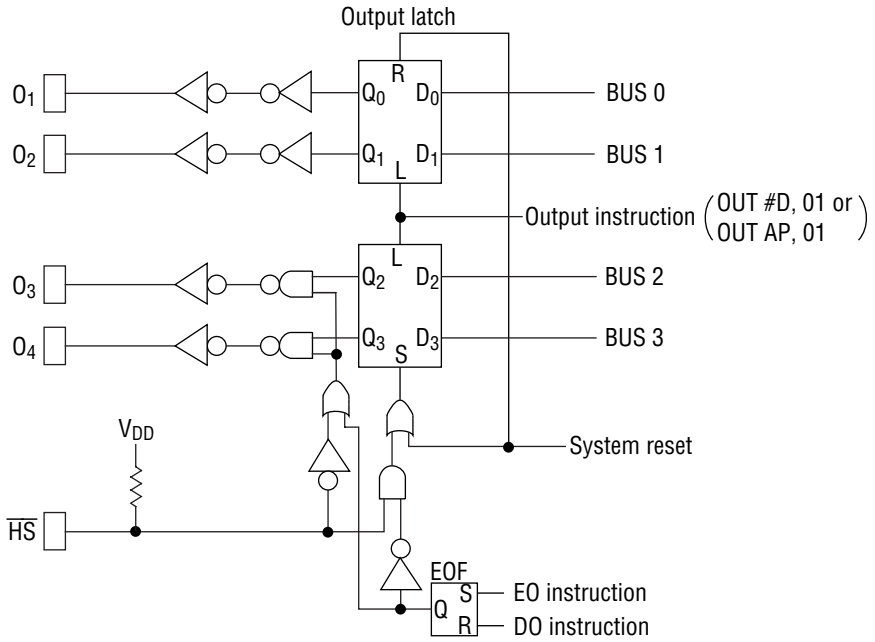


Figure 6. Output Port (O_1-O_4) Configuration

Output Port (EO_1-EO_4)

Output only port that consists of 4 bits (EO_1, EO_2, EO_3, EO_4). The contents of the output latch can be rewritten by the output instruction.
A low level signal is output to each output pin at the time of the system reset.
EO_1 to EO_4 are CMOS outputs.

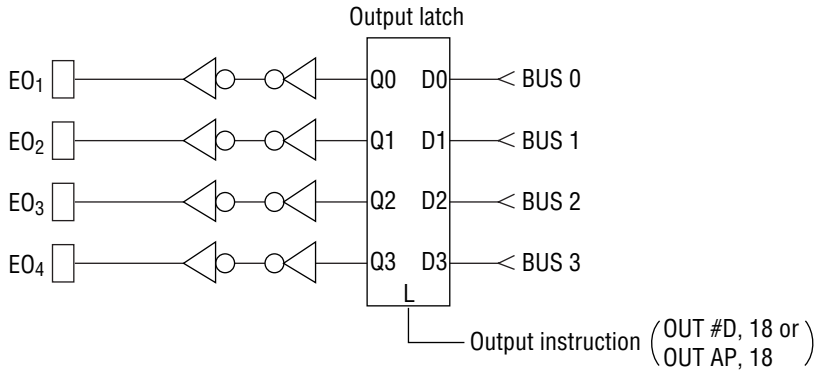


Figure 7. Output Port (EO_1-EO_4) Configuration

Input/Output Port (IO_1~IO_4)

Input-output port that consists of 4 bits (IO_1, IO_2, IO_3, IO_4). The port status is determined and the output latch is rewritten by the input-output instruction.
This port goes into the output by the OM instruction and the input mode by the IM instruction. During the input mode, each pin is at a high impedance state irrespective of the contents of the output latch.
At the time of the system reset, this port enters output mode and a low level signal is output to each pin.
During the output mode, IO1 to IO4 are CMOS at outputs.

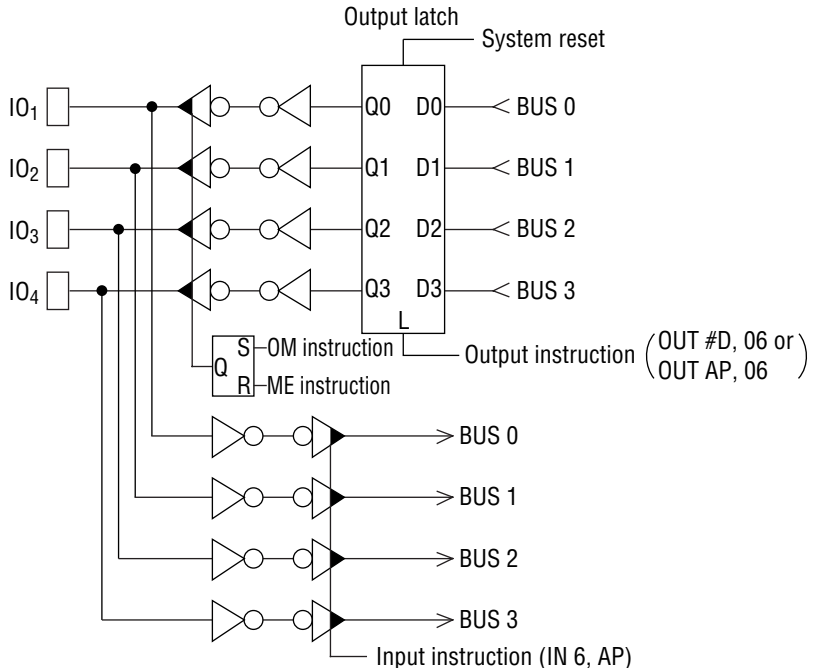


Figure 8. Input-Output Port (IO_1~IO_4) Configuration

IOE Output Pin

IOE is 1-bit output pin. A load signal is output at this pin when the output latch's (IO_1 to IO_4) contents are rewritten.
IOE is CMOS output.

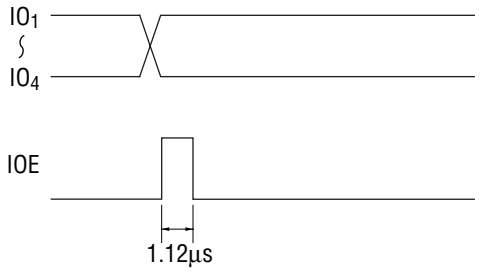


Figure 9. IOE Output Timing

DTMF Output Pin

DTMF output pin to output DTMF signals. Start and stop of the DTMF output are done by the output instruction.

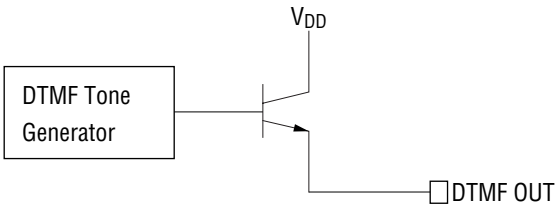


Figure 10. DTMF Output Pin Configuration

DP Output Pin

Dial pulse output pin. Start and stop of the dial pulse output can be done by the output instruction.

When "1" is written to the output latch for O_3 of output port (O_1, O_2, O_3, O_4), a low level signal is always output tot he DP OUT pin even if dial pulse output is started, if the EOF flag for the programmable timer is reset and the off-hook dial mode is selected.

When the EOF flag is set and the on-hook dial mode is selected, dial pulses can be output irrespective of the contents of the latch for O_3.

DP OUT is CMOS output.

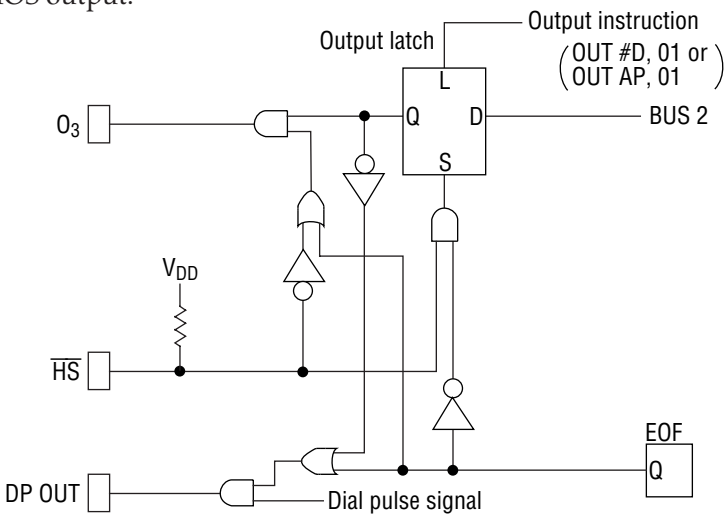


Figure 11. DP Output Pin Configuration

BD Output Pin

BD output pin for the buzzer output. The buzzer output can be started and stopped by the output instruction. BD is CMOS output.

32 kHz Output Pin

It is an output pin to output 31.960 kHz clock (duty: 50%) which is obtained by dividing the 3.579545 MHz system clock by 112. This clock outputs as long as the system clock is in oscillation.

32 kHz output pin is CMOS output.

XT, $\overline{XT}$ Pins

These are input and output pins of the oscillator inverter, and the oscillator circuit is provided with the built in feed back resistor. By connecting to them oscillation of system clock status.

3.579545 MHz ceramic resonator and capacitors.

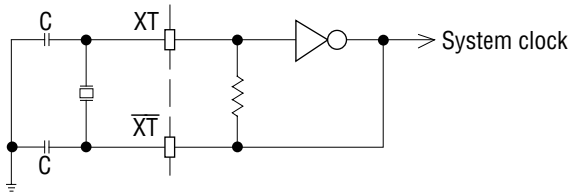


Figure 12. Oscillator Circuit

AC input pin

Input pin for system reset. This pin is pulled down to V_{SS} (low level) through a resistor. When a high level (V_{DD}) signal is input to this pin, the system clock starts oscillation. If this pin is held at the high level for more than 1 machine cycle after the oscillation has gone into the stationary state, the internal state is reset. While a high level signal is applied to the AC pin, the execution of the instruction stored at address 0H is repeated. The system reset is released 0 to 17.9 microseconds after the AC pin is opened, and then the PC is incremented by 1.

Note that the following cannot be stored at address 0H: RDAR instruction, MVAR instruction, subroutine instructions, jump instructions, and branch instructions.

An AC input takes precedence over any other signal and has the following functions:

- Resets all the bits in the program counter to "0".
- Resets the output latch for the output port (C_1-C_4) to "0" and puts it into the disable (the output depends on the HS input pin status) state.
- Resets the output latch for O_1 and O_2 of the output port and sets the output latch for O_3 and O_4 to "1".
- Resets the output latch for the output port (EO_1-EO_4) to "0".
- Puts the input-output port (IO_1-IO_4) into output mode and resets the output latch.
- Resets the ETAF and TMF of the timer start circuit and realtime interrupt circuit to "0".
- Resets the 1/100 dividing circuit, PTC, IRQF, EIF, EOF and DPF of the programmable timer to "0".
- Resets the ETAF, TMF, and ACTF of the halt mode release control circuit and sets the HSTF to "1".
- Resets the HSF1, HSF2, and RF of the stop mode release control circuit to "0" and sets the HSTF to "1".
- Stops the watchdog timer.
- Resets the DTMF register of the DTMF output circuit to "0" and sets the HSTF to "1".
- Resets the BD register of the BD output circuit to "0".

The contents of the accumulator (ACC), condition flags (Z, C, G), bank register (B), page register (P), address registers (AR_1, AR_2), loop counter (L), dividing circuit (DIV), and RAM are undefined.

TEST input pin

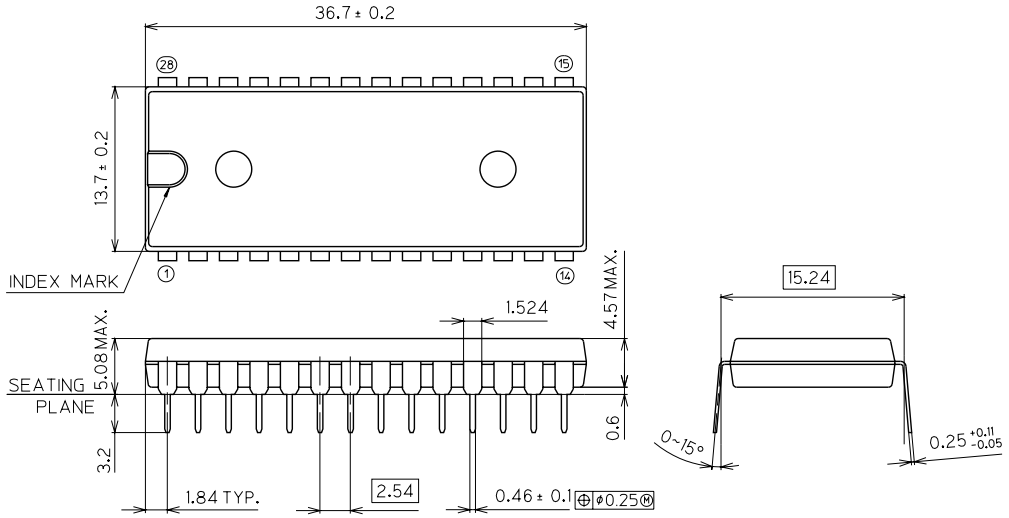
Input pin for IC testing. This pin is pulled down to V_{SS} (low level) through a resistor and used to test the internal logic circuits of the IC during manufacturing process.

Connect this pin to V_{SS}.

PACKAGE DIMENSIONS

(Unit : mm)

DIP28-P-600-2.54



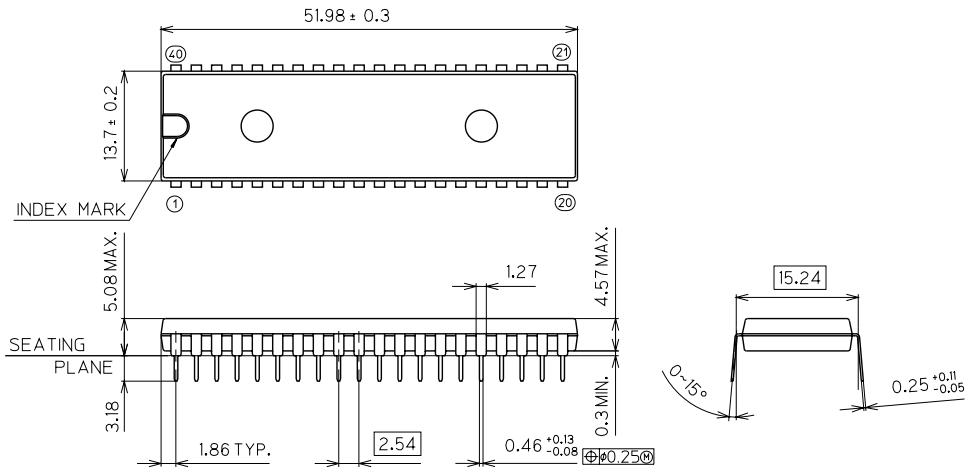
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	4.30 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

DIP40-P-600-2.54



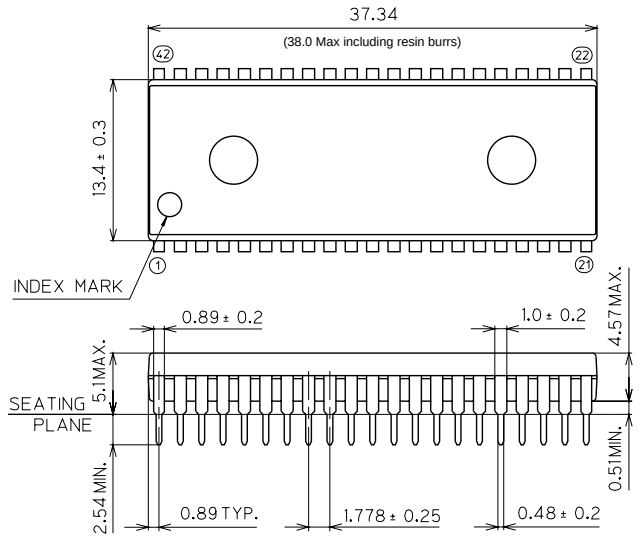
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	6.10 TYP.

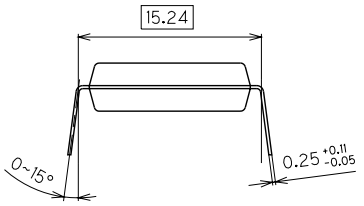
Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

SDIP42-P-600-1.78





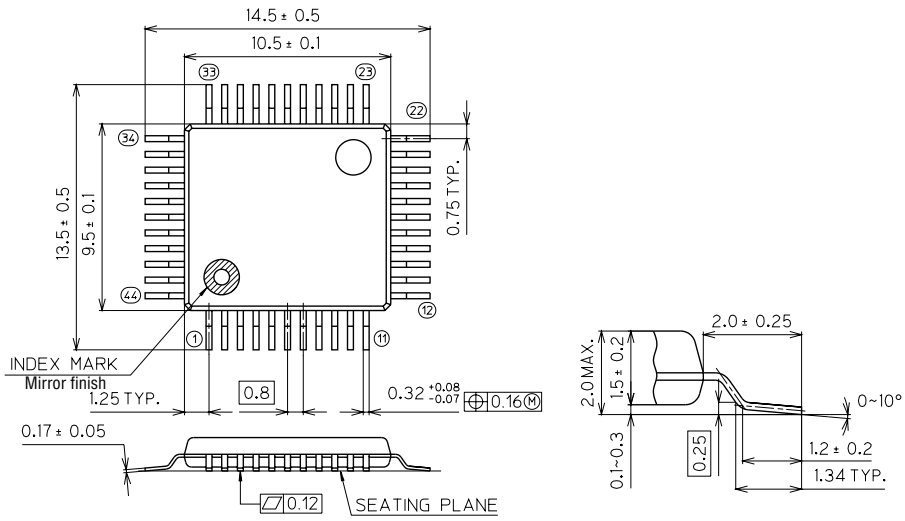
Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	4.50 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP44-P-910-0.80-K



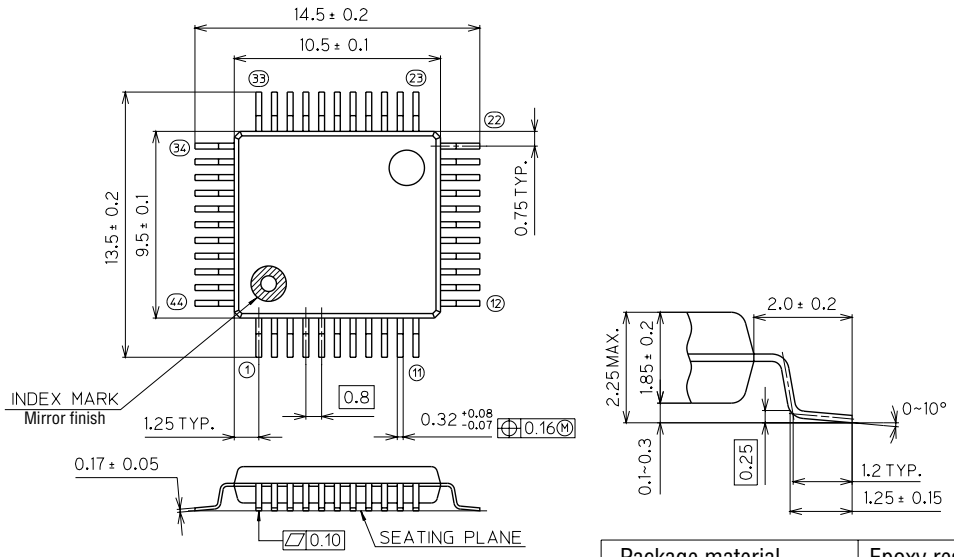
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.35 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).