OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM65512A/65P512A

High Performance 8-Bit Microcontroller

GENERAL DESCRIPTION

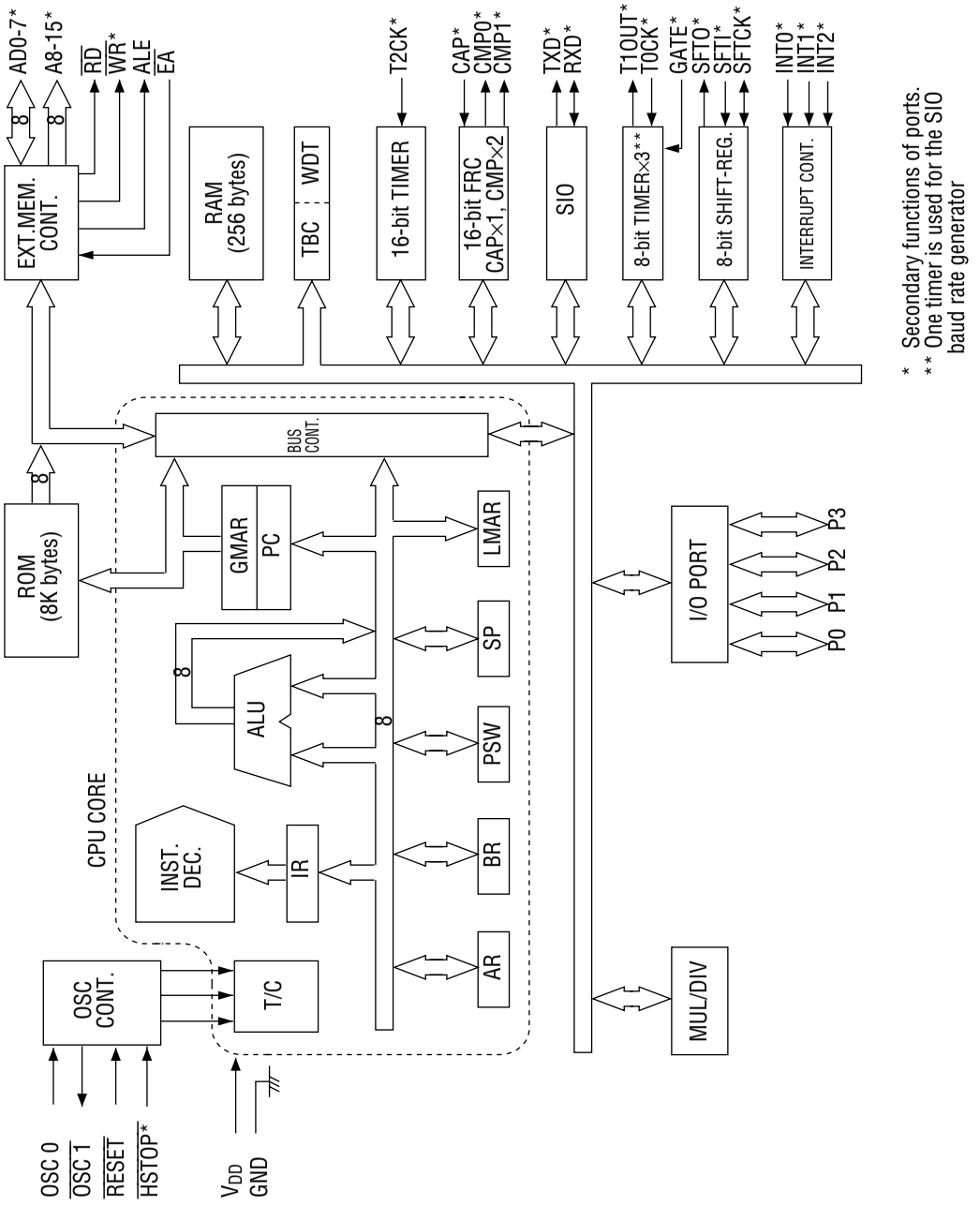
The MSM65512A is a high-performance 8-bit microcontroller that employs OKI original nX-8/50 CPU core. With a minimum instruction execution time of 400 ns (10MHz clock), the MSM65512A is capable of high-speed processing, and includes 8K bytes of program memory, 256 bytes of data memory, timers and serial ports. Also available are the MSM65P512A, which replaces the MSM65512's built-in program memory with one-time PROM, and the MSM65X512A, which uses external program memory.

FEATURES

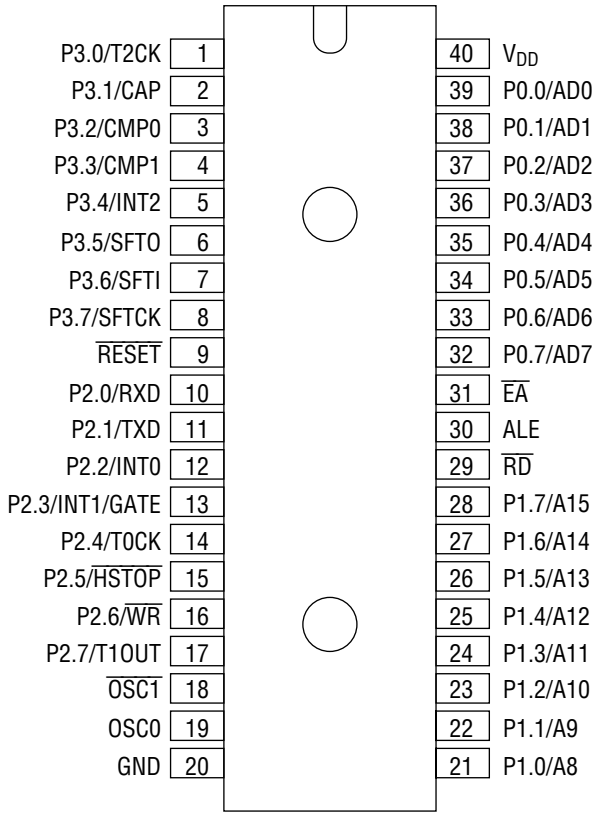
- Operating range
  - Operating frequency : 0 to 10 MHz (V_{DD}=4.5 to 5.5 V)
    0 to 5 MHz (V_{DD}=2.7 to 5.5 V)
  - Operating voltage : 2.7 to 5.5 V
  - Operating temperature : –40 to +85°C (Operation at +125°C is assured by the other specification.)
- Memory space : 64K bytes
  - Internal program memory : 8K bytes
  - Internal data memory : 256 bytes
- Minimum instruction execution time : 400 ns @ 10 MHz
- Powerful instruction set : 83 basic instructions
  8/16-bit operation instructions
  Bit manipulation instructions
  Compound function instructions
- Abundant addressing modes
- Multiplication/division operation functions : 8 × 8 → 16
  16/8 → 16 ... 8
- I/O ports
  - Input-output port : 4 ports × 8 bits
- Timers : 8-bit auto-reload timer × 2
  16-bit auto-reload timer × 1
  Watchdog timer × 1
- Counters : Time base counter × 1
  16-bit free-running counter × 1
- Capture input : 1 channel
- Compare output : 2 channels
- Serial ports : Shift register × 1
  Serial port with baud rate generator (UART/synchronous) × 1
- External interrupts : 3
- Interrupt sources : 15
- Package
  - 40-pin plastic DIP (DIP40-P-600-2.54) : (MSM65512A-×××RS, MSM65P512A-×××RS)
  - 44-pin plastic QFP (QFP44-P-910-0.80-2K) : (MSM65512A-×××GS-2K, MSM65P512A-×××GS-2K)
  - 44-pin plastic QFJ (PLCC) (QFJ44-P-S650-1.27) : (MSM65512A-×××JS, MSM65P512A-×××JS)

  ××× indicates the code number.

BLOCK DIAGRAM

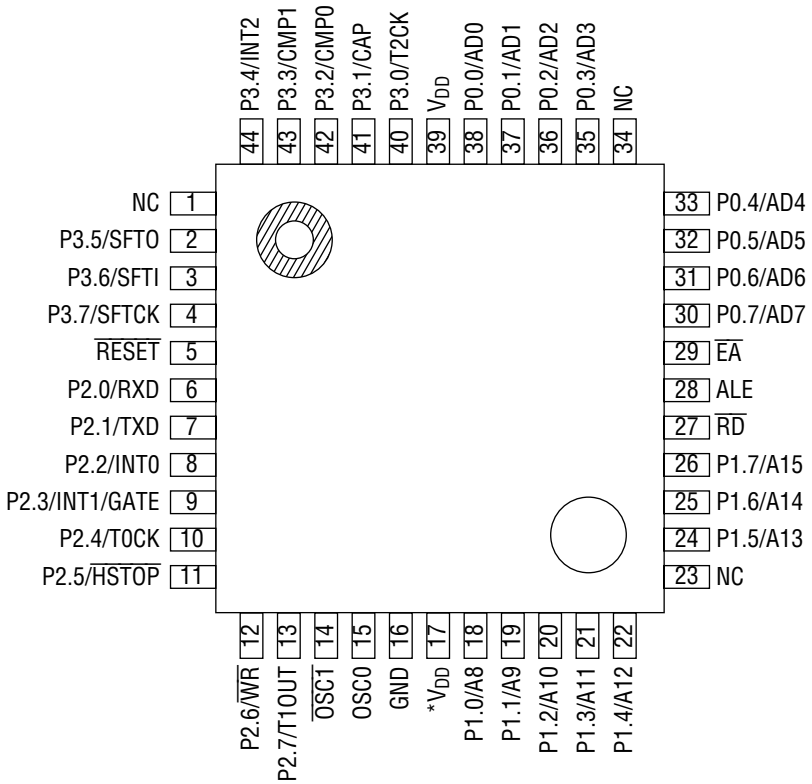


PIN CONFIGURATION (TOP VIEW)



40-Pin Plastic DIP

PIN CONFIGURATION (TOP VIEW) (Continued)

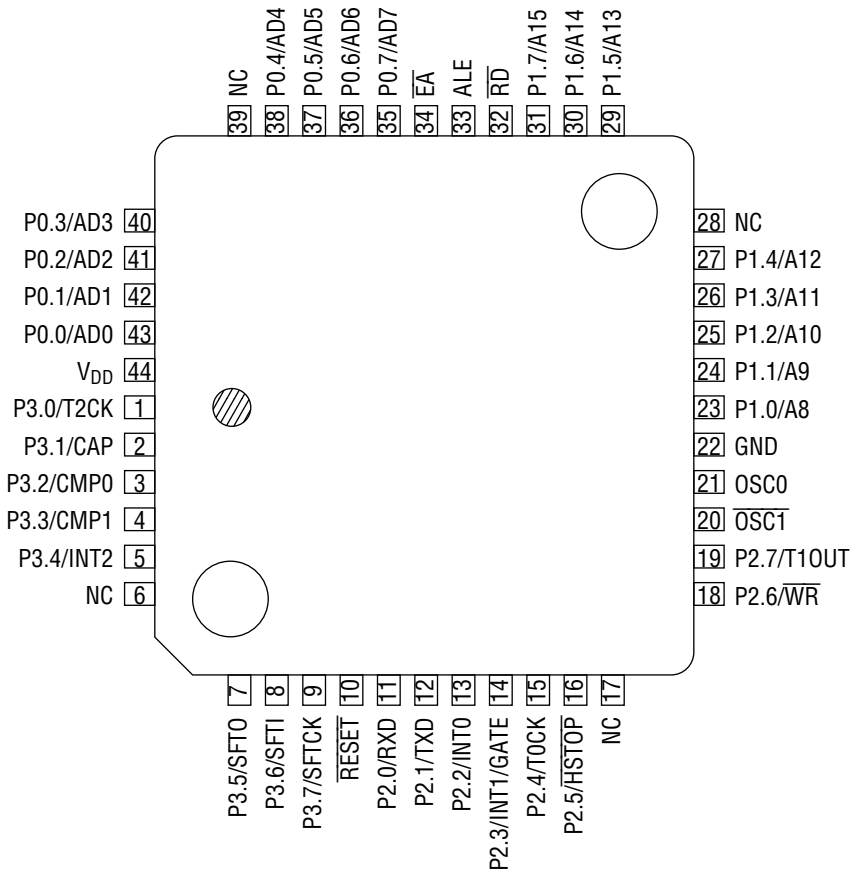


* No-connection pin for MSM65P512A

NC: No-connection pin

44-Pin Plastic QFP

PIN CONFIGURATION (TOP VIEW) (Continued)



NC: No-connection pin

44-Pin Plastic QFJ (PLCC)

PIN DESCRIPTIONS

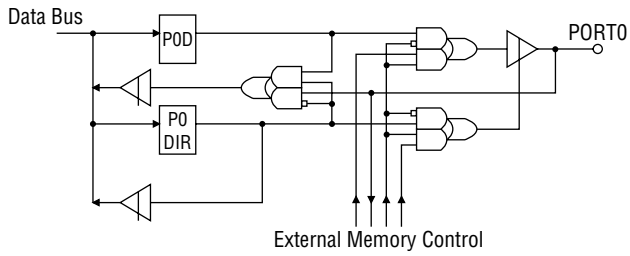
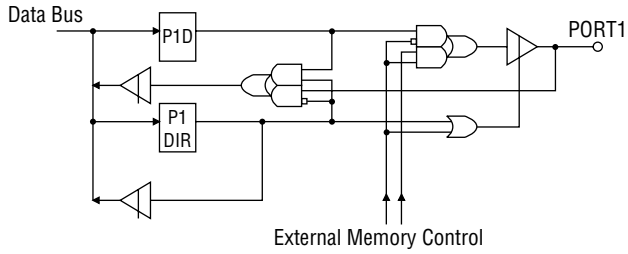
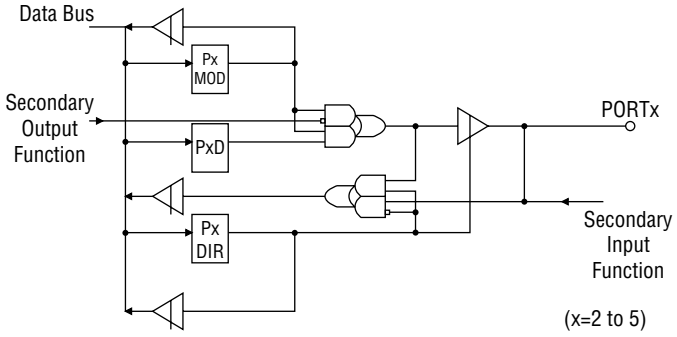
Basic Functions

Function	Symbol	Type	Description
Power Supply	V_{DD}	—	+5V power supply
	GND	—	0V digital ground
Oscillation	OSC0	I	Crystal oscillation input/external clock input
	$\overline{OSC1}$	O	Crystal oscillation output
Control	$\overline{RESET}$	I	System reset input (program starts from address 0040H); internal pull-up resistor
	$\overline{EA}$	I	Program memory select input pin. "L" level input for external program memory; "H" level input for internal program memory.
	$\overline{RD}$	O	Read strobe signal during external memory access
	ALE	O	Address latch signal during external memory access
Port	PORT 0	I/O	8-bit Input-output port During external memory access, becomes address/data bus for address output, instruction fetch or data read/write along with ALE, $\overline{RD}$ and $\overline{WR}$ pins
	PORT 1	I/O	8-bit Input/output port Address bus during external memory access
	PORT 2 PORT 3	I/O	8-bit Input/output port × 2. Secondary functions shown in following table are added for ports 2 and 3.

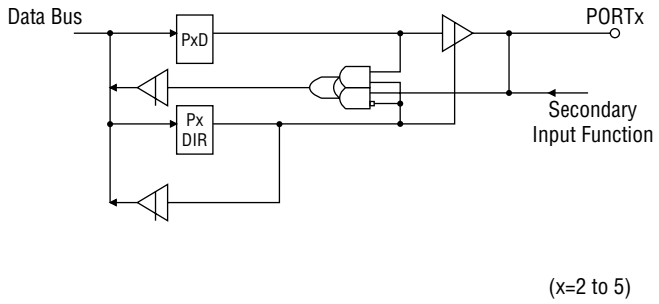
Secondary Functions

Symbol	Type	Description
RXD	I/O	P2.0 secondary functions UART: Input pin for serial port receive data. Synchronous: Input/output pin for serial port transmit/receive data.
TXD	O	P2.1 secondary functions UART: Output pin for serial port transmit data. Synchronous: Output pin for serial port synchronizing clock.
INT0	I	P2.2 secondary function External interrupt 0 input pin.
INT1/GATE	I	P2.3 secondary functions External interrupt 1 input pin. Also used as input pin for gate signal for timer 0 count enable/disable.
T0CK	I	P2.4 secondary function Timer 0 external clock input pin.
$\overline{\text{HSTOP}}$	I	P2.5 secondary function Hard stop mode input pin; stops system clock oscillation with "L" level input.
$\overline{\text{WR}}$	O	P2.6 secondary function Write strobe signal output pin during external data memory access.
T1OUT	O	P2.7 secondary function Output pin for signal obtained by dividing timer overflow by 2.
T2CK	I	P3.0 secondary function Timer 2 external clock input pin.
CAP	I	P3.1 secondary function Capture trigger input pin.
CMP0	O	P3.2 secondary function Compare output channel 0 output pin.
CMP1	O	P3.3 secondary function Compare output channel 1 output pin.
INT2	I	P3.4 secondary function External interrupt 2 input pin
SFTO	O	P3.5 secondary function Shift register data output pin.
SFTI	I	P3.6 secondary function Shift register data input pin.
SFTCK	I/O	P3.7 secondary function Shift register synchronizing clock input/output pin.

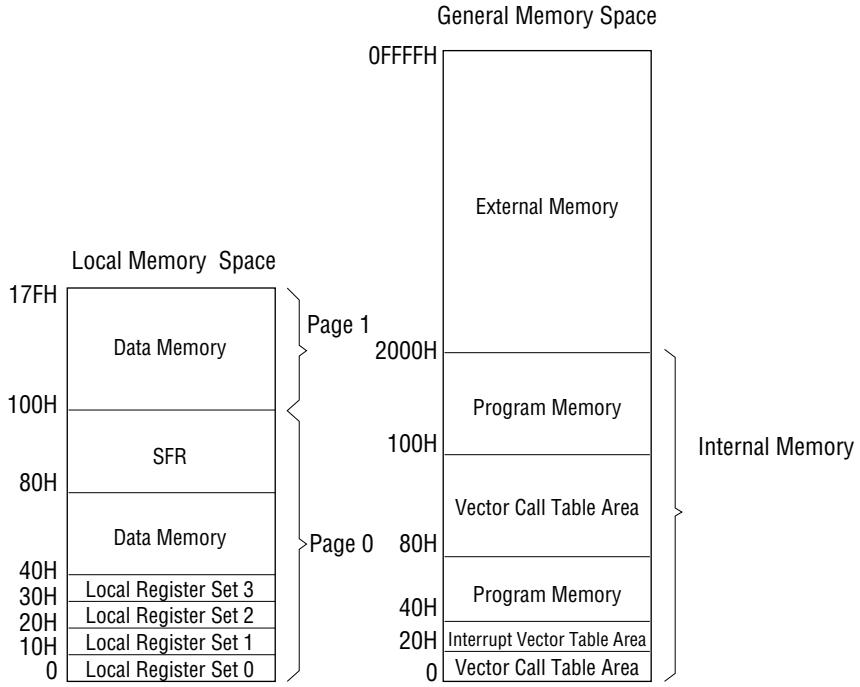
Port Circuit Configuration

Type	Port	Circuit Configuration	Electrical Characteristics (V_{DD}=5V)
1	P0.0/AD0- P0.7/AD7		"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=–400µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=3.2mA
2	P1.0/A8- P1.7/A15		"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=–200µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=1.6mA
3	P2.0/RXD, P2.1/TXD, P2.6/$\overline{WR}$, P2.7/T1OUT, P3.2/CMP0, P3.3/CMP1, P3.5/SFT0, P3.7/SFTCK		"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V P2.6/$\overline{WR}$ "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=–400µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=3.2mA Excluding P2.6/$\overline{WR}$ "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=–200µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=1.6mA

Port Circuit Configuration (Continued)

Type	Port	Circuit Configuration	Electrical Characteristics (V_{DD}=5V)
4	P2.2/INT0, P2.3/INT1/GATE, P2.4/T0CK, P2.5/$\overline{\text{HSTOP}}$, P3.0/T2CK, P3.1/CAP, P3.4/INT2, P3.6/SFTI	 (x=2 to 5)	"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=–200µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=1.6mA

MEMORY MAPS



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta=25°C	–0.3 to 7.0	V
Input Voltage	V_I		–0.3 to V_{DD}+0.3	
Output Voltage	V_O		–0.3 to V_{DD}+0.3	
Power Dissipation	P_D	Ta=25°C per package	400	mW
		Ta=25°C per output	50	
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	Refer to Figure 1.	2.7 to 5.5	V
Memory Hold Voltage	V_{DDMH}	f_{OSC}=0 Hz	2.0 to 5.5	
Oscillation Operating Frequency *1	f_{OSC}	Refer to Figure 1.	1 to 10	MHz
External Clock Operating Frequency	f_{EXTCLK}	Refer to Figure 1.	0 to 10	MHz
Operating Temperature	T_{op}	—	–40 to +85	°C

*1 This is due to the standard of a crystal oscillator or ceramic resonator.

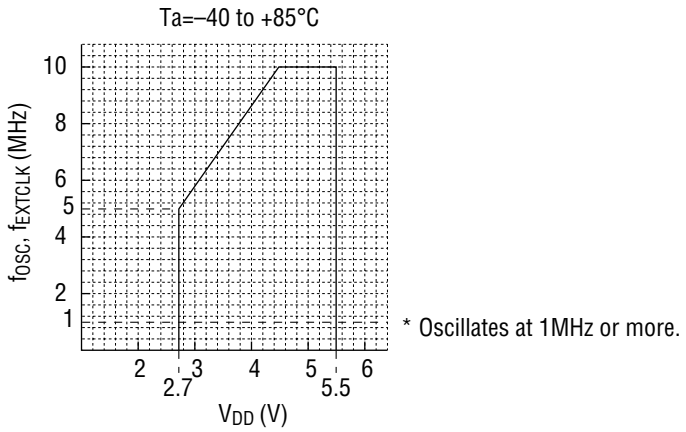


Figure 1. Operating Frequency vs. Power Supply Voltage

ELECTRICAL CHARACTERISTICS

DC Characteristics 1 (V_{DD}=4.5 to 5.5V)

(GND=0V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 *1	V_{IH1}	—	2.4	—	V_{DD}+0.3	V
"H" Input Voltage 2 *2	V_{IH2}	—	0.7V_{DD}	—	V_{DD}+0.3	
"L" Input Voltage	V_{IL}	—	–0.3	—	0.8	
"H" Output Voltage 1 *3	V_{OH1}	I_{OH}=–200µA	0.75V_{DD}	—	—	
"H" Output Voltage 2 *4	V_{OH2}	I_{OH}=–400µA	0.75V_{DD}	—	—	
"L" Output Voltage 1 *3	V_{OL1}	I_{OL}=1.6mA	—	—	0.4	
"L" Output Voltage 2 *4	V_{OL2}	I_{OL}=3.2mA	—	—	0.4	
Input Leakage Current 1 *5	I_{LI1}	V_I=V_{DD}/0V	—	—	±1	µA
Input Leakage Current 2 *6	I_{LI2}	V_I=V_{DD}/0V	—	—	±10	
"L" Input Current *7	I_{IL}	V_I=0V	–40	–200	–400	
Input Capacitance	C_I	f=1MHz, Ta=25°C	—	5	—	pF
Current Consumption	I_{DDS}	5V, Stop mode *8	—	—	50	µA
	I_{DDS}	10MHz, 5V, no load *9	—	20	40	mA

*1 Excluding OSC0 and $\overline{\text{RESET}}$
*2 OSC0 and $\overline{\text{RESET}}$
*3 Excluding P0, ALE, $\overline{\text{RD}}$, P2.6/$\overline{\text{WR}}$
*4 P0, ALE, $\overline{\text{RD}}$, P2.6/$\overline{\text{WR}}$
*5 $\overline{\text{EA}}$
*6 Excluding $\overline{\text{RESET}}$, $\overline{\text{EA}}$
*7 $\overline{\text{RESET}}$
*8 The ports configured as inputs should be coupled to V_{DD} or 0V. Other ports should not be loaded.
*9 Refer to Figure 2.

DC Characteristics 2 ($2.7 \leq V_{DD} < 4.5V$)

(GND=0V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 *1	V_{IH1}	—	$0.5V_{DD}+0.2$	—	$V_{DD}+0.3$	V
"H" Input Voltage 2 *2	V_{IH2}	—	$0.6V_{DD}+0.4$	—	$V_{DD}+0.3$	
"L" Input Voltage	V_{IL}	—	–0.3	—	$0.15V_{DD}+0.1$	
"H" Output Voltage 1 *3	V_{OH1}	I_{OH}=–10µA	$0.75V_{DD}$	—	—	
"H" Output Voltage 2 *4	V_{OH2}	I_{OH}=–20µA	$0.75V_{DD}$	—	—	
"L" Output Voltage 1 *3	V_{OL1}	I_{OL}=10µA	—	—	0.1	
"L" Output Voltage 2 *4	V_{OL2}	I_{OL}=20µA	—	—	0.1	
Input Leakage Current 1 *5	I_{LI1}	$V_I=V_{DD}/0V$	—	—	±1	µA
Input Leakage Current 2 *6	I_{LI2}	$V_I=V_{DD}/0V$	—	—	±10	
"L" Input Current *7	I_{IL}	V_{DD}=2.7 to 3.3V, V_I=0V	–40	–120	–240	
Input Capacitance	C_I	f=1MHz, Ta=25°C	—	5	—	pF
Current Consumption	I_{DDS}	3V, Stop mode *8	—	—	25	µA
	I_{DD}	5MHz, 3V, no load *9	—	6	15	mA

*1 Excluding OSC0 and $\overline{\text{RESET}}$
*2 OSC0 and $\overline{\text{RESET}}$
*3 Excluding P0, ALE, $\overline{\text{RD}}$, P2.6/$\overline{\text{WR}}$
*4 P0, ALE, $\overline{\text{RD}}$, P2.6/$\overline{\text{WR}}$
*5 $\overline{\text{EA}}$
*6 Excluding $\overline{\text{RESET}}$, $\overline{\text{EA}}$
*7 $\overline{\text{RESET}}$
*8 The ports configured as inputs should be coupled to V_{DD} or 0V. Other ports should not be loaded.
*9 Refer to Figure 2.

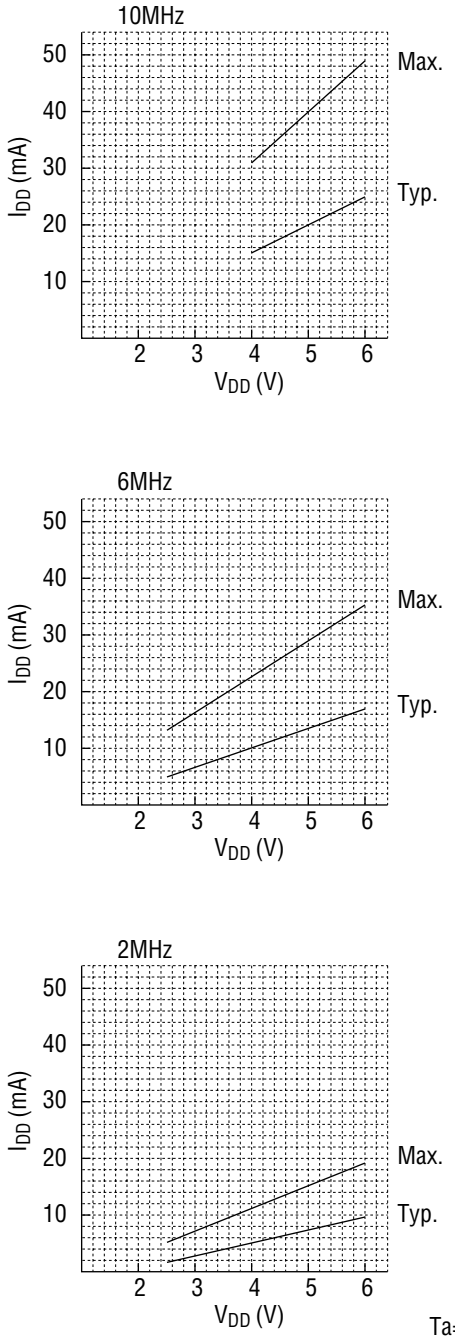


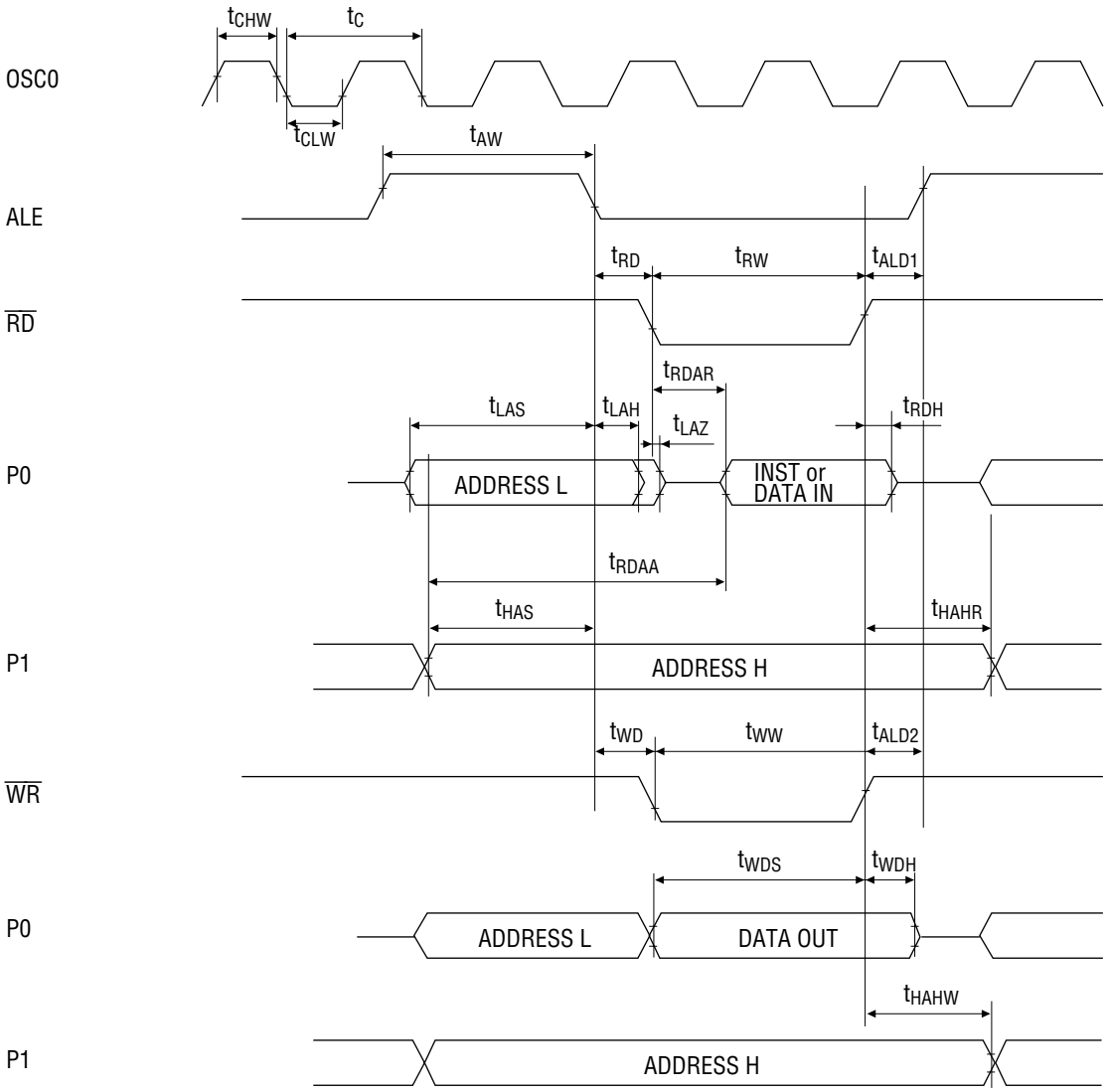
Figure 2. Operating Current Consumption vs. Power Supply Voltage

AC Characteristics

• External memory control

(V_{DD}=2.7 to 5.5V, GND=0V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Cycle	t_C	V_{DD}=4.5 to 5.5V	100	—	ns
"L" Clock Pulse Width	t_{CLW}		45	—	
"H" Clock Pulse Width	t_{CHW}		45	—	
Clock Cycle	t_C	V_{DD}=2.7 to 5.5V	200	—	
"L" Clock Pulse Width	t_{CLW}		90	—	
"H" Clock Pulse Width	t_{CHW}		90	—	
ALE Pulse Width	t_{AW}	C_L=100pF	$t_C+t_{CHW}-20$	—	
ALE Pulse Delay Time 1	t_{ALD1}		$t_{CLW}-20$	—	
ALE Pulse Delay Time 2	t_{ALD2}		$t_{CLW}-20$	—	
RD Pulse Width	t_{RW}		$t_C+t_{CHW}-40$	—	
RD Pulse Delay Time	t_{RD}		$t_{CLW}-40$	$t_{CLW}+20$	
$\overline{WR}$ Pulse Width	t_{WW}		$t_C+t_{CHW}-40$	—	
$\overline{WR}$ Pulse Delay Time	t_{WD}		$t_{CLW}-20$	$t_{CLW}+40$	
"L" Address Setup Time	t_{LAS}		t_C-40	—	
"H" Address Setup Time	t_{HAS}		t_C-40	—	
"L" Address Hold Time	t_{LAH}		$t_{CLW}-20$	—	
Bus Float Time	t_{LAZ}		—	20	
"H" Address Hold Time	t_{HAHR}		t_C-20	—	
"H" Address Hold Time	t_{HAHW}		t_C-20	—	
Read Data Access Time	t_{RDAA}		—	$t_C+t_{CLW}-15$	
Read Data Access Time	t_{RDAR}		—	$t_{CHW}+10$	
Read Data Hold Time	t_{RDH}		0	—	
Write Data Setup Time	t_{WDS}		$t_C+t_{CLH}-40$	—	
Write Data Hold Time	t_{WDH}		$t_{CLW}-20$	—	


OSC0
ALE
RD
P0
P1
WR
P0
P1
tCHW
tC
tCLW
tAW
tRD
tRW
tALD1
tRDAR
tLAS
tLAH
tLAZ
tRDH
ADDRESS L
INST or
DATA IN
tRDAA
tHAS
tHAHR
ADDRESS H
tWD
tWW
tALD2
tWDS
tWDH
ADDRESS L
DATA OUT
tHAHW
ADDRESS H

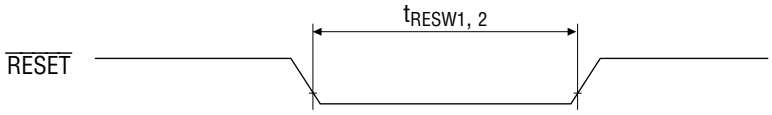
• **CPU control**

(V_{DD}=2.7 to 5.5V, GND=0V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{\text{RESET}}$ Pulse Width *1	t_{RESW1}	—	20	—	ns
$\overline{\text{RESET}}$ Pulse Width *2	t_{RESW2}	—	*3	—	—

*1 Excluding power ON, stop mode and hard stop mode.
*2 During power ON, in stop mode and hard stop mode.
*3 Oscillation stabilization time depends on resonator.

$\overline{\text{RESET}}$ pulse width

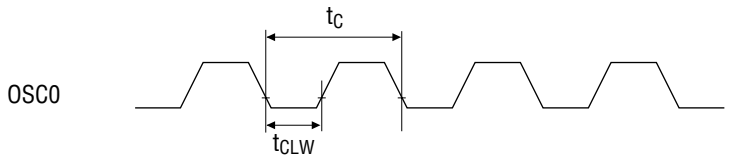


• **Peripheral control 1**

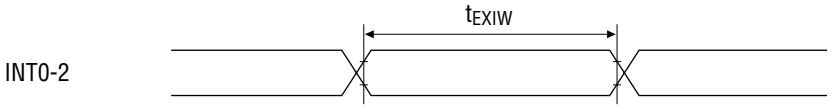
(V_{DD}=2.7 to 5.5V, GND=0V, Ta=–40 to +85°C)

Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Cycle	t_C	V_{DD}=4.5 to 5.5V	100	—	ns
			V_{DD}=2.7 to 5.5V	200	—	
EXI	External Interrupt Pulse Width	t_{EXIW}	—	4 t_C	—	
T0	External Clock Pulse Width	t_{T0CW}		4 t_C	—	
	GATE Pulse Width	t_{T0GW}		1 t_{T0CLK} *	—	
T2	External Clock Pulse Width	t_{T2CW}		4 t_C	—	
CAP	CAP Pulse Width	t_{CAPW}		12 t_C	—	

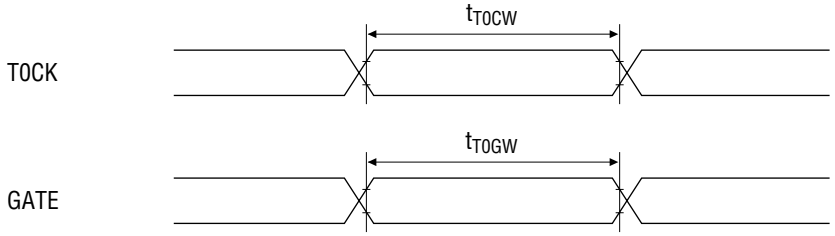
* t_{T0CLK} : Timer 0 count clock cycle selected by T0CON.



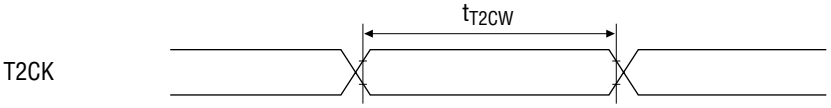
1) EXI pulse width



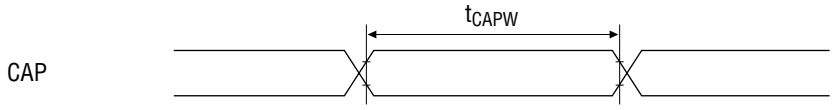
2) T0



3) T2



4) CAP

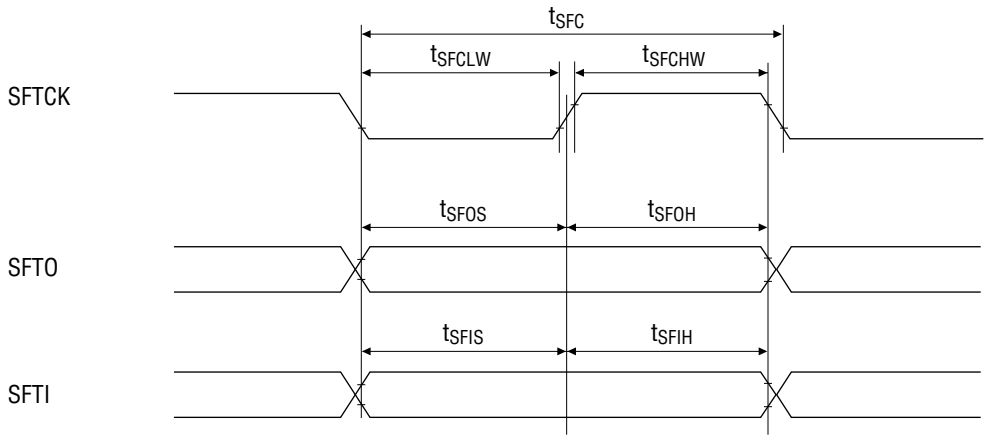


• **Peripheral control 2**

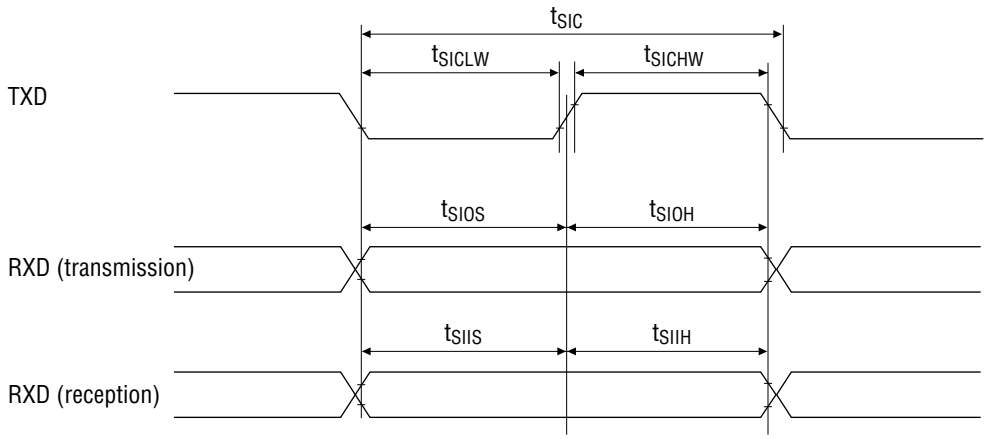
(V_{DD}=2.7 to 5.5V, GND=0V, Ta=–40 to +85°C)

Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Cycle	t_C	V_{DD}=4.5 to 5.5V	100	—	ns
			V_{DD}=2.7 to 5.5V	200	—	
SFT	SFTCK Cycle	t_{SFC}	C_L=100pF	8 t_C	—	
	SFTCK "L" Pulse Width	t_{SFCLW}		4 t_C–20	—	
	SFTCK "H" Pulse Width	t_{SFCHW}		4 t_C–20	—	
	SFTCK Setup Time	t_{SFOS}		t_{SFCLW}–100	—	
	SFTO Hold Time	t_{SFOH}		t_{SFCHW}–100	—	
	SFTI Setup Time	t_{SFIS}		100	—	
	SFTI Hold Time	t_{SFIH}		100	—	
SIO (Clock Synchronous)	Synchronous Clock Cycle	t_{SIC}		8 t_C	—	
	Synchronous Clock "L" Pulse Width	t_{SICLW}		4 t_C–20	—	
	Synchronous Clock "H" Pulse Width	t_{SICHW}		4 t_C–20	—	
	Output Data Setup Time	t_{SIOS}		6 t_C–100	—	
	Output Data Hold Time	t_{SIOH}		2 t_C–100	—	
	Input Data Setup Time	t_{SIIS}		t_C+t_{CLW}+100	—	
	Input Data Hold Time	t_{SIIH}		0	—	

1) SFT



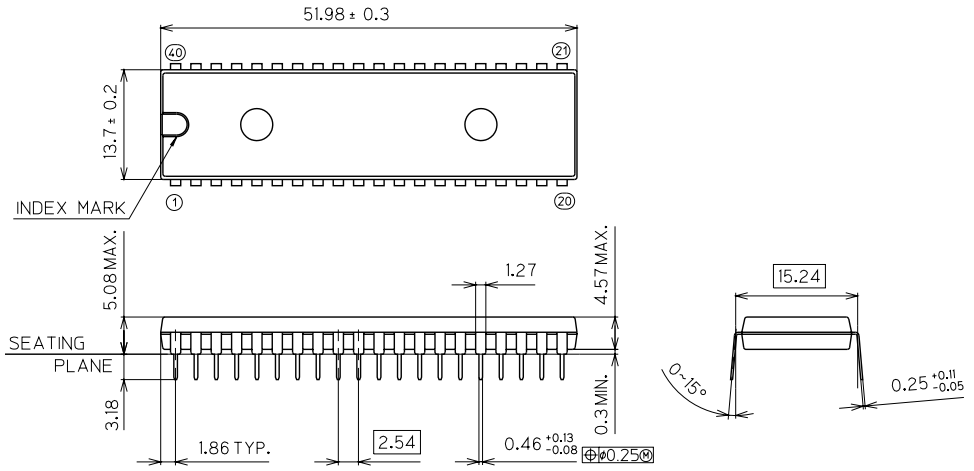
2) SIO
(Clock synchronous mode)



PACKAGE DIMENSIONS

(Unit : mm)

DIP40-P-600-2.54



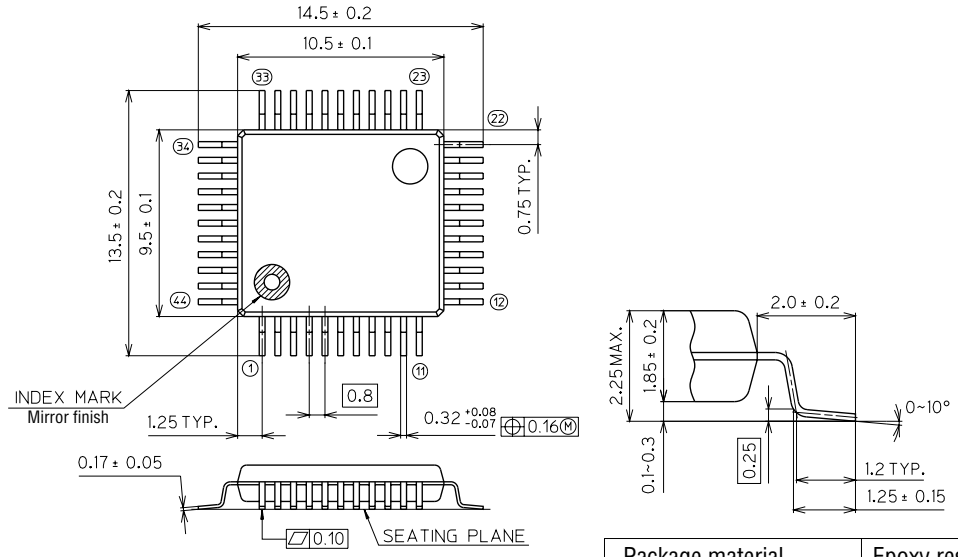
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	6.10 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP44-P-910-0.80-2K



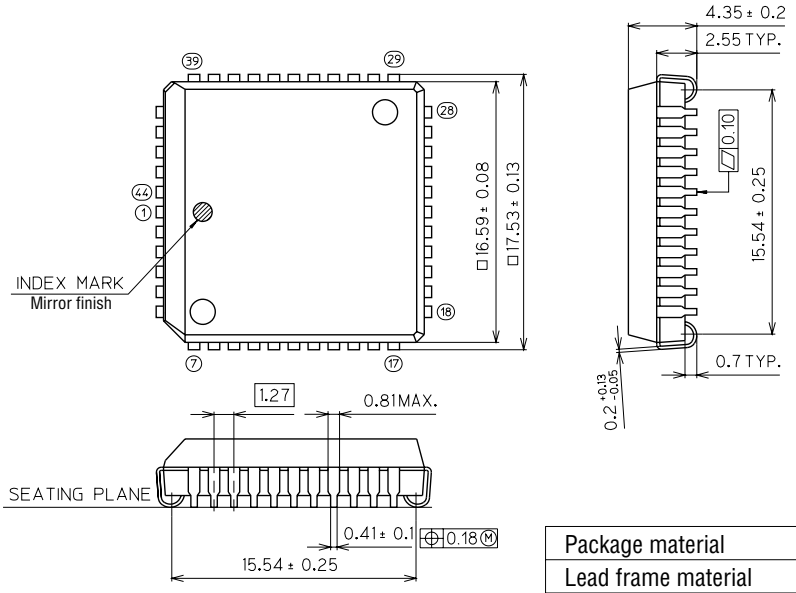
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFJ44-P-S650-1.27



Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	2.00 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).