OKI Semiconductor

This version: Nov. 1997
Previous version: Mar. 1996

MSM6599B

80-DOT SEGMENT DRIVER

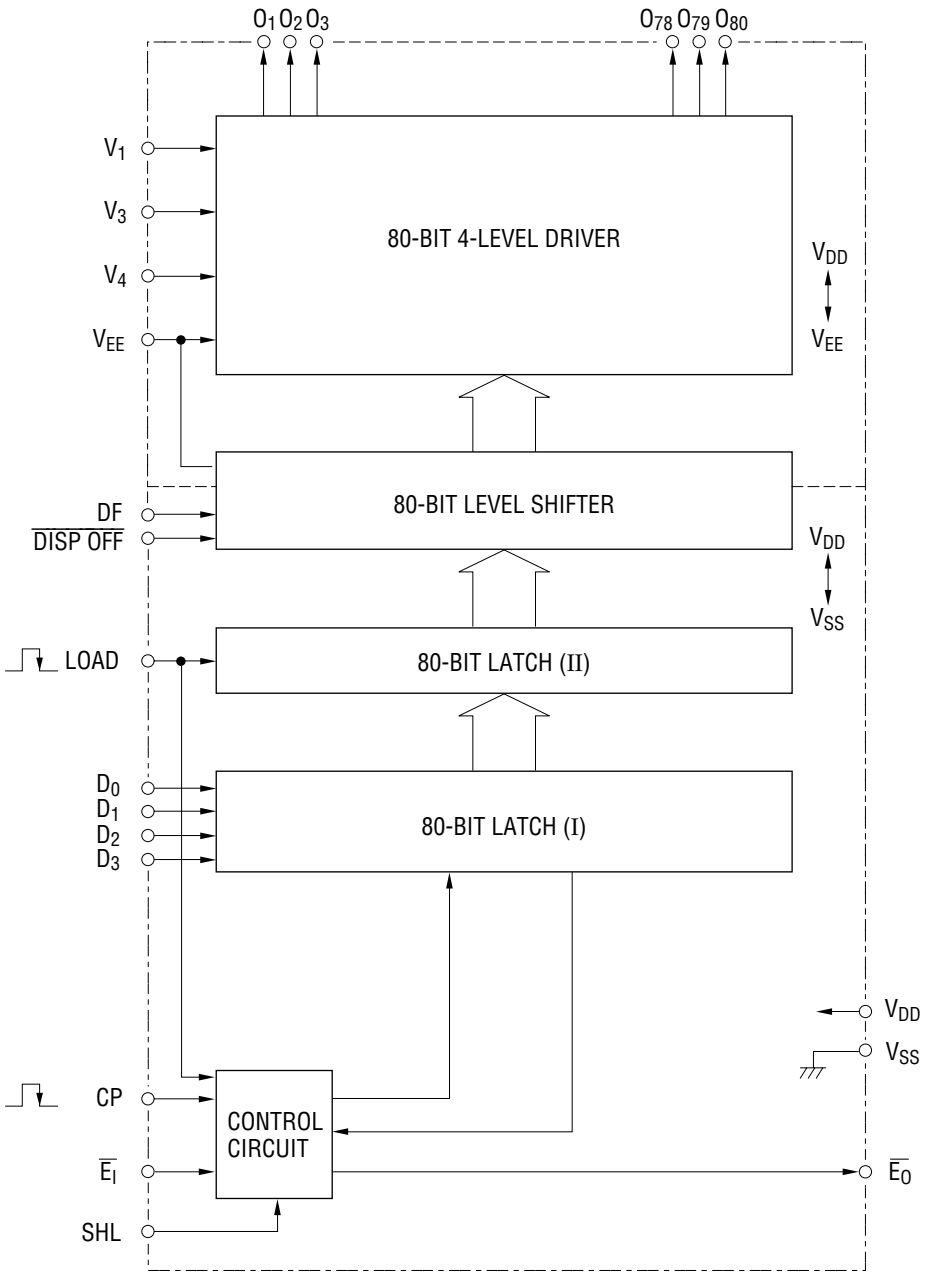
GENERAL DESCRIPTION

The MSM6599B is a dot matrix LCD segment driver LSI which consists of two 80-bit latches, an 80-bit level shifter and an 80-bit 4-level driver.
It latches the 4-bit parallel display data transferred from a microcomputer or LCD controller LSI, then outputs the LCD driving waveform to the LCD.

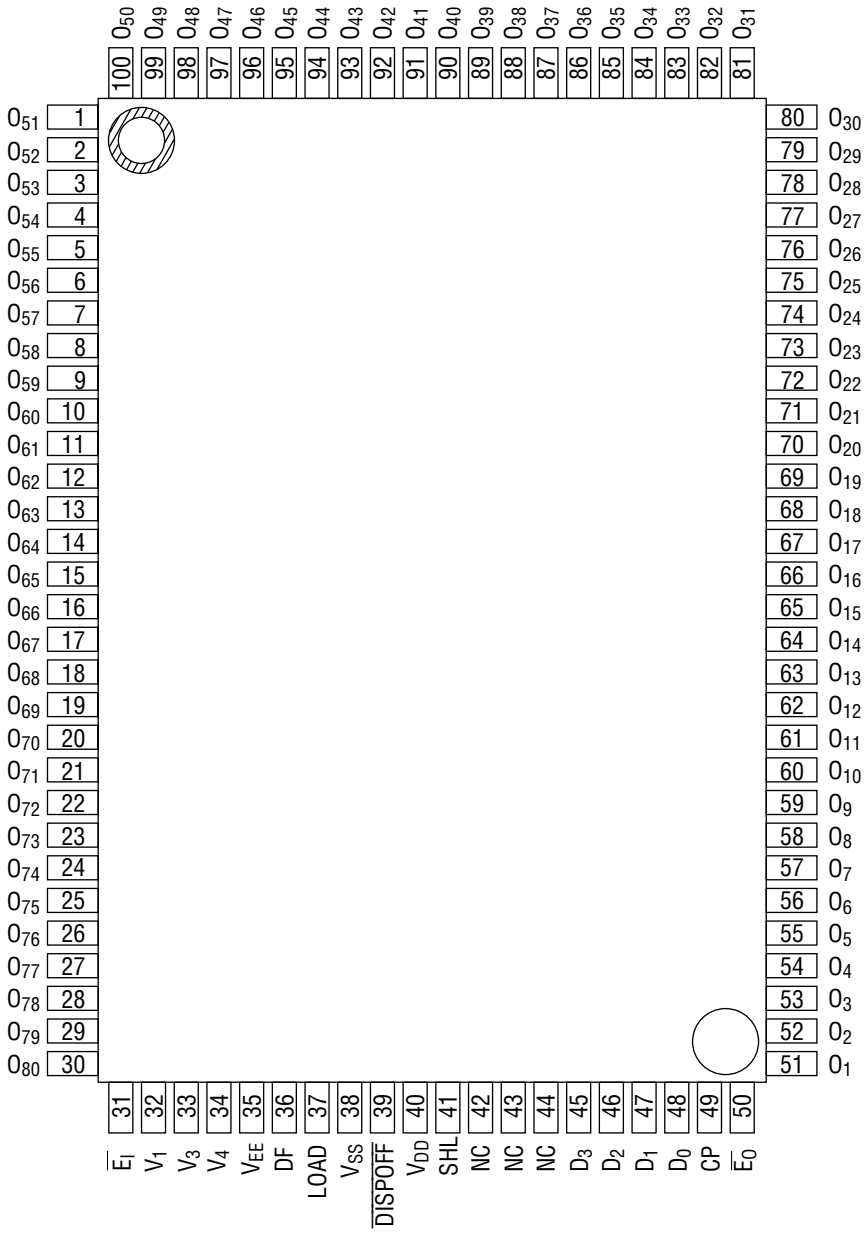
FEATURES

- Supply voltage : 4.5 to 5.5 V
- LCD driving voltage : 18 to 28 V
- Applicable LCD duty : 1/64 to 1/256
- LCD output : 80
- Because of 4-bit parallel transfers, the transfer speed is 1/4 that of conventional serial transfer, insuring low power consumption.
- Applicable common driver : MSM6698 (80 outputs)
- Package options:
  100-pin plastic QFP (QFP100-P-1420-0.65-K) (Product name : MSM6599B GS-K)
  100-pin plastic QFP(QFP100-P-1420-0.65-BK) (Product name : MSM6599B GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No connection

100-Pin Plastic QFP

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	Ta = 25°C	–0.3 to +6.5	V
Supply Voltage (2)	V_{DD}– V_{EE} *1	Ta = 25°C	0 to 32	V
Input Voltage	V_I	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

*1 $V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$

RECOMMENDED OPRATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage (1)	V_{DD}	—	4.5 to 5.5	V
Supply Voltage (2)	$V_{DD} – V_{EE}$ *1	—	18 to 28	V
Operating Temperature	T_{op}	—	–20 to +75	°C

*1 $V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 5V ±10%, Ta = –20 to +75°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH} *1	—	0.7V_{DD}	—	V_{DD}	V
"L" Input Voltage	V_{IL} *1	—	V_{SS}	—	0.3V_{DD}	V
"H" Input Current	I_{IH} *1	V_I = V_{DD}, V_{DD} = 5.5V	—	—	1	µA
"L" Input Current	I_{IL} *1	V_I = 0V, V_{DD} = 5.5V	—	—	–1	µA
"H" Output Voltage	V_{OH}*2	I_O = –0.2mA, V_{DD} = 4.5V	V_{DD}–0.4	—	—	V
"L" Output Voltage	V_{OL}*2	I_O = 0.2mA, V_{DD} = 4.5V	—	—	0.4	V
ON Resistance	R_{ON}*4	V_{DD}–V_{EE} = 25V, *3 $\lvert V_N - V_O \rvert$ = 0.25V V_{DD} = 4.5V	—	1.5	3.0	kΩ
Standby Current	I_{DDSBY}	f_{CP} = 6.0 MHz, V_{DD} = 5.5V V_{DD}–V_{EE} = 25V, No load *5	—	—	300	µA
Supply Current (1)	I_{DD1}	f_{CP} = 6.0 MHz, V_{DD} = 5.5V V_{DD}–V_{EE} = 25V, No load *6	—	—	1.5 / 1.0	mA
Supply Current (2)	I_V	f_{CP} = 6.0 MHz, V_{DD} = 5.5V V_{DD}–V_{EE} = 25V, No load *7	—	—	100	µA
Input Capacitance	C_I	f = 1 MHz	—	5	—	pF

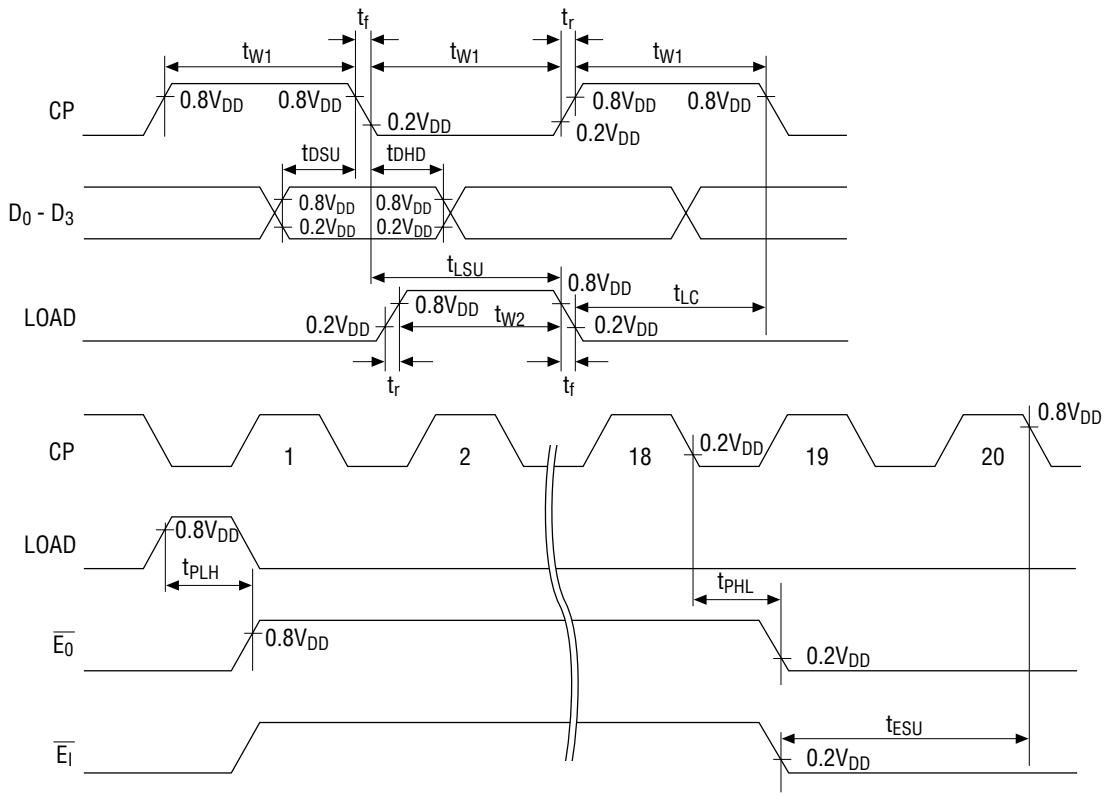
*1 Applicable to LOAD, CP, D_0 to D_3, $\overline{E_I}$, DF, $\overline{DISPOFF}$, SHL.
*2 Applicable to $\overline{E_O}$.
*3 V_N = V_1 to V_{EE} V_4 = 14/16 (V_{DD}–V_{EE}), V_3 = 2/16 (V_{DD}–V_{EE}), V_{DD} = V_1.
*4 Applicable to O_1 to O_{80}.
*5 Display Data 1010 f_{DF} = 45 Hz, current from V_{DD} to V_{SS} when the display data is not being processed.
*6 Display Data 1010 f_{DF} = 45 Hz, current (V_{DD} side current) from V_{DD} to V_{SS} and V_{EE}, and current (V_{EE} side current) from V_{DD} to V_{EE} when the display data is being processed. V_{EE} / V_{DD}
*7 Display Data 1010 f_{DF} = 45 Hz, f_{LOAD} = 20 kHz, current on V_1, V_3 and V_4.

Switching Characteristics

(V_{DD} = 5V ±10%. Ta = –20 to +75°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Frequency	f_{CP}	DUTY = 50%	—	—	6.5	MHz
Clock Pulse Width	t_{W1}	—	56	—	—	ns
Load Pulse Width	t_{W2}	—	70	—	—	ns
Rise/Fall Time	t_r, t_f	—	—	—	20	ns
Data Setup Time	t_{DSU}	—	50	—	—	ns
Data Hold Time	t_{DHD}	—	50	—	—	ns
Load Setup Time	t_{LSU}	—	80	—	—	ns
Load-to-Clock Time	t_{LC}	—	80	—	—	ns
Propagation Delay Time	t_{PLH}, t_{PHL}	CL=15pF	—	—	236	ns
$\overline{E_I}$ Setup Time	t_{ESU}	—	50	—	—	ns

Note: When display control by the $\overline{DISPOFF}$ pin is performed, the rise and fall time must be ≤ 1µs.



FUNCTIONAL DESCRIPTION

Pin Functional Description

- **$\overline{E_I}$, $\overline{E_O}$**
  These are enable pins. When a cascade connection is required, set the first MSM6599B's $\overline{E_I}$ pin at "L" level and connect $\overline{E_O}$ pin to the next MSM6599B's $\overline{E_I}$ pin. When a single MSM6599B is used, $\overline{E_I}$ should be set at "L" level.

- **CP**
  Clock input pin for display data input. Data is clocked in the latch (I) at the falling edge of the clock pulse. The clock pulse from this pin is active when the enable F/F is set, and inactive when it is not set.

- **LOAD**
  Input pin to latch the display data of one line stored in the latch (I). The latch (I) data is transferred to the latch (II) at the falling edge. At this time, the control circuit to save the power is reset and the display data of the next line can be stored.

- **DF**
  Synchronous signal input pin for alternate signal for LCD driving . Frame inversion signal is input to this pin.

- **V_{DD}, V_{SS}**
  Power supply pins of the MSM6599B. V_{DD} is generally set to 4.5V to 5.5V. V_{SS} is the GND pin, which is set to 0V.

- **D_0, D_1, D_2, D_3**
  Display data input pins for the 80-bit latch (I). The display data is input at the falling edge of clock pulse. Table 1 shows the relationship between display data, DF, LCD driver output, and display.

Table 1

Display Data	DF	LCD Driver Output	Display
L	L	Non-select level (V_3)	OFF
H	L	Select level (V_1)	ON
L	H	Non-select level (V_4)	OFF
H	H	Select level (V_{EE})	ON

- **SHL**
  Input pin to select the loading direction of display data. Set this pin to "H" or "L" level during power-on. Table 2 shows the relationship between shift direction of data (D_0 to D_3) and driver output (O_1 to O_{80}).

Table 2

SHL	Direction of Data Loading
L	$D_0 \rightarrow O_1 \rightarrow O_5$ ---------- $\rightarrow O_{77}$ $D_1 \rightarrow O_2 \rightarrow O_6$ ---------- $\rightarrow O_{78}$ $D_2 \rightarrow O_3 \rightarrow O_7$ ---------- $\rightarrow O_{79}$ $D_3 \rightarrow O_4 \rightarrow O_8$ ---------- $\rightarrow O_{80}$
H	$D_0 \rightarrow O_{80} \rightarrow O_{76}$ ---------- $\rightarrow O_4$ $D_1 \rightarrow O_{79} \rightarrow O_{75}$ ---------- $\rightarrow O_3$ $D_2 \rightarrow O_{78} \rightarrow O_{74}$ ---------- $\rightarrow O_2$ $D_3 \rightarrow O_{77} \rightarrow O_{73}$ ---------- $\rightarrow O_1$
	↑ Last Data ↑ First Data

- **V_1, V_3, V_4, V_{EE}**
  Bias supply voltage pins used to drive the LCD. Use an external bias voltage supply for driving the LCD

- **O_1 - O_{80}**
  Output pins for the 4-level driver that directly correspond to each bit of the 80-bit latch (II) contents. One of V_1, V_3, V_4 and V_{EE} is selected and output by a combination of latched content and DF signals. See the "Truth Table". Connect this output to the segment side of the LCD.

- **$\overline{\text{DISP OFF}}$**
  Input pin to control O_1 to O_{80} outputs. The V_1 level is output from O_1 to O_{80} pins regardless of the display data during "L" level input. See the "Truth Table".

Truth Table

DF	Latch Data	$\overline{\text{DISPOFF}}$	Driver Output (O_1 to O_{80})
L	L	H	V_3
L	H	H	V_1
H	L	H	V_4
H	H	H	V_{EE}
X	X	L	V_1

X : Don't Care

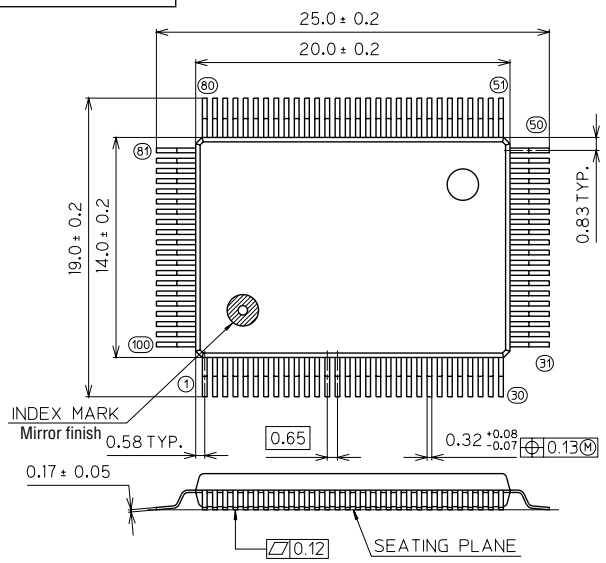
NOTES ON USE

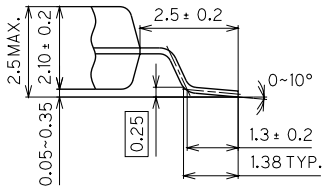
Precautions when turning power ON/OFF:
The LCD drivers of this IC require a high voltage. For this reason, if a high voltage is applied to the LCD drivers with the logic power supply floating, excess current flows. This may damage the IC.
Be sure to follow the sequence below when turning the power ON or OFF.
Power ON : Logic circuits ON → LCD drivers ON, or both ON at a time
Power OFF : LCD drivers OFF → logic circuits OFF, or both OFF at a time

PACKAGE DIMENSIONS

(Unit : mm)

QFP100-P-1420-0.65-K





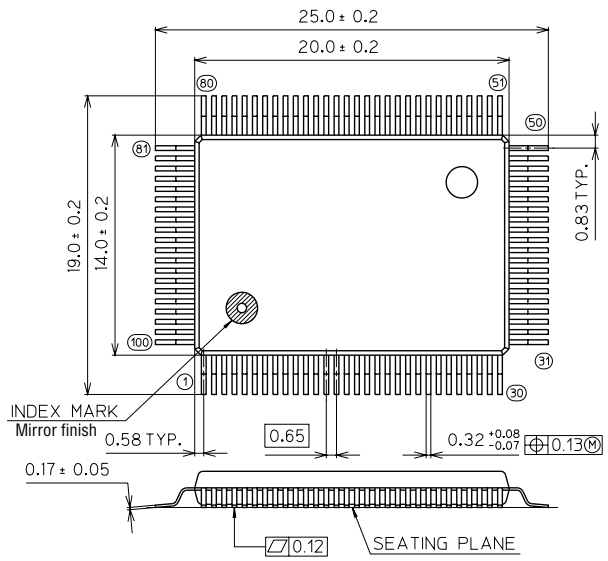
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.29 TYP.

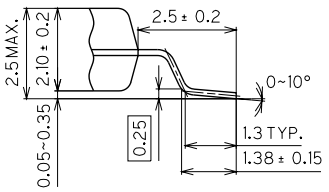
Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP100-P-1420-0.65-BK





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