# MSM6636
# USER'S GUIDE

Oki Electric Industry Co., Ltd.

# INTRODUCTION

This manual describes the functions of SAE-J1850 protocol and introduces its application examples. This manual also details the functions of MSM6636, and introduces control examples of a LAN (Local Area Network) using MSM6636. For details on the commands of MSM6636, see “MSM6636 Users Manual”.

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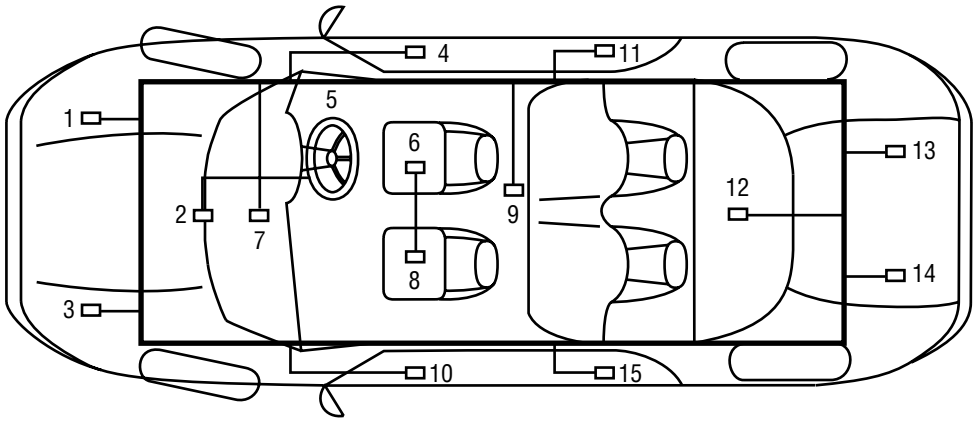
*Chapter 1*

# INTRODUCTION

# 1. INTRODUCTION

Many wiring connectors are used for various switches, sensors, lights and motors positioned throughout automobiles. To interconnect these devices efficiently using multiplex transmission communication technology, a small scale LAN (Local Area Network) is constructed, and data communication between devices is performed using common lines. SAE-J1850 is a communication format (protocol) of multiplex transmission communication adapted by the Society of Automotive Engineers (SAE) in the United States. MSM6636 is an automotive LAN controller based on this protocol. MSM6636 can be applied not only to the control of various devices in automobiles, as shown below, but also to integrated vehicle control systems, such as car navigation, car audio and electronic control 4WD, and to on-vehicle problem diagnosis systems.




1. Front right area control
2. Front window control
3. Front left area control
4. Front right door control
5. Switch module control
6. Driver seat control
7. Total warning control
8. Seat next to driver control
8. Seat next to driver control
9. Roof control
10. Front left door control
11. Rear right door control
12. Rear window control
13. Rear right area control
14. Rear left area control
15. Rear left door control

**Figure 1-1 Automotive LAN**

## 1.1 What is J1850?

An overview of the communication regulation of J1850 protocol is shown below.
In J1850, each node (communication station) connected to the LAN can transmit messages equally, and has an address (physical address and functional address) to identify itself. A physical address is an address unique to each node. There is no other node with the same physical address on the LAN. A functional address, on the other hand, is an address to send messages at the same time to devices which have the same function. This means that multiple nodes which have the same function have the same functional address.

Communication is performed by specifying the receive destination address in the message. If the physical address is specified to the receive destination address, only the specified node will receive the message. If the functional address is specified to the receive destination address, multiple nodes will receive the message.

There is a function for the node which received the message to return its physical address value (response transmission) when it receives the message normally. By this function, the message transmission node can know whether the specified receive destination node received the message normally.

## 1.2 LAN Configuration of J1850

Figure 1-2 shows the LAN configuration of J1850. The LAN bus uses 2 lines: BUS (+) and BUS (-). BUS (+) is connected to ground (GND) with resistance R (+), and BUS (-) is connected to power supply (VDD) with resistance R (-). At each node, the PNP transistor bus driver is connected to BUS (+), and the NPN transistor bus driver is connected to BUS (-), to drive the LAN bus. Inverted signals (Figure 1-3) are output to both BUS (+) and BUS (-). When node 1 turns the bus drivers on (turns the PNP and NPN transistors on), BUS (+) becomes VDD potential and BUS (-) becomes GND potential. Even if node 2 turns the bus drivers on or off after this, the status of BUS (+) and BUS (-) does not change. This status is called "node 1 is occupying the bus", and the status of BUS (+) and BUS (-) at this time is called "dominant status". Only when all nodes connected to the LAN turn the bus drivers off, BUS (+) becomes GND potential, and BUS (-) becomes VDD potential. This status is called "the bus is open", and the status of BUS (+) and BUS (-) at this time is called "passive status". The format in which transistors of multiple nodes are connected to one common line in this manner is called a "wired OR" connection.

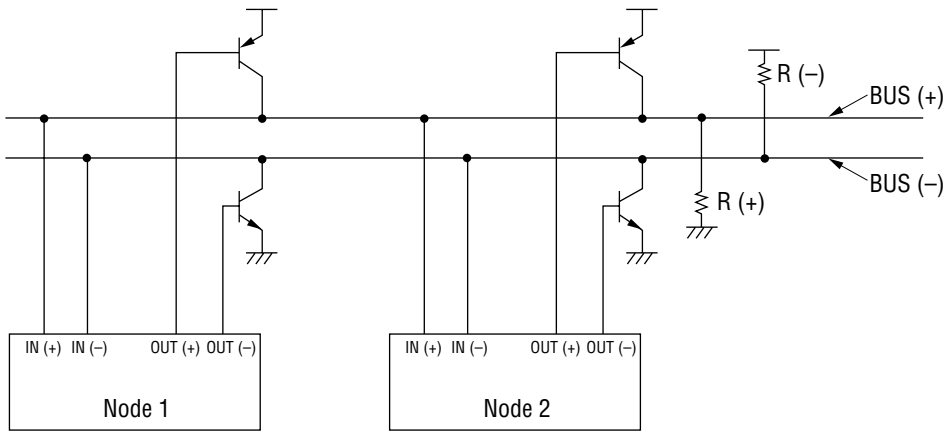



**Figure 1-2 Configuration fo J1850 LAN**

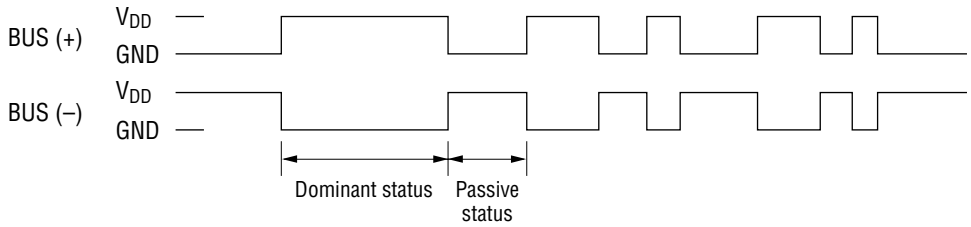



**Figure 1-3 Signal Wave Form of BUS (+) and BUS (–)**

## 1.3 Bit Format of J1850

In J1850, a message signal output to the LAN bus is detected by the status whether the bus is or is not occupied for a specified “short time”. In other words, communication is performed by pulse width modulation (PWM).

In J1850, codes (bits) necessary for several types of communication are expressed by a combination of bus occupancy and bus open as follows.

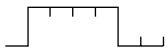
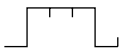
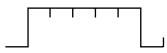
| Code | Contents | Combination of Bus Occupancy/Open | Wave Form |
|---|---|---|---|
| SOF | Indicates beginning of message frame (Start Of Frame) | Bus is continuously occupied for 4 short time units, then bus is opened for 2 short time units |  |
| "1" | Indicates binary bit "1". | Bus is occupied for 1 short time unit, then bus is opened for 2 short time units. |  |
| "0" | Indicates binary bit "0". | Bus is continuously occupied for 2 short time units, then bus is opened for one short time units. |  |
| EOD | Indicates end of transmission data (END Of Data) | Bus is continuously opened for 3 short time units. |  |
| EOF | Indicates end of message frame (End Of Frame) | Bus is continuously opened for 6 short time units. |  |
| IFS | Indicates interval period to distinguish one message frame from another. (Inter-Frame Separation) | Bus is continuously opened for 3 short time units. |  |
| BRK | Indicates a force-stop of communication. (Break) | Bus is continuously occupied for 5 short time units, then bus is opened for 1 short time unit. |  |

**Figure 1-4 PWM Bit Format of J1850**

## 1.4 Asynchronous Transmission Communication System of J1850

In J1850, communication is performed asynchronously. This communication is implemented by making the communication speed of all nodes of the LAN equal. This means that by communicating using certain small time units of the PWM bit format, a node on the LAN receives a message synchronizing the internal circuit when the occupancy of the bus starts (when the bus changes from passive to dominant status). When transmitting a message, the message is sent according to the timing of the node sending message, with the receive node synchronizing the transmission node. Since each bit of the PWM system synchronizes, there is little deviation of the data sample for start-stop synchronization. This makes high-speed communication possible.

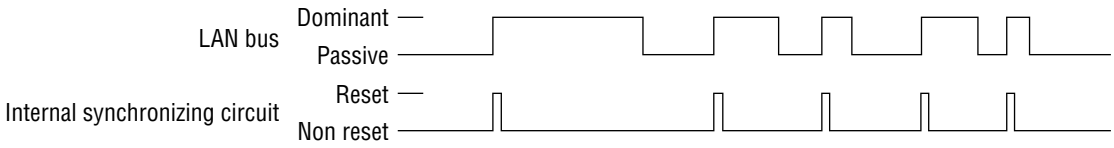



**Figure 1-5 Synchronization of J1850**

## 1.5 Multiplex Transmission Communication System of J1850

For all nodes on the LAN to start communication (message communication) according to the respective request, it is necessary to avoid collision which occurs when transmission starts at the same time. There are various means to prevent collision, and in the J1850, CSMA/CD (Carrier Sense Multiple Access/Collision Detection) is used. In this system, collision is avoided by "stopping transmission and re-transmission". Each node checks the bus status at every small time unit, and starts transmission after confirming that the bus is in idle status (status in which the passive status of the bus is continuing for a certain time). The bus is continuously checked during transmission, judging whether the data transmitted by the local node is output normally to the bus. If a message transmission node is outputting a passive status to the bus while the bus is in dominant status, the node detects collision, and stops transmission. This in no way affects the message of the node outputting dominant status to the bus, so this node continues message transmission. By avoiding collision in this way, all nodes on the LAN can perform message transmission at any time equally. Using this system, priorities can be assigned to messages, which improves network efficiency.

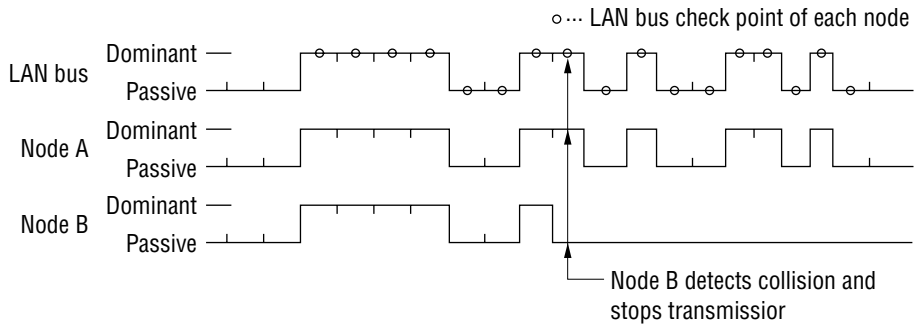
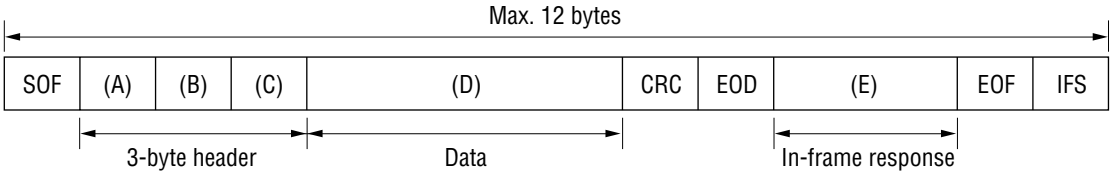



**Figure 1-6 Collision Detection of J1850**

## 1.6 Communication Format of J1850

The frame format of J1850 follows.




SOF : Start Of Frame
CRC : Cyclic Redundancy Check
EOD : End Of Data
EOF : End Of Frame
IFS : Inter-Frame Separation

**Table 1-1 Communication Format**

| | No. of Bytes | Content |
|---|---|---|
| (A) | 1 | Priority and message type |
| (B) | 1 | Physical address or functional address of receive node |
| (C) | 1 | Physical address of transmission node |
| (D) | *1 | Data |
| CRC | 1 | CRC code |
| (E) | *1 | In-frame response (IFR) |

*1 Sum of number of bytes of (D) and number of bytes of (E) is 0~8 bytes.

(A) Bit configuration of priority and message type

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| H (P3) | P2 | P1 | P0 | K | Y | Z1 | Z0 |

H ..... Header format setting bit
0: 3 byte header
1:1 byte header
(MSM6636 does not support 1 byte headers.)

P2, P1, P0 .... Priority setting bit
When multiple nodes on a network start message transmission at the same time, these bits determine the priority of the messages. The smaller the priority value, the higher the priority. MSM6636 can use the “H bit” as the priority setting bit.

(Supplement)
MSM6636 is designed based on the J1850 standard issued in December 1991. Under the current standard, however, the position of the H bit and P2~P0 bits are different, due to partial standard changes by SAE. This does not cause hardware problems in the MSM6636, since the H bit is not used to control 3 byte/1 byte header selection (fixed to a 3-byte header). If meeting the latest standard is considered, design software which handles P3~P1 bits as a priority field.

Y .....Address type setting bit
0: Specifies the functional address to address (B) of the receive node.
1: Specifies the physical address to address (B) of the receive node.

K, Z1, Z0 .....In-frame response type setting bit
The response type is set by a combination of K, Z1 and Z0 bits.

The message type and response type are determined by the low-order 4 bits of the header byte (A), including the Y bit. The classification is shown below.

**Table 1-2 Message Type and IRF Type List**

| | ZZ KY10 | Address Type | IFR Type | Message Type |
|---|---|---|---|---|
| 0 | 0000 | Functional | 2 | Receives multiple IDs from multiple listeners |
| 1 | 0001 | ↑ | 1 | Broadcast (*1) |
| 2 | 0010 | ↑ | 2 | Receives multiple IDs from multiple listeners |
| 3 | 0011 | ↑ | 3 | Receives DATA from selected listeners |
| 4 | 0100 | Physical | 1 | Receives ID from selected listener |
| 5 | 0101 | ↑ | 3 | Receives DATA from selected listener |
| 6 | 0110 | ↑ | 0 | SEA reserve (*2) |
| 7 | 0111 | ↑ | 3 | Receives DATA from selected listener |
| 8 | 1000 | Functional | 0 | To multiple listeners (command/status) |
| 9 | 1001 | ↑ | ↑ | To multiple listeners (request) |
| A | 1010 | ↑ | ↑ | — |
| B | 1011 | ↑ | ↑ | — |
| C | 1100 | Physical | ↑ | — |
| D | 1101 | ↑ | ↑ | — |
| E | 1110 | ↑ | ↑ | — |
| F | 1111 | ↑ | ↑ | — |

(*1) Broadcast : Sends the same data to multiple listeners selected by the functional address. Only the listener with the highest priority ID (physical address) can send the ID as an IFR. (IFR can be sent only once. Other listeners cannot send an IFR.)

(*2) SAE reserve : MSM6636 does not respond, even if an IFR request is received by this header.

For details on IFR types, see “1.6.1 In-frame response type”.

(B) Physical address or functional address of receive node

The 1st byte (A) of the 3 byte header (Y bit) selects whether an address is physical or functional, and the 2nd byte (B) indicates the address of the receive node.

(C) Physical address of transmission node

Indicates the physical address (ID) of the transmission node.

(D) Data

Indicates arbitrary transmission data.
Data is increased or decreased in byte units. The maximum number of bytes is 8, including the response.

(E) In-frame response

The message transmission node can request a response within the message frame to the message receive node. This response is called an “in-frame response”.

### 1.6.1 In-frame response type

An in-frame response is transmitted or received within 1 message frame to make communication efficient. The four types follow.

<IFR type 0>
Does not request an in-frame response.

| SOF | HEADER | DATA | CRC | EOF |
|---|---|---|---|---|

<IFR type 1>
Requests an ID (physical address) from one receive node as an in-frame response.

| SOF | HEADER | DATA | CRC | EOD | ID | EOF |
|---|---|---|---|---|---|---|

<IFR type 2>
Requests an ID from multiple receive nodes as an in-frame response. In this type, an ID is sent from the receive nodes in sequence according to their ID priority.

| SOF | HEADER | DATA | CRC | EOD | ID1 | · · · | IDn | EOF |
|---|---|---|---|---|---|---|---|---|

<IFR type 3>
Request multi-byte data with CRC from one receive node as an in-frame response.

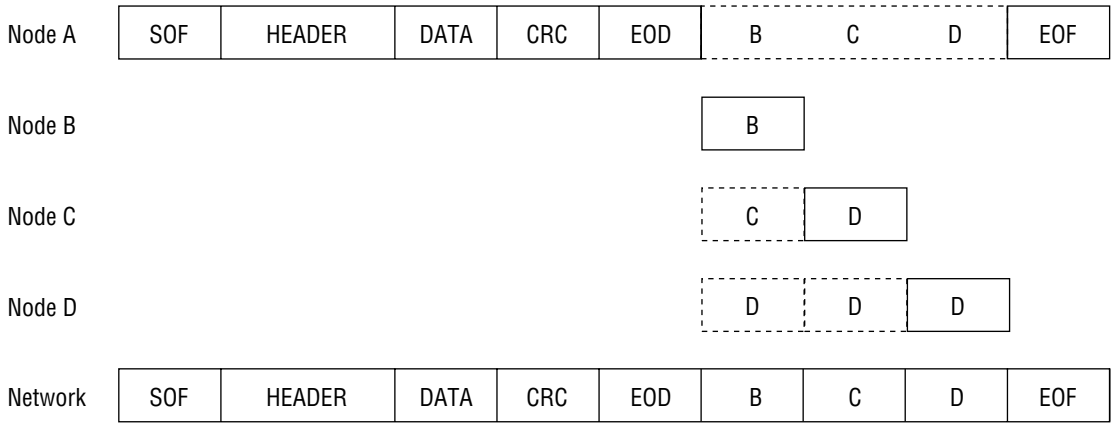
| SOF | HEADER | DATA | CRC | EOD | IFR DATA | CRC | EOF |
|---|---|---|---|---|---|---|---|

### 1.6.2 Message type

Message types are classified by a combination of address type setting bit Y and the in-frame response type setting bits K, Z1 and Z0.

(a) Functional address +IFR type 2

Since the functional address is specified as the address of the receive node, multiple nodes can receive a message. The physical address (ID) is requested from all of the receive nodes as a response. Node A=message transmission node, Nodes B, C and D=message receive nodes and message status on the network are shown below.

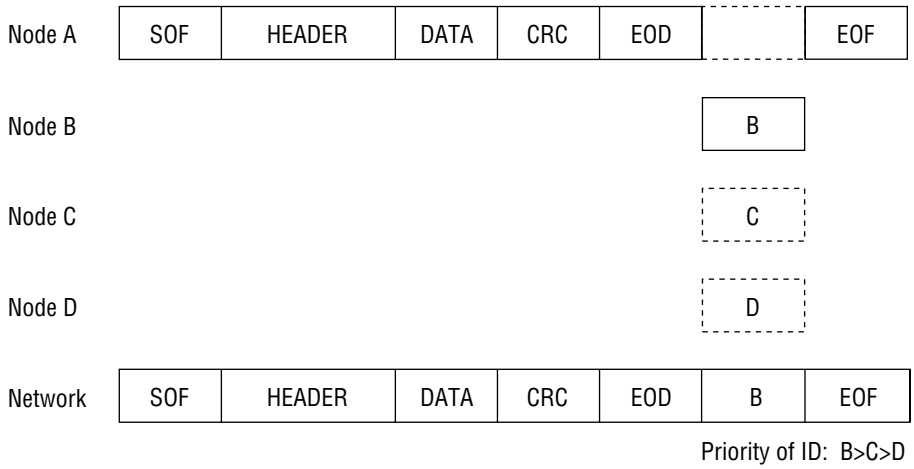



Priority of ID: B>C>D

When each message receive node enters the in-frame response transmission area, each message receive node starts to send an ID. The sequence of sending a response starts from the receive node with the higher priority ID. A node with a low priority ID waits for completion of the response transmission of the nodes with higher priority IDs, and then starts sending a response. Nodes which have completed a response transmission do not send a response again. Such a response transmission process is repeated for the number of receive nodes.

(b) Functional address + IFR type 1

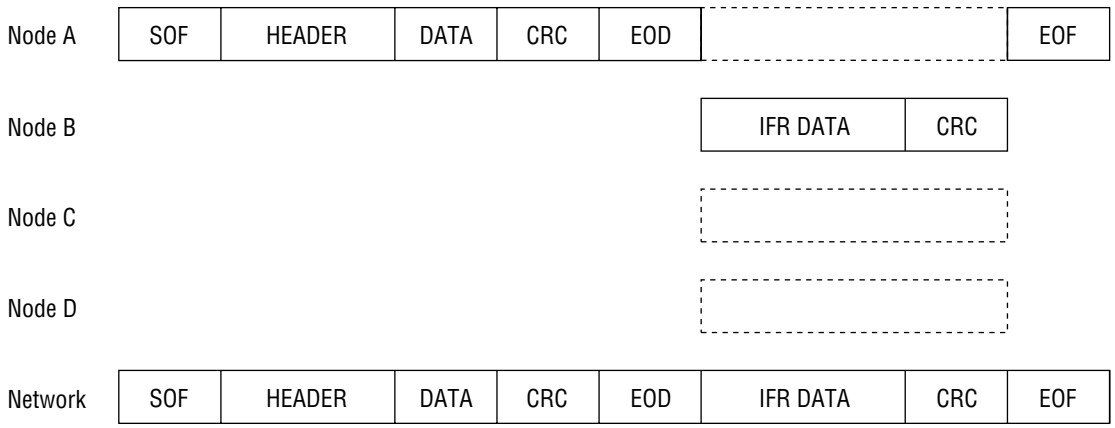
An ID is sent from multiple nodes as a response, just as in "(a)", but a response is sent only from the receive node with the highest priority ID, and response transmission is completed. A response is sent only once. The other receive nodes cannot send a response.




Priority of ID: B>C>D

(c) Functional address + IFR type 3

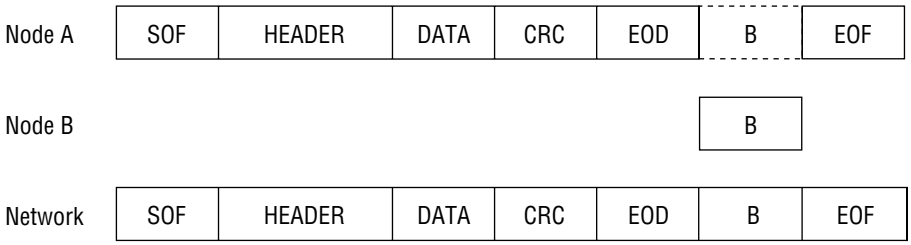
Multiple byte data with CRC is sent from multiple nodes as a response. In this case as well, just as in "(b)", only the receive node with the highest priority sends a multiple byte data response, and the response transmission is completed. A response is sent only once. The other receive nodes cannot send a response.




Priority of IFR DATA: B>C>D

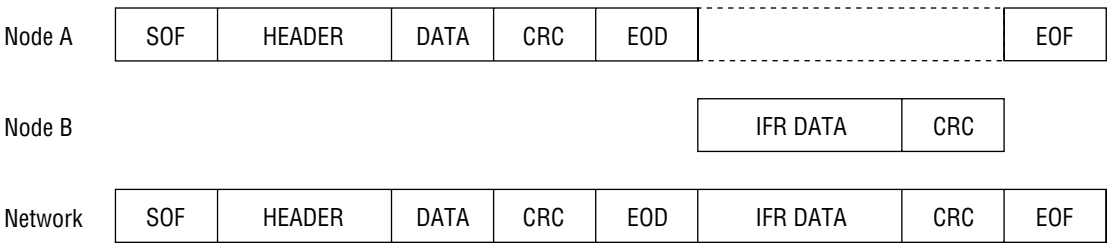
(d) Physical address +IFR type 1

Since a physical address is specified as the address of the receive node, one node receives the message. In this case, communication is one to one, and the message receive node sends an ID as the response.



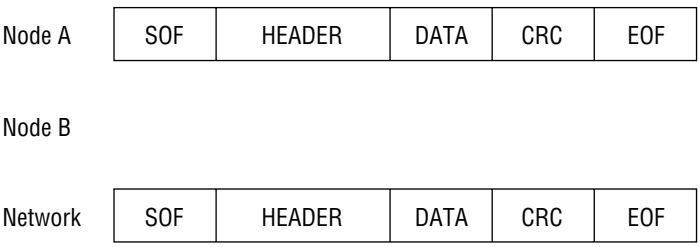

(e) Physical address +IFR type 3

Communication is one to one, just as in "(d)", and the message receive node sends multi-byte data with CRC as a response.




(f) Physical address or functional address +IFR type 0

Since a response is not requested, the message frame is completed when the message transmission ends. In this case, message transmission node completes the transmission operation without judging whether the message receive node received the message normally.



*Chapter 2*

# MSM6636 INTERNAL REGISTER LIST

## 2. MSM6636 INTERNAL REGISTER LIST

The MSM6636 internal register list is shown below. For details on each register, see “2.1 Description on internal registers”.

**Table 2-1 Internal Register List (1/2)**

| Address | MSB | — | — | — | — | — | — | LSB | Register Content | Register Name | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | H | P2 | P1 | P0 | K | Y | Z1 | Z0 | Communication type | Transmission register | W |
| 01 | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | Receive destination address | | |
| 02 | — | — | — | — | — | — | — | — | — | | |
| 03 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Transmission data | | |
| 04 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Transmission data | | |
| 05 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Transmission data | | |
| 06 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Transmission data | | |
| 07 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Transmission data | | |
| 08 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Transmission data | | |
| 09 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Transmission data | | |
| 0A | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Transmission data | | |
| 0B | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | IFT data | Response register | |
| 0C | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | IFT data | | |
| 0D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | IFT data | | |
| 0E | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | IFT data | | |
| 0F | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | IFT data | | |
| 10 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | IFT data | | |
| 11 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | IFT data | | |
| 12 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | IFT data | | |
| 13 | — | — | — | — | DL3 | DL2 | DL1 | DL0 | Transmission data length | Transmission status register | |
| 14 | — | — | — | — | RL3 | RL2 | RL1 | RL0 | Response data length | | |
| 15 | H | P2 | P1 | P0 | K | Y | Z1 | Z0 | Communication type | Receive register | R |
| 16 | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | Receive destination address | | |
| 17 | TA7 | TA6 | TA5 | TA4 | TA3 | TA2 | TA1 | TA0 | Transmission source address | | |
| 18 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Receive data | | |
| 19 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Receive data | | |
| 1A | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Receive data | | |
| 1B | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Receive data | | |
| 1C | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Receive data | | |
| 1D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Receive data | | |
| 1E | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Receive data | | |
| 1F | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Receive data | | |

**Table 2-1 Internal Register List (2/2)**

| Address | MSB | — | — | — | — | — | — | LSB | Register Content | Register Name | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 20 | — | — | — | — | RL3 | RL2 | RL1 | RL0 | Receive data length | Receive data length register | R |
| 21 | — | — | — | — | — | — | — | — | Completion command | Initialization/RD completion register | W |
| 22 | LEN | ABN | D–P | OVER | CRC | FORM | INV | IFS | Message abnormality flag | Interrupt request flag | R/W |
| 23 | BUSY | NOACK | NRSP | — | BRK | RSP | RCV | TR | Message transmission /receive flag | | |
| 24 | PAR | — | WAKR | WAKD | BPG | BPV | BNG | BNV | LAN bus flag | | |
| 25 | LEN | ABN | D–P | OVER | CRC | FORM | INV | IFS | Message abnormality flag | Interrupt enable flag | |
| 26 | BUSY | NOACK | NRSP | — | BRK | RSP | RCV | TR | Message transmission /receive flag | | |
| 27 | PAR | — | WAKR | WAKD | BPG | BPV | BNG | BNV | LAN bus flag | | |
| 28 | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 | Sleep command | Sleep command register | W |
| 29 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | BRK transmission command | Break command register | |
| 2A | D2 | D1 | D0 | PBO | NBO | NAK | N1 | N0 | Mode setting | Mode setting register | R/W |
| 2B | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 | Physical address | Physical address register | |
| 2C | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | Functional address register | |
| 2D | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 2E | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 2F | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 30 | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 31 | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 32 | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 33 | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 34 | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 35 | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 36 | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 37 | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 38 | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 39 | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 3A | FA7 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | Functional address | | |
| 3B | NA7 | NA6 | NA5 | NA4 | NA3 | NA2 | NA1 | NA0 | NAK return date | NAK register | |

## 2.1 Description of Internal Registers

Data read and write enable/disable and the status at reset of MSM internal registers are listed below.

**Table 2-2 Description on Internal Registers**

| Internal Address | R/W | Register Name | Status at Reset |
|---|---|---|---|
| 00H~0AH | W | Transmission register | Undefined |
| 0BH~12H | W | Response register | Undefined |
| 13H~14H | W | Transmission status register | 00H |
| 15H~1FH | R | Receive register | Undefined |
| 20H | R | Receive data length register | 00H |
| 21H | W | Initialization/RD completion register | — |
| 22H~24H | R/W | Interrupt request flag | 00H |
| 25H~27H | R/W | Interrupt enable flag | 00H |
| 28H | W | Sleep command register | 00H |
| 29H | W | Break command register | 00H |
| 2AH | R/W | Mode setting register | Undefined |
| 2BH | R/W | Physical address register | Undefined |
| 2CH~3AH | R/W | Functional address register | Undefined |
| 3BH | R/W | NAK register | Undefined |

A) Transmission register

A register to write a message for transmission. The content of this register is sent as a message. Write the priority of the message, message type, receive destination address and arbitrary transmission data. The register does not exist at address 02H, but the physical address value at address 2.

BH is automatically sent as the transmission source address when a message is sent. Since CRC code is automatically added at the end of the message, it is not necessary to write CRC code to this register.

This register is write only, and cannot be read data. If this register is read, all 00H is read. Since the register does not exist at address 02H, any data can be written to 02H.

B) Response register

A register to write multi-byte data to be sent as an in-frame response when an IFR type 3 message is received. When sending a response, the number of bytes specified by address 14H is sent sequentially from address 0BH. Since a CRC code is automatically added at the end of the transmission response, it is not necessary to write CRC code to this register.

C) Transmission status register

Address 13H is a register to specify the transmission data length. Write the total number of bytes (excluding CRC) of the 3 byte header and the arbitrary transmission data. Message transmission starts by writing this register. A minimum of 3 bytes and a maximum of 12 bytes can be specified as the transmission data length. The maximum number of bytes, however, is different, depending on the type of message to be sent. Write the number of bytes such that the total number of bytes of the message to send and respond (including CRC) do not exceed 12 bytes. If the total number of bytes exceed 12 bytes, a message length error occurs (see “6.1 Receive message length error interrupt”), and normal communication cannot be performed.

Address 14H is a register to specify the IFR type 3 response data length. A minimum of 1 byte and maximum of 7 bytes can be specified as the response data length. Writing this register becomes the IFR type 3 response transmission standby command. This standby status is held until the IFR type 3 message is received, and a response is sent. This status can be reset by a reset input.

D) Receive register

A received message or response is stored sequentially from address 15H. If a message is received, only the received message (including CRC) is stored, the response is not stored. If a message to a request response is sent, only the received response (including the CRC of the response, in the case of an IFR type 3 response) is stored. A received message or response is stored to the receive register when a message frame ends. Since it is stored temporarily to another receive buffer when receiving a message or response, previous received data of the receive register can be read, even when receiving data. The content of the receive buffer, however, cannot be read. When a receive error occurs, data is not transferred from the receive buffer to the receive register, therefore received message data cannot be read at this time.

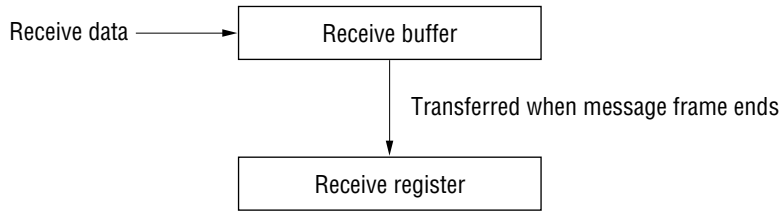



**Figure 2-1 Receive Register**

Newly received data is overwritten to the receive register. Since the receive register is not cleared, if the newly received data length is shorter than the previously received data length, the previously received data remains after the newly received data.

E) Receive data length register

The byte length (excluding CRC) of the receive data stored to the receive register is stored. When interrupt request flag RSP or RCV is set, the new receive data length is stored. After reading this register, read the receive register if necessary.

F) Initialization/RD completion register

After initializing or reading the receive register, receiving a new message or response is enabled by writing to this register. There is no specification on data to be written. If the new message or response receiving ends before writing to this register, an overrun error occurs (see “6.4 Overrun error interrupt”), and received data is not stored to the receive register. After inputting a reset, or when interrupt request flag RSP or RCV is set, be certain to write to this register.

G) Interrupt request flag

MSM6636 sets this flag and requests an interrupt to the CPU. There are message related flags, a LAN bus line related flag, etc. in an interrupt request flag. For details, see “6. CPU interrupt”.

H) Interrupt enable flag

Enables an interrupt generation to the CPU. For details, see “6. CPU interrupt”.

I) Sleep command register

MSM6636 enters sleep status by writing “AAH” to address 28H. In sleep status, the oscillation circuit stops and MSM6636 enters low current consumption mode. For details, see “8. Sleep function”.

J) Break command register

The break command is transmitted by writing “55H” to address 29H. For details, see “10. Break function”.

K) Mode setting register

This register sets the transmission speed, re-transmission function and a LAN bus output prohibit. Set this register first before initialization. For details, see MSM6636 Users Manual “3.11 Mode setting register”.

L) Physical address register

Set the physical address (ID) of each node.

M) Functional address register

The functional address is the address of nodes with the same function. A maximum of 15 types of functional addresses can be set. In the case of communication by functional addressing, 15 types of address values are automatically filtered in sequence. Even if 15 types are not used for functional addressing, all functional address registers are filtered. Set the functional address value to all address areas during initialization.

N) NAK register

Response data, to be transmitted when the NAK return function is used, is written. For details, see MSM6636 Users Manual “3.14 NAK register”.

*Chapter 3*

# INITIALIZING MSM6636

## 3. INITIALIZING MSM6636

### 3.1 Initializing Node

The following is an example of initializing one node connected to the LAN.

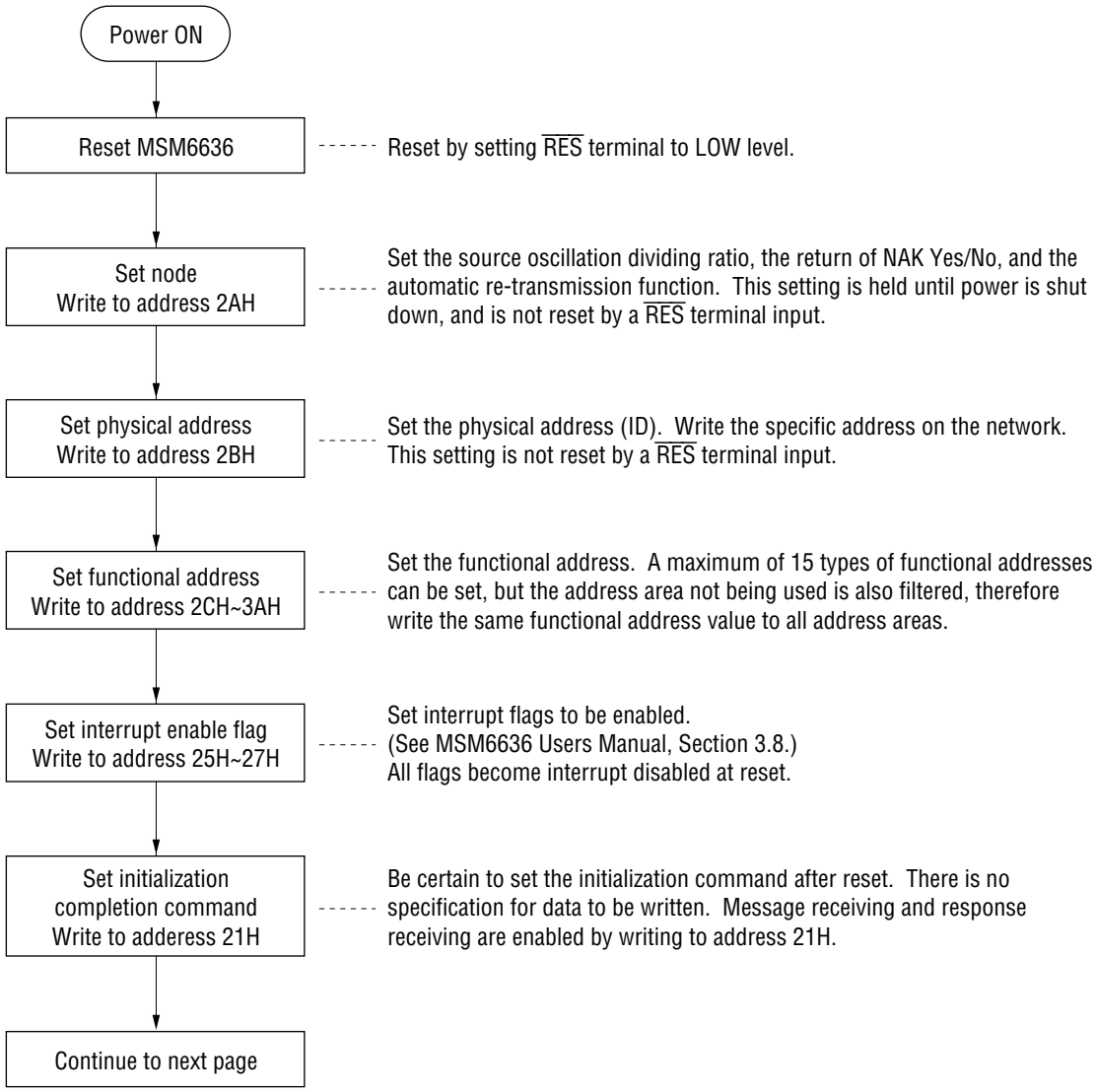



**Figure 3-1 Node Initialization Flow (1/2)**

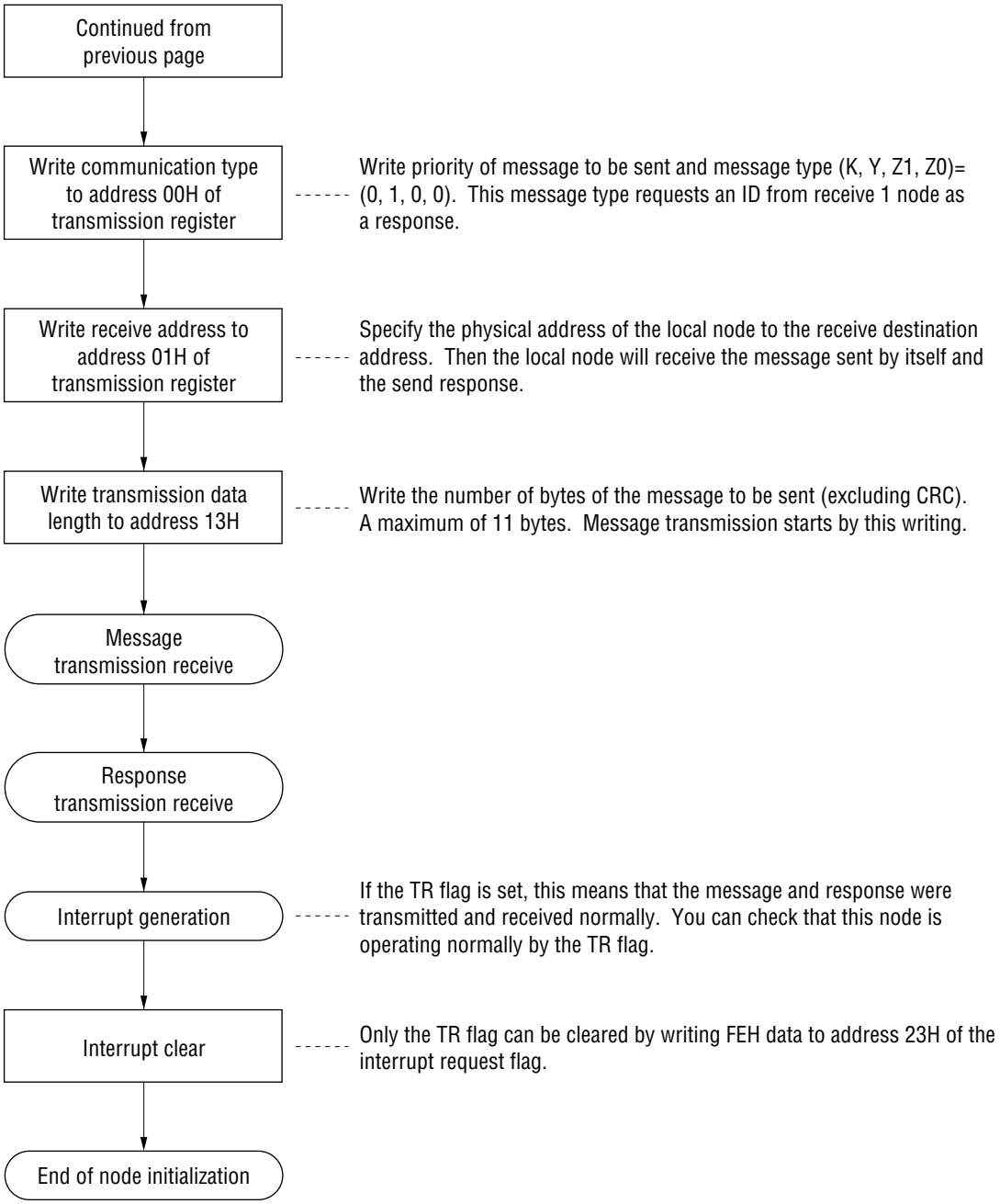



**Figure 3-1 Node Initialization Flow (2/2)**

## 3.2 Initializing Network

The following is an example of checking communication status among nodes connected on the network after all nodes are initialized.
In this example, one node (node A) sends a message to all other nodes, and checks that responses are returned from each node. This operation can check that connection of all nodes on the network is normal.

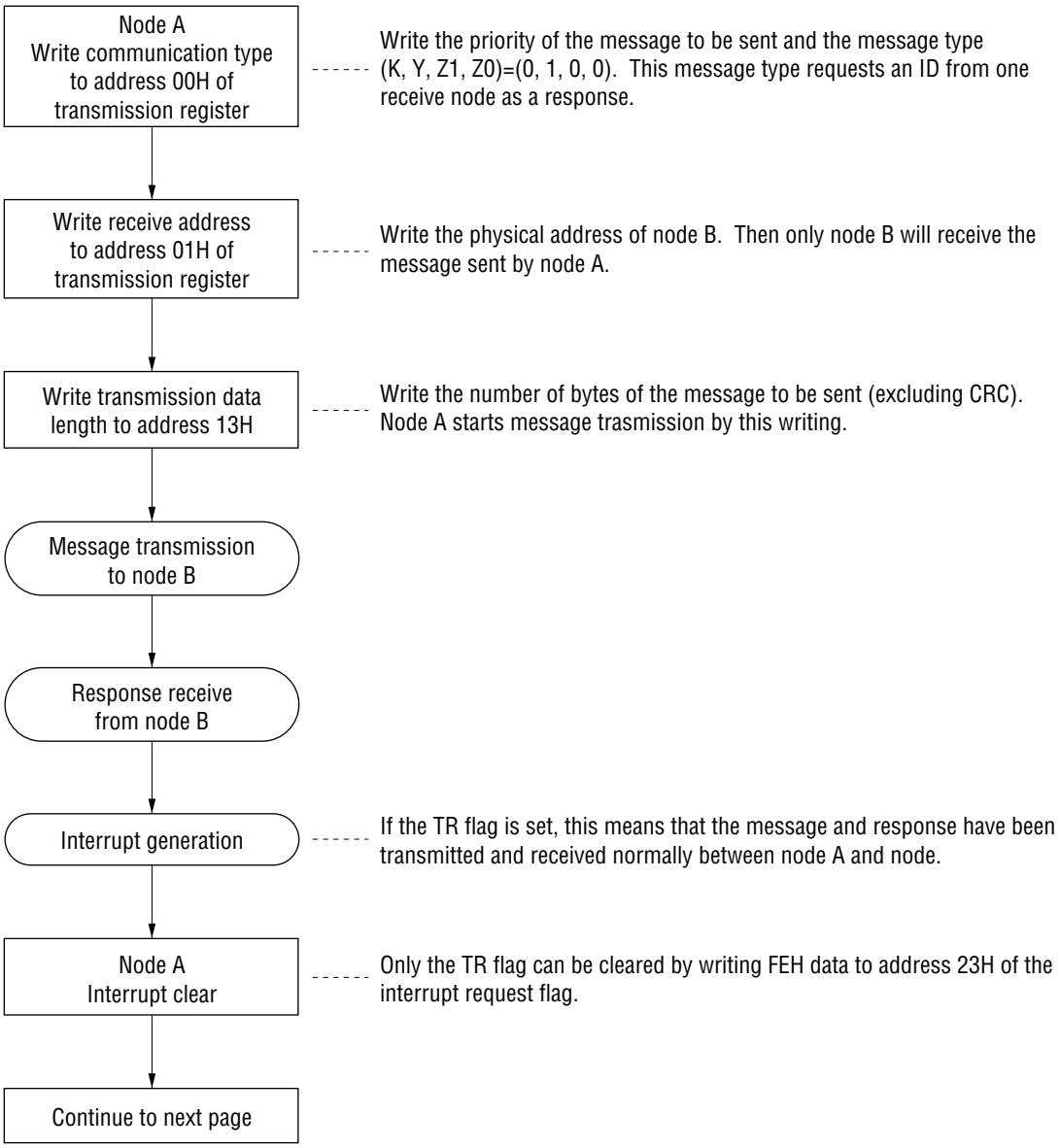



**Figure 3-2 Network Initialization Flow (1/2)**

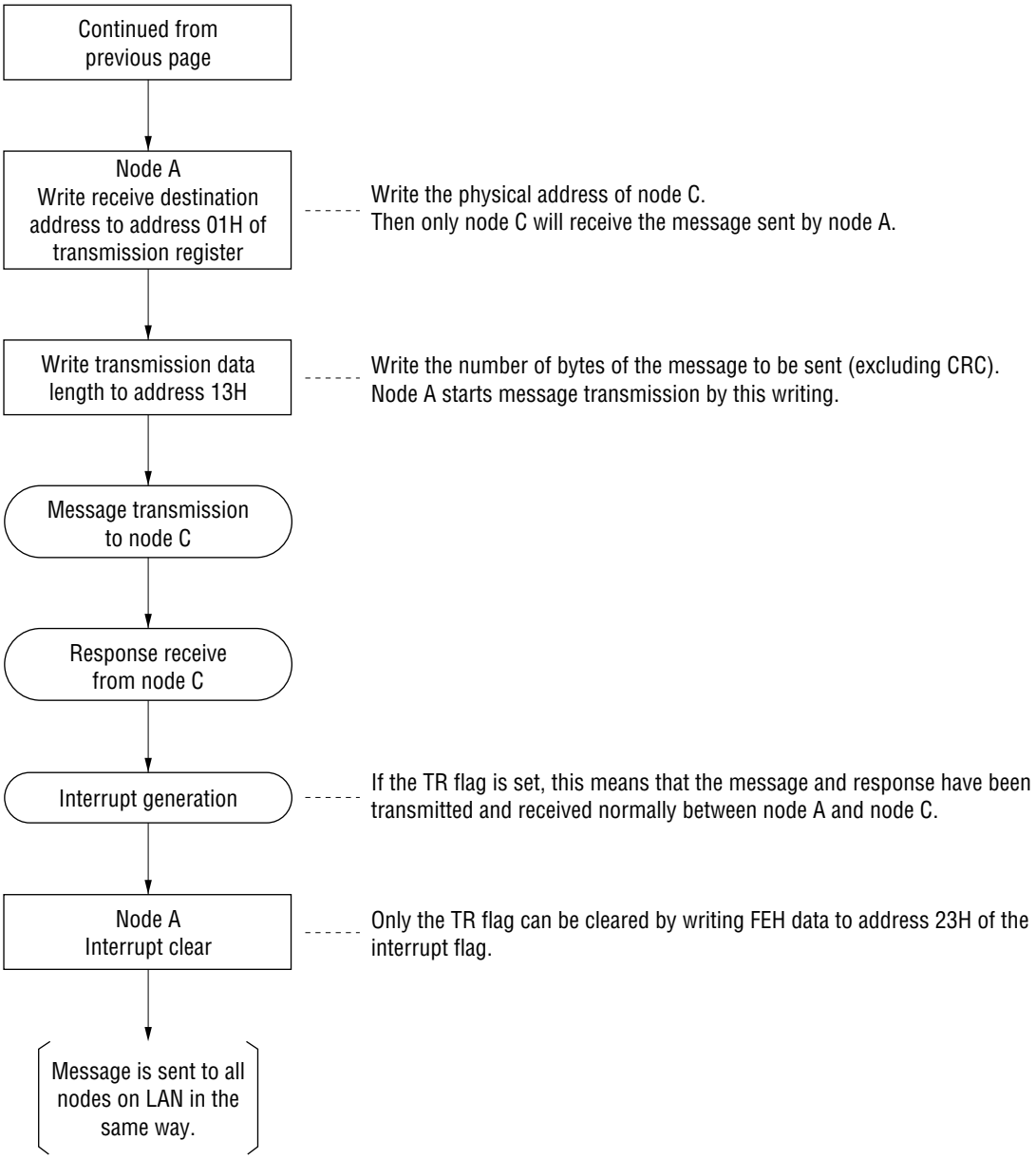



**Figure 3-2 Network Initialization Flow (2/2)**

*Chapter 4*

# MESAGE TRANSMISSION AND RESPONSE RECEIVE OPERATION

# 4. MESSAGE TRANSMISSION AND RESPONSE RECEIVE OPERATION

## 4.1 Message Transmission Operation of IFR Type 0

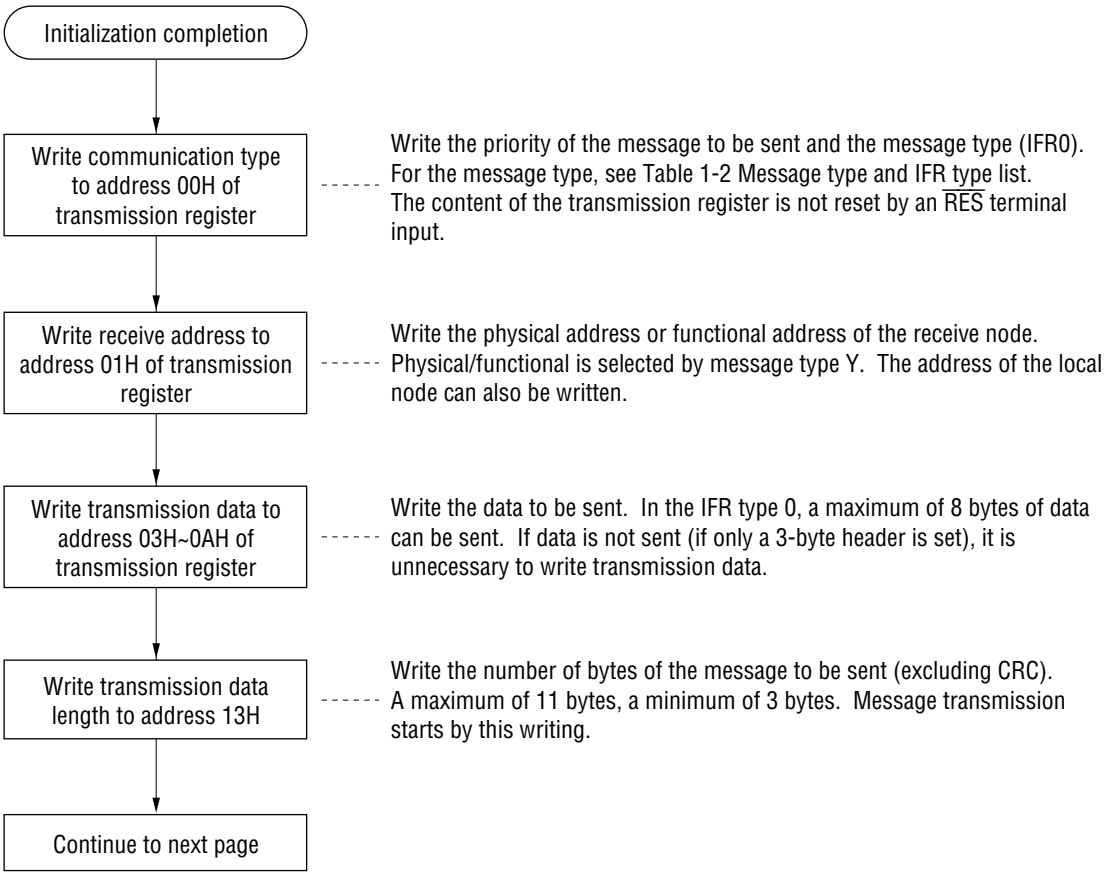



**Figure 4-1 IFR Type 0 Transmission Flow (1/2)**

## OKI: Keyed Text for Preceding Page

(A) If the LAN bus is in idle status when writing transmission data length ends, the operation moves to B. If another node is using the LAN bus at this time, operation move to H.

(B) Message transmission starts and operation moves to C.

(C) If lost in contension with the message of another node, operation moves to G, otherwise operation moves to D.

(D) If message transmission ends and “EOD” is detected, the interrupt request flag TR is set and operation moves to E.

(E) If the interrupt enable flag for the TR flag has been set, operation moves to F. If not, the message transmission operation ends.

(F) An interrupt signal is output from the INT terminal, and message transmission operation ends.

(G) If the number of times of bus busy re-transmission has been set to 2 at mode setting (address 2AH), and a bus busy has not yet been resent twice, operation moves to H. If a busy bus has been sent twice, of if the setting is no re-transmission, operation moves to I.

(H) After detecting that other nodes have finished using the LAN bus, operation moves to B.

(I) Interrupt request flag BUSY is set, and operation moves to J.

(J) If interrupt enable flag for the BUSY flag has been set, operation moves to F. If not, message transmission operation ends.

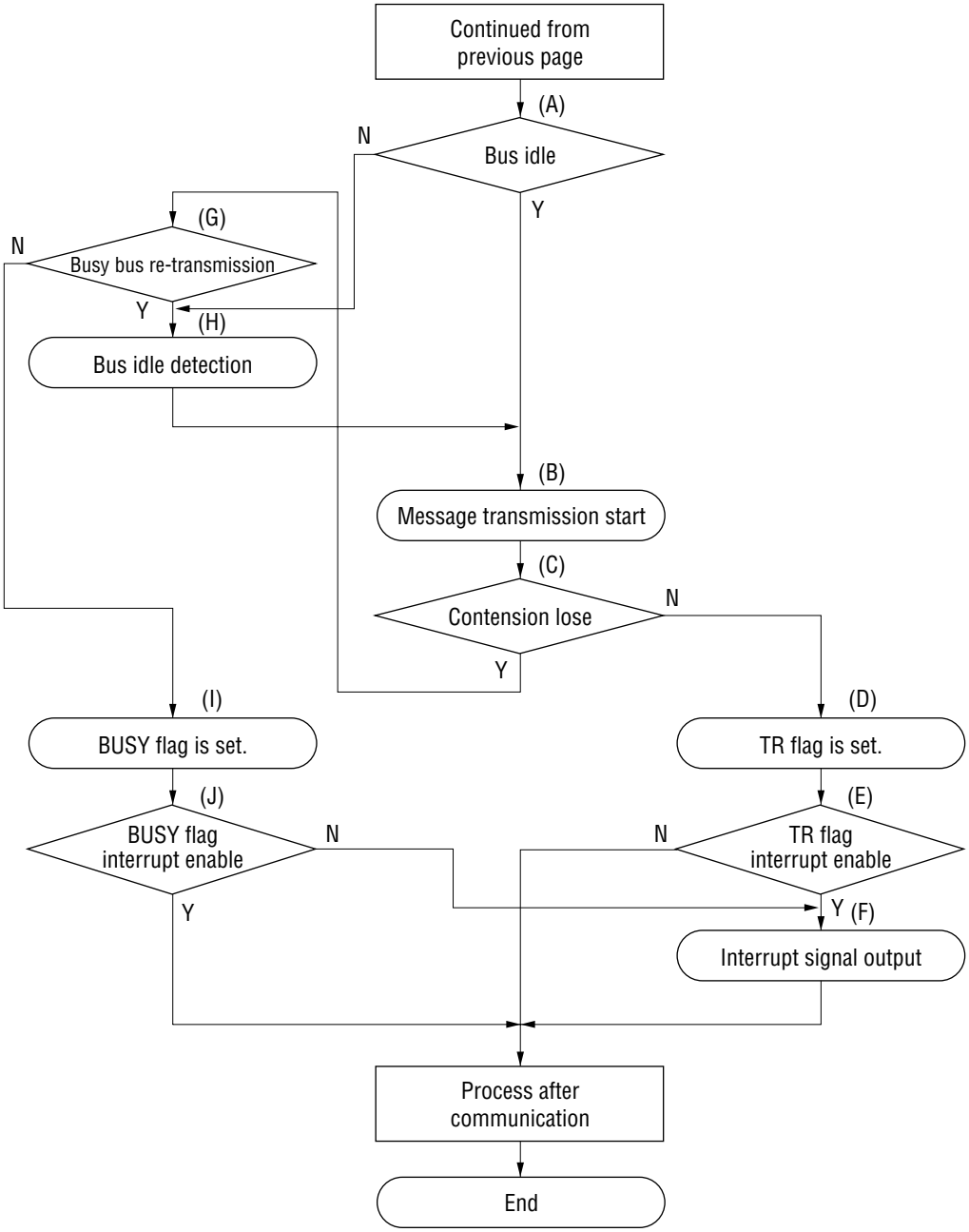



**Figure 4-1 IFR Type 0 Transmission Flow (2/2)**

## 4.2 Message Transmission and Message Receive Operation of IFR Type 1 (addressing by functional address)

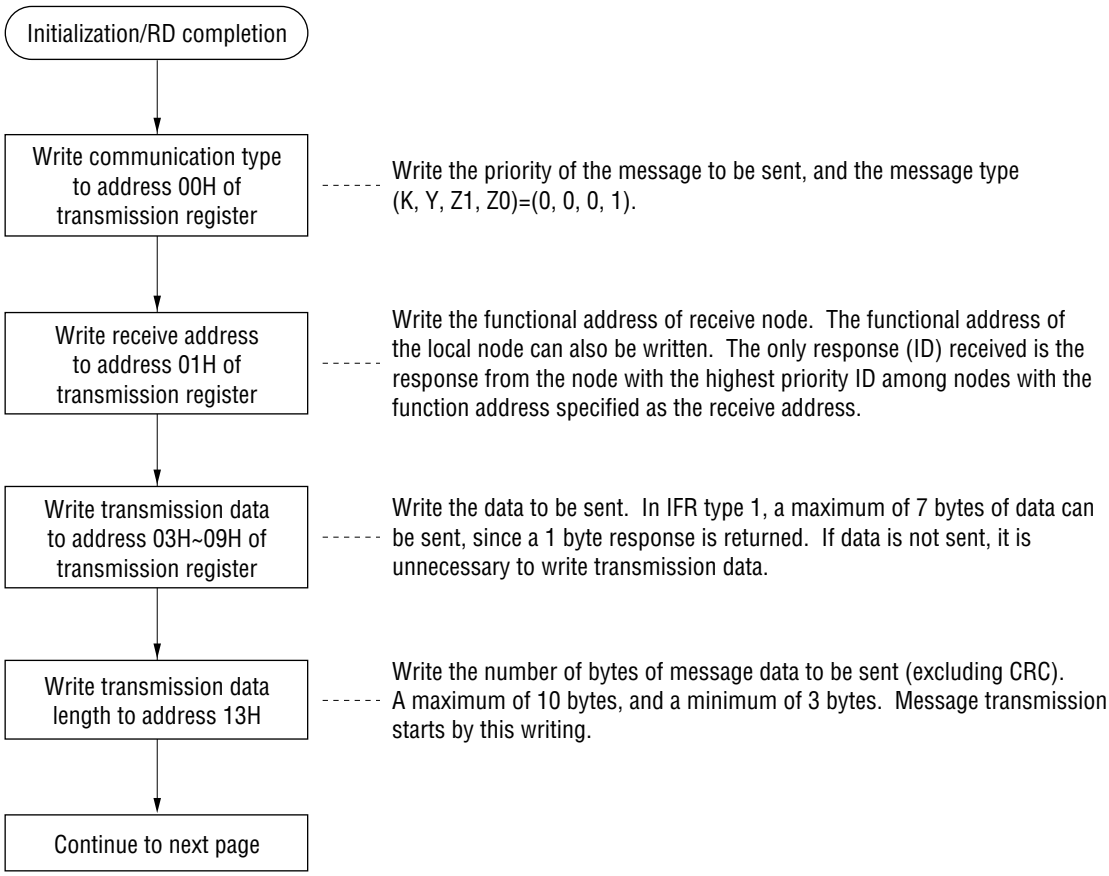



**Figure 4-2 IFR Type 1 (1) Transmission Flow (1/2)**

OKI: Keyed Text for Preceding Page

(A) If the LAN bus is in idle status when writing transmission data length ends, operation moves to B. If another node is using the LAN bus at this time, operation moves to K.

(B) Message transmission starts and operation moves to C.

(C) If lost in contension with the message of another node, operation moves to J, otherwise operation moves to D.

(D) If a response from the receive node is received normally, operation moves to E. If a response is not received, operation moves to N. Response at this time comes only from the node with the highest priority ID among nodes which received the message.

(E) If the initialization/RD completion command (address 21H) has been set, operation moves to F. If not, operation moves to Q.

(F) The received response is stored to the receive register (address 15H). Receive data length 01H is stored to the receive data length register (address 20H), and operation moves to G.

(G) Interrupt request flag TR and RSP are set, and operation moves to H.

(H) If the interrupt flag for TR or the RSP flag has been set, operation moves to I. It not, message transmission operation ends.

(I) An interrupt signal is output from the INT terminal, and message transmission operation ends.

(J) If the number of times of bus busy re-transmission has been set to 2 at mode setting (address 2AH), and a busy bus has not yet been resent twice, operation moves to K. If a busy bus has been sent twice, or if the setting is no re-transmission, operation moves to L.

(K) After detecting that other nodes finished using the LAN bus, operation moves to B.

(L) The interrupt request flag BUSY is set, and operation moves to M.

(M) If an interrupt enable flag for the BUSY flag has been set, operation moves to I. If not, message transmission operation ends.

(N) If the number of times to of a non ACK re-transmission has been set to 2 at mode setting (address 2AH), and a non ACK has not yet been resent twice, operation moves to K. If a non ACK has been sent twice, or if the setting is no re-transmission, operation moves to O.

(O) The interrupt request flag NOACK is set, and operation moves to P.

(P) If the interrupt enable flag for NOACK has been set, operation moves to I. If not, message transmission operation ends.

(Q) The interrupt request flag OVER is set, and operation moves to R. The response received at this time is not stored to the receive register.

(R) If the interrupt enable flag for the OVER flag has been set, operation moves to S. If not, operation moves to N.

(S) An interrupt signal is output from the INT terminal, and operation moves to N.

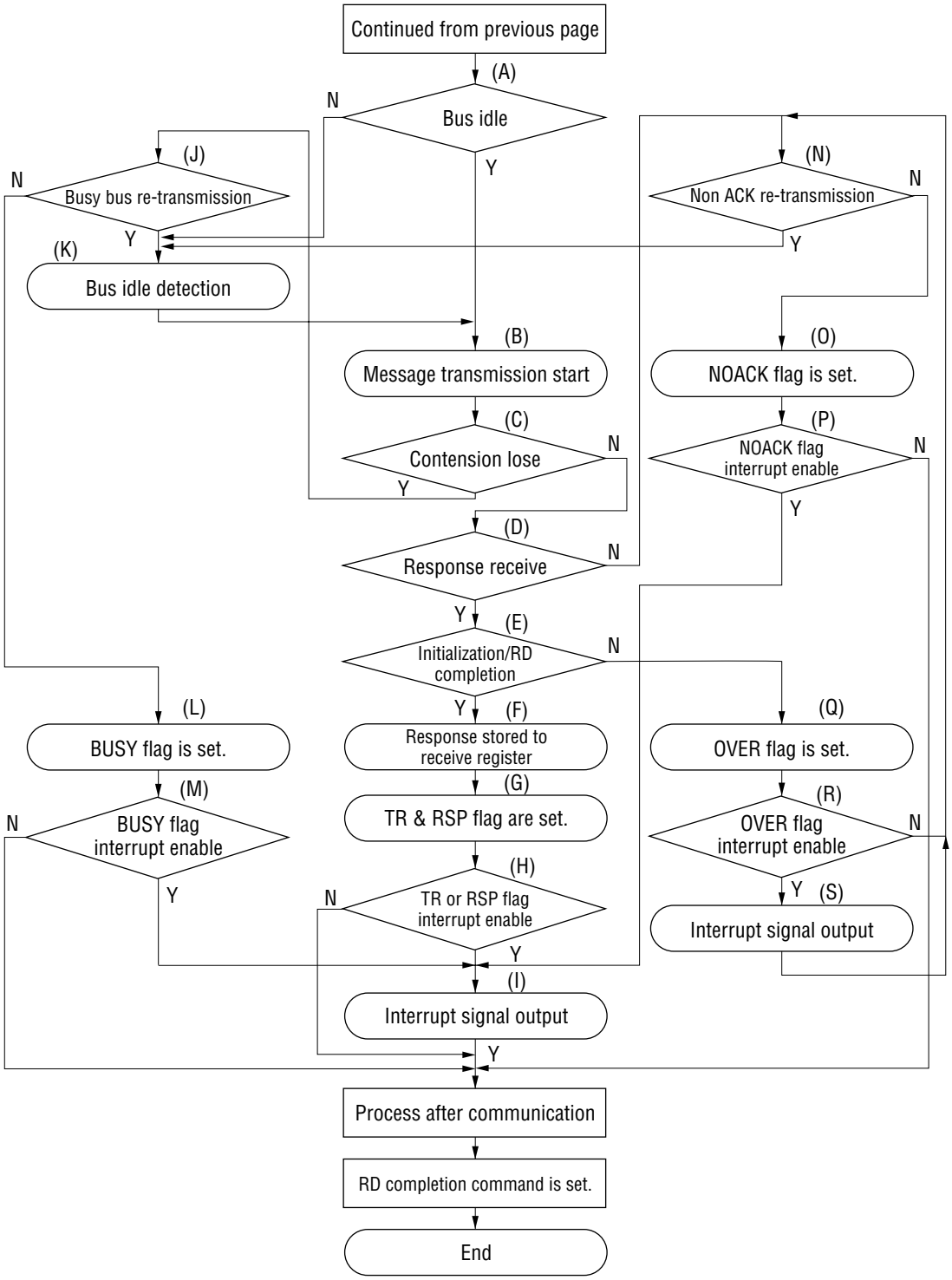



**Figure 4-2 IFR Type 1 (1) Transmission Flow (2/2)**

## 4.3 Message Transmission and Response Receive Operation of IFR Type 1 (addressing by physical address)

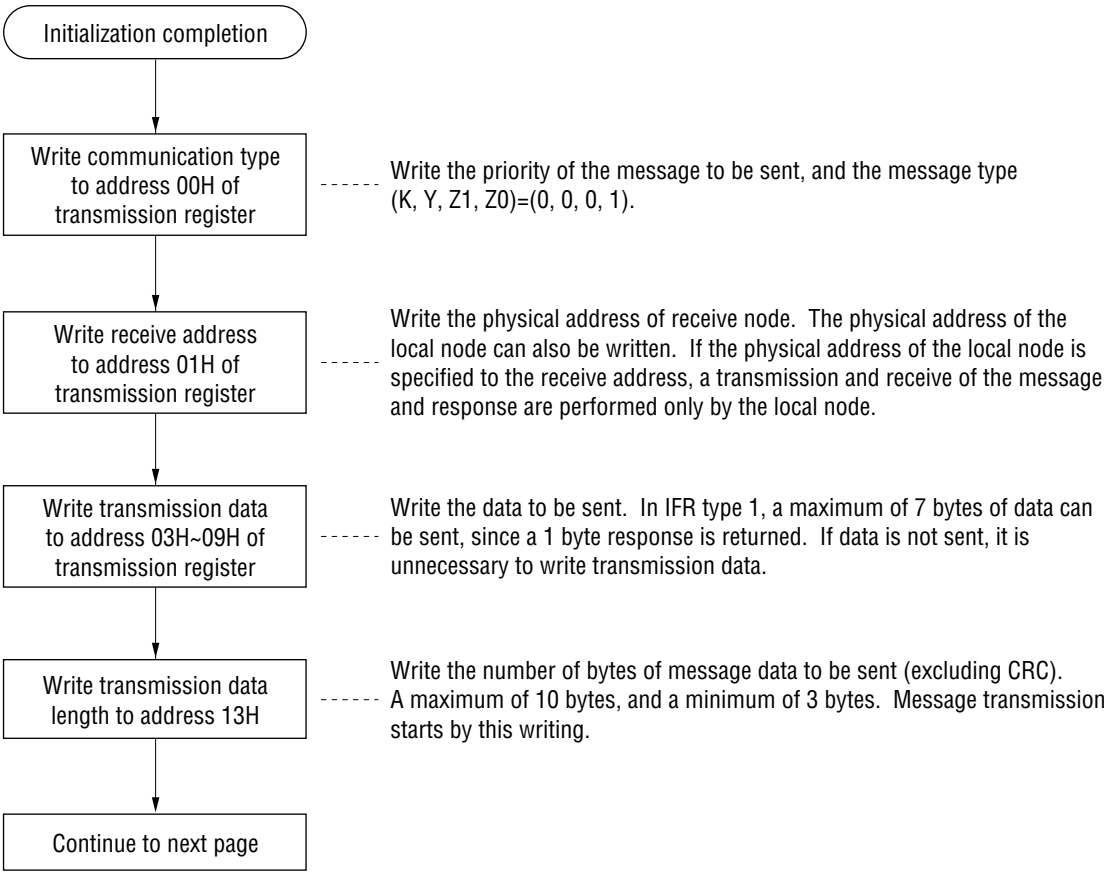



**Figure 4-3 IFR Type 1 (2) Transmission Flow (1/2)**

## OKI: Keyed Text for Preceding Page

(A) If the LAN bus is in idle status when writing transmission data length ends, operation modes to B. If another node is using the LAN bus at this time, operation moves to I.

(B) Message transmission starts and operation moves to C.

(C) If lost in contension with the message of another node, operation moves to H, otherwise operation moves to D.

(D) If the received response and address value specified as the receive address match, operation moves to E. If there is no match, or if a response was not returned, operation moves to L.

(E) Interrupt request flag TR is set, and operation moves to F. The response received at this time is not stored to the receive register, nor is the receive data length stored either.

(F) If the interrupt enable flag for the TR flag has been set, operation moves to G. If not, message transmission operation ends.

(G) An interrupt signal is output from the INT terminal, and message transmission operation ends.

(H) If the number of times of bus busy re-transmission has been set to 2 at mode setting (address 2AH), and a busy bus has not yet been resent twice, operation moves to I. If a busy bus has been sent twice, or if the setting is no re-transmission, operation moves to J.

(I) After detecting that other nodes finished using the LAN bus, operation moves to B.

(J) The interrupt request flag BUSY is set, and operation moves to K.

(K) If an interrupt enable flag for the BUSY flag has been set, operation moves to G. If not, message transmission operation ends.

(L) If the number of times of non ACK re-transmission has been set to 2 at mode setting (address 2AH), and a non ACK has not yet been resent twice, operation moves to I. If a non ACK has been sent twice, or if the setting is no re-transmission, operation moves to M.

(M) The interrupt request flag NOACK is set, and operation moves to N.

(N) If the interrupt enable flag for NOACK has been set, operation moves to G. If not, message transmission operation ends.

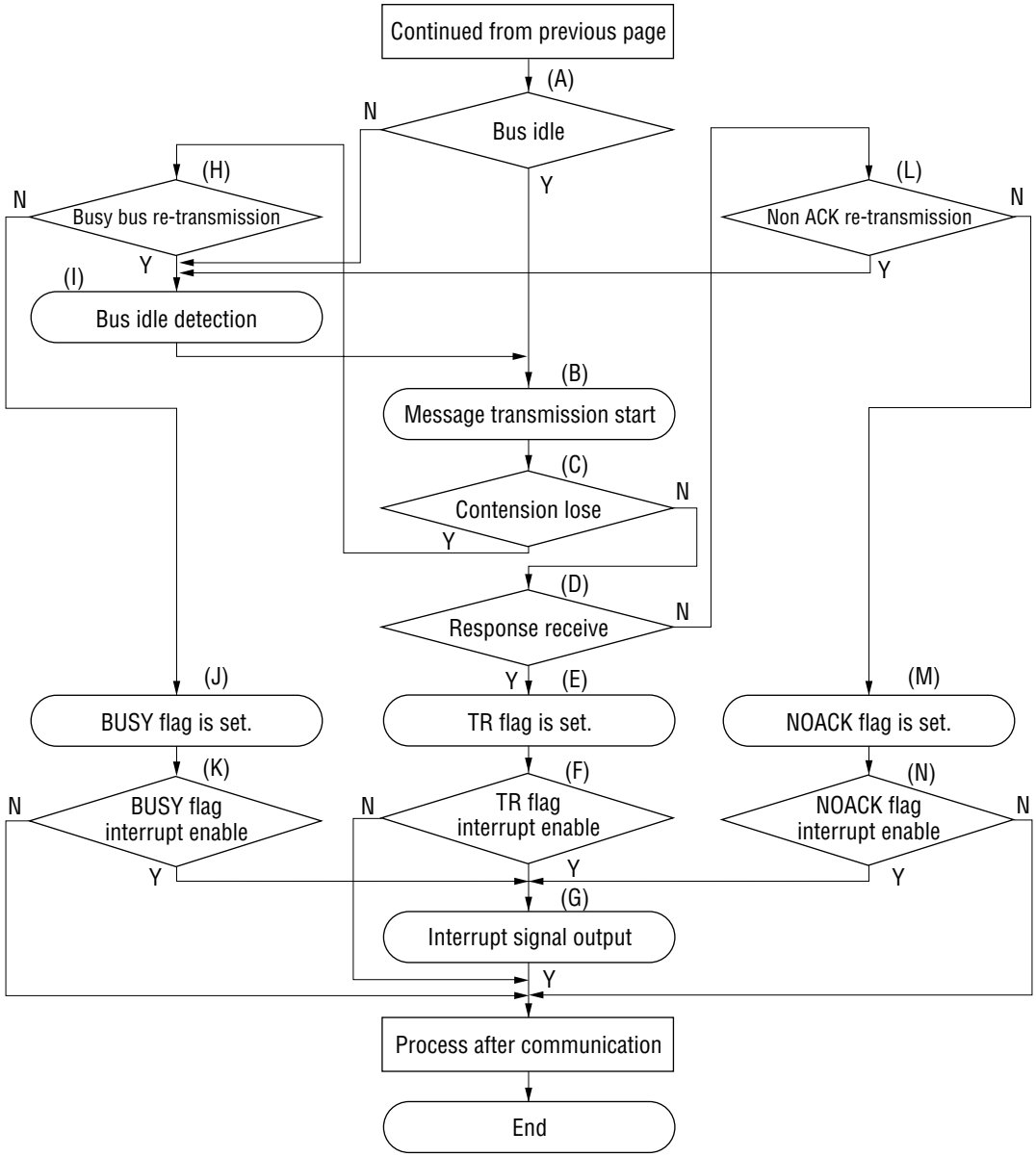



**Figure 4-3 IFR Type 1 (2) Transmission Flow (2/2)**

## 4.4 Message Transmission and Response Receive Operation of IFR Type 2

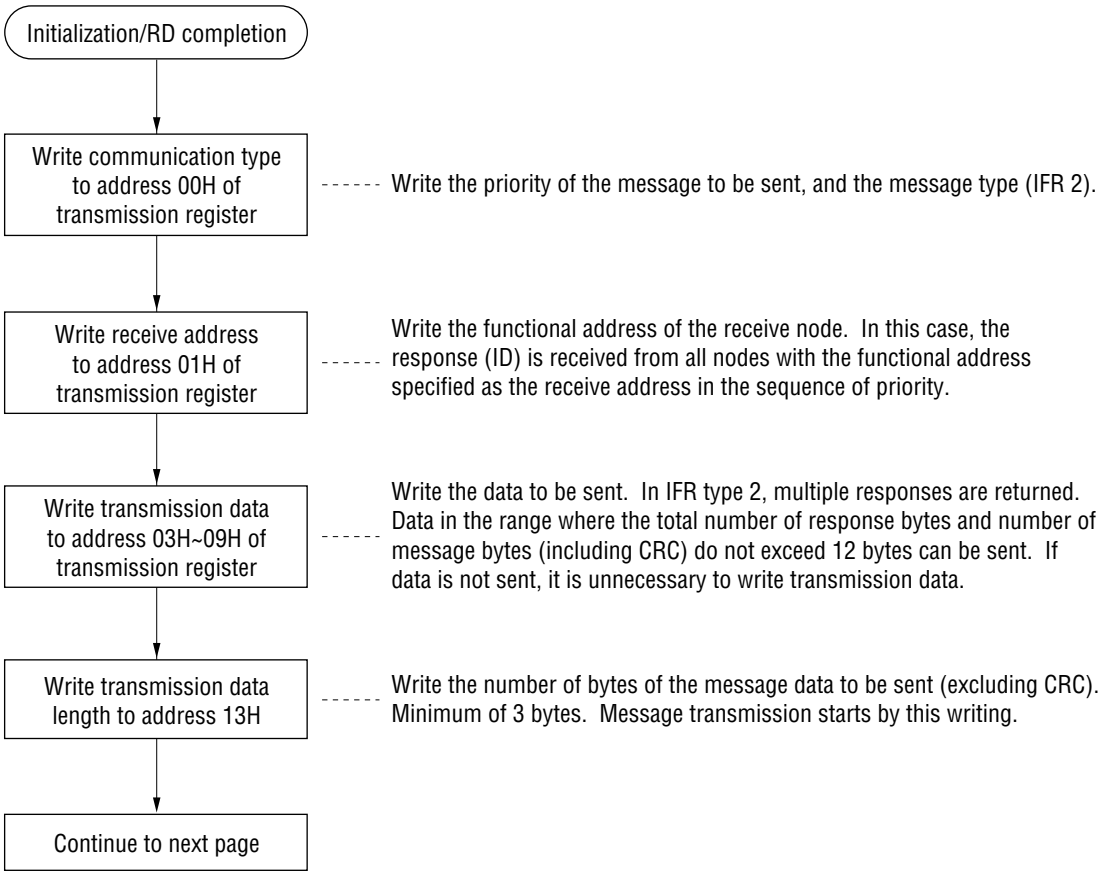



**Figure 4-4 IFR Type 2 Transmission Flow (1/2)**

A~S except D and F, are the same as 4.2 IFR type 1 (addressing by functional address)

(D) If responses from all receive nodes are received, operation moves to E, and if responses are not returned, operation moves to N. A maximum of 8 bytes of response can be received when the transmission data length (13H) is 3 bytes (excluding CRC).

(F) All received responses are stored from address 15H of the receive register in the sequence of priority. The receive data length (number of bytes of received responses) is stored to the receive data length register (address 20H), and operation moves to G.

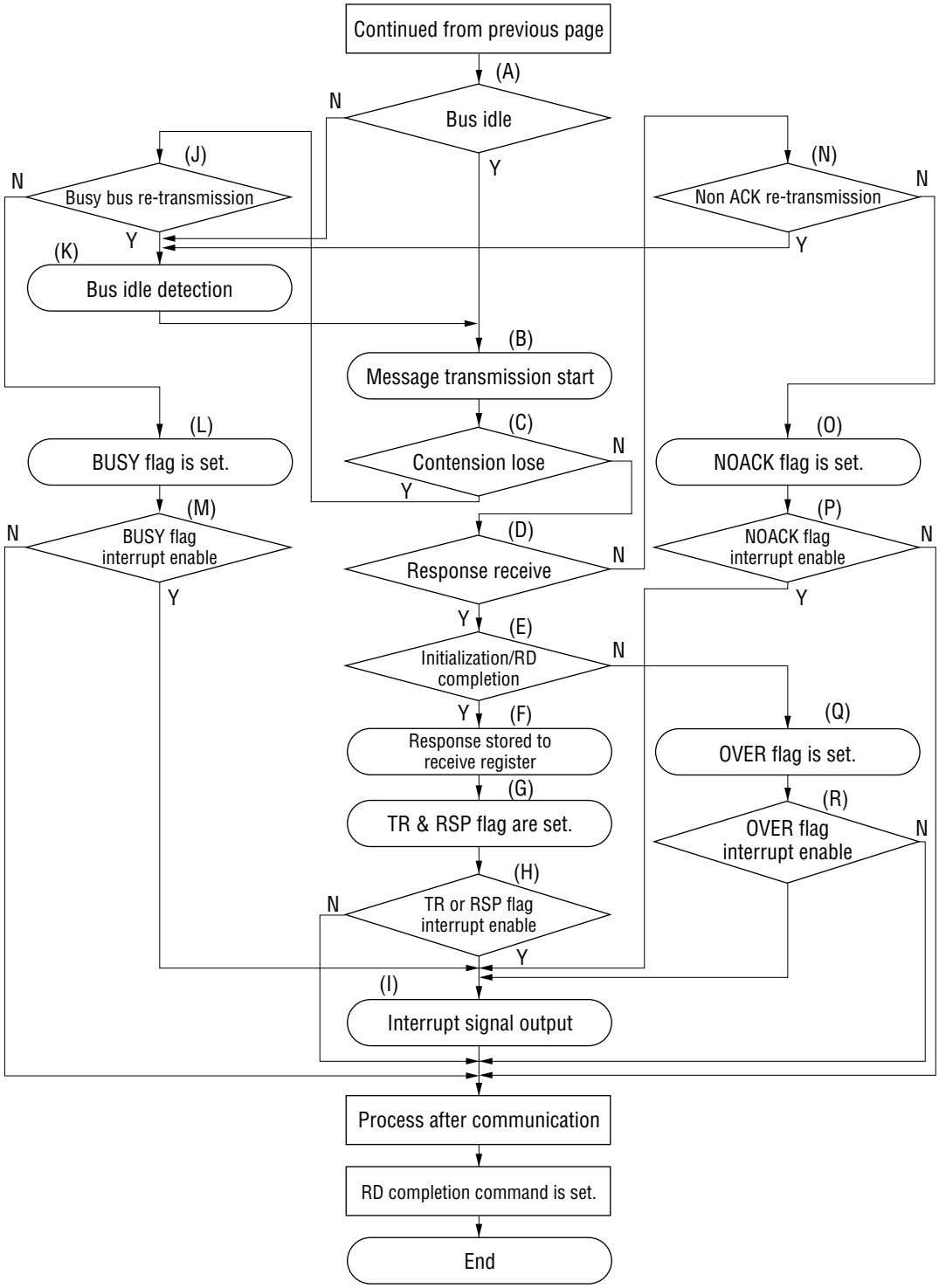



**Figure 4-4 IFR Type 2 Transmission Flow (2/2)**

## 4.5 Message Transmission and Response Receive Operation of IFR Type 3

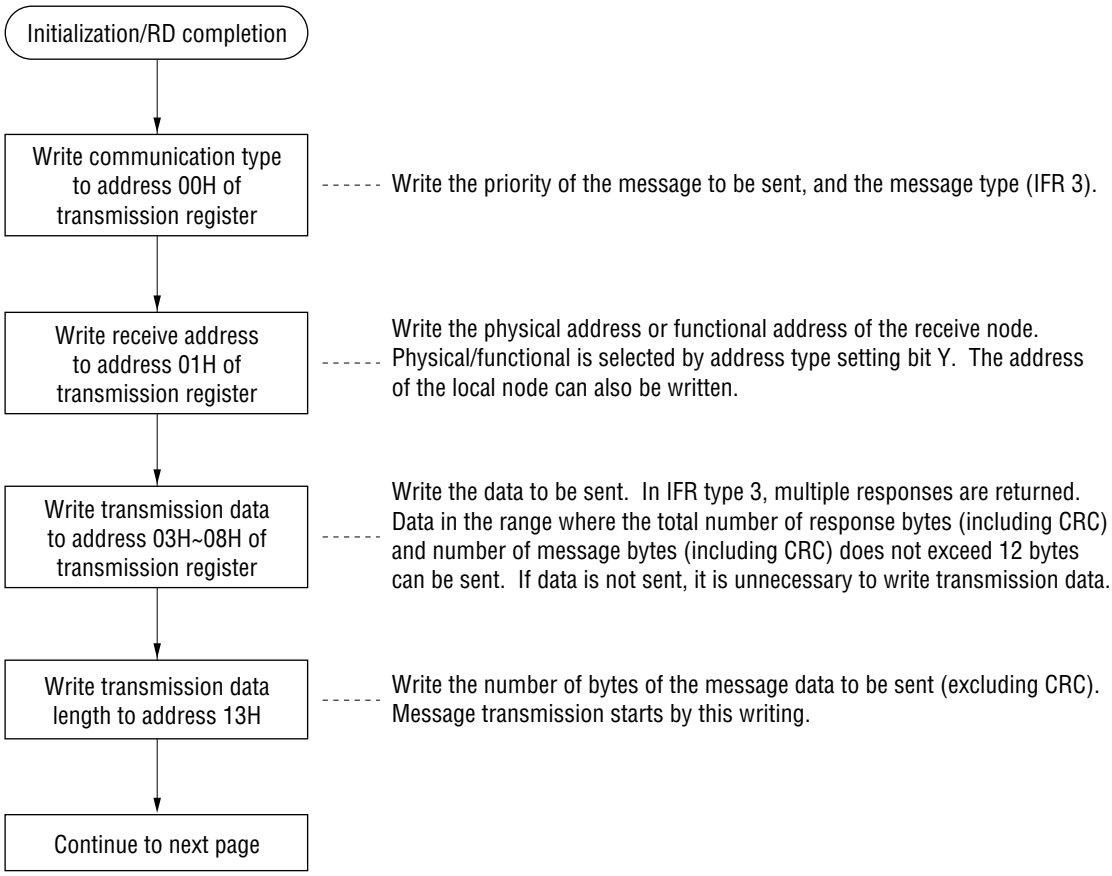



**Figure 4-5 IFR Type 3 Transmission Flow (1/2)**

## OKI: Keyed Text for Preceding Page

(A) If the LAN bus is in idle status when writing transmission data length ends, operation modes to B. If another node is using the LAN bus at this time, operation moves to L.

(B) Message transmission starts and operation moves to C.

(C) If lost in contension with the message of another node, operation moves to K, otherwise operation moves to D.

(D) If responses from all the receive nodes are received, operation moves to E and F, and if responses are not received, operation moves to Q.

(E) The CRC code of the received response is checked. If normal, operation moves to G, and if an error is detected, operation moves to T.

(F) If the initialization/RD completion command (address 21H) has been set, operation moves to G. If not, operation moves to O.

(G) If a CRC error and OVER error are not detected, all received responses are stored from address 15H of the receive register. The receive data length (excluding CRC) is stored to the receive data length register (address 20H), and operation moves to H.

(H) Interrupt request flag TR and RSP are set, and operation moves to I.

(I) If the interrupt enable flag for TR or the RSP have been set, operation moves to J. If not, message transmission operation ends.

(J) An interrupt signal is output from the INT terminal, and message transmission operation ends.

(K) If the number of times of bus busy re-transmission has been set to 2 at mode setting (address 2AH), and a busy bus has not yet been resent twice, operation moves to L. If a busy bus has been sent twice, or if the setting is no re-transmission, operation moves to M.

(L) After detecting that other nodes finished using the LAN bus, operation moves to B.

(M) The interrupt request flag BUSY is set, and operation moves to N.

(N) If an interrupt enable flag for the BUSY flag has been set, operation moves to J. If not, message transmission operation ends.

(O) Interrupt request flag OVER is set, and operation moves to P.

(P) If the interrupt enable flag for the OVER flag has been set, operation moves to V. If not, operation moves to Q.

(Q) If the number of times of non ACK re-transmission has been set to 2 at mode setting (address 2AH), and a non ACK has not yet been resent twice, operation moves to L. If a non ACK has been sent twice, or if the setting is no re-transmission, operation moves to R.

(R) The interrupt request flag NOACK is set, and operation moves to S.

(S) If the interrupt enable flag for NOACK has been set, operation moves to J. If not, message transmission operation ends.

(T) Interrupt request flag CRC is set, and operation moves to U.

(U) If the interrupt enable flag for the CRC flag has been set, operation moves to V, if not, operation moves to Q.

(V) An interrupt signal is output from the INT terminal, and operation moves to Q.

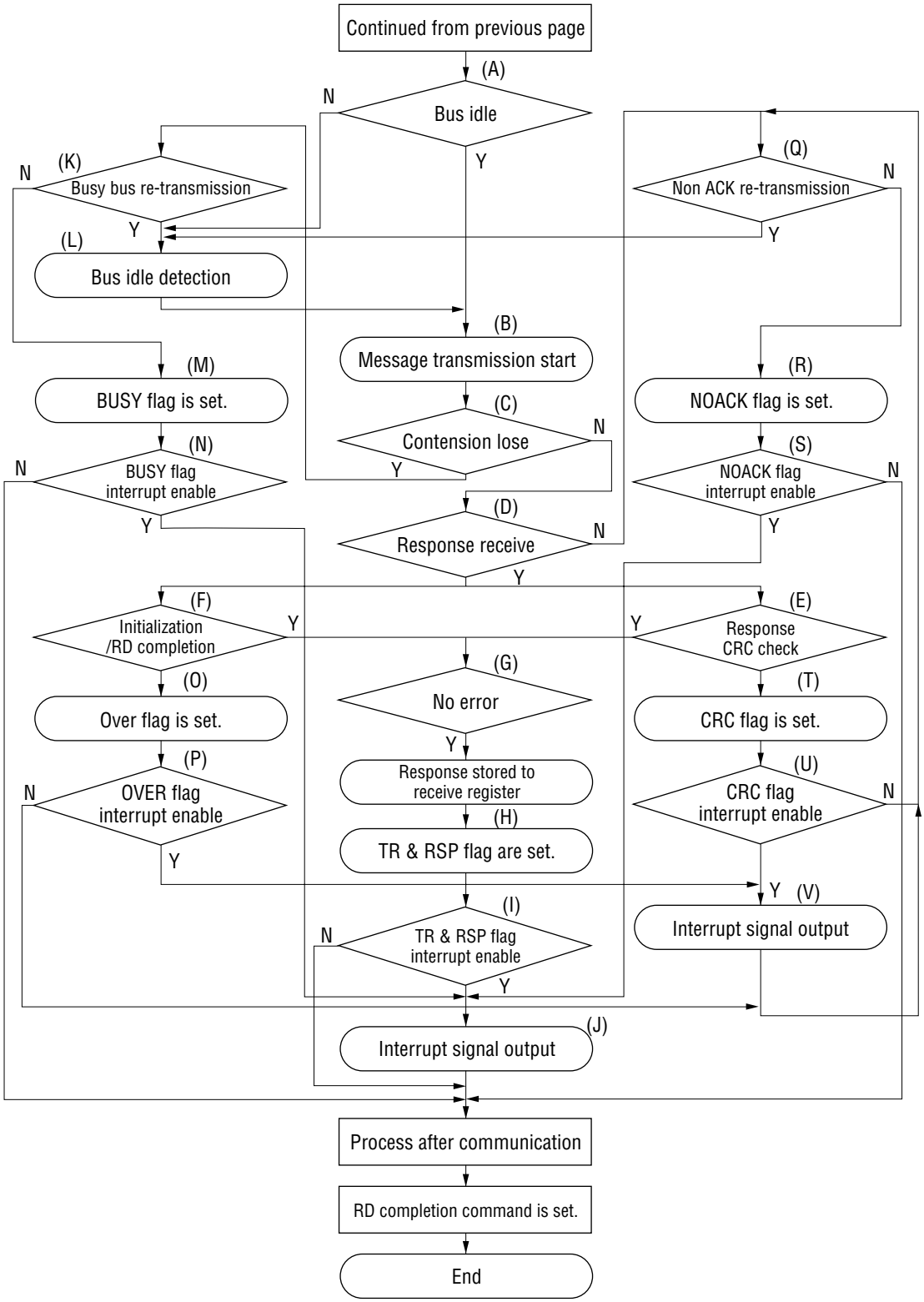



**Figure 4-5 IFR Type 3 Transmission Flow (2/2)**

*Chapter 5*

# MESSAGE RECEIVE AND RESPONSE TRANSMISSION OPERATION

## 5. MESSAGE RECEIVE AND RESPONSE TARNSMISSION OPERATION

### 5.1 Message Receive Operation of IFTR Type 0

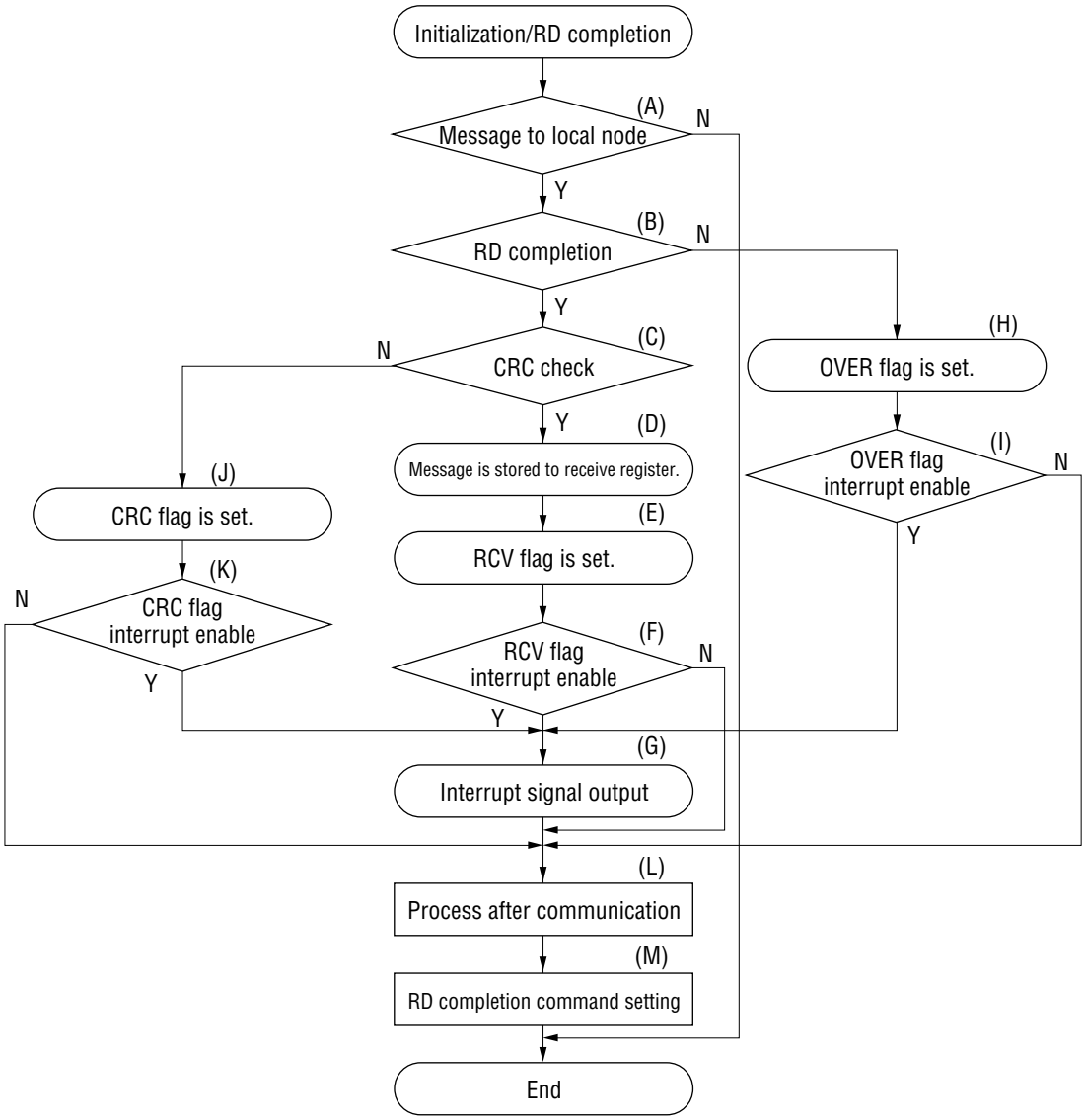



**Figure 5-1 IFR Type 0 Receive Flow**

(A) Receive address of received message and physical or functional address of local node are compared. Only if matched, the message is judged as a message to the local node, and operation moves to B. If not matched, receive operation ends.

(B) If the RD completion command has been set before receiving “EOD”, operation moves to C. If not, operation moves to H.

(C) The CRC code of the received message is checked. If normal, operation moves to D, if an error is detected, operation moves to J.

(D) All received messages are stored from address 15H of the receive register, and operation moves to E. The receive data length (excluding CRC) is stored to the receive data length register (address 20H).

(E) The interrupt request flag RCV is set, and operation moves to F.

(F) If the interrupt of the RCV flag is enabled, operation moves to G, and if not, the message receive operation ends, and operation moves to L.

(G) An interrupt signal is output from the INT terminal, the message receive operation ends, and operation moves to L.

(H) The interrupt request flag OVER is set, and operation moves to I.

(I) If the interrupt of the OVER flag is enabled, operation moves to G, and if not, the message receive operation ends, and operation moves to L.

(J) The interrupt request flag CRC is set, and operation moves to K.

(K) If the interrupt of the CRC flag is enabled, operation moves to G, and if not, the message receive operation ends, and operation moves to L.

(L) Processes after communication (reading receive register, clearing interrupt request flag, etc.) is performed.

(M) The RD completion command (address 21H) is set. This setting enables receiving the next message and response.

## 5.2 Message Receive and Response Transmission Operation of IFR Type 1

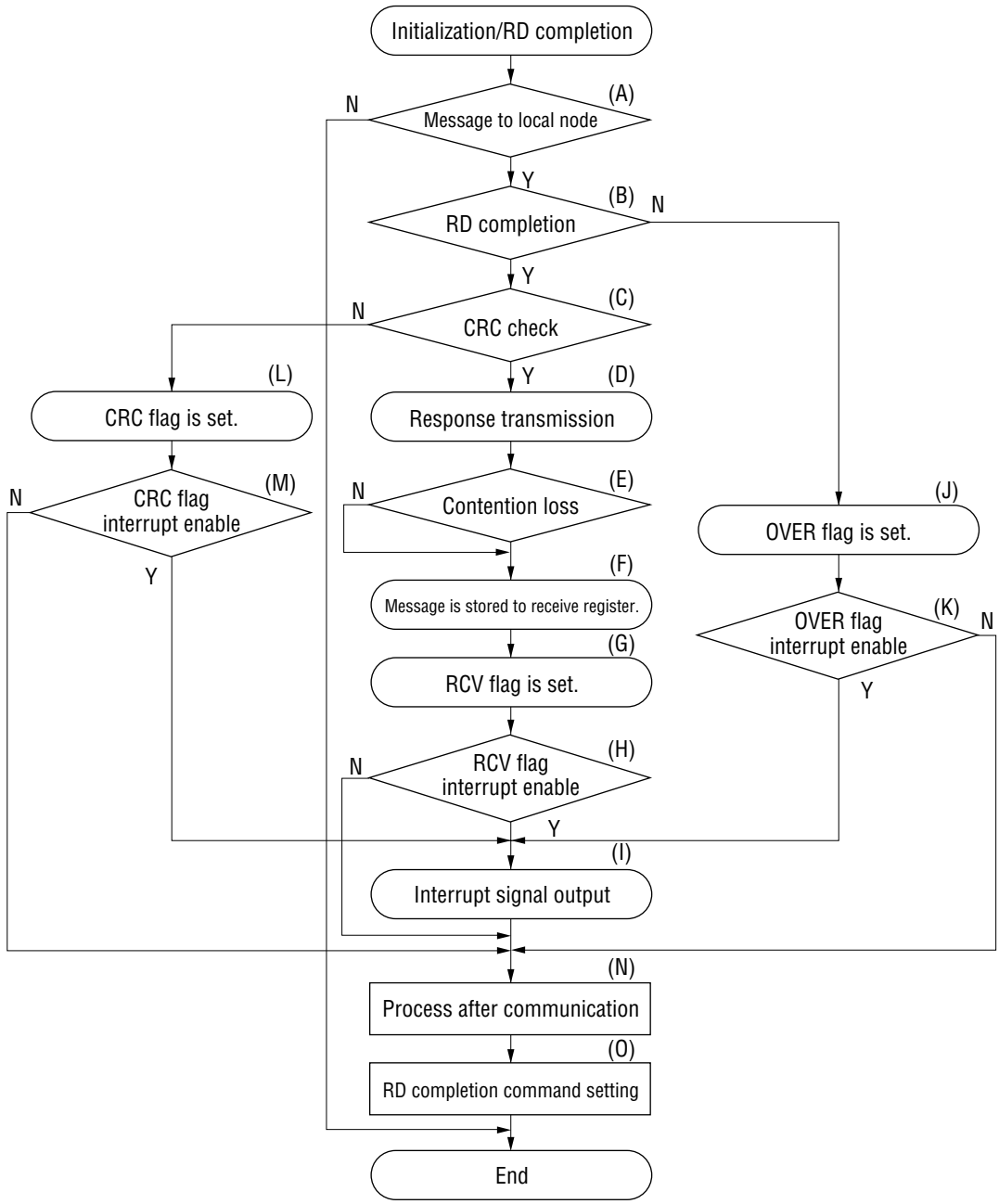



**Figure 5-2 IFR Type 1 Receive Flow**

(A) Receive address of received message and physical or functional address of local node are compared. Only if matched, the message is judged as a message to the local node, and operation moves to B. If not matched, receive operation ends.

(B) If the RD completion command has been set before receiving “EOD”, operation moves to C. If not, operation moves to J.

(C) The CRC code of the received message is checked. If normal, operation moves to D, if an error is detected, operation moves to L.

(D) The physical address value of the local node is sent as the response, and operation moves to E.

(E) If lost in contention with the response of another node, response transmission stops, and operation moves to F. Even if loss is not detected, operation still moves to F.

(F) All received messages are stored from address 15H of the receive register, and operation moves to G. The response is not stored. The number of bytes of the received message (excluding CRC and response) is stored to the receive message length register (address 20H).

(G) The interrupt request flag RCV is set, and operation moves to H.

(H) If the interrupt of the RCV flag is enabled, operation moves to I, and if not, the message receive operation ends, and operation moves to N.

(I) An interrupt signal is output from the INT terminal, message receive operation ends, and operation moves to N.

(J) The interrupt request flag OVER is set, and operation moves to K.

(K) If the interrupt of the OVER flag is enabled, operation moves to I, and if not, message receive operation ends, and operation moves to N.

(L) The interrupt request flag CRC is set, and operation moves to K.

(M) If the interrupt of the CRC flag is enabled, operation moves to I, and if not, message receive operation ends, and operation moves to N.

(N) Processes after communication (reading receive register, clearing interrupt request flag, etc.) is performed.

(O) The RD completion command (address 21H) is set. This setting enables receiving the next message and response.

## 5.3 Message Receive and Response Transmission Operation of IFR Type 2

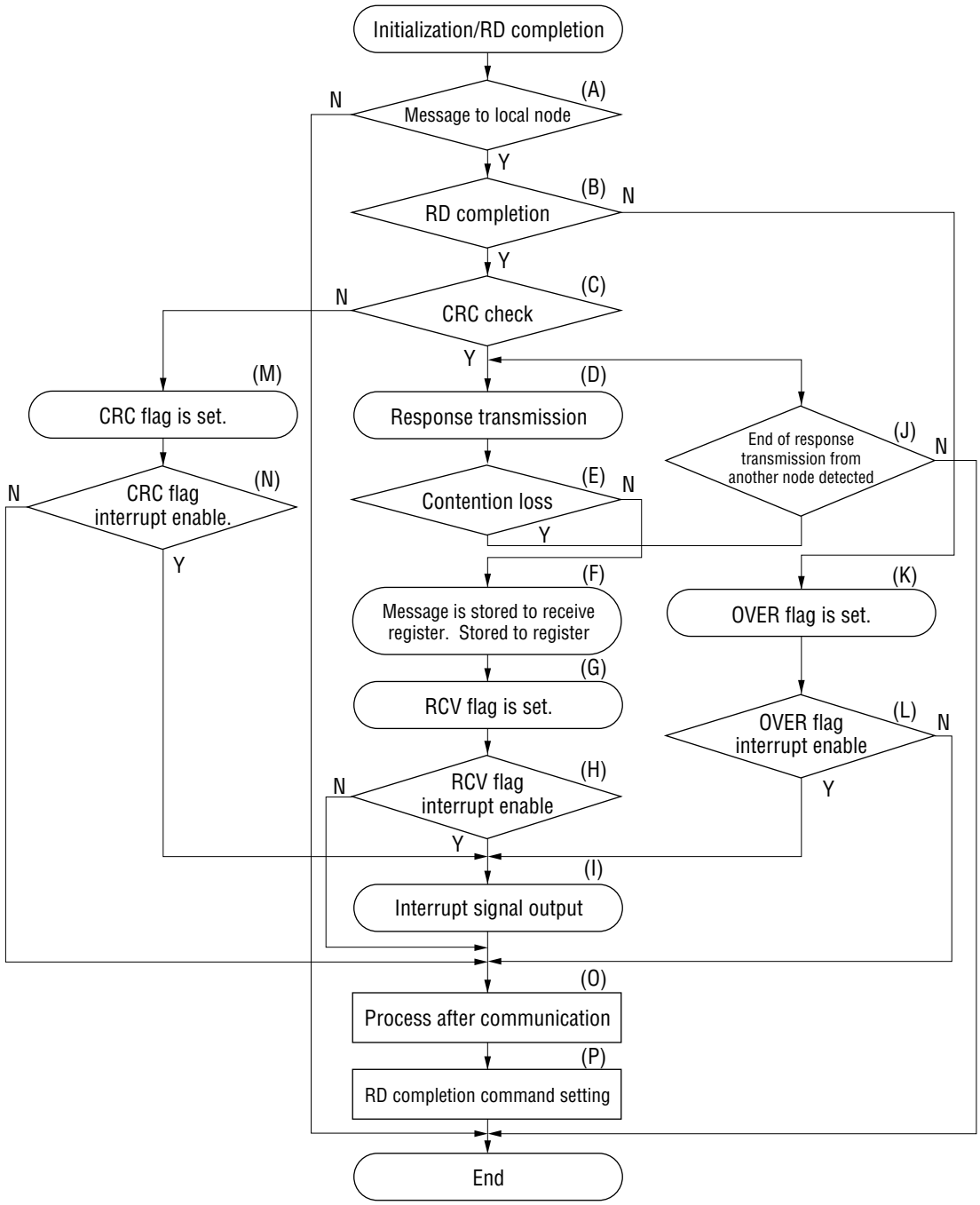



**Figure 5-3 IFR Type 2 Receive Flow**

(A) The receive address of the received message and the functional address of the local node are compared. Only if matched, the message is judged as the message to the local node, and operation moves to B. If not matched, receive operation ends.

(B) If the RD completion command has been set before receiving “EOD”, operation moves to C. If not, operation moves to K.

(C) The CRC code of the received message is checked. If normal, operation moves to D, if an error is detected, operation moves to M.

(D) The physical address value of the local node is sent as the response, and operation moves to E.

(E) If lost in with the response of another node, operation moves to J. If not, operation moves to F.

(F) All received messages are stored from address 15H of the receive register, and operation moves to G. The response is not stored. The number of bytes of the received message (excluding CRC and response) is stored to the receive message length register address (20H).

(G) The interrupt request flag RCV is set, and operation moves to H.

(H) If the interrupt of the RCV flag is enabled, operation moves to I, and if not, the message receive operation ends, and operation moves to O.

(I) An interrupt signal is output from the INT terminal, message receive operation ends, and operation moves to O.

(J) If the end of an 8-bit transmission of the response from another node is detected, operation moves to D. If not (response transmission stopped due to noise, etc.), message receive operation ends.

(K) The interrupt request flag OVER is set, and operation moves to L.

(L) If the interrupt of the OVER flag is enabled, operation moves to I, and if not, message receive operation ends, and operation moves to O.

(M) The interrupt request flag CRC is set, and operation moves to N.

(N) If the interrupt of the CRC flag is enabled, operation moves to I, and if not, message receive operation ends, and operation moves to O.

(O) Processes after communication (reading receive register, clearing interrupt request flag, etc.) is performed.

(P) The RD completion command (address 21H) is set. This setting enables receiving the next message and response.

## 5.4 Message Receive and Response Transmission Operation of IFR Type 3

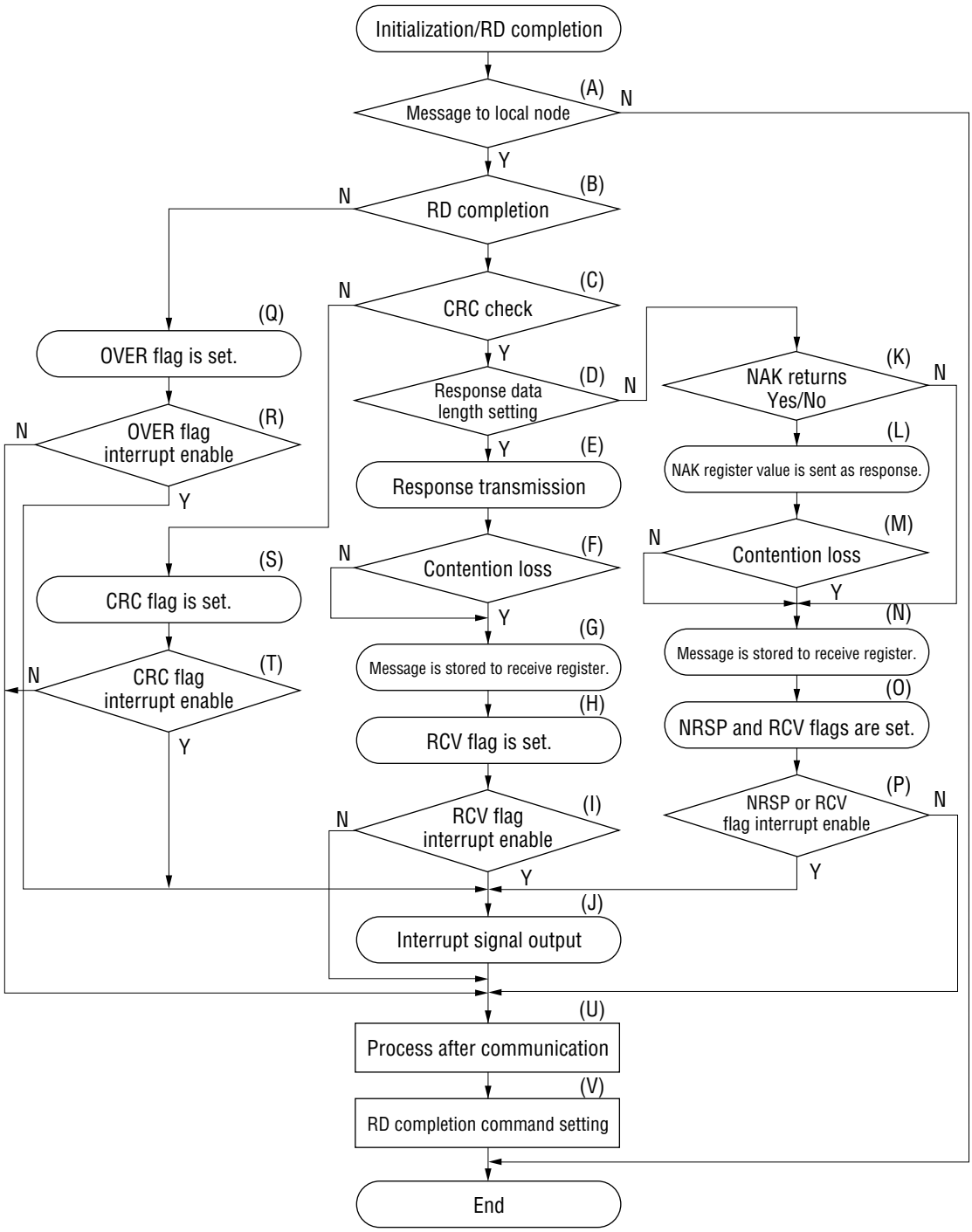



**Figure 5-4 IFR Type 3 Receive Flow**

(A) Receive address of received message and physical or functional address of local node are compared. Only if matched, the message is judged as a message to the local node, and operation moves to B. If not matched, receive operation ends.

(B) If the RD completion command has been set before receiving “EOD”, operation moves to C. If not, operation moves to Q.

(C) The CRC code of the received message is checked. If normal, operation moves to D, if an error is detected, operation moves to S.

(D) If the response data length address (14H) has been set before receiving “EOD”, operation moves to E. If not, operation moves to K.

(E) The data stored from address 0BH of the response register is sent for the number of bytes specified by the response data length (address 14H) as the response, and operation moves to F. CRC code is automatically added at the end of the response.

(F) If lost in contention with the response of another node, response transmission stops, and operation moves to G. Even if loss is not detected, operation still moves to G.

(G) All received messages are stored from address 15H of the receive register, and operation moves to H. The response is not stored. The number of bytes of the received message (excluding CRC and response) is stored to the receive message length register (address 20H).

(H) The interrupt request flag RCV is set, and operation moves to I.

(I) If the interrupt of the RCV flag is enabled, operation moves to J, and if not, the message receive operation ends, and operation moves to U.

(J) An interrupt signal is output from the INT terminal, message receive operation ends, and operation moves to U.

(K) If NAK return has been set to returning the NAK register value at the mode setting (address 2AH), operation moves to L. If set to no IFR, operation moves to N.

(L) The value of the NAK register (address 3BH) is sent as the response, and operation moves to M. CRC code is automatically added at the end of the response.

(M) If lost in contention with the response of another node, response transmission stops, and operation moves to N. Even if loss is not detected, operation still moves to N.

(N) All received messages are stored from address 15H of the receive register, and operation moves to O. The response is not stored. The number of bytes of the received message (excluding CRC and response) is stored to the receive message length register address 20H).

(O) Interrupt request flags NRSP and RCV are set, and operation moves to P.

(P) If the interrupt of NRSP or RCP flags is enabled, operation moves to J, and if not, message receive operation ends, and operation moves to U.

(Q) The interrupt request flag OVER is set, and operation moves to R.

(R) If the interrupt of the OVER flag is enabled, operation moves to J, and if not, message receive operation ends, and operation moves to U.

(S) The interrupt request flag CRC is set, and operation moves to T.

(T) If the interrupt of the CRC flag is enabled, operation moves to J, and if not, message receive operation ends, and operation moves to U.

(U) Processes after communication (reading receive register, clearing interrupt request flag, etc.) is performed.

(V) The RD completion command (address 21H) is set. This setting enables receiving the next message and response.

*Chapter 6*

# CPU INTERRUPT

## 6. CPU INTERRUPT

When transmission/receive is completed, or when various errors occur, an interrupt can be requested to the host CPU by an INT output (low active). Also an interrupt enable/disable can be set for each interrupt factor.

<Interrupt request flag>

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| 22H | LEN | ABN | D-P | OVER | CRC | FORM | INV | IFS |

Message abnormality, etc.

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| 23H | BUSY | NOACK | NRSP | — | BRK | RSP | RCV | TR |

Message transmission/receive status, etc.

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| 24H | PAR | — | WAKR | WAKD | BPG | BPV | BNG | BNV |

LAN bus line related, etc.

"1" indicates that a corresponding interrupted was generated. If a bit to which a flag is not assigned is read, "0" is read. All bits are automatically set to "0" at reset.

<Interrupt enable flag>

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| 25H | LEN | ABN | D-P | OVER | CRC | FORM | INV | IFS |

Message abnormality, etc.

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| 26H | BUSY | NOACK | NRSP | — | BRK | RSP | RCV | TR |

Message transmission/receive status, etc.

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| 27H | PAR | — | WAKR | WAKD | BPG | BPV | BNG | BNV |

LAN bus line related, etc.

"1" enables a corresponding interrupt. All bits are automatically set to "0" at reset. A bit to which a flag is not assigned can also be written, and the written value can be read. Even if "1" is written to a bit to which a flag is not assigned, this bit does not generate an interrupt.

An interrupt is cleared by writing “0” to the corresponding bit of the interrupt request flag by which an interrupt is generated. Even if “1” is written to the interrupt request flag, the flag is not set and the previous status is held. Therefore by writing “0” only to the bits corresponding to the factor to be cleared, and by writing “1” to the other bits, another interrupt can be accepted during a clear operation.

An interrupt request is cleared when all bit set to interrupt enable status are cleared.

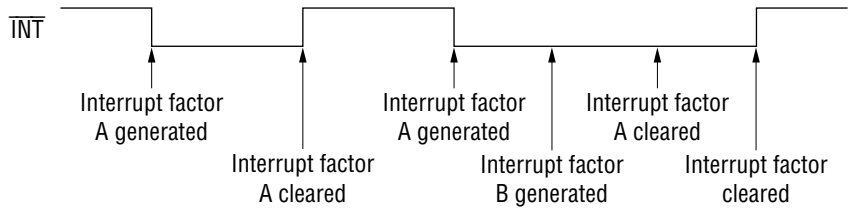



**Figure 6-1 Clearing Interrupt Request**

## 6.1 Receive Message Length Error Interrupt (LEN)

This interrupt is generated when the frame length of a receive message exceeds 12 bytes (including CRC). Only the message transmission node and message receive node generate this interrupt. The node which transmits the message must determine the transmission data length (excluding CRC) considering the number of bytes of a response, so that the frame length of the message does not exceed 12 bytes.

For example, when 10 bytes of an IFR type 2 message (excluding CRC) is sent, and the response is 3 bytes (3 nodes receive this message), the operation of the message transmission node and the 3 message receive nodes become as follows.

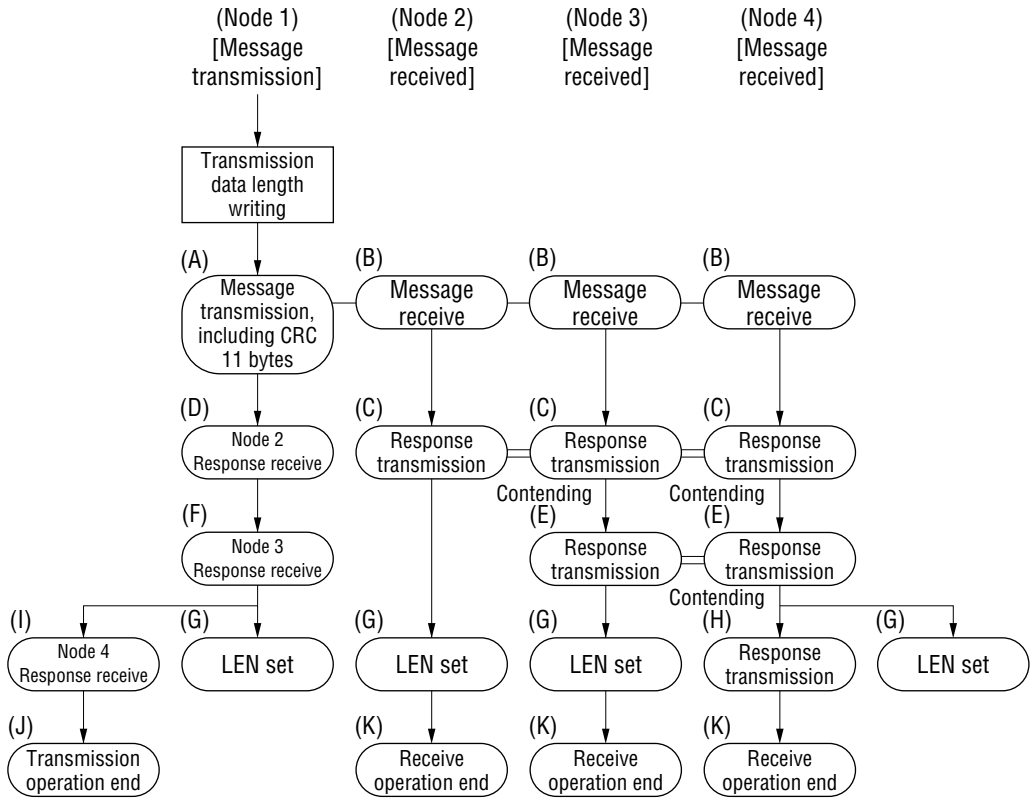



**Figure 6-2 Example of LEN Interrupt Flow**
**(in the case of message 10 bytes and response 3 bytes)**

(A) Node 1 sends an IFR type 2 message to Nodes 2, 3 and 4. This transmission data length is 11 bytes, including CRC.

(B) Nodes 2, 3 and 4 receive the message sent from Node 1.

(C) When the message from Node 1 is received, Nodes 2, 3 and 4 start sending a response at the same time. If the priority of the response (physical address value) at this time is node >Node 3>Node 4, Nodes 3 and 4 detect loss, and they stop sending a response.

(D) Node 1 receives a response from Node 2.

(E) When the response transmission of Node 2 ends, Nodes 3 and 4 start a response transmission again. Node 4 detects loss again, and it stops sending a response.

(F) Node 1 receives a response from Node 3.

(G) When the response transmission of Node 3 ends, the frame length of the message becomes 13 bytes. Nodes 1, 2, 3 and 4 set the receive message length error flag LEN.

(H) When the response transmission of Node 3 ends, Node 4 starts a response transmission again. Although a receive message length error flag LEN has been detected at this time, response transmission is continued.

(I) Node 1 receives a response from Node 4.

(J) When Node 1 receives a response from Node 4, message transmission operation ends. Response node 1 received is not stored to the response register. At this time the interrupt request flag LEN and NOACK have been set (when the number of times of re-transmission at non ACK is set to “no re-transmission”).

(K) When the response transmission of Node 4 ends, Nodes 2, 3 and 4 end message receive operation. The message sent from Node 1 is not stored to the receive register. At this time the interrupt request flag LEN has been set.

Interrupt generation timing is shown below (when the transmission speed setting is 41.6 Kbps).

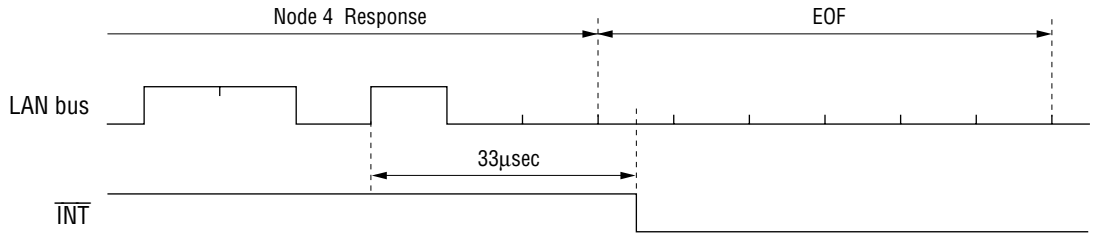



**Figure 6-3 LEN Interrupt Generation Timing**

Note: In the case of an IFR type 0 message transmission, if the transmission data length is set to 12 bytes or more, the transmission node does not detect a message length error, only the receive node does. Since a response is not returned in the case of an IFR type 0 message transmission, the transmission data length is a maximum of 11 bytes (excluding CRC).

In the case of an IFR type 2 message transmission, if the transmission data length is set to 3 bytes, nodes which return a response become a maximum of 8 nodes. Therefore nodes with the same functional address are a maximum of 8 nodes.

## 6.2 LAN Bus Dominant Time Length Error Interrupt (ABN)

This error flag is set when the dominant time of one or both LAN buses continues for 48 msec or more (when the transmission speed setting is 41.6 Kbps).

If this error occurs, all nodes detect the error and stop either message transmission or receive operation. This error flag is always set when the LAN bus is shorted to dominant status (BUS (+) is to $V_{DD}$, or BUS (–) is to GND). When this error flag is set, the bit format error (INV) flag is also set at the same time.

The interrupt generation timing is shown below (when the transmission speed setting is 41.6 Kbps).

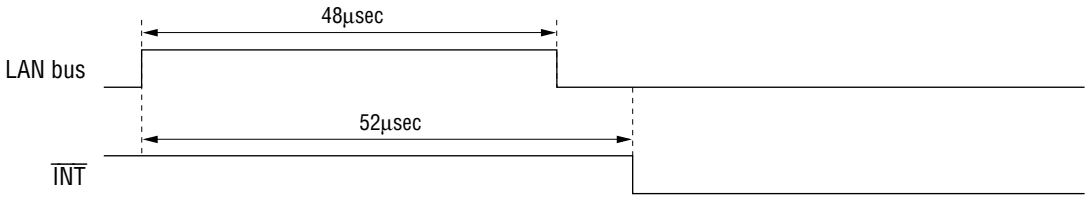



**Figure 6-4 ABN Interrupt Generation Timing**

This interrupt is generated when the transmission speed of all nodes on the LAN are not set the same, or when the LAN bus is shorted to dominant status.

## 6.3 Local Bus Driver Error Interrupt (D-P)

This error flag is set when a dominant status is output to the LAN bus during message transmission or response transmission, however both BUS (+) and BUS (–) of the LAN bus are in passive status. This flag indicates that an abnormality occurred to the bus drivers of the local node. If this flag is set, message or response transmission stops. If either one of the bus drivers is normal, however, this error flag is not set.

When both LAN bus output inhibit setting bits (PB0, NB0) of the mode setting register (address 2AH) are set to inhibit ("0"), this flag is always set before sending a message or response. Do not set both PB0 and NB0 bits to inhibit, otherwise a message or response cannot be set.

Interrupt generation timing is shown below.

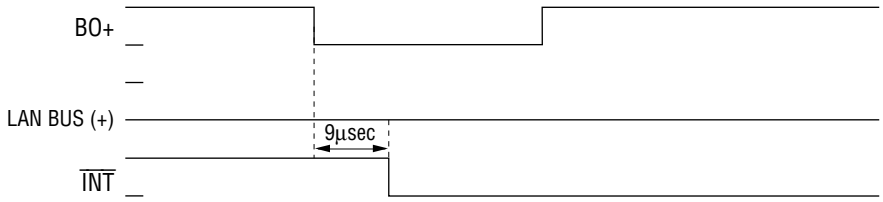



**Figure 6-5 D-P Interrupt Generation Timing**

## 6.4 Overrun Error Interrupt (OVER)

This error flag is set when the next message is receive before the host CPU completes processing a receive message (before the read completion command (21H) is set).

If this flag is set, the message and response received next are not stored to the receive register. When a reset is executed, when the receive message is stored to the receive register (when the message receive completion flag RCV is set), and when the receive response is stored to the receive register (when the response receive completion flag RSP is set), always set the read completion command (address 21H).

If the read completion command is set before the “EOD” code of the next receive message, The overrun error flag (OVER) is not set.

Interrupt generation timing is shown below.

(Overrun error when receiving a message)

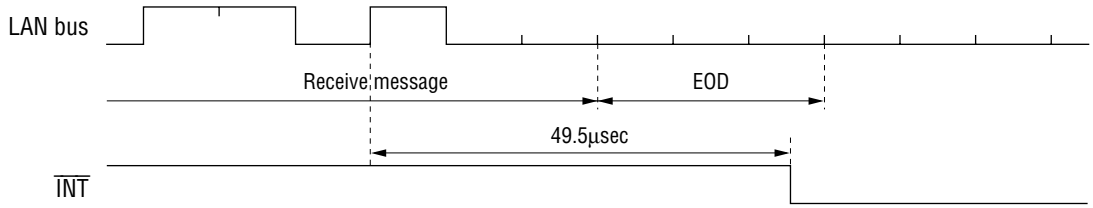



**Figure 6-6 OVER Interrupt Generation Timing 1**

(Overrun error when receiving a response)

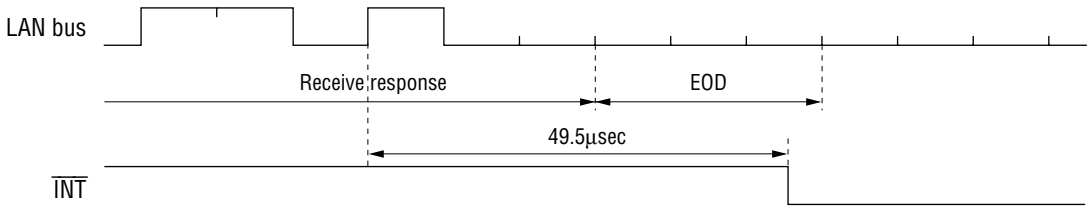



**Figure 6-7 OVER Interrupt Generation Timing 2**

## 6.5 CRC Error Interrupt (CRC)

When message receiving starts and the “EOD” code is detected, a CRC check is performed. If an error occurs at this time, this flag is set only at the node receiving the message.
If this flag is set, message receive operation stops, and the received message is not stored to the receive register.

When an IFR type 3 response is received, if the “EOD” code is detected after receiving the response, a CRC check is performed. If an error occurs at this time, the CRC error flag is set only at the node receiving the response as well. The received response is not stored to the receive register.

Interrupt generation timing is shown below.

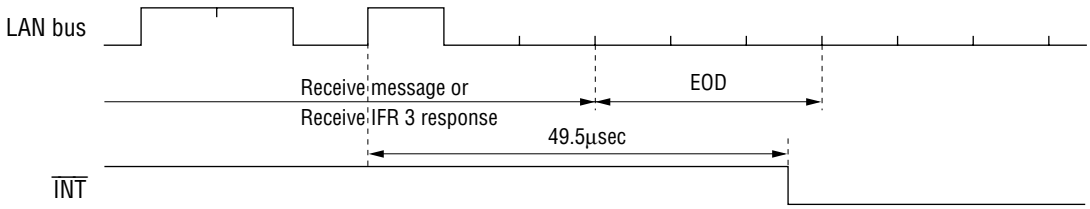



**Figure 6-8 CRC Interrupt Generation Timing**

Note: When the “EOD” code is detected before receiving 2 bytes of the message due to an abnormality, all nodes on the LAN perform a CRC check. If a CRC error is detected at this time, all nodes on the LAN set a CRC error flag.

## 6.6 Message Format Error Interrupt (FORM)

This error flag is set when a message with an abnormal message format is received. For example, when “SOF” is detected when receiving a message, or when “EOD” or “EOF” is detected at an area other than the boundary byte of the receive message.

If a message format error occurs before receiving the receive destination address part of the message, all nodes on the LAN set this error flag. If a message format error occurs after receiving the receive destination address part, only the receive node sets the error flag.

Interrupt generation timing is shown below.

(When “SOF” is detected when receiving a message)

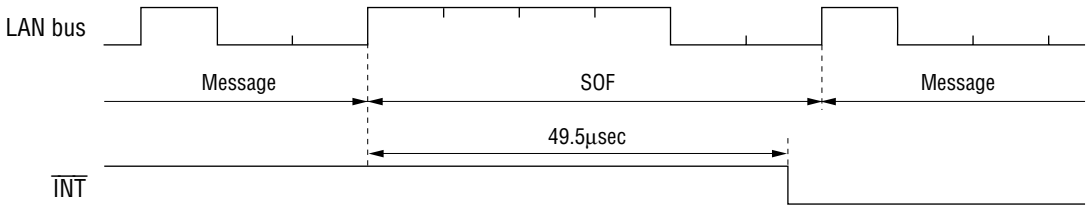



**Figure 6-9 FORM Interrupt Generation Timing 1**

(When “EOD” is detected at an area other than a boundary byte)

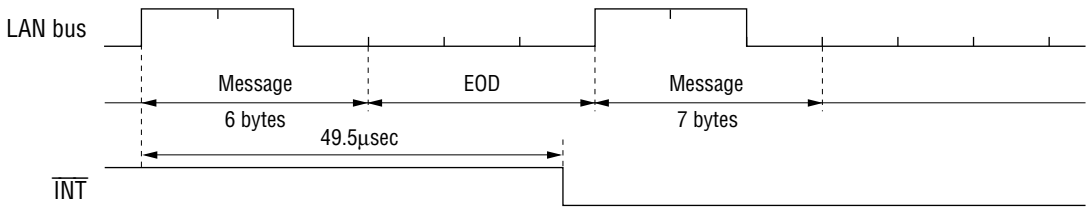



**Figure 6-10 FORM Interrupt Generation Timing 2**

Note: When “EOD” is detected at an area other than a boundary byte, a CRC check is performed, and a CRC error occurs. Therefore the CRC error flag is also set at the same time.

## 6.7 Bit Format Error Interrupt (INV)

This error flag is set when an undefined bit format signal is received.

If this error occurs, message transmission/receive and response transmission/receive operation stops, and all nodes on the LAN set the error flag.

Example of an undefined bit format, which generate a bit format error, are shown below.

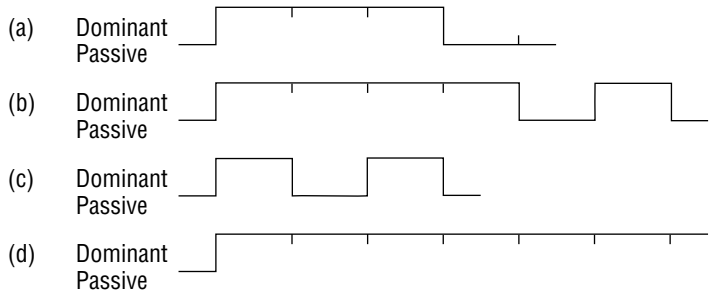



**Figure 6-11 INV Detection Bit Format Example**

If bit format (d) is received, the dominant time length error flag is also set at the same time.

Interrupt generation timing is shown below.

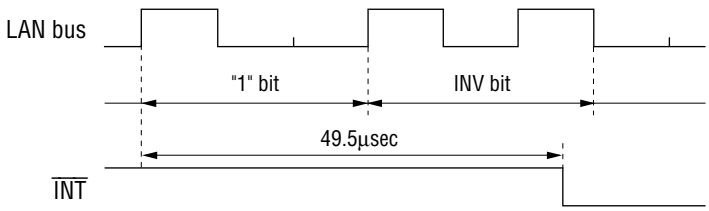



**Figure 6-12 INV Interrupt Generation Timing**

## 6.8 IFS Error Interrupt (IFS)

This error flag is set when a node starts message transmission during 'IFS".

If this error occurs, all nodes on the LAN set the error flag. Even if this error occurs, message transmission and message receive continue, and communication is performed normally. (This is the same as normal communication, except the IFS error flag is set. However, the arbitration function when messages are sent simultaneously is lost, and the node which started the message transmission during "IFS" has priority in message transmission.) The message receive node stores the received message to the receive register and sets the message receive completion flag RCV. The message transmission node, on the other hand, sets the message transmission completion flag TR. If a response is requested, the received response is stored to the receive register and the response receive completion flag RSP is set.

Interrupt generation timing is shown below.

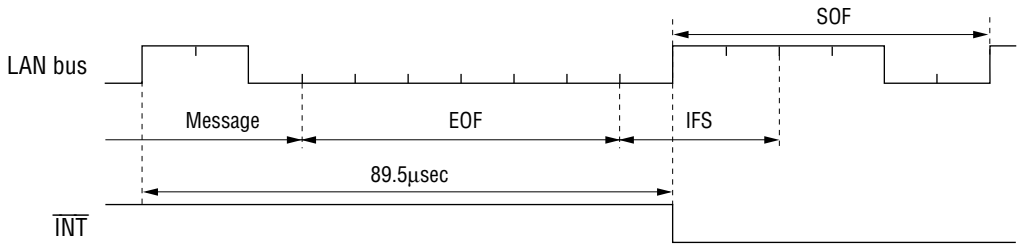



**Figure 6-13 IFS Interrupt Generation Timing 1**

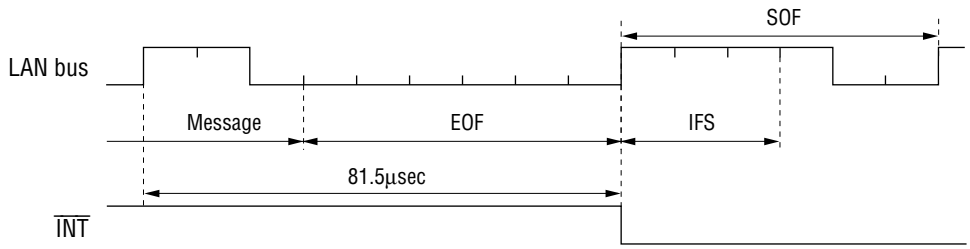



**Figure 6-14 IFS Interrupt Generation Timing 2**

## 6.9 Bus Busy Interrupt (BUSY)

This flag is set when a message was sent for the specified number of times of re-transmission, but is lost in contention. When sending a message and another node is communicating, message communication starts after the communication of the node ends. If the setting of the NO bit has been set to “1”, which is “No re-transmission”, the bus busy flag is set after the first contention loss, and message transmission attempts end after only one try.

If the NO bit has been set to “Re-transmission twice”, message transmission is attempted for a maximum of 3 times.

When the bus busy flag is set and message transmission stops, the same message can be set by writing the transmission data length (address 13H) again. Since the bus busy flag is not automatically cleared at this time, clear the flag.

Interrupt generation timing is shown below.

(When lost in contention with another node message)

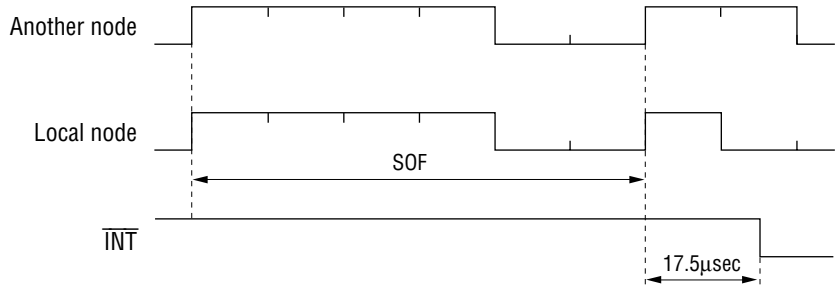



**Figure 6-15 BUSY Interrupt Generation Timing**

Note: When bus idle status has continued for a while and contending multiple nodes start message transmission at the same time during this bus idle period, loss may be detected when “SOF” is sent. This is caused by out of synchronization, which occurs when the source oscillation frequency of each node differs. If the bus idle time is short (when a message is sent when the message transmission of another node ends), loss is not detected when “SOF” is sent, because out of synchronization is small. For details, see the section on source oscillation frequency errors. When loss is detected when “SOF” is sent, the bus busy flag is set if NO bit is set to “No re-transmission”, since this is counted as one transmission attempt.

The maximum time from message transmission command output to bus busy flag set is shown below (when the transmission speed setting is 41.6 Kbps).

**Table 6-1 Maximum Busy Interrupt Generation Time**

| | No re-transmission | Re-transmission twice |
|---|---|---|
| BUSY interrupt generation time | 4.5975msec | 9.4935msec |

If message re-transmission is set to twice, the time from message transmission command output to bus busy flag set becomes the maximum in the following cases.

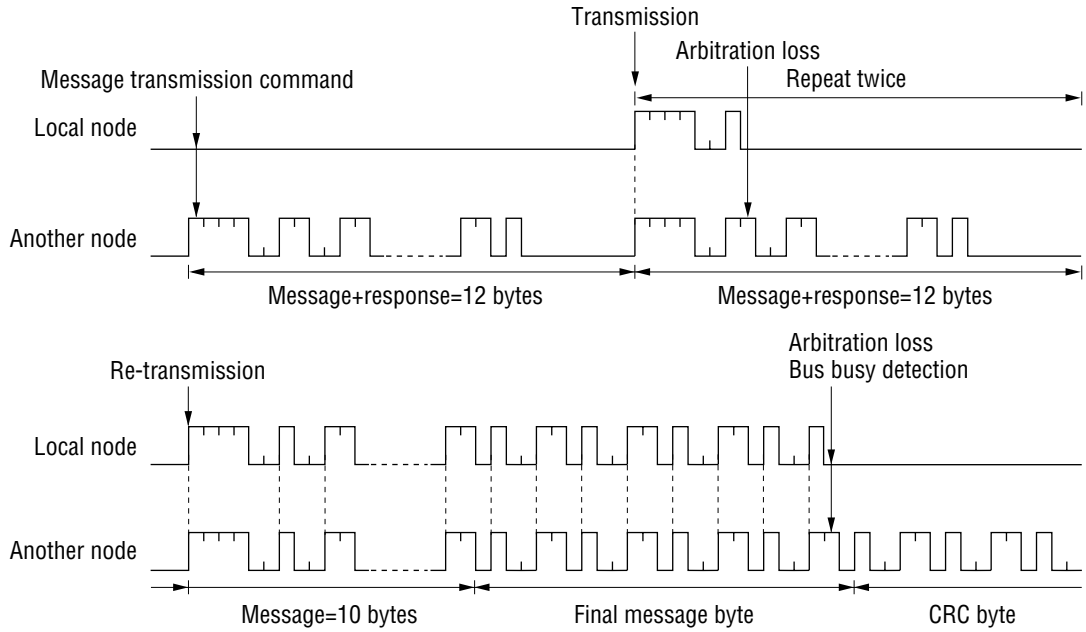



**Figure 6-16 Maximum BUSY Interrupt Generation Time**

- When the message transmission command is output, another node has just started to send a message, and the local node must wait to send a message.
- The message of another node requests a response, and its message frame length is 12 bytes (maximum).
- The message frame of another node ends and message transmission stars, but arbitration loss was detected in with the message of another node, and the message of another node was the same as the above message (arbitration loss: once).
- The message frame of another node ends and message transmission starts, but arbitration loss was detected in with the message of another node, and the message of another node was the same as above (arbitration loss: twice).
- The message frame of another node ends again and message transmission starts, but arbitration loss was detected at the 11th bit (final bit) of the transmission message in with the message of another node. (arbitration loss: 3 times = bus busy detection)

## 6.10 Non ACK Interrupt (NOACK)

This flag is set when the message requesting a response was re-transmitted for the specified number of times, but a response was not returned.

If the N1 bit of the mode setting register (address 2AH) has been set to “0”, which is “Re-transmission twice”, a message transmission is attempted for a maximum of 3 times. If the N1 bit has been set to “1”, which is “No re-transmission”, a message is sent only once.

When the Non ACK flag is set and message transmission stops, the same message can bet sent by writing the transmission data length (address 13H) again. Since the Non ACK flag is not automatically cleared at this time, clear the flag.

The interrupt generation timing is shown below.

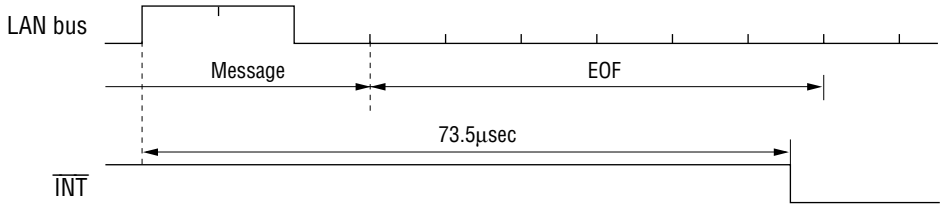



**Figure 6-17 NOACK Interrupt Generation Timing**

The maximum time from message transmission command output to Non ACK flag set is shown below (when the transmission speed setting is 41.6 Kbps).

**Table 6-2 Maximum NOACK Interrupt Generation Time**

| | No re-transmission | Re-transmission twice |
|---|---|---|
| NOACK generation time | 4.2215msec | 9.1175msec |

If the message re-transmission is set to twice, the time from message transmission output to Non ACK flag set becomes the maximum in the following cases.

- When the message transmission command is output, another node has just started sending a message, and the local node must wait to send a message.
- The message of another node requests a response , and its message frame length is 12 bytes (maximum).
- When 11 bytes of an IFR type 1 message was sent, but a response was not returned.

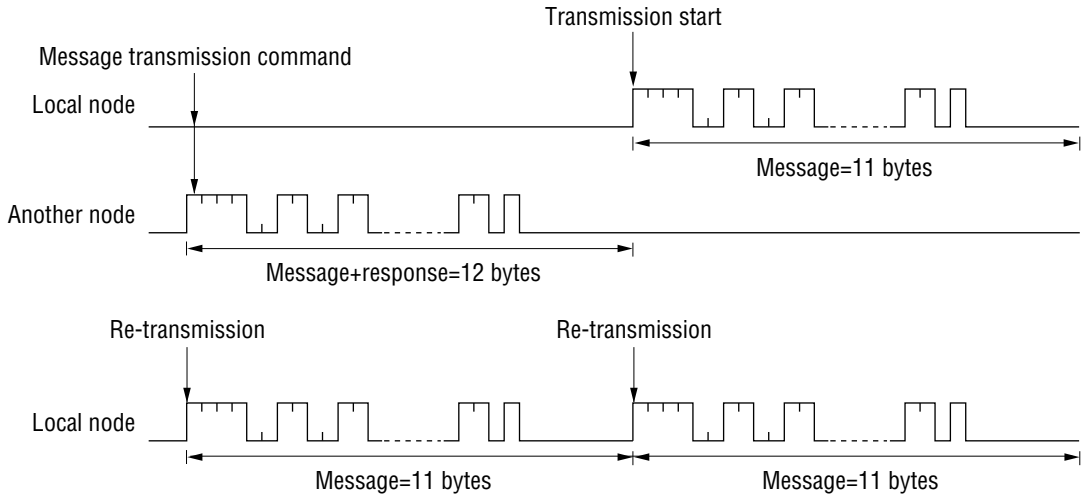



**Figure 6-18 Maximum NOACK Interrupt Generation**

## 6.11 Response Transmission Standby Error Interrupt (NRSP)

This flag is set when an IFR type 3 message was received, but the response data length (address 14H) has not been written.

If the response data length is written before the “EOD” bit of the received message, the response transmission error flag is not set.

Once the response data length is written, the IFR type 3 response transmission standby status is held until the IFR type 3 message is received and an IFR type 3 response is sent. Even if a message, other than an IFR type 3, is received or transmitted after the response data length is written, it is not necessary to write the response data length again. The written response data length is reset by an RES terminal input.

Interrupt generation timing is shown below.

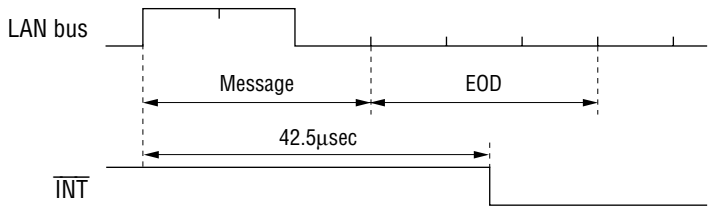



**Figure 6-19 NRSP Interrupt Generation Timing**

## 6.12 Break Receive Interrupt (BRK)

This flag is set when a break signal is received.

All nodes on the LAN set this flag, and the node which sent the break signal also receives a break signal, and sets this flag. If the break signal is received, message transmission/receive and response transmission/receive stop, and the message re-transmission function do not work. However the internal register status is not reset after receiving the break signal. To re-transmit the message after the break signal is received when sending the message, merely write the transmission data length (address 13).

Interrupt generation timing is shown below.

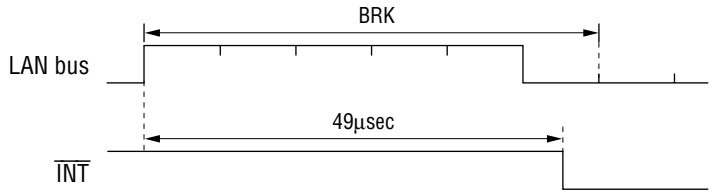



**Figure 6-20 BRK Interrupt Generation Timing**

## 6.13 Response Receive Completion Interrupt (RSP)

This flag is set when the message which requests a response was sent and the returned response was received normally. At this time, the received response is stored to the receive register, and the received response length (excluding CRC) is stored to the receive data length register (address 20H).

If this flag is set, always set the read completion command (address 21H) after reading the receive register. If the read completion command is not set, the next message or response cannot be received, and the overrun error flag (OVER) is set.

Interrupt generation timing is shown below.

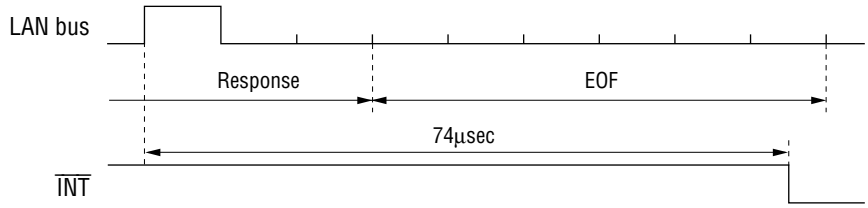



**FIgure 6-21 RSP Interrupt Generation Timing**

## 6.14 Message Receive Completion Interrupt (RCV)

This flag is set when a message is received normally. At this time, the received message is stored to the receive register, and the received message length (excluding CRC) is stored to the receive data length register (address 20H). Even if the received message is a type which requests a response, the response is not stored to the receive register.

If this flag is set, always set the read completion command (address 21H) after reading the receive register. If the read completion command is not set, the next message or response cannot be received, and the overrun error flag (OVER) is set.

Interrupt generation timing is shown below.

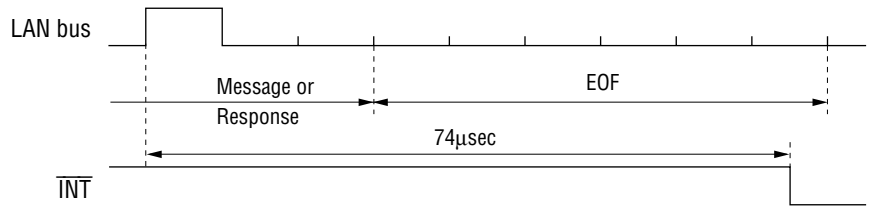



**Figure 6-22 RCV Interrupt Generation Timing**

## 6.15 Message Transmission Completion Interrupt (TR)

This flag is set when a message is transmitted normally. Even if a response is not returned normally (when a response was not returned, or when the received response and the address value specified as the receive address did not match when sending an IFR type 1 (K, Y, Z1, Z0)=(0, 1, 0, 0, ) message, or when a CRC error was detected in response when sending an IFR type 3 message), or if message transmission stops due to bus busy, this flag is not set.

Interrupt generation timing is shown below.

(When a message without requesting a response is sent:)

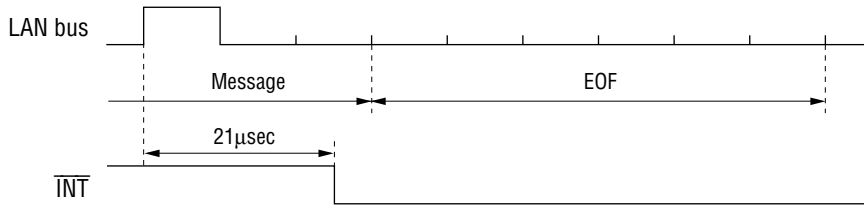



**Figure 6-23 TR Interrupt Generation Timing 1**

(When a message requesting a response is sent:)

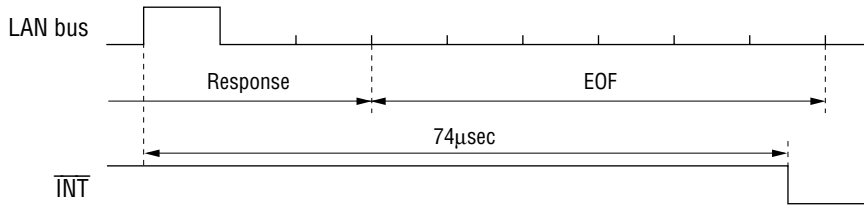



**Figure 6-24 TR Interrupt Generation Timing 2**

## 6.16 Parity Error Interrupt (PAR)

This flag is set when a parity error is detected in the receive data from the CPU during UART communication (with parity) between CPUs.

If this error flag is set, the receive data is invalid.

Interrupt generation timing is shown below.

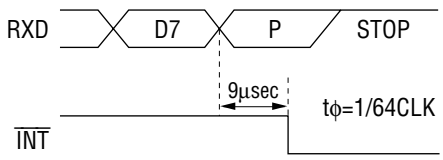



**Figure 6-25 PAR Interrupt Generation Timing**

## 6.17 Wake Up Interrupt by RXD (WAKR)

This flag is set when a wake up occurs during sleep, due to a change of the RXD terminal. To prevent a malfunction caused by noise, etc., a wake up does not occur if the pulse change width of an RXD terminal is less than 50 nsec.

The oscillation circuit stops during sleep. If an oscillator, such as a ceramic oscillator, is used, the interface between CPUs cannot be used until the specified oscillation stabilization time passes.

Interrupt generation timing is shown below.

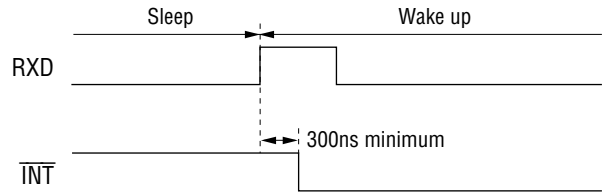



**Figure 6-26 WAKR Interrupt Generation Timing**

## 6.18 Wake Up Interrupt by LAN Bus (WAKD)

This flag is set when a wake up occurs during sleep, due to a passive → dominant change of both or one of BUS (+) and BUS (–) of the LAN bus. A wake up does not occur if the pulse change width of passive to dominant is less than 1 msec.

The oscillation circuit stops during sleep. If an oscillator, such as a ceramic oscillator, is used, the message receive operation doe not become normal until the specified oscillation stabilization time passes. If oscillation is not stabilized at this time, the following error flags may be set. If a wake up by the LAN bus occurs, clear all these error flags after oscillation stabilizes.

- LAN bus dominant time length error (ABN)
- Message format error (FORM)
- Bit format error (INV)
- IFS error (IFS)
- Break receive (BRK)

Interrupt generation timing is shown below.

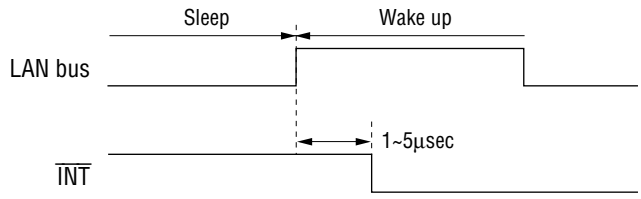



**Figure 6-27 WAKD Interrupt Generation Timing**

## 6.19 LAN Bus (–) GND Short Detection Interrupt (BNG)

This flag is set when the LAN bus (–) side is shorted to GND potential for 48µsec or longer (when the transmission speed setting is 41.6 Kbps), or when the LAN bus (+) changes as dominant Æ passive → dominant when the LAN bus (–) is in dominant status.

If the LAN bus (–) is shorted to GND potential for 48µsec or longer, the bit format error flag (INV) and the LAN bus dominant time length error flag (ABN) are also set at the same time.
Since the bus receiver circuit is switched to make only input signals from the LAN bus (+) valid at this time, communication can be performed normally using only the LAN bus (+), even if the LAN bus (–) is shorted to GND.

For details, see section “9. Fault tolerance function”.

Interrupt generation timing when the LAN bus (–) is shorted to GND for 48µsec or longer is shown below.

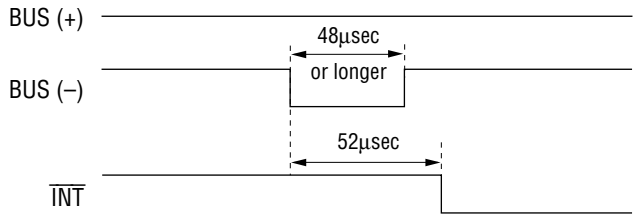



**Figure 6-28 BNG Interrupt Generation Timing**

## 6.20 LAN Bus (+) $V_{DD}$ Short Detection Interrupt (BPV)

This flag is set when the LAN bus (+) side is shorted to $V_{DD}$ potential for 48µsec or longer (when the transmission speed setting is 41.6 Kbps) or when the LAN bus (–) is changed as dominant → passive → dominant while the LAN bus (+) is in dominant status.

If the LAN bus (+) is shorted to $V_{DD}$ potential for 48µsec or longer, the bit format error flag (INV) and the LAN bus dominant time length error flag (ABN) are also set at the same time.
Since the bus receiver circuit is switched to make only input signals from the LAN bus (–) valid at this time, communication can be performed normally using only the LAN bus (–), even if the LAN bus (+) is shorted to $V_{DD}$.

For details, see the section “9. Fault tolerance function”.

Interrupt generation timing when the LAN bus (+) is shorted to $V_{DD}$ for 48µsec or longer is shown below.

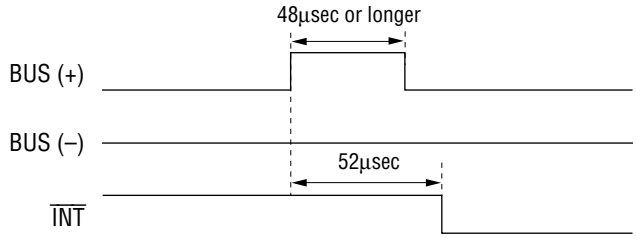



**Figure 6-29 BPV Interrupt Generation Timing**

## 6.21 LAN Bus (–) $V_{DD}$ Short Detection Interrupt (BNV)

This flag is set when the LAN bus (–) side is shorted to $V_{DD}$ or opened.

A $V_{DD}$ short or open of the LAN bus (–) is detected when the LAN bus (+) changes from passive to dominant status, and the flag is set when the LAN bus (+) changes from dominant to passive status. This LAN bus error is not detected when communication is not occurring.

If a LAN bus (–) error is detected, the bus receiver circuit is switched to make only input signals from the LAN bus (+) valid, therefore communication can be performed normally using only the LAN bus (+).

For details, see section “9. Fault tolerance function”.

Interrupt generation timing is shown below.

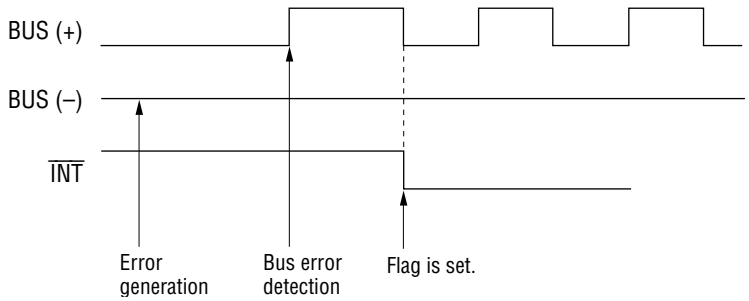



**Figure 6-30 BNV Interrupt Generation Timing**

## 6.22 LAN Bus (+) GND Short Detection Interrupt (BPG)

This flag is set when the LAN bus (+) side is shorted to GND or is opened.

A GND short or an open of the LAN bus (+) is detected when the LAN bus (–) changes from passive to dominant status, and the flag is set when the LAN bus (–) changes from dominant to passive status. When communication is not going on, this LAN bus error is not detected.
If a LAN bus (+) error is detected, the bus receiver circuit is switched to make only input signals from the LAN bus (–) valid, therefore communication can be performed normally using only the LAN bus (–).

For details, see section “9. Fault tolerance function”.

Interrupt generation timing is shown below.

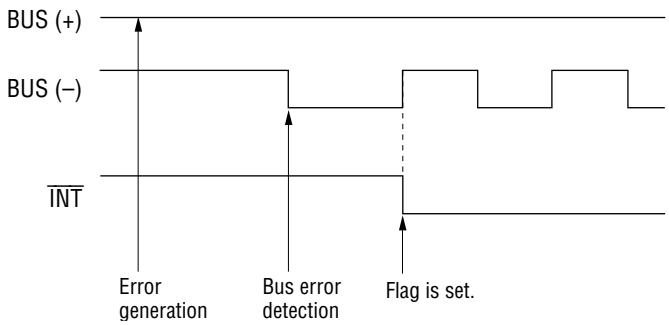



**Figure 6-31 BPG Interrupt Generation Timing**

*Chapter 7*

# ARBITRATION FUNCTION

## 7. ARBITRATION FUNCTION

Multiple nodes are connected to the LAN bus, therefore if multiple nodes start to transmit at the same time, MSM6636 detects non-destructive collision and controls priority using the arbitration function. Only the node transmitting a message with the highest priority can complete a transmission. Priority is set such that the node outputting in dominant status is higher than the node outputting in passive status. MSM6636 constantly monitors the LAN bus status, even during transmission, comparing the output data of the local node and the LAN bus status. If the local node is in passive status output, but a dominant status is detected on the LAN bus, MSM6636 judges this as a loss, and immediately stops transmission operation.

The arbitration function activates in the following statuses.

(A) When multiple nodes start message transmission at the same time during a bus idle status.

(B) When multiple nodes attempt to send message while another node is communicating, and all had to backup for message re-transmission.

(C) When a broadcast message was received and a response is sent.

(D) When an IFR type 2 message was received and a response is sent.

(A) When multiple nodes start message transmission at the same time during a bus idle status:

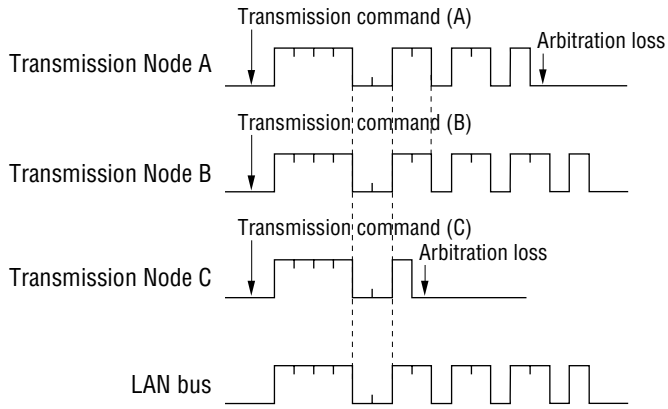



**Figure 7-1 Arbitration A**

In this case, the node transmitting a message with the highest priority can complete a message transmission. If the priority of transmitting messages is all equal, priority is determined by the bits of the message type.

(B) When multiple nodes attempt to send message while another node is communicating, and all had to backup for a message re-transmission:

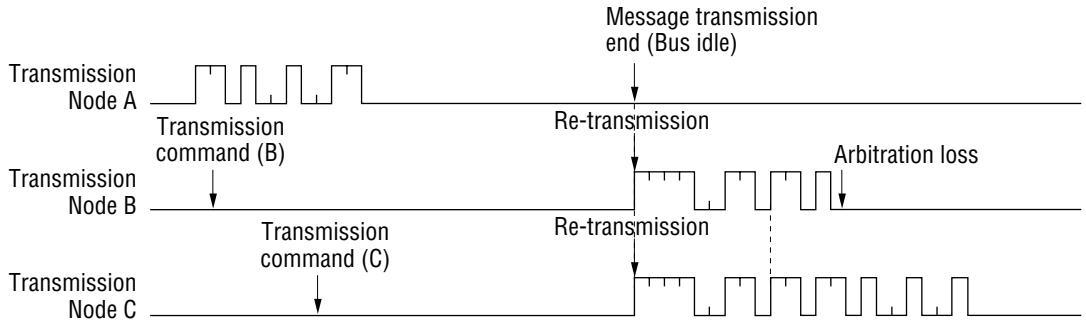



**Figure 7-2 Arbitration B**

In this case as well, as in A, the node transmitting a message with the highest priority can complete a message transmission.

(C) When a broadcast message is received and a response is sent:

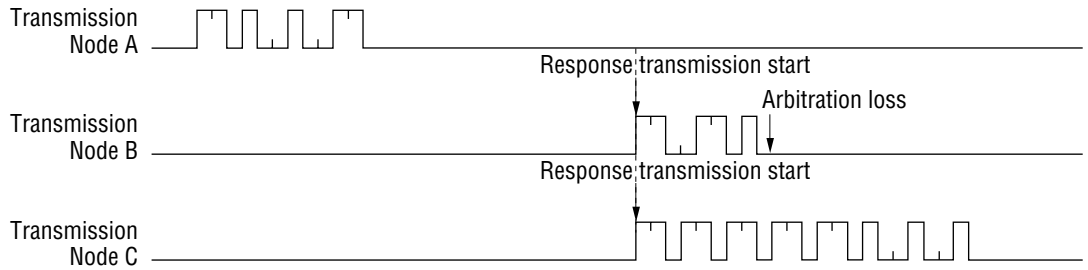



**Figure 7-3 Arbitration C**

In this case, only the node whose response (physical address) has the highest priority can return a response. The response transmission of other nodes stop when an arbitration loss is detected.

(D) When a broadcast message is received and a response is sent:

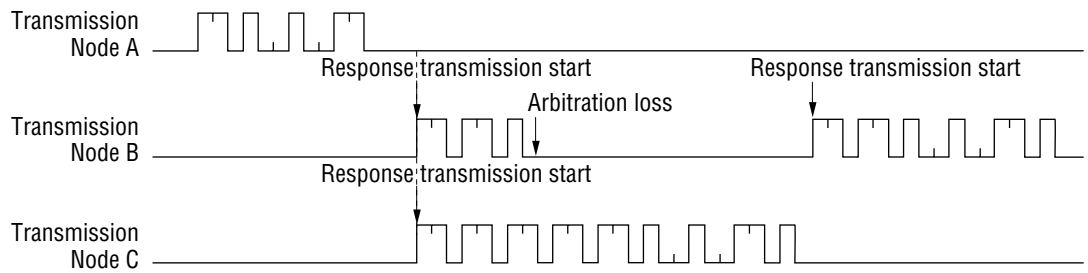



**Figure 7-4 Arbitration D**

In this case, a response is sent sequentially from the node whose response (physical address value) has the highest priority. A response re-transmission is repeated until response transmission ends.

*Chapter 8*

# SLEEP FUNCTION

## 8. SLEEP FUNCTION

MSM6636 enters sleep status by writing “AAH” to the sleep command register (28H).

However, if MSM6636 is receiving a message or transmitting a response, MSM6636 enter sleep status after completing processing and detecting a bus idle status. Do not enter sleep status during message transmission.

In sleep status, oscillation stops and MSM6636 enters low current consumption mode, and continues outputting a passive status to the LAN bus. After entering sleep status, the value of the sleep command register (28H) is automatically set to “00H”. It is automatically set to “00H” at reset.

Timing entering into sleep status is shown below.

<Entering sleep status in bus idle status>

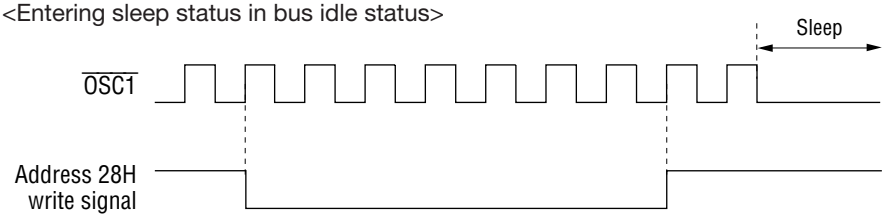



**Figure 8-1 Timing to Enter Sleep Status 1**

<Entering sleep status when receiving a message>

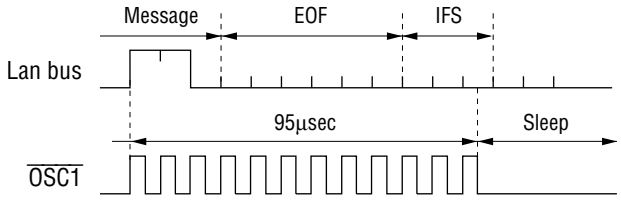



**Figure 8-2 Timing to Enter Sleep Status 2**

Wake up conditions are:

(1) LAN bus changes from passive to dominant
(2) RXD terminal of CPU interface changes status

When detecting these conditions, MSM6636 enables oscillation circuit operation, and at the same time, reports on wake up completion to the CPU by outputting INT (in the case of a wake up interrupt enable).

Wake up is also caused by the LAN bus when either BUS (+) or BUS (–) changes from passive to dominant.

Wake up timing is shown below.

<Wake up by LAN bus>

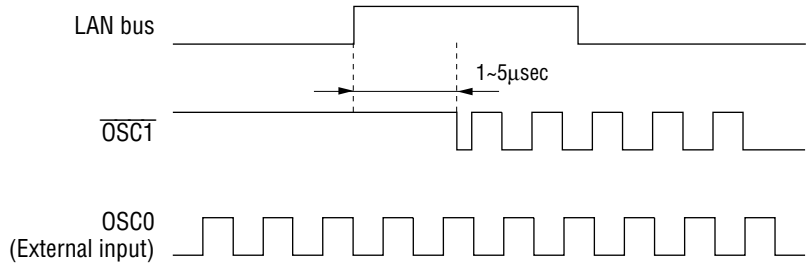



**Figure 8-3 LAN Bus Wake Up**

<Wake up by RXD terminal>

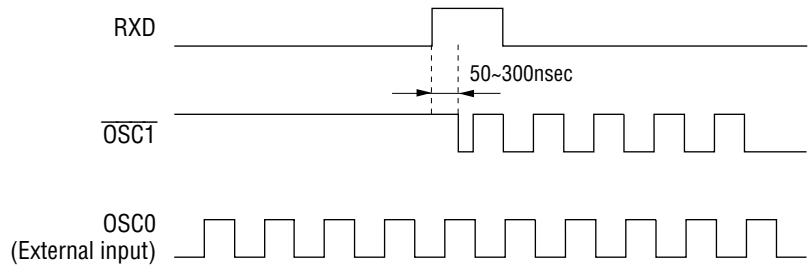



**Figure 8-4 RXD Wake Up**

The oscillation circuit stops during sleep status. If an oscillator, such as a ceramic oscillator, is being used, the CPU interface cannot be used, and a message cannot be sent/received until the specified oscillation stabilization time passes.

In the case of a wake up by the LAN bus, the following interrupt request flags may be set because oscillation is unstable. After oscillation stabilizes, clear all these flags.

- LAN bus dominant time length error (ABN)
- Message format error (FORM)
- Bit format error (INV)
- IFS error (IFS)
- Break receive (BRK)

## 8.1 Example of Sleep Transition Routine

This section introduces an example of the routine to enter sleep status.

Assign a functional address for sleep to all nodes of the LAN. In this section “CCH” is selected as this address value. Set data for a sleep transition instruction, and program the CPU so that all nodes on the LAN enter sleep status whenever this data is received. The 3 byte data string “CCH, CCH, CCH” is selected in this section as the sleep transition instruction data.

When Node A wants to enter sleep, Node A sends an IFR type 0 message to all nodes, A, B, C and D, on the LAN using the functional address. When the CPU confirms that all nodes, A, B, C and D on the LAN received the data string “CCH, CCH, CCH” at the message data area, the respective CPU lets MSM6636 enter sleep status, and the CPU stops accessing MSM6636.

If for any reason a node wants to delay entering sleep status, it can do so by sending data other than “CCH, CCH, CCH” using the functional address after receiving sleep code. In that case, the CPU waits for the specified time after receiving sleep code, and if there is no communication from another node during the wait period, the CPU performs the sleep transition process. The node who sent the delay instruction must send the sleep instruction to all nodes again when the sleep transition process is over. Then all nodes on the LAN can enter sleep status all at once.

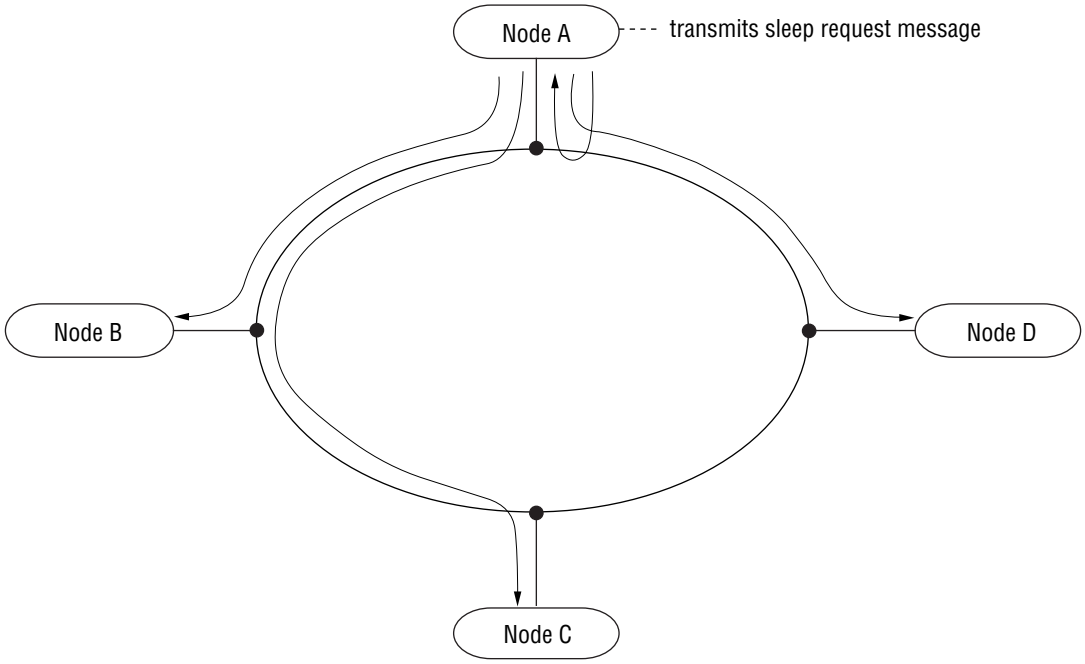
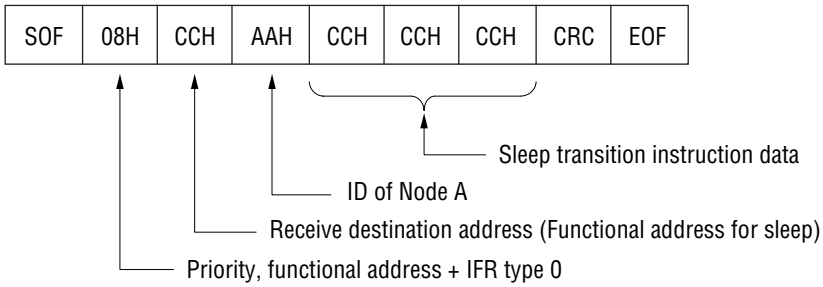



**Figure 8-5 Message Flow When Entering Sleep Status**

Transmission message of Node A



Example of sleep transition process routine of each node

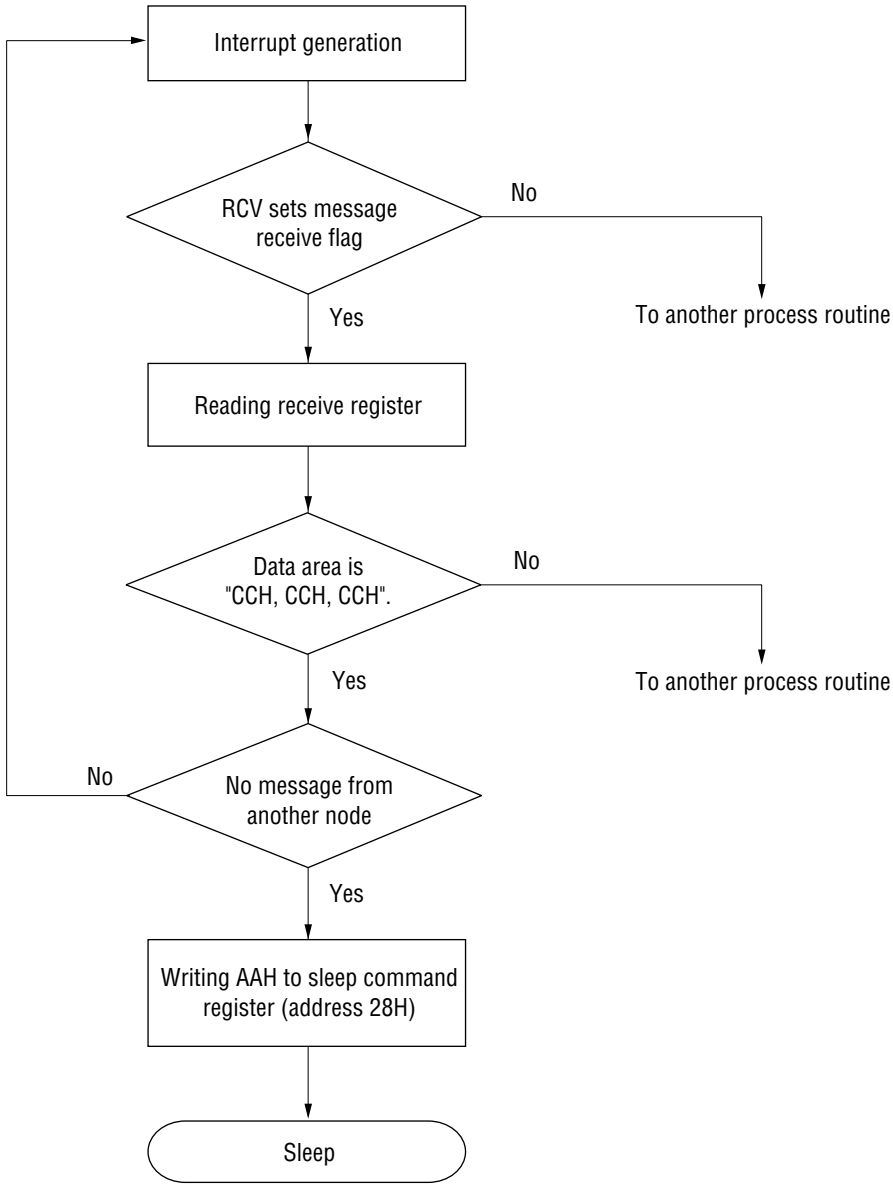



**Figure 8-6 Sleep Transition Process Flow**

*Chapter 9*

# FAULT TOLERANT FUNCTION

## 9. FAULT TOLERANCE FUNCTION

### 9.1 BUS (–) GND Short

<Short occurred during bus idle status>

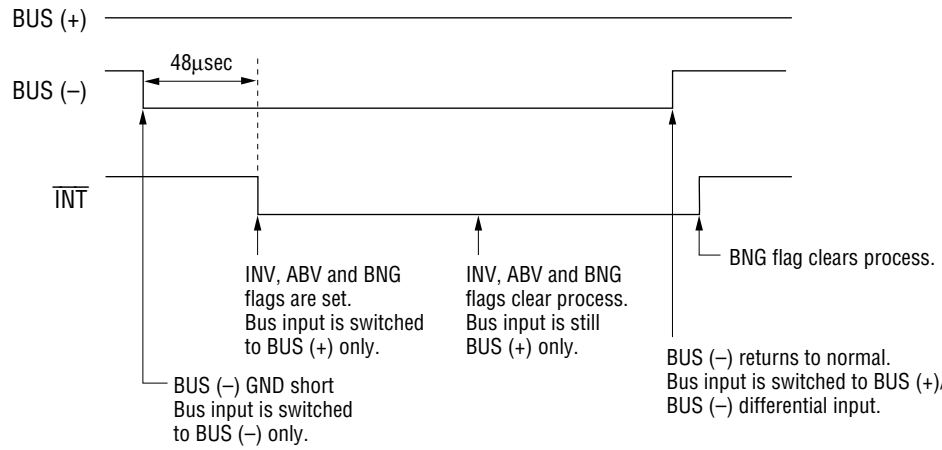



**Figure 9-1 Fault Tolerance 1**

<Short occurred when passive status is output during message transmission>

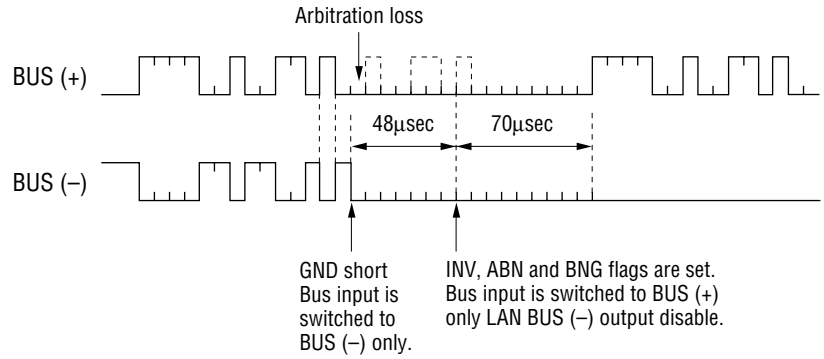



**Figure 9-2 Fault Tolerance 2**

When BUS (–) shorts to GND when passive status is output to the LAN bus during message transmission, MSM6636 judges the status as BUS (+) shorted to GND, and switches the receive input to BUS (–) only. This is because MSM6636 recognizes the bus whose status changed first as the normal bus. Since the LAN bus is in dominant status while passive status is output to the LAN bus, arbitration loss is detected and message transmission stops.
If the bus busy re-transmission count has been set to "2", a message is resent when the status changes to bus idle.

If a BUS (–) GND short status continues for 48 msec or longer (when the transmission speed setting is 41.6 Kbps), a dominant time length error of the bus is detected. At this time interrupt request flag BNG is set, and receive input is switched to BUS (+) only. If the BNG flag is set, the output of LAN BUS (–) is automatically disabled, and LAN BUS (–) is not driven when a message is sent after this.

<Short occurred when dominant status is output during message transmission>

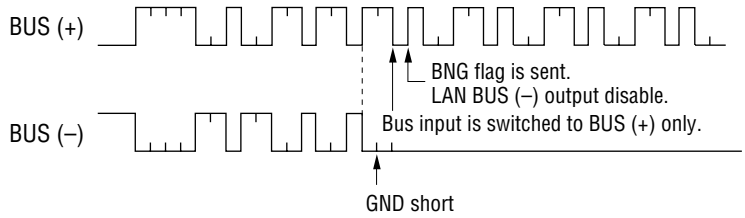



**Figure 9-3 Fault Tolerance 3**

When BUS (–) shorts to GND when dominant status is output to the LAN bus during message transmission, MSM6636 judges the status as BUS (–) shorted to GND, and switches the bus input to BUS (+) only, because BUS (–) does not change to passive status even if passive status is output to the LAN bus. In this case, an arbitration loss is not detected and message transmission continues.

If BUS (+) next changes from passive to dominant status, the BNG flag is set and LAN BUS (–) output is automatically disabled. LAN BUS (–) is not driven after this.

## 9.2 BUS (–) $V_{DD}$ Short

<Short occurred during bus idle status>

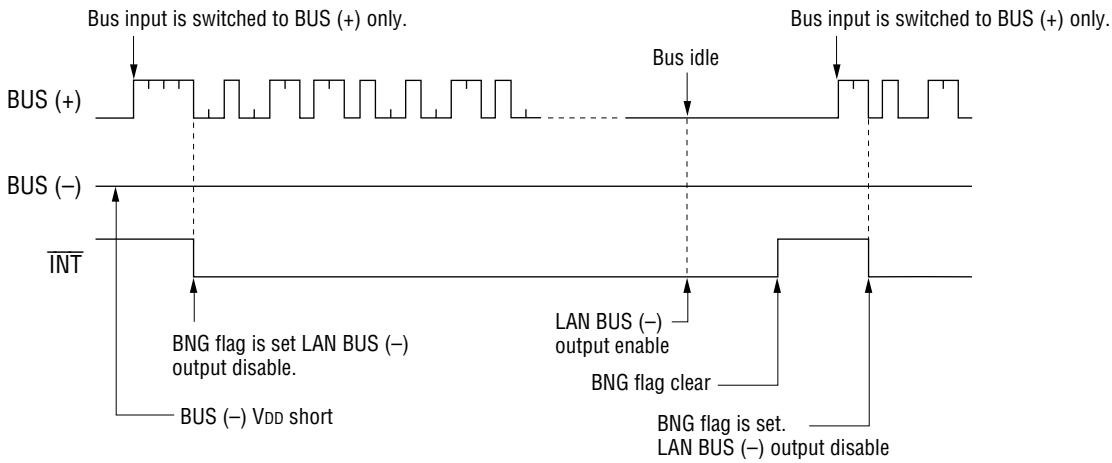



**Figure 9-4 Fault Tolerance 4**

When BUS (–) shorts to $V_{DD}$ during bus idle status, LAN bus status does not change, therefore an abnormality of the LAN bus is not detected until a message is output to the LAN bus (until LAN bus status changes). If a message is output to the LAN bus and BUS (+) changes to dominant status, MSM6636 judges the status as BUS (–) shorted to $V_{DD}$, and switches bus input to BUS (+) only. When BUS (+) changes from dominant status to passive status after this, interrupt request flag BNV is set, and LAN BUS (–) output is disabled. At this time, LAN BUS (–) is driven while an SOF signal is dominant, and excess current flows to the bus driver. When the status returns to bus idle again, the BUS (–) $V_{DD}$ short detection is cleared, LAN BUS (–) output is enabled, and bus input is switched to BUS (+) BUS (–) differential input. If the BNV flag is cleared at this time, a LAN bus abnormality is not detected until a message is output to the LAN bus again.

If the LAN BUS output disable setting bit (NBO) is “0”, LAN BUS (–) output is disabled when the BNV flag is set. LAN BUS (–) output is enabled again when one frame of communication ends and the status returns to bus idle. As long as a BUS (–) $V_{DD}$ short continues, the external transistor is driven for every communication frame the initial SOF signal is dominant.

If the LAN BUS output disable setting bit (NBO) is set to “1”, LAN BUS (–) output is kept disabled. Therefore excess current flowing into the external transistor can be prevented.

<Short occurred when passive status is output during message transmission>

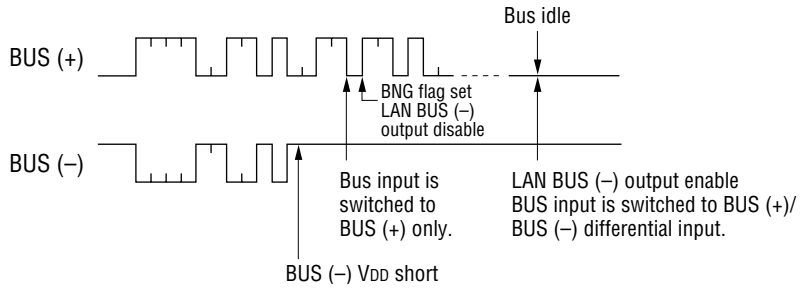
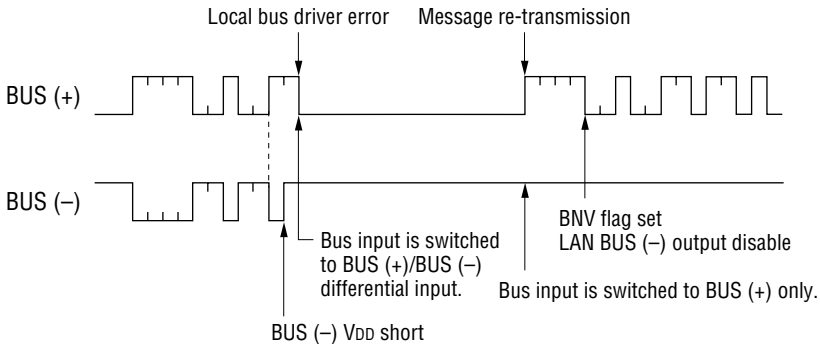



**Figure 9-5 Fault Tolerance 5**

When BUS (–) shorts to $V_{DD}$ when a passive status is output to the LAN bus during message transmission, MSM6636 judges the status as BUS (–) shorted to $V_{DD}$, and sets interrupt flag BNV, since BUS (–) does not change to dominant status even if a dominant status is output to the LAN bus. Bus input is switched to BUS (+) only, so message transmission continues without detecting a local bus driver error. If the BNV flag is set, LAN BUS (–) output is disabled, therefore LAN BUS (–) is not driven until the bus idle status is detected after this.

If a bus idle status is detected, the BUS (–) $V_{DD}$ short detection is cleared, LAN BUS (–) output is enabled, and bus input is switched to BUS (+)/BUS (–) differential input.

<Short occurred when dominant status is output during message transmission>




**Figue 9-6 Fault Tolerance 6**

When BUS (–) shorts to $V_{DD}$ when a dominant status is output during message transmission, MSM6636 judges the status as BUS (+) shorted to $V_{DD}$, and switches receive input to BUS (–) only. This is because MSM6636 recognizes the bus whose status changed first as the normal bus. Since the LAN bus is in passive status while a dominant status is output to the LAN bus, a local bus driver abnormality is detected, and message transmission stops. If the bus busy re-transmission count has been set to "2", a message is resent when the status changes to bus idle.

If message transmission stops, BUS (+) changes from dominant status to passive status. At this time MSM6636 judges the status as BUS (+) returned to normal, and switches the bus input to BUS (+) / BUS (–) differential input. If message re-transmission starts when a bus idle is detected, only BUS (+) changes to dominant status.

MSM6636 judges this status as BUS (–) shorted to $V_{DD}$, and switches the bus input to BUS (+) only. If BUS (+) changes from dominant status to passive status after this, the BNV flag is set and LAN BUS (–) output is disabled. The message receive node may detect a message format error (FORM) or a CRC error.

If a bus idle is detected, the BUS (–) $V_{DD}$ short detection is cleared, LAN BUS (–) output is enabled, and bus input is switched to BUS (+)/BUS (–) differential input.

## 9.3 BUS (+) GND short

<Short occurred during bus idle status>

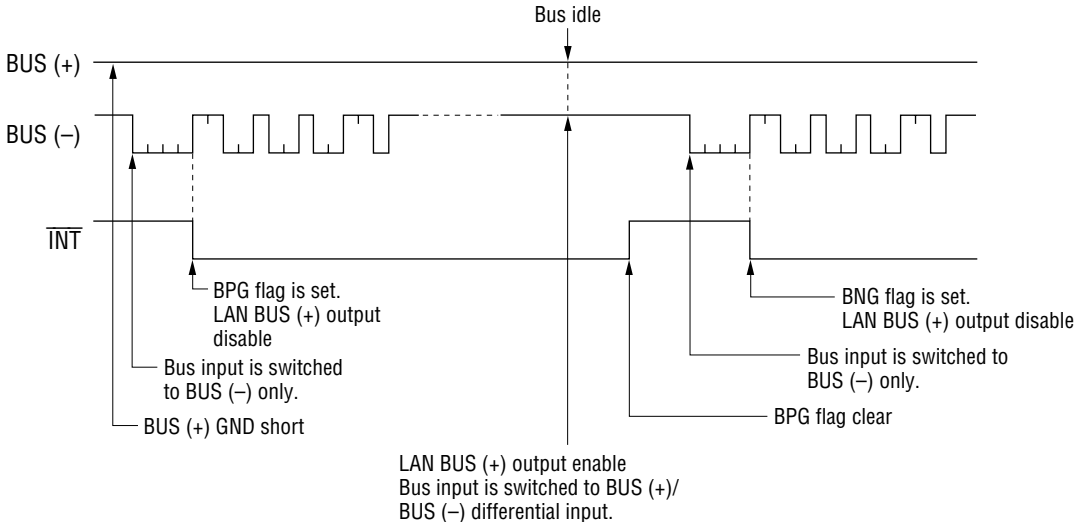



**Figure 9-7 Fault Tolerance 7**

When BUS (+) shorts to GND during bus idle status, it is detected in the same way as a BUS (–) $V_{DD}$ short.

<Short occurred when passive status is output during message transmission>

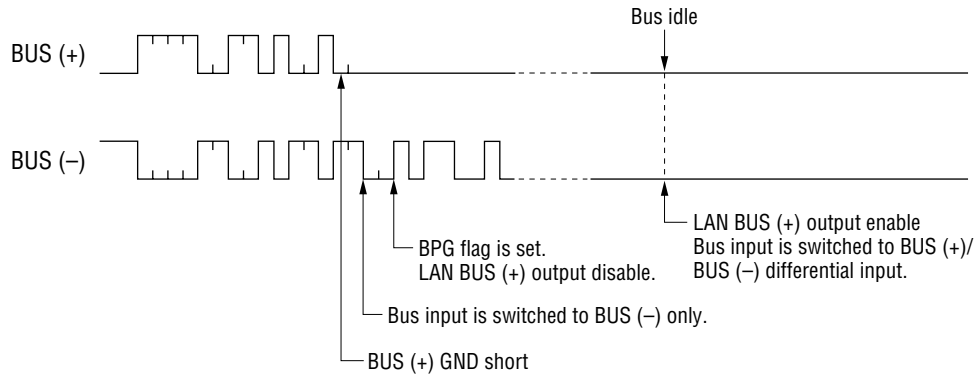



**Figure 9-8 Fault Tolerance 8**

When BUS (+) shorts to GND when passive status is output during message transmission, it is detected in the same way as a BUS (–) $V_{DD}$ short.

<Short occurred when dominant status is output during message transmission>

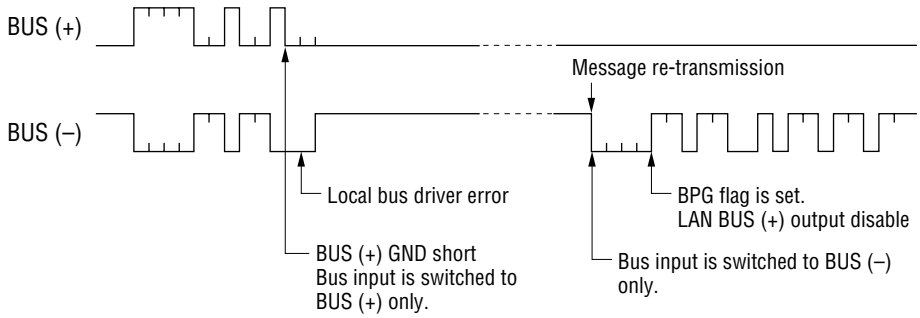



**Figure 9-9 Fault Tolerance 9**

When BUS (+) shorts to GND when dominant status is output to the LAN bus during message transmission, it is detected in the same way as a BUS (–) $V_{DD}$ short.

## 9.4 BUS (+) $V_{DD}$ Short

<Short occurred during bus idle status>

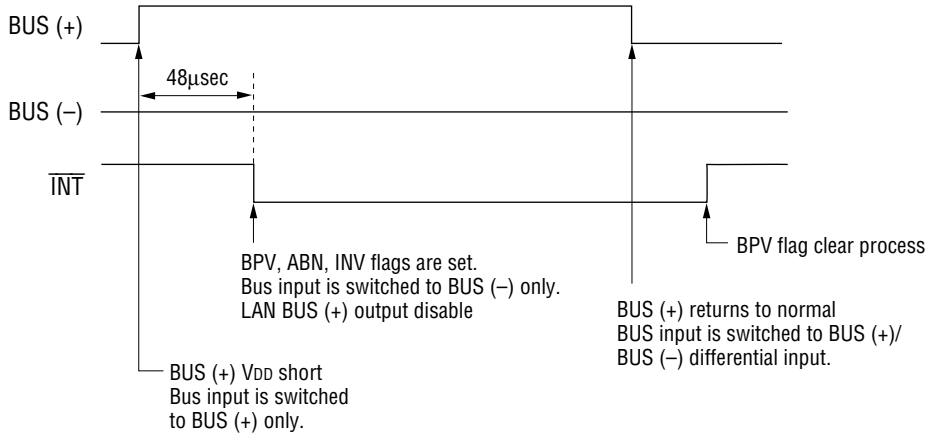



**Figure 9-10 Fault Tolerance 10**

When BUS (+) shorts to $V_{DD}$ during bus idle status, a BUS (+) $V_{DD}$ short is detected via the same flow of a BUS (–) GND short, and LAN bus input is switched to make for normal communication.

When BUS (+) returns to normal status, it is detected in the same way as a BUS (–) GND short.

<Short occurred when passive status is output during message transmission>

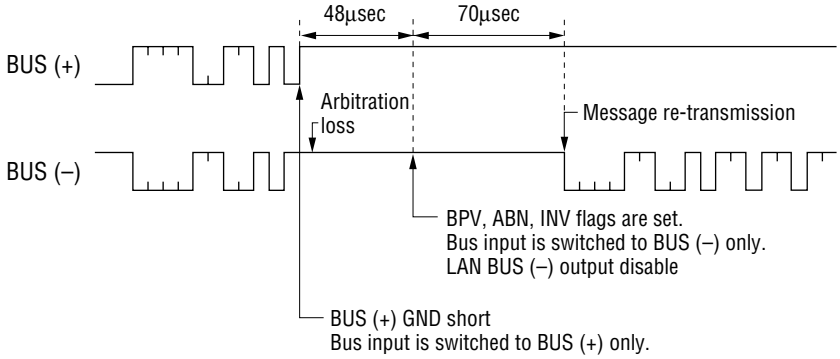



**Figure 9-11 Fault Tolerance 11**

When BUS (+) shorts to $V_{DD}$ when passive status is output to the LAN bus during message transmission, it is detected in the same way as a BUS (–) GND short.

<Short occurred when dominant status is output during message transmission>

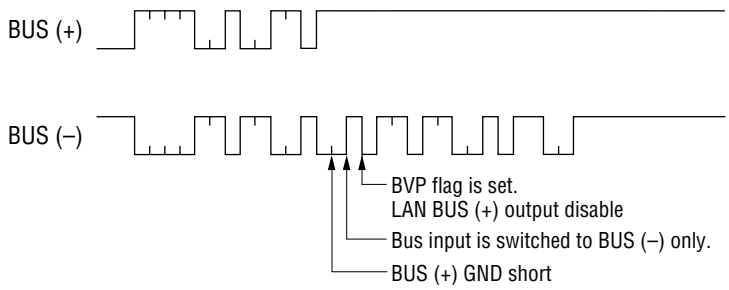



**Figure 9-12 Fault Tolerance 12**

When BUS (+) shorts to $V_{DD}$ when dominant status is output to the LAN bus during message transmission, it is detected in the same way as a BUS (–) GND short.

## 9.5 LAN Bus Open

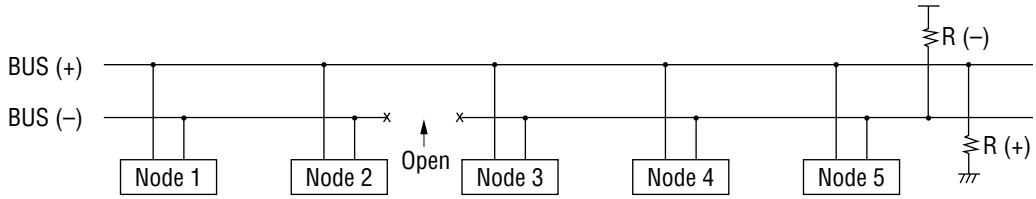



**Figure 9-13 LAN bus open**

When BUS (–) is disconnected as in the above example, each node detects the following errors.

(A) When Node 1 sends a message to all nodes:
Nodes 1 and 2 : communicate normally
Nodes 3 ~ 5 : BUS (–) shorts to $V_{DD}$ (BNV flag is set)

The bus receive input of each node is pulled up at the BI - terminal, and is pulled down at the BI + terminal on-board MSM6636 (pull-up/down resistance: 100 kΩ). Therefore Nodes 1 and 2 can communication normally if the capacity of BUS (–) of Nodes 1 and 2 is small (wave form change of BUS (–) is small), even if there is no pull-up resistance R (–) of LAN BUS (–). If capacity is large (it is slow for BUS (–) to change from dominant status to passive status) however, the status is recognized as BUS (–) shorts to GND, and the BNG flag is set. In Nodes 3~5 detect BUS (–) shorts to $V_{DD}$, and sets the BNV flag since BUS (–) does not become dominant status.

Note: The setting of the BNG flag can be further avoided by setting pull-up/pull down resistance R (+) and R (–) of the LAN bus at several locations on the LAN. If the LAN bus is loop-connected, a bus error is not detected even if a bus disconnection occurs at one location.

(B) When Node 5 sends a message to all nodes:
Nodes 1 and 2 : BUS (–) shorts to $V_{DD}$ (BNV flag is set)
Nodes 3~5 : communication normally

In Nodes 1 and 2 detect BUS (–) shorts to $V_{DD}$, and sets the BNV flag since BUS (–) does not become dominant status. Nodes 3~5 can communicate normally because pull-up resistance R (–) of the LAN bus is connected to BUS (–).

## 9.6 Example of Fault Tolerance Function Process Routine

This section introduces a process routine example for an interrupt request of the fault tolerance function. A flow chart of this process is shown on the next page.

When a LAN bus abnormality occurs, unexpected abnormal signals are usually generated on the LAN bus. Therefore interrupt requests generated by MSM6636 are also unexpected. If multiple LAN bus related interrupts (BPG, BPV, BNG and BNV flags) are generated, check whether the break command receive flag (BRK) is set, then clear all interrupt request flags. If the break command receive flag is set at this time, message transmission stops, so there is no node which outputs a message on the LAN after an abnormality occurs on the LAN bus. If a local node is sending a message, a message transmission instruction is output to MSM6636 again.

Even if the break command receive flag is not set, a message transmission instruction is output to MSM6636 again if all nodes of the LAN are not set to no re-transmission (non ACK and bus busy). If a message is output to the LAN bus, one of the LAN bus related interrupts is generated, and a process according to the interrupt is performed.

If only one LAN related interrupt is generated when a LAN bus abnormality occurs, the interrupt request flag is not cleared as above.
Example of LAN bus wave form when BUS (+) shorts to $V_{DD}$:

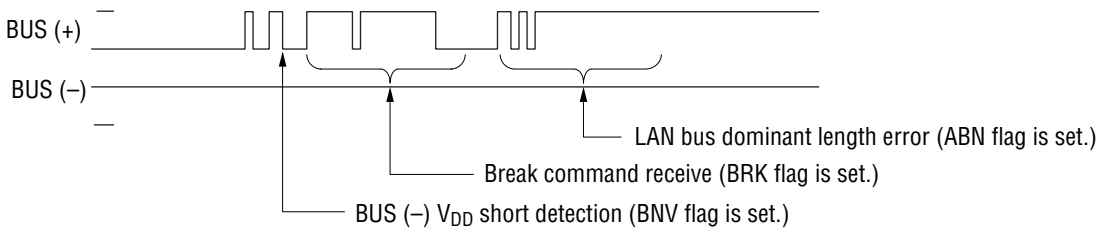



**Figure 9-14 Example of Bus Short Wave Form**

Note: If the LAN bus output is set to disable in the process routine example introduced here, all nodes output a message only to one bus, therefore it cannot be judged whether the LAN bus returned to normal. In this case, clear the LAN bus output disable when clearing sleep status, and check the LAN bus.

LAN bus output is disabled, to prevent excess current from flowing into the external bus driver when sending “SOF”.

Example of fault tolerance process flow

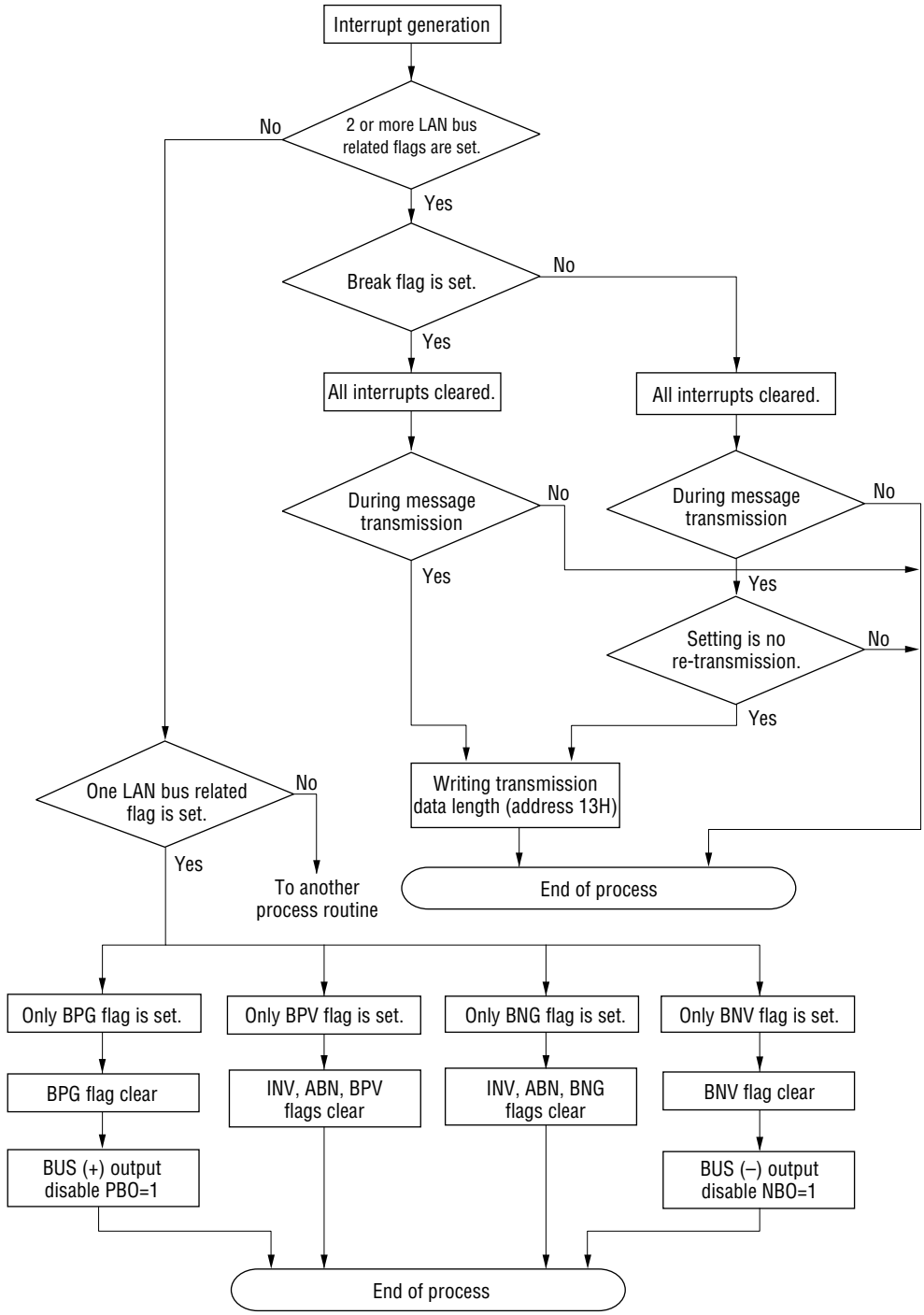



**Figure 9-15 Example of Fault Tolerance Process Flow**

*Chapter 10*

# BREAK FUNCTION

## 10. BREAK FUNCTION

A break command is transmitted by writing “55H” to the break command register (address 29H).

If the LAN bus is in transmission, a BRK transmission status when the end of the PWM bit format is detected after a break command transmission instruction. If a break command is sent, all nodes on the LAN (including the BRK transmission node) receive the break command, communication is force-stopped, and the LAN bus enters idle status.

Break command transmission timing is shown below.

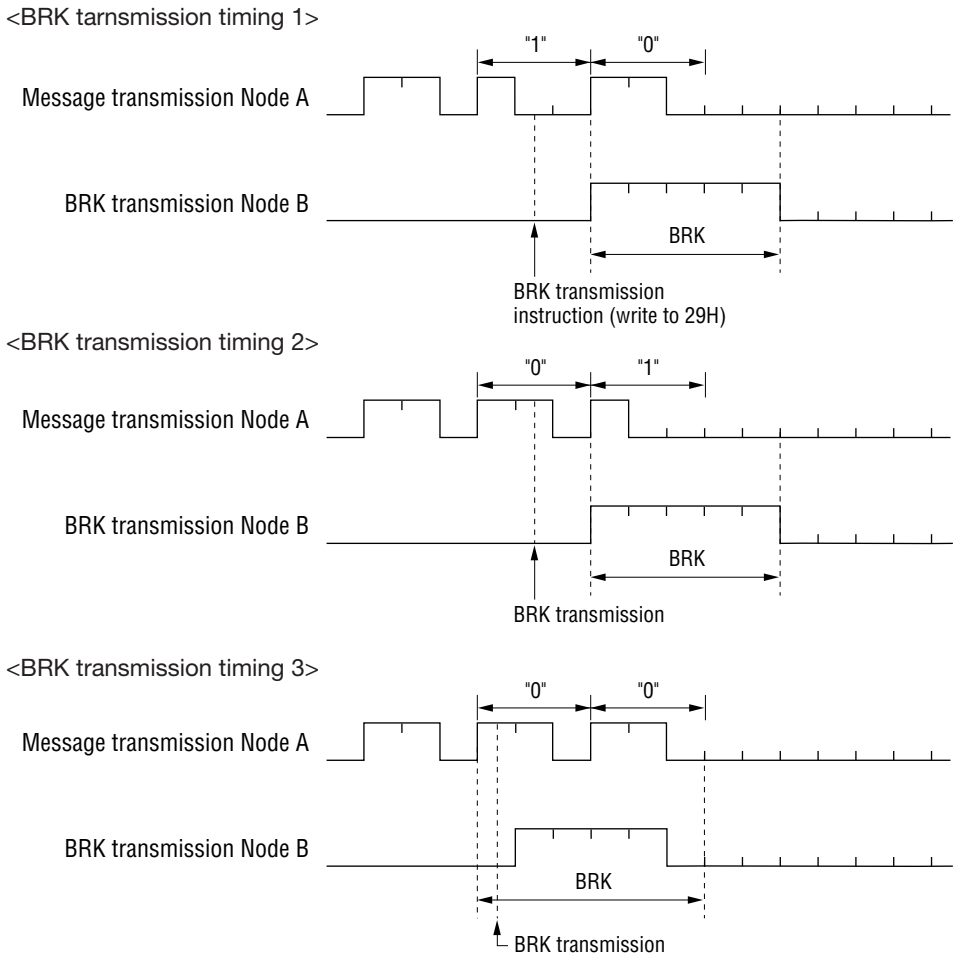



**Figure 10-1 BRK Transmission Timing (1/2)**

<BRK transmission timing 4>

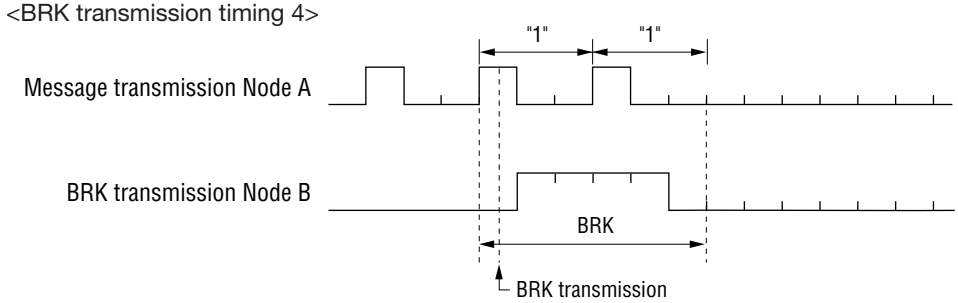



**Figure 10-1 BRK Transmission Timing (2/2)**

When a break command is received during message transmission, the message re-transmission function (re-transmission for non ACK and bus busy) does not work. Also a response is not re-transmitted when a break command is received during an IFR type 2 response transmission.

## 10.1 Example of Break Function Routine

This section introduces an example using the break function.

A break function is generally used to transmit an urgent message.

When it is necessary to send an urgent message to Node A, the CPU instructs MSM6636 to send a break command. By the break command, all nodes on the LAN set the break command receive flag (BRK), Node B in-communication stops communication, and the LAN bus becomes idle status. Node A, who sent the break command, also generates an interrupt by break receive. When the interrupt is generated, Node A outputs a message transmission instruction, then message transmission to Node A can be performed immediately.

Break function routine example

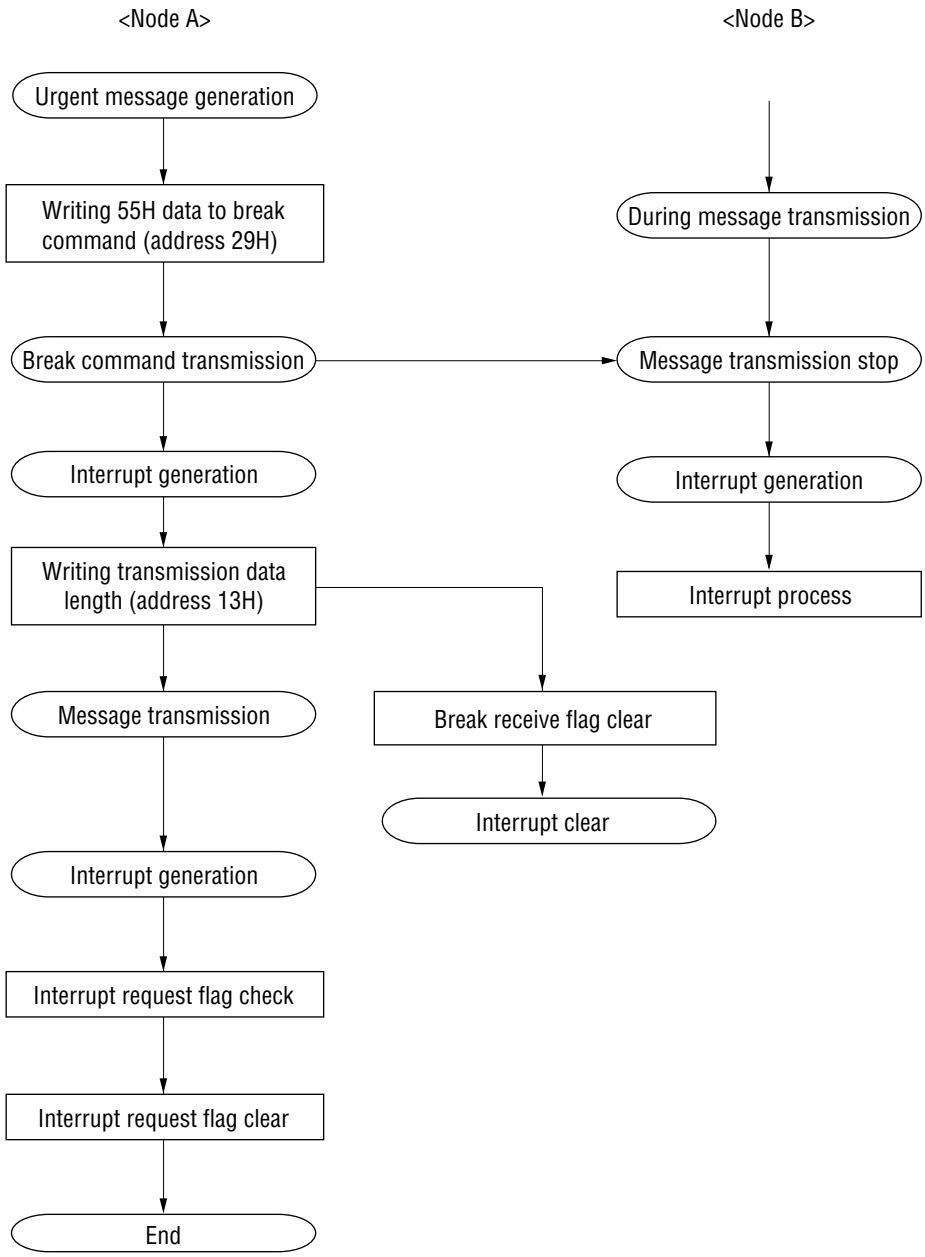



**Figure 10-2 Example of BRK Function Routine**

*Chapter 11*

# COMMUNICATION EXAMPLE USING IFR TYPE 3

## 11. EXAMPLE OF COMMUNICATION USING IFR TYPE 3

IFR type 3 communication is appropriate for such cases as a data collecting node reads status of other nodes (switch information, sensor information, etc.) periodically (cyclic) preparing multi-byte response data in advance. An example of communication using IFR type 3 is introduced here.

The following is an example of node configuration.

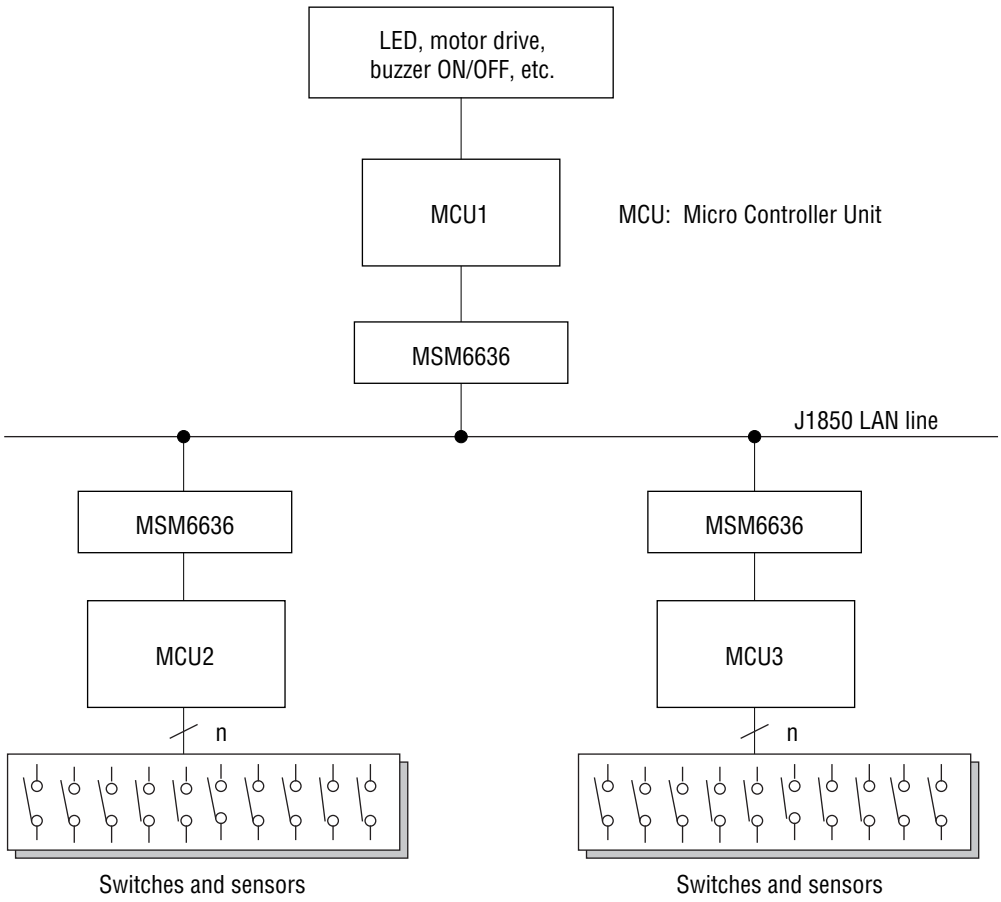



**Figure 11-1 Example of Node Configuration of IFR Type 3 Communication**

- MCU2 periodically updates switch and sensor status information in the response register.
- MCU3 also updates the status in the response register.
- MCU1 periodically receives the switch status, etc. as response data via IFR type 3 communication to MCU2 and 3.

As the above example shows, the MCU of each node can execute respective process routines independently. The process flow, MCU1 sends a “data request” to MCU2, MCU2 collected data with the request as a trigger, and “sends data” to MCU1, can be simplified by IFR type 3 communication.

MCU 2 and 3, can of course communicate with other nodes using IFR type 1 or 2 communication. Since MCU 2 and 3 are still waiting for a request by IFR type 3 communication, they immediately send status information as a response whenever a request is received.

## 11.1 How to Use NAK Register

In the case of IFR type 3 communication, the response transmission node must be in response transmission standby status before receiving a message requesting an IFR type 3 response. This means that data to send as an IFR type 3 response must have been written to the response register (0BH~12H), and the response data length must have been written to the response data length register (14H) in advance.

In a system design which uses IFR type 3, each node often executes respective processes independently, so in some cases the preparation of response data may be too late.

For example, a response may not be ready due to various factors, such as “Updating data delayed because it took time for the CPU to perform another interrupt process”, “Hardware trouble occurred to the node itself”, or “Microcomputer run away occurred”. In SAE-J1850 standard, there is “Response is not returned” when preparation delays, however MSM6636 also supports a mode “to return the content of the NAK register as a response”.

To use the NAK function, select “Yes” for the NAK return “Yes/No setting flag of the mode setting register (2AH) in the node initialization routine, and set the specified data at the NAK register (3BH).

Then if the microcomputer process is delayed in the request destination in IFR type 3 communication, NAK is returned. In the case of a hardware problem, nothing is returned.

*Chapter 12*

# BUS DRIVER

## 12. BUS RECEIVER

MSM6636 has an internal bus driver shown in Figure 12-1.

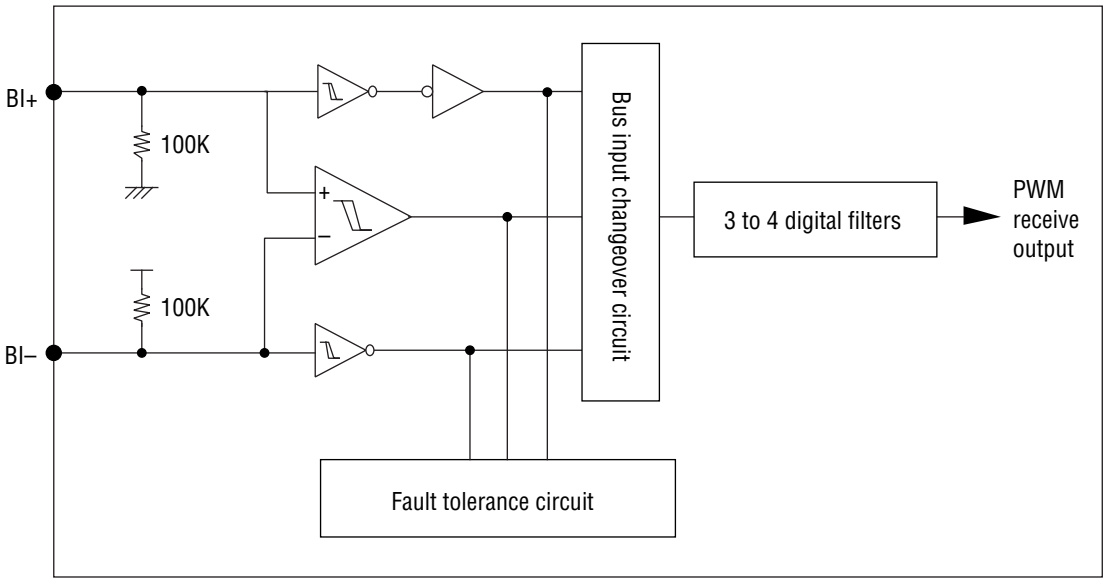



**Figure 12-1 Bus Receiver**

When the LAN bus is normal (no problems, such as a $V_{DD}$ short), a bus input signal is output from a comparator having hysteresis with BI+ and BI– terminal as input. This input signal is input into 3 to 4 digital filters, and its output signal becomes the receive signal.

The operation frequency of a digital filter is 1 MHz when the transmission speed is set to 41.6 Kbps.

When an abnormality is detected at BUS (+), a Schmitt inverter output with the BI– terminal as input becomes the bus input signal, and when an abnormality is detected at BUS (–), a Schmitt inverter output with the BI+ terminal as input becomes the bus input signal.

*Chapter 13*

# SOURCE OSCILLATION FREQUENCY TOLERANCE

# 13. SOURCE OSCILLATION FREQUENCY TOLERANCE

If the difference of source oscillation frequency among nodes is large, the arbitration function does not operate normally. If the difference is even larger, a PNW bit format error occurs, and communication becomes impossible. “Normal arbitration” here means that priority is normally determined by the priority field, etc. when a transmission start contention occurs among nodes.

## 13.1 Source Oscillation Frequency Tolerance of Arbitration Function

This section describes the source oscillation frequency tolerance with which arbitration function operates normally when sending a message or response.

Arbitration status occurs in the following 3 cases.

(A) Each node starts communication at the same time in bus idle status or in non-communication status, and their “SOF” signals collide.

(B) Since a message transmission instruction was output when the status is not bus idle status, the multiple nodes standby for message transmission until this message frame ends, and bus idle status is detected.

(C) Arbitration in response frame during communication by functional address of IFR types 1 and 2.

(A) occurs with extreme rarity. Since each node executes an independent application by an independent host CPU, it is “rare” that message transmission requests occur at the same time, and transmission starts under the exact same timing.

In case (B), a standby for message transmission by detecting non-bus idle status is quite likely to occur. It is necessary for the arbitration function to operate and to determine priority normally by a priority field or by an ID field.

In J1850, each node synchronizes the internal circuit each time it detects a change of the LAN bus from passive to dominant status. However, when the source oscillation frequency of each node is different, the difference accumulates and an out of sync occurs if the passive status of the LAN bus is long. In this case, the arbitration function does not operate normally.

The source oscillation frequency tolerance of cases (A)~(C) is described below. (B) is described first.

<Case (B)> During message re-transmission

Let us examine a case when Nodes B and C retransmit a message after the transmission of Node A ends, for example. In this example the source oscillation frequency of Nodes A and B are the same, and the source oscillation frequency of Node C is lower than that of Nodes A and B.

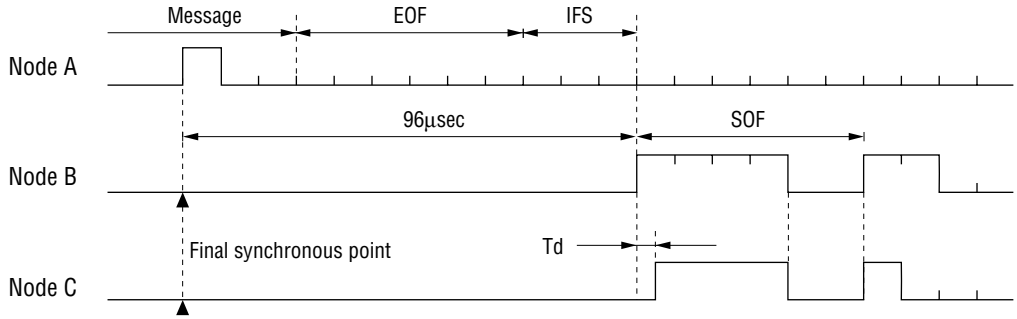



**Figure 13-1 Source Oscillation Frequency Error During Message Re-transmission**

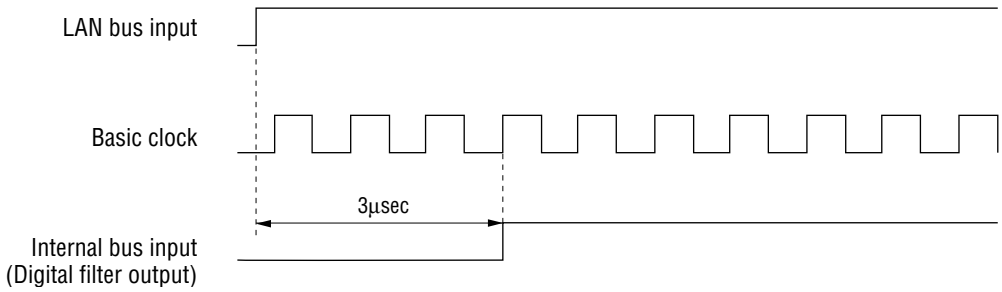



**Figure 13-2 MSM6636 Internal Digital Filter Output**

In MSM6636, bus input signals have been filtered through digital filters. Therefore a bus input signal input into MSM6636 delays, and a change of the LAN bus from passive to dominant status is detected at a minimum of 3μsec after the actual change of the LAN bus (see Figure 13-2). This means that the time from the transmission start of Node B to the transmission start of Node C (Td) (Figure 13-1) must be less than 3μsec for Node C to start transmission in normal arbitration status. If this time, Td, becomes 3μsec or longer, Node C synchronizes with the bus output of Node B, loses transmission timing, and detects a non-bus idle status. As a consequence, the source oscillation frequency tolerance with which the arbitration function can operate normally during message re-transmission is calculated as follows.

The time from the final synchronous point of the nodes (Figure 13-1) to "SOF" transmission is 96μsec, so

$3\mu s/96\mu s \times 100=3.125\%$
$\pm 3.125/2 \fallingdotseq \pm 1.56\%$

This value does not include the delay caused by the bus driver or by the bus receiver. If these delays at their longest are considered, the tolerance becomes even smaller.

<Case (A)> Simultaneous message transmission start during bus idle status

When message transmission starts at the same time during bus idle status, the source oscillation frequency tolerance with which the arbitration function operates normally becomes smaller as the bus idle time becomes longer.

When the bus idle time is 1 msec, the time from the final synchronous point to "SOF" transmission is 1msec + 96μsec, and at this time, the source oscillation frequency tolerance is:

$3\mu sec/(1msec + 96\mu sec) \times 100 \fallingdotseq 0.27\% = \pm 0.135\%$

In J1850, 8μsec is 1 cycle of synchronization. This means that the accumulation of the source oscillation frequency difference among nodes becomes virtually "0" when the accumulation becomes 8μsec. In other words, when the bus idle status is long, the accumulation of the source oscillation frequency difference is circulating in a 0μsec~8μsec range. Therefore when the accumulation of the source oscillation frequency differences is less than 3μsec, the arbitration function operates normally regardless the source oscillation frequency tolerance.

<Case (C)> During response transmission

If the source oscillation frequency tolerance, with which the arbitration function operates normally during response transmission, is determined, less than 3μsec of the source oscillation deviation accumulation can be tolerated until "EOD" is detected, just like in case (B). If this value is divided by 48μsec, the time until "EOD" is detected:

$3\mu sec/48\mu sec \times 100=6.25\%=\pm 3.125\%$

The source oscillation frequency tolerance with which the arbitration function operates normally during response transmission.

## 13.2 Source Oscillation Frequency Tolerance of Communication Function

This section describes the source oscillation frequency tolerance with which communication (message transmission/receive) can be performed normally.

When receiving a message, internal circuits are synchronized each time the LAN bus changes from passive to dominant status, so the accumulation of source oscillation deviation during message receiving becomes largest when “SOF” is received. Since the receive tolerance of “SOF” is 45μsec~52μsec in “SOF” lengths, if the “SOF” length of the transmission source is 48μsec, a minimum of 3μsec of the accumulation of the oscillation deviation can be tolerated. Therefore the source oscillation frequency tolerance to receive a message is:

$$3\mu sec/48\mu sec \times 100=6.25\%=\pm 3.125\%$$

*Chapter 14*

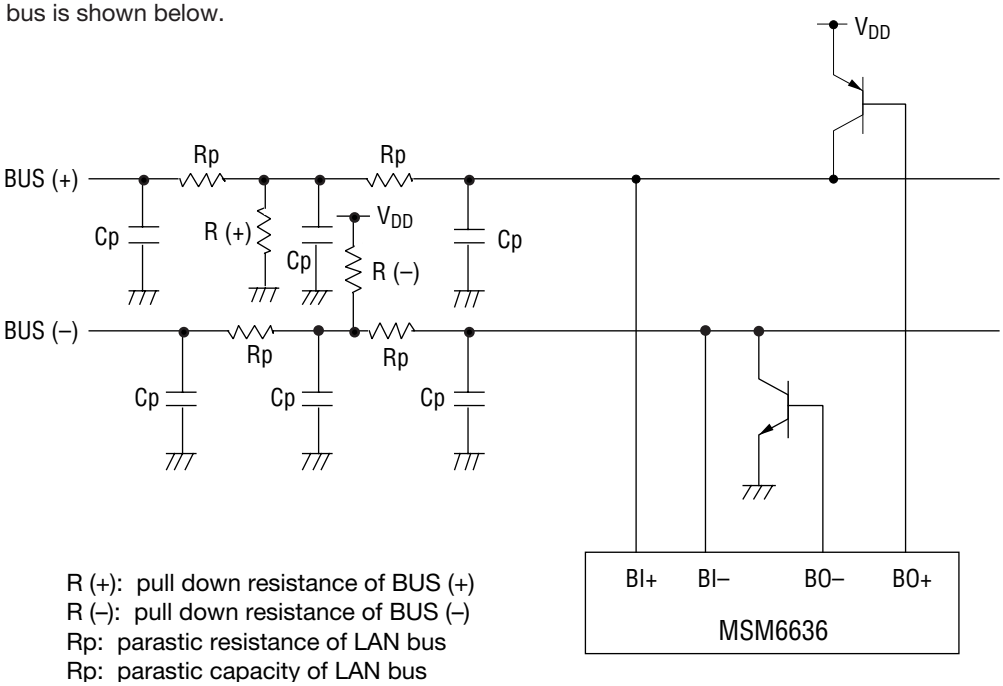
# PRECAUTIONS WHEN DESIGNING LAN USING MSM6636

## 14. PRECAUTIONS WHEN DESIGNING LAN USING MSM6636

This section explains precautions when designing a LAN using MSM6636 and introduces design examples.

### 14.1 Precautions When Designing LAN Bus

Since a LAN bus uses wired OR logic, a LAN bus needs pull-up resistance and pull down resistance. The time for a LAN bus to change from dominant to passive status is determined by this resistance value and by parasitic capacity and the parasitic resistance of the LAN bus. In other words, the time is determined by a CR discharge duration. An equivalent circuit of an actual LAN bus is shown below.




R (+): pull down resistance of BUS (+)
R (–): pull down resistance of BUS (–)
Rp: parastic resistance of LAN bus
Rp: parastic capacity of LAN bus

**Figure 14-1 LAN Bus Equivalent Circuit**

A comparison of LAN bus waveforms depending on the resistance value of pull-up and pull down resistances R (+) and R (–) of a LAN bus is shown below.

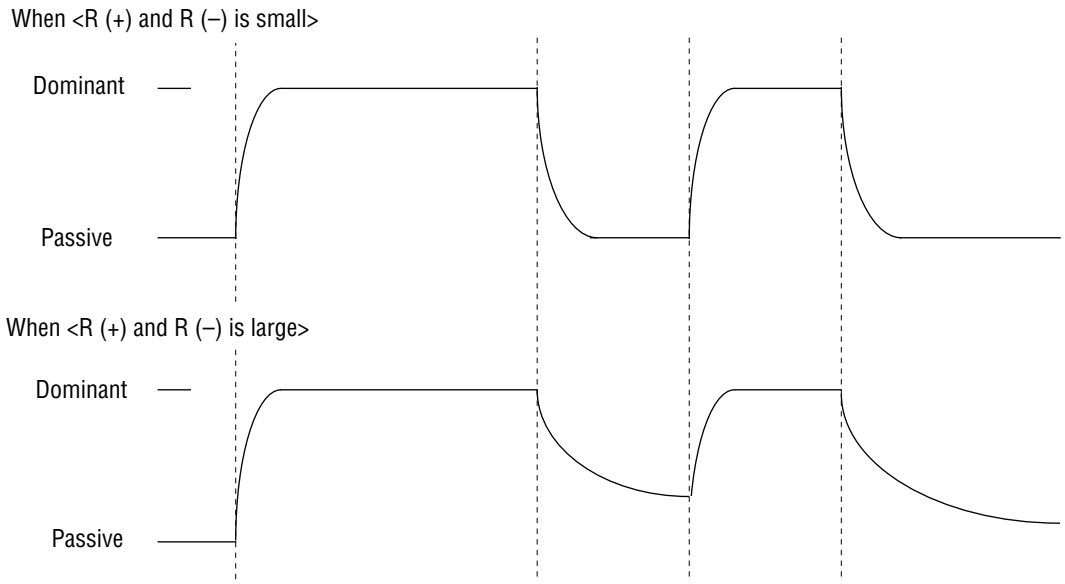



**Figure 14-2 Comparison of LAN Bus Waveforms Depending on resistance Value of R (+) and R (–)**

If the resistance values of R (+) and R (–) is large, LAN bus waveforms are distorted and the passive period disappears, which may make normal communication difficult. In a LAN which extends over a wide range, the parasitic element Rp and the Cp values become large. In this case as well, LAN bus waveforms are distorted, and normal communication may become difficult.

The change of LAN bus waveforms depending on the configuration of the LAN bus and the setting of pull-up resistance and pull down resistance is described below.

Let us consider the LAN shown in Figure 14-3, which has an overall length of 40mm and 6 nodes. Each node is connected with equal spacing, the parasitic element value does not negate each value as equal, and the parasitic element value per unit length of the LAN bus is equal.

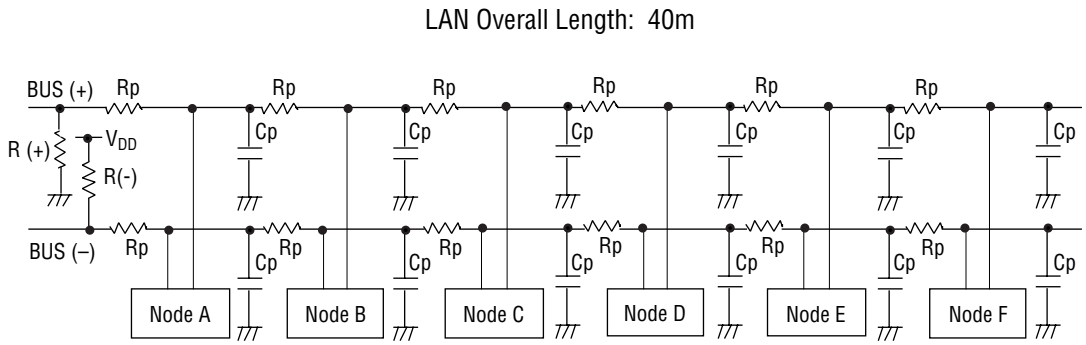



**Figure 14-3 LAN Configuration Example 1**

If Node A transmits a message to Node F, the distance and parasitic element value between nodes is largest in Node A to Node F, and the LAN bus wave form which Node F receives is considerably distorted, which may make normal communication difficult.

To improve this problem, let us consider the LAN configuration shown in Figure 14-4. Since the distance between nodes is longest when Node A sends a message to Node D, the longest distance and parasitic resistance value between nodes becomes half that of the LAN configuration of Figure 14-3, and the distortion of LAN bus waveforms is less than that of Figure 14-3.

However, in both Figures 14-3 and 14-4, Node A, the closest to pull-up resistance and pull down resistance of the LAN bus, receives the least distorted LAN bus waveforms. The distortion of the LAN bus waveforms which each node receives are all different.

This problem has been improved in the LAN configuration shown in Figure 14.5. In this LAN configuration, each node has pull-up and pull down resistance of the LAN bus to equalize the LAN bus wave form distortions which each node receives.

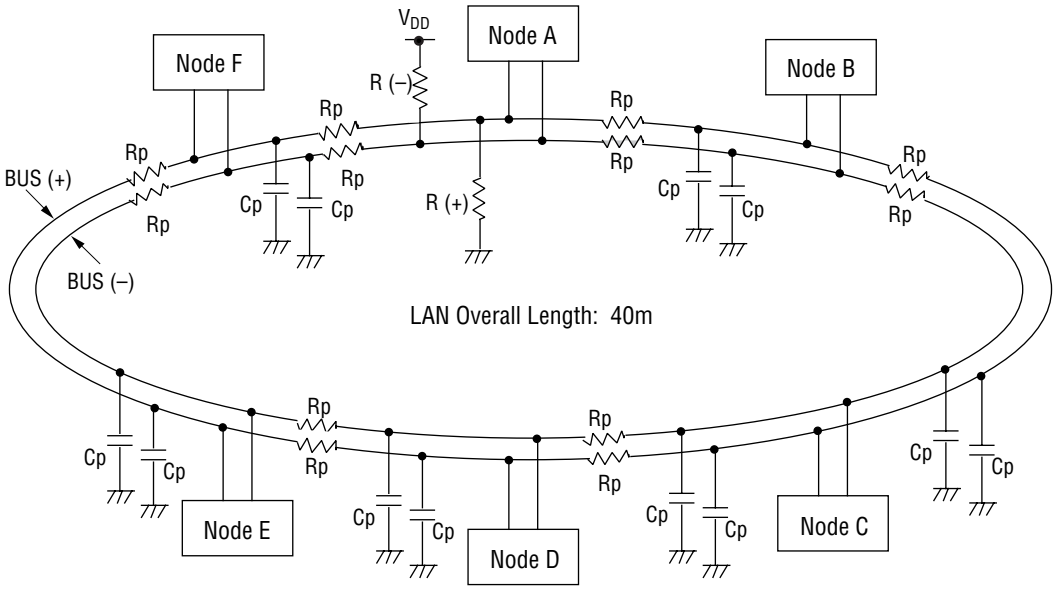



**Figure 14-4 LAN Configuration Example 2**

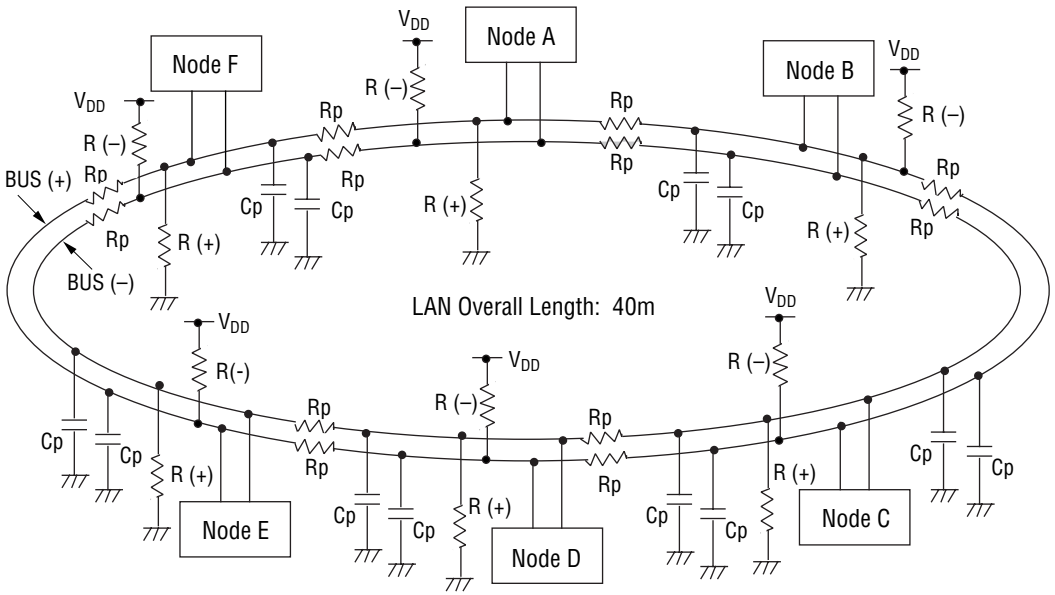



**Figure 14-5 LAN Configuration Example 3**

## 14.2 Precautions When Designing Bus Driver

A bus driver circuit example is shown below.

Resistances R1 and R6 limit the electric current which flows into the PNP transistor and the NPN transistor of the bus driver. Resistances R2 and R5 limit the output current of bus output terminals B0+ and B0– of MSM6636. The bus output of MSM6636 is CMOS output, and has about a 4mA output current capacity. When designing a bus driver, it is necessary to determine the drive current capacity of the bus driver, so that the loads of pull-up resistance R (–) and pull down resistance R (+) of the LAN bus can easily be driven. It is also necessary to match the drive capacity, speed, etc. of the BUS (+) side with the BUS (–) side. If this matching is incomplete, LAN bus drive waveforms become as follows. In this case the fault tolerance function works, and LAN bus abnormalities are detected.

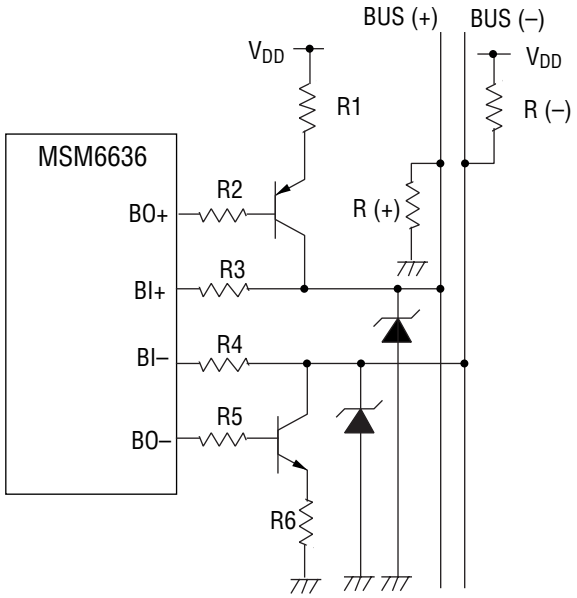
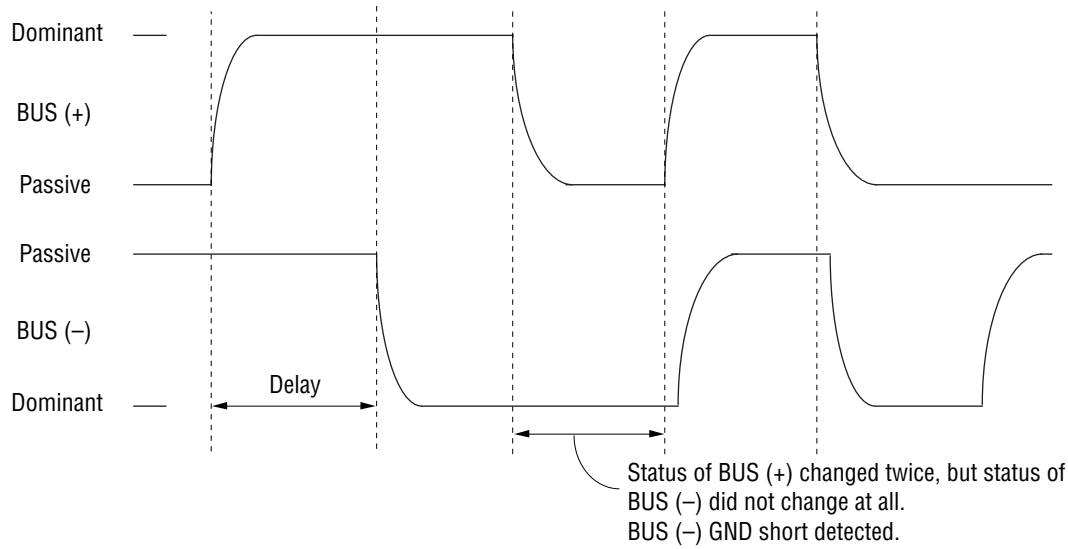



**Figure 14-6 Example of Bus Driver Circuit**

<Mismatching of Speed>




<Mismatching of Drive Capacity>

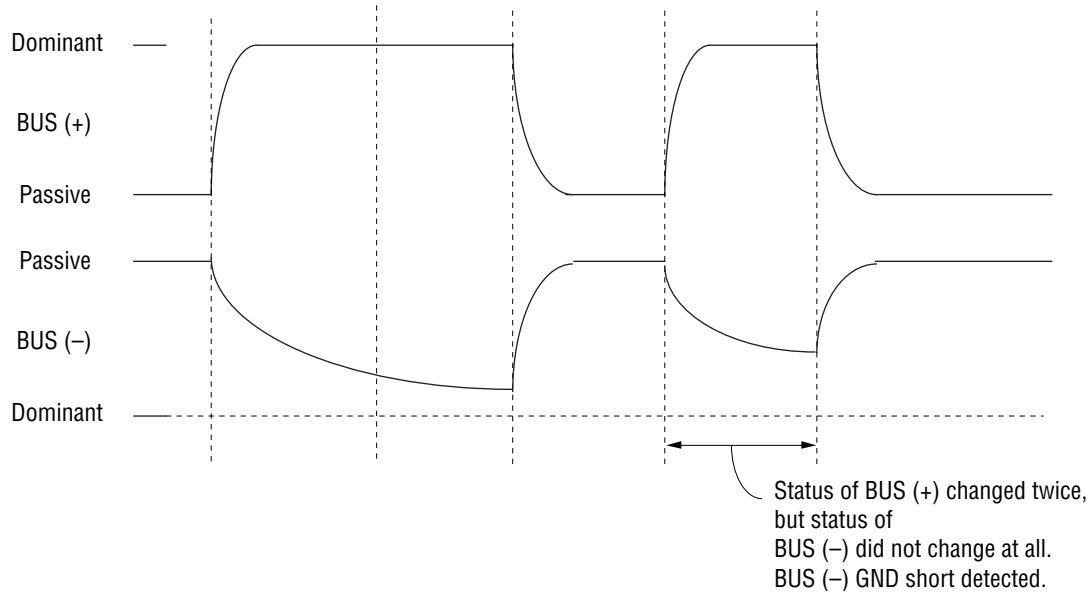



**Figure 14-7 LAN Bus Waveforms When Bus Drivers Mismatch**

## 14.3 GND Offset

This section describes precautions when the GND potential of each node on a LAN is different.

Figure 14-8 shows the case when difference between the GND potential of Unit B, and the GNE potential of Unit A is voltage V0ff.

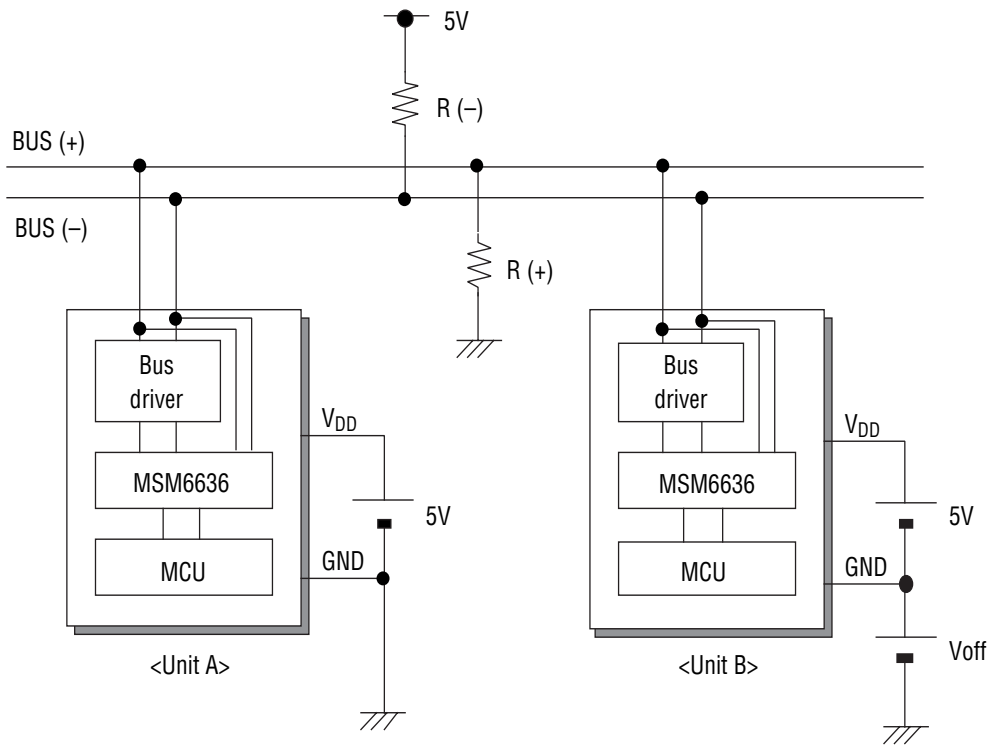



**Figure 14-8 LAN with GND Offset**

When Unit A receives a message from Unit B, Unit A receives a LAN bus wave form having voltage Voff of the offset, as shown below.

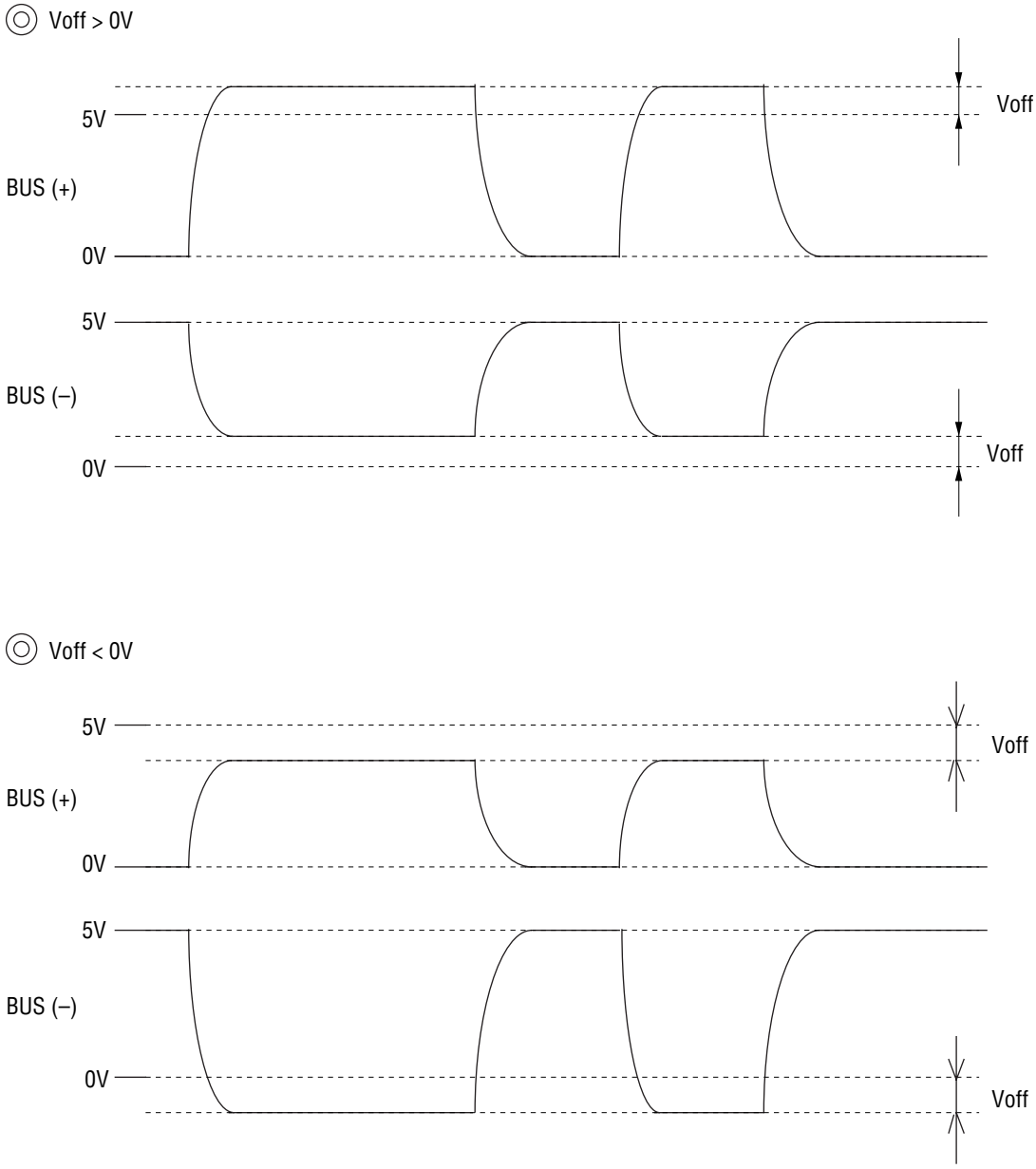



**Figure 14-9 LAN Bus Waveforms with GND Offset**

A protective diode is positioned between the power terminal ($V_{DD}$) and the GND terminal (GND) at LAN bus input terminals BI+ and BI– of MSM6636. If this GND offset Voff becomes ± 1V or more, electric current flows through this protective diode. To limit electric current from flowing into the protective diode, we recommend that you insert resistance RIN between the LAN bus and LAN bus input terminals BI+ and BI–. About 100 kΩ of pull down and pull-up resistances are internally connected to LAN bus input terminals BI+ and BI- respectively. If resistance RIN is input, the input voltage of the LAN bus input terminals become a voltage in which resistance is divided into resistance RIN and internal pull-up/pull down resistances.

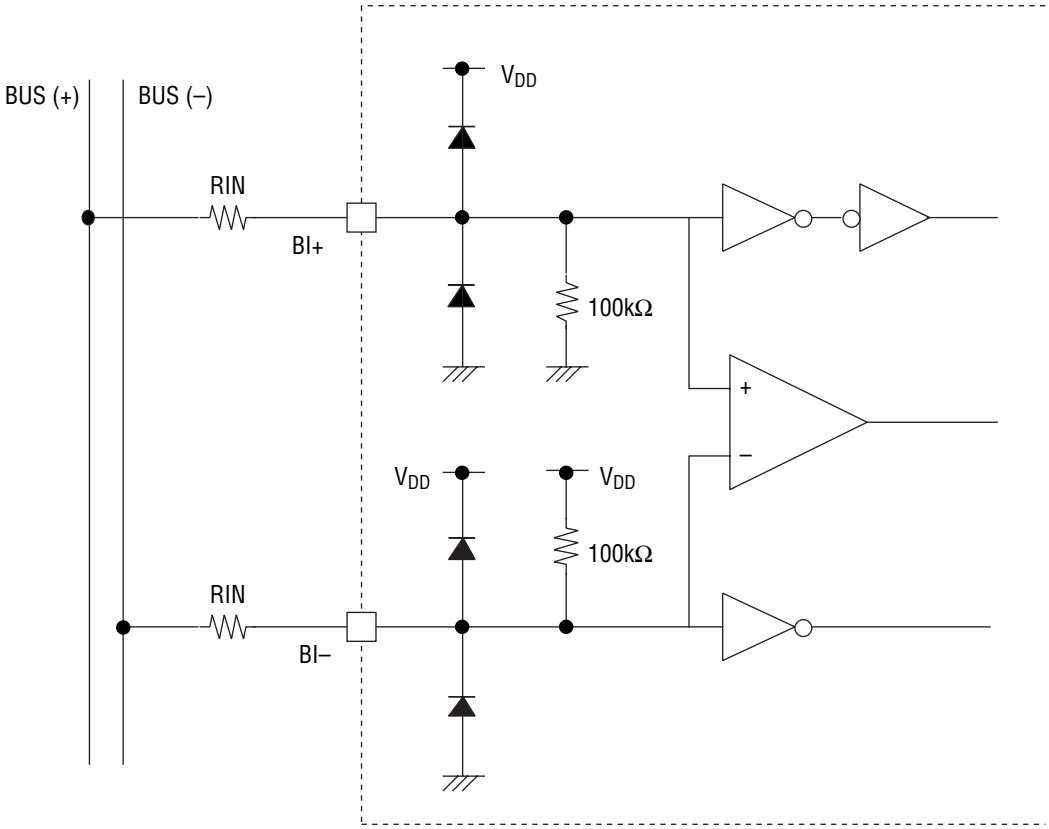



**Figure 14-10 Internal Equivalent Circuit of LAN Bus Input Terminals BI+ and BI–**

## 14.4 CPU Interface Selection and Message Receive Processing Time

MSM6636 has 6 types of CPU interfaces. Depending on the selection of the CPU interface, the communication speed between MSM6636 and the CPU differs. The CPU interface must be selected considering the selection of the source oscillation frequency and the speed of LAN communication.

Let us think about the time required for message receive processing by the CPU when the shortest message is continuously sent to a node. Figure 14-11 shows an example of a series of processes from when a message receive interrupt is generated to when a message receive process ends.

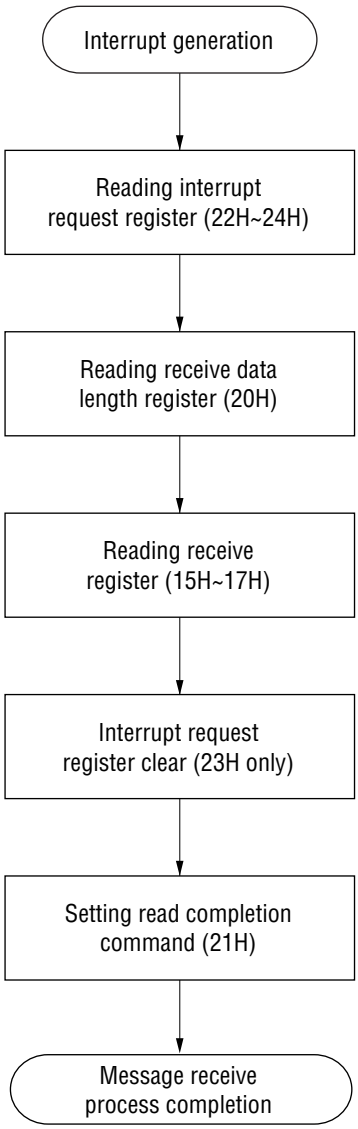



**Figure 14-11 Message Receive Process Flow**

The minimum communication time of each CPU interface to perform the process shown in Figure 4-11 is as follows. The source oscillation cycle is tϕ.

[1]: clock synchronous normal mode=1872tϕ
[2]: clock synchronous MPC mode=2096tϕ
[3]: UART normal mode without parity=11660tϕ
[4]: UART normal mode with parity=12812tϕ
[5]: UART MPC mode without parity=12812tϕ
[6]: UART MPC mode with parity=13964tϕ

A list of MSM6636 processing times, depending on the selection of the source oscillation frequency, is shown below.

[Unit: µsec]

| Source oscillation / Interface | 2MHz | 4MHz | 5MHz | 8MHz | 10MHz | 12MHz | 16MHz |
|---|---|---|---|---|---|---|---|
| [1] | 936 | 468 | 374.4 | 234 | 187.2 | 156 | 117 |
| [2] | 1048 | 524 | 419.2 | 262 | 209.6 | 174.7 | 131 |
| [3] | 5830 | 2915 | 2332 | 1457.5 | 1166 | 971.7 | 728.6 |
| [4] | 6406 | 3203 | 2562.4 | 1601.5 | 1281.2 | 1067.7 | 800.8 |
| [5] | 6406 | 3203 | 2562.4 | 1601.5 | 1281.2 | 1067.7 | 800.8 |
| [6] | 6982 | 3491 | 2792.8 | 1745.5 | 1396.4 | 1163.7 | 872.8 |

**Figure 14-12 Receive Processing Time vs. Source Oscillation Frequency**

Figure 14-13 shows the case when a message receive interrupt is generated to a node and the next receiving message starts as soon as the message frame ends. At this time, the CPU of this node starts a message receive process triggered by a message receive interrupt generation, however the data newly received after this is not stored to the receive register unless the read completion command (address 21H) is set. If the read completion command is set before receiving EOD code of the new message (before detecting an overrun error), the new message is received normally and is stored to the receive register.

Since the time from a message receive interrupt generation to an overrun error detection is about 860 µsec, a message receive process must be completed within 860 µsec. If CPU interface [6] is used, it is necessary to select either 16 MHz of the source oscillation frequency or a LAN communication speed slower than 41.6 Kbps.

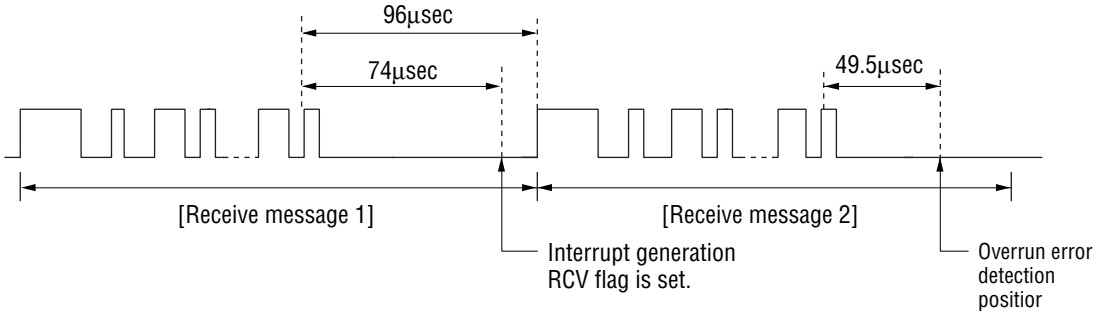



**Figure 14-13 Continuous Message Receive**

## 14.5 Off Node Process

Depending on the application, some units may not be used for LAN construction. The following is an example of how to process a unit which is not used (off node process).
If Unit D is not used in the following LAN configuration, the power of Unit D is usually shut off, but the electric current path from the LAN bus to the off node unit still exists.
When BUS (+) becomes dominant status (BUS (+)=5V), electric current flows from the bus driver of the unit, which made BUS (+) dominant status, to the internal protective diode of MSM6636. This is one such electric current path. Another path is the path from pull-up resistance of BUS (–) to BI– terminal input pull-up resistance on-board MSM6636 of the off node. Figure 14-17 shows these electric current paths.

To prevent this electric current from flowing, be certain to shut the unit power OFF, and to disconnect the unit from the LAN bus.

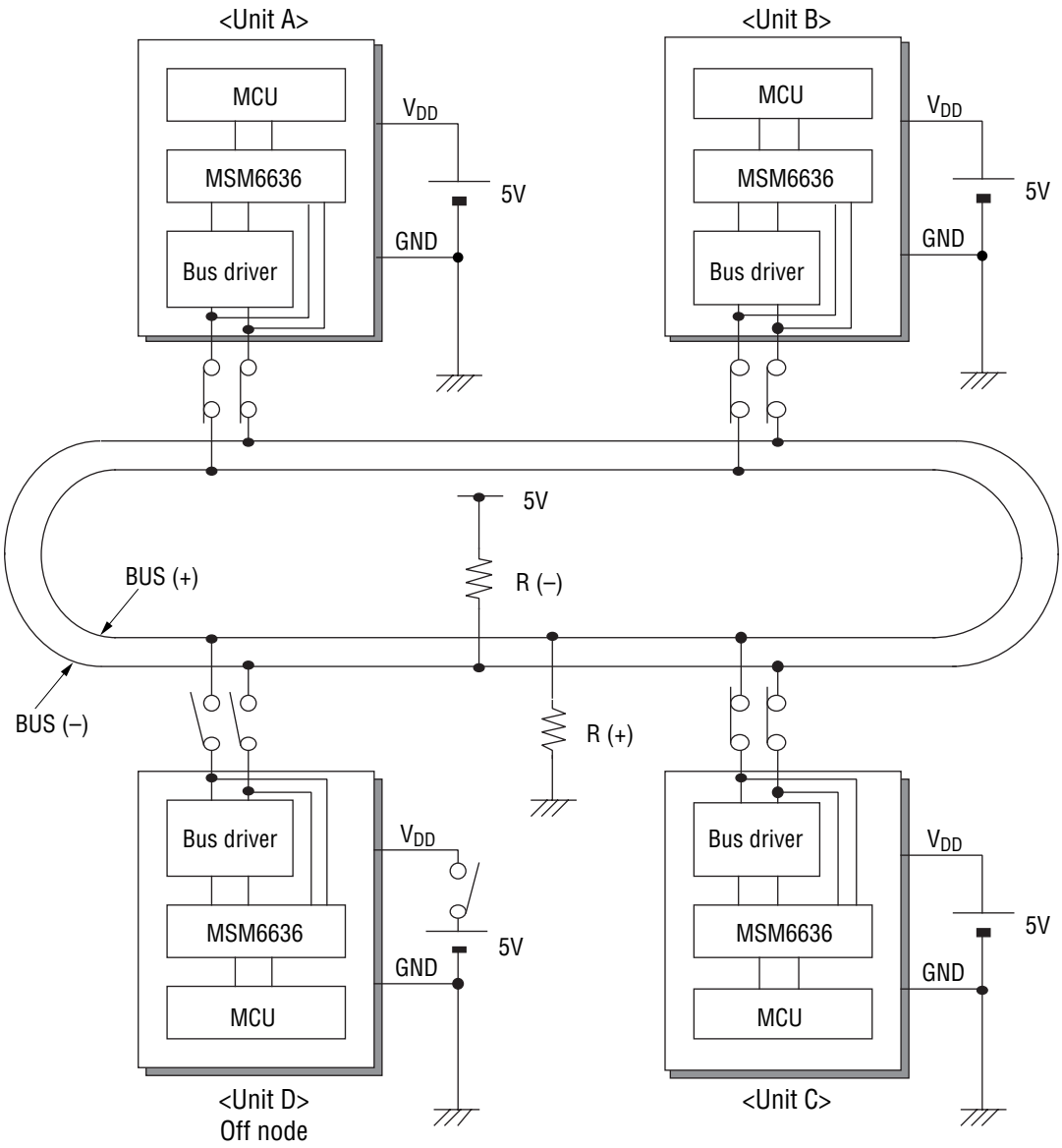



**Figure 14-14 LAN with Off Node**

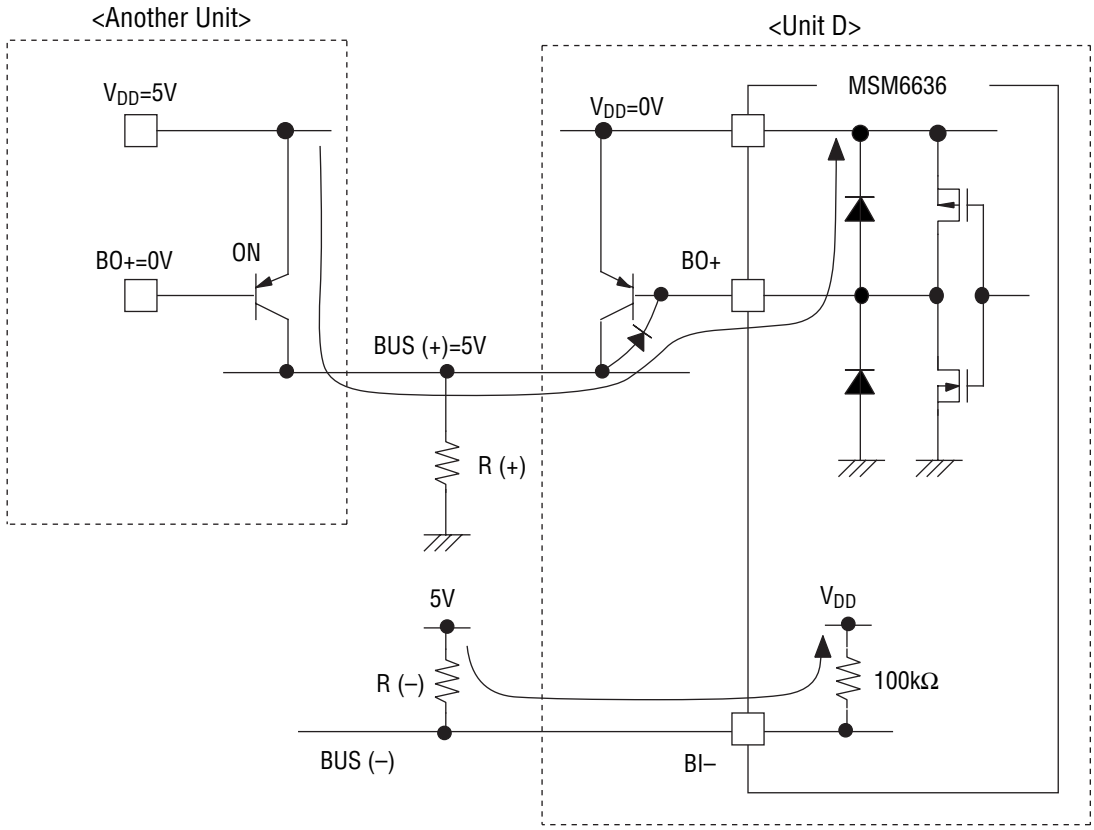



**Figure 14-15 Electric Current Path to Off Node Unit**