PEDL6666-04

OKI Semiconductor

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MSM6666 Preliminary

LCD Active Matrix Gate Driver

GENERAL DESCRIPTION

The MSM6666 is an LCD active matrix gate driver fabricated in CMOS technology.
The device is composed of a 200-bit bi-directional shift register circuit, input level shifter circuit, etc. High voltage operation at 40 V has been realized using high breakdown voltage CMOS process.

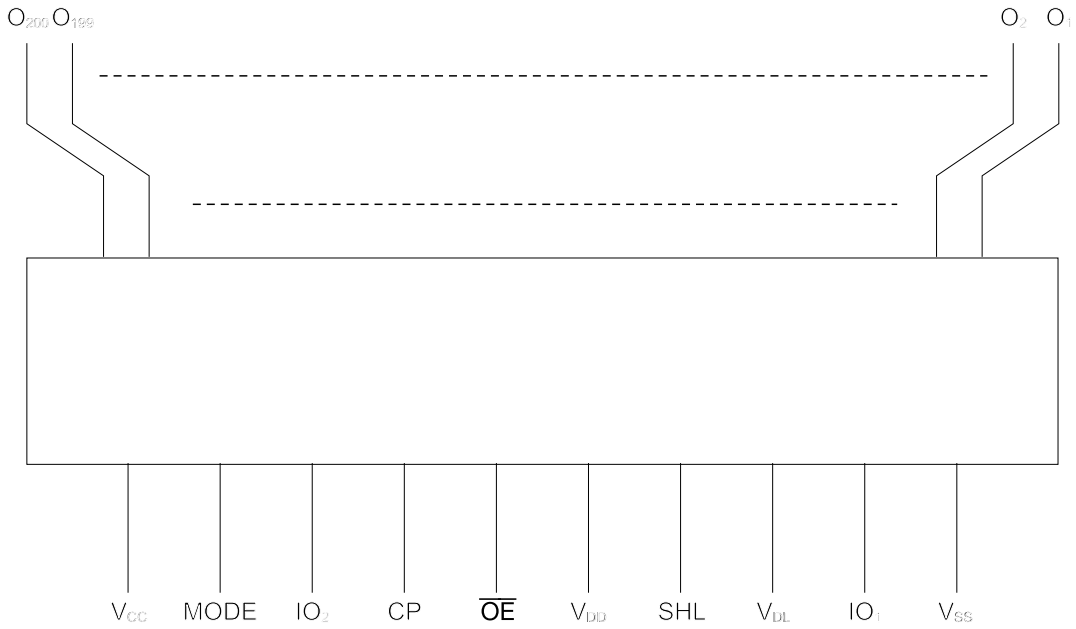
FEATURES

- Number of LCD control outputs: 192 or 200
- LCD control signal amplitude : 40 V (max.)
- LCD control signal voltage : Positive voltage/negative voltage outputs can be made.
- Variable shift register scanning direction
- Slim TCP package

PACKAGE SHAPE

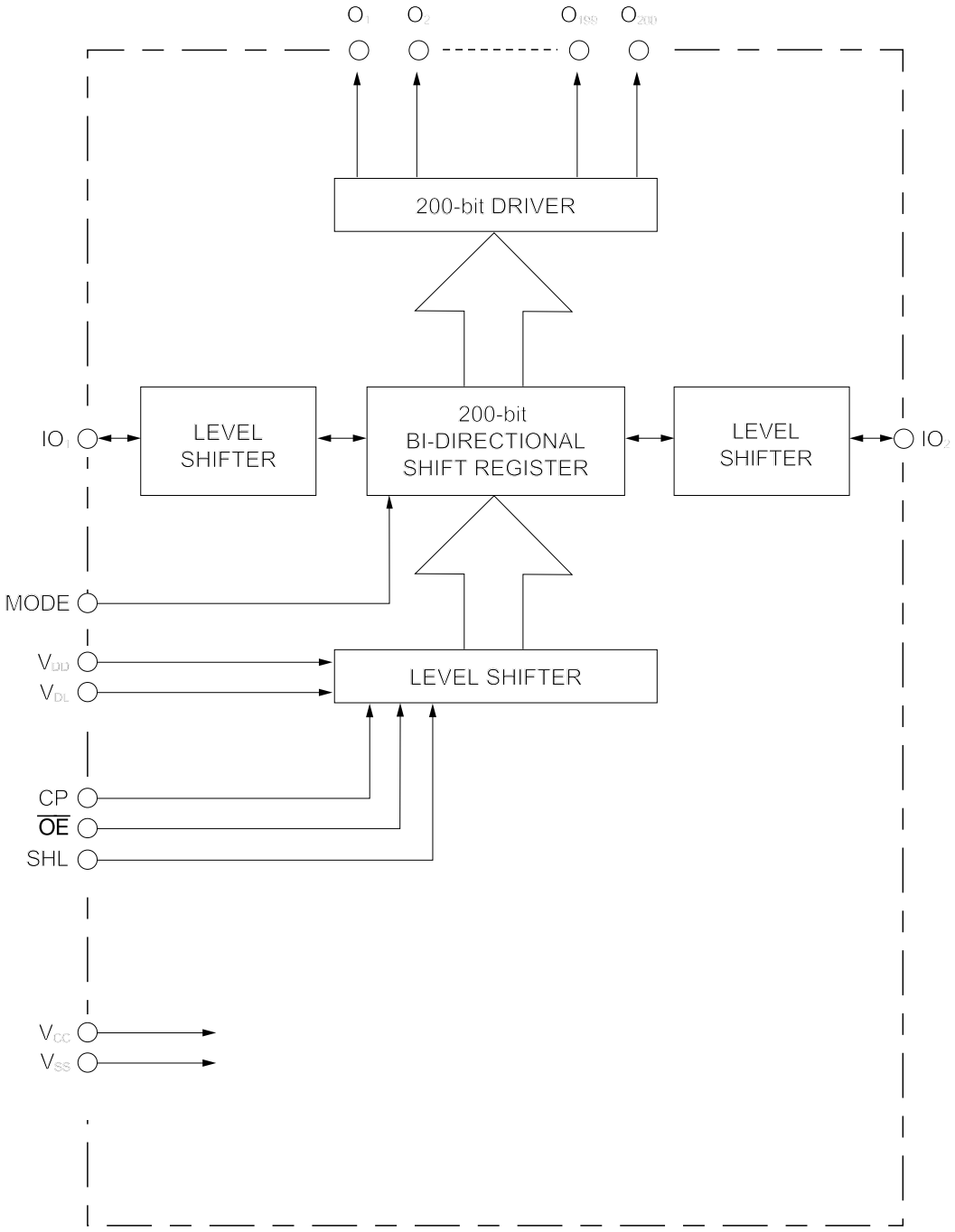
- 35 mm-wide film TCP mounting
- Tin-plated

TCP PIN CONFIGURATION (TOP VIEW)



This is a pin configuration example when the chip pins (excluding dummy pins) are used as TCP pins.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

Parameter	Symbol	Conditions	Rating	Unit
Power Supply Voltage (1)	V_{CC}	Ta = –20°C to +75°C	–0.3 to +42.0 V	V
Power Supply Voltage (2)	V_{DL}		–0.3 to V_{DD} + 0.3	V
Power Supply Voltage (3)	V_{DD}		–0.3 to +22.0	V
Input Voltage	V_I		–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

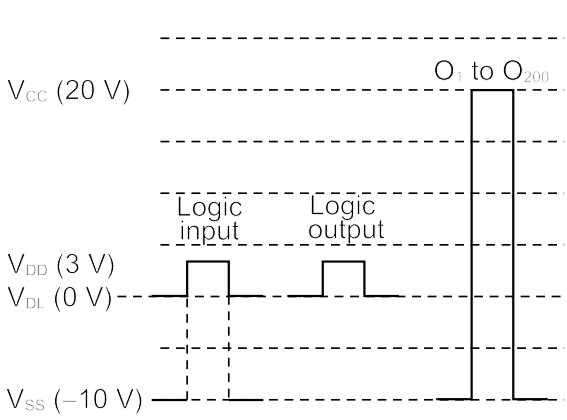
(V_{SS} = 0 V)

Parameter	Symbol	Conditions	Rating	Unit
Power Supply Voltage (1)	V_{CC}	Ta = 25°C	20 to 40	V
Power Supply Voltage (2)	V_{DL}		0 to 20	V
Power Supply Voltage (3)	V_{DD}		V_{DL} + 3 to V_{DL} + 5.5	V
Power Supply Voltage (4)	$V_{CC} – V_{DL}$		10 to 25	V
Operating Temperature	T_{OP}	—	–20 to +75	°C

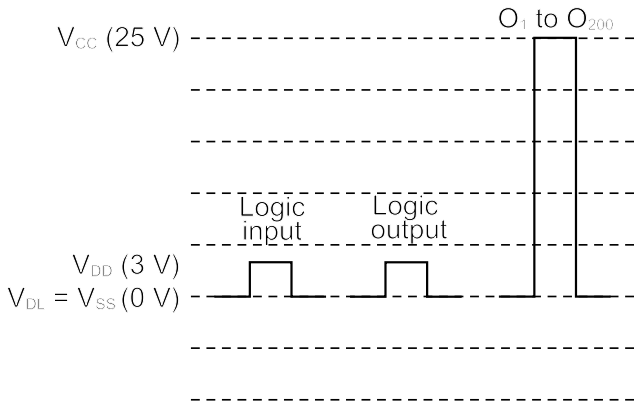
Voltage settings

1) The MSM6666 can be set to give a positive voltage or negative voltage LCD control output. An example of negative voltage output is shown in 1-1), and an example of positive voltage output is shown in 1-2).

1-1) Example of negative voltage output (V_{SS} = –10 V, V_{DL} = 0 V)



1-2) Example of positive voltage output (V_{SS} = V_{DL} = 0 V)



2) Input the logic input signals (CP, SHL, $\overline{OE}$, IO_1, IO_2) with an amplitude of $V_{DD} – V_{DL}$.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = 20 V, V_{SS} = –10 V, Ta = –20 to +75°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH1} *1	—	$0.7 \times (V_{DD} - V_{DL}) + V_{DL}$	—	V_{DD}	V
	V_{IH2} *2	—	$0.9 \times V_{CC}$	—	V_{CC}	
"L" Input Voltage	V_{IL1} *1	—	V_{DL}	—	$0.3 \times (V_{DD} - V_{DL}) + V_{DL}$	V
	V_{IL2} *2	—	V_{SS}	—	$0.1 \times V_{CC}$	
"H" Output Voltage	V_{OH} *3	IO = –40 µA	V_{DD} – 0.4 V	—	V_{DD}	V
"L" Output Voltage	V_{OL} *3	IO = 40 µA	V_{DL}	—	V_{DL} + 0.4 V	V
Input Current	I_I *1	—	–5.0	—	+5.0	µA
"H" Output Resistance	R_{OH} *4	$V_O = V_{CC} - 0.5$ V	—	600	1500	Ω
"L" Output Resistance	R_{OL} *4	$V_O = V_{SS} + 0.5$ V	—	600	1500	Ω
Supply Current	I_{DD}	No load f_{CP} = 50 kHz 1/600 duty	—	30	50	µA
	I_{CC}		—	500	900	µA

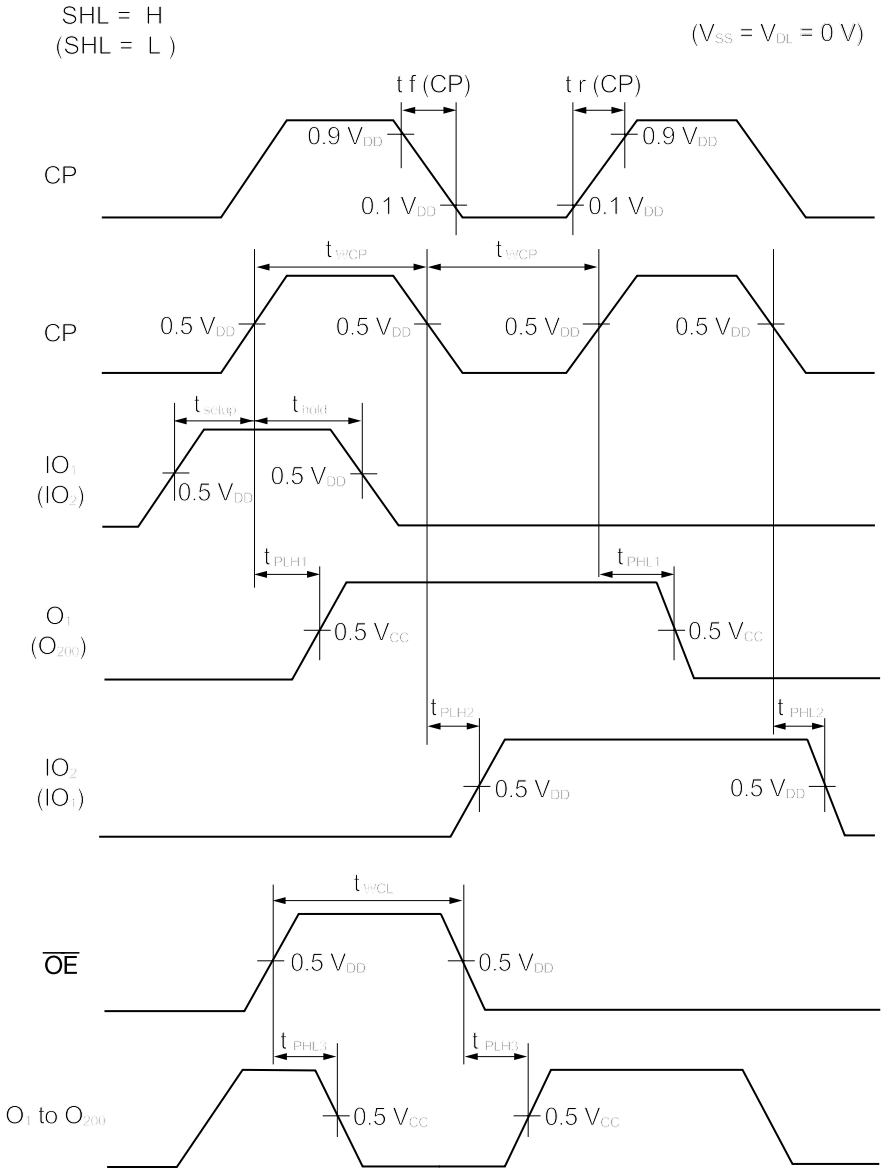
*1) Applicable to pins CP, SHL, IO_1, IO_2 and $\overline{OE}$.
*2) Applicable to pin MODE.
*3) Applicable to pins IO_1 and IO_2.
*4) Applicable to pins O_1 to O_{200}.

Switching Characteristics

(V_{CC} = 20 V, V_{DD} = 5 V, V_{DL} = 0 V, V_{SS} = –10 V, Ta = –20 to +75°C)

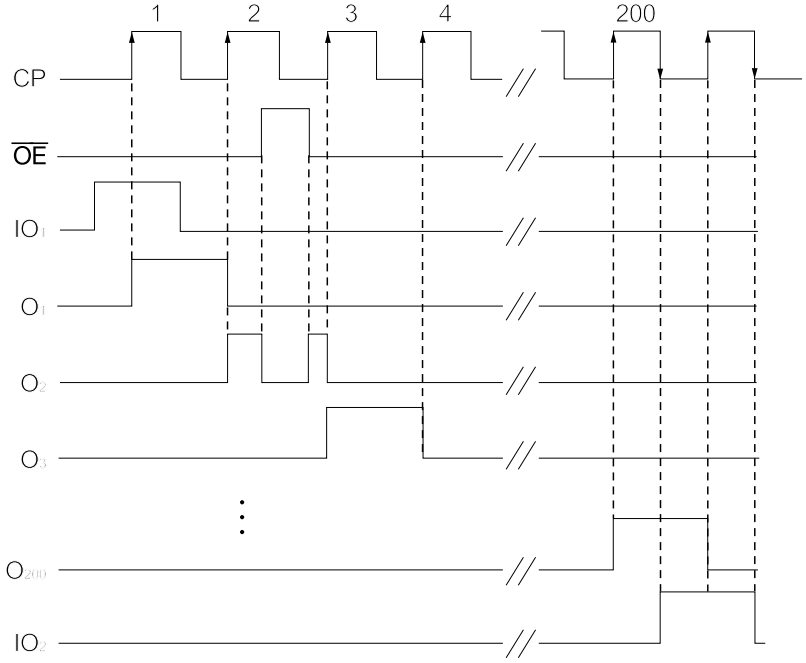
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock Frequency	f_{CP}	—	—	—	100	kHz
CP Pulse Width	t_{WCP}	—	400	—	—	ns
Clear Enable Time	t_{WCL}	—	1	—	—	µs
Data Setup Time	t_{setup}	—	300	—	—	ns
Data Hold Time	t_{hold}	—	300	—	—	ns
CP Rise Time	t_r (CP)	—	—	—	30	ns
CP Fall Time	t_f (CP)	—	—	—	30	ns
Propagation Delay Time	t_{PLH1} (t_{PHL1})	C_L = 300 pF	—	—	700	ns
	t_{PLH2} (t_{PHL2})	C_L = 30 pF	—	—	400	ns
	t_{PLH3} (t_{PHL3})	C_L = 300 pF	—	—	700	ns

TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

The MSM6666 generates signals to control the 200-bit TFT gate using the 200-bit bi-directional shift register circuit and outputs them after level conversion.
The input signal for the shift register circuit is input in at the rising edge of the clock pulse from the data input/output pin IO_1 (or IO_2). This signal is shifted at the rising edge of the clock pulse and is output at the falling edge of the clock pulse from the data input/output pin IO_2 (or IO_1). The LCD output signals generated in the shift register circuit is output via the output pins O_1 to O_{200} in parallel.
The direction of shifting the data can be selected by the input given to the shifting direction selection pin SHL. If the input to SHL is kept fixed at the "H" level, the data will be shifted successively in the direction IO_1 to O_1 ... O_{200} to IO_2. If the input to SHL is kept fixed at the "L" level, the data will be shifted successively in the direction IO_2 to O_{200} ... O_1 to IO_1.
When an "H" level input is given to the clear input pin $\overline{OE}$, the outputs at all the output pins O_1 to O_{200} go to the "L" level irrespective of the shift data.
The timings of operations are shown below when an "H" level input is given to SHL.



Pin Functional Description

- IO_1, IO_2
  These are the data input/output pins for the 200-bit bi-directional shift register.
  The input data is read in at the rising edge of CP, and is output at the falling edge of CP after a shift register delay corresponding to 200 bits.

- SHL
  This is the input pin for selecting the shifting direction of 200-bit bi-directional shift register. The functions of IO_1, IO_2, and SHL are given in the following table.

SHL	Shifting direction	Data input/output pin	
"L"	O_{200} to O_1	Input	IO_2
		Output	IO_1
"H"	O_1 to O_{200}	Input	IO_1
		Output	IO_2

- CP
  This is the clock pulse input pin for the 200-bit bi-directional shift register.
  The scanned data is shifted at the rising edge of the input clock pulse.

- MODE
  This pin is used to set the number of LCD control outputs to either 200 or 192.
  The pins to be connected to the MODE pin are shown in the following table.

No. of outputs	MODE connection pin
200	V_{SS}
192	V_{CC}

  When the number of outputs is 192, the output pins O_{97} to O_{104} are always set to the "L" level. In the shift register, the data on O_{96} (or O_{105}) shifts onto O_{105} (or O_{96}).
  * The MODE pin should be connected to the V_{SS} or V_{DD} pin.

- $\overline{OE}$
  This is the CLEAR input pin that fixes all the LCD control outputs to the "L" level irrespective of the shift data that is input in the shift register.
  The LCD control outputs are fixed at "L" level by setting the $\overline{OE}$ pin to "H" level.

- O_1 to O_{200}
  These are the output pins and correspond directly to each bit of the shift register.
  Data in the shift register is output after level conversion.

- V_{DD}, V_{DL}
  These are the bias power supply input pins.

- V_{CC}, V_{SS}
  These are the power supply pins for this IC.

CAUTIONS

Since the voltage of the LCD driving section is high in this IC, applying a high voltage to the LCD driving section with the logic section power supply left in the floating condition can cause excessive currents to flow thereby destroying the IC.
Always adhere to the following sequences when switching ON and OFF the power supply to this IC.

Sequence 1
At the time of power supply ON : V_{DL} to V_{DD} to Logic inputs to V_{SS} to V_{CC}
At the time of power supply OFF : V_{CC} to V_{SS} to Logic inputs to V_{DD} to V_{SS}

Sequence 2
At the time of power supply ON : V_{DL} to V_{DD} to V_{SS} to Logic inputs to V_{CC}
At the time of power supply OFF : V_{CC} to Logic inputs to V_{SS} to V_{DD} to V_{DL}

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